

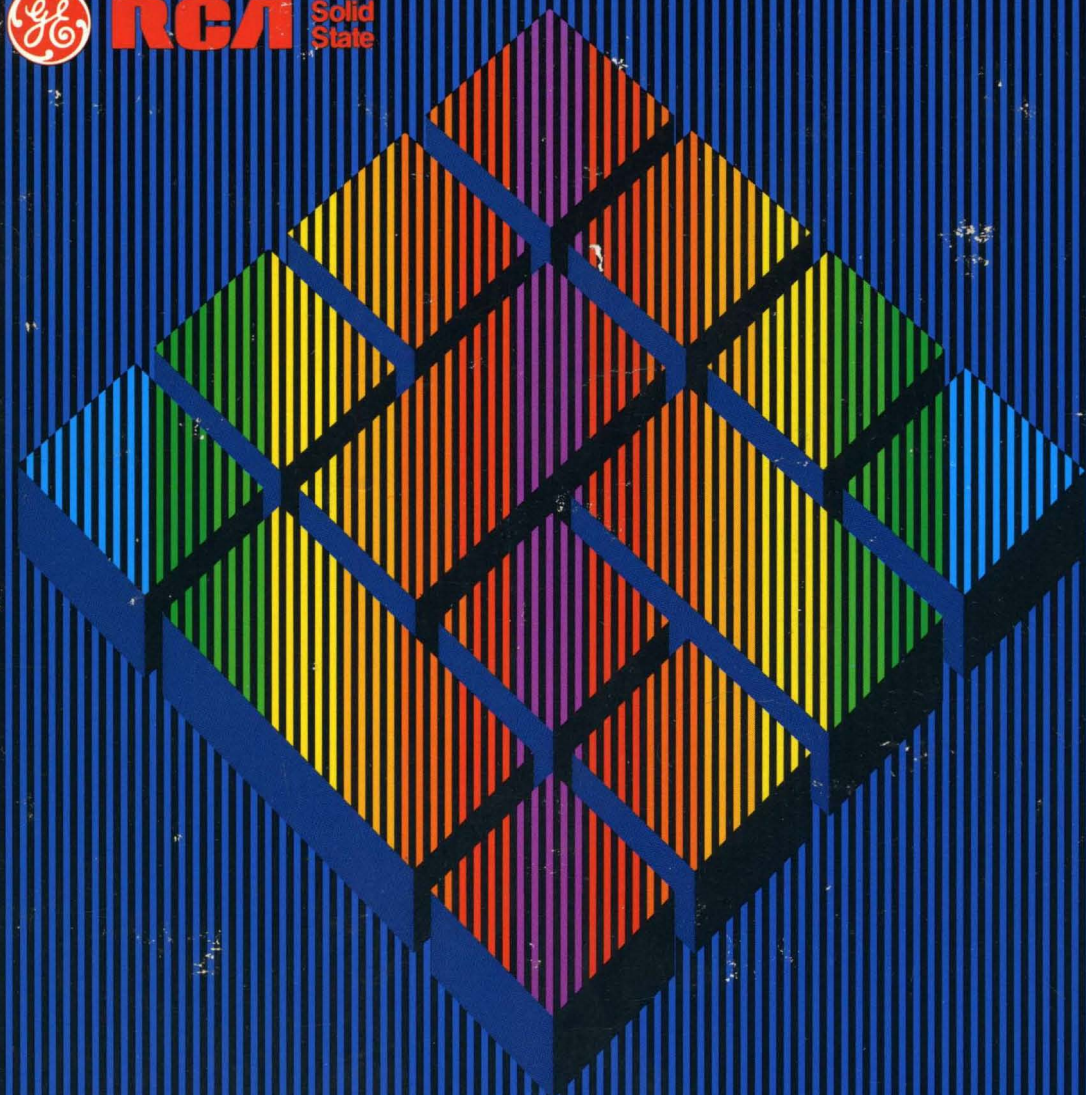
Component Data Catalog 1987

Excellence in Integrated Signal Processing IC's

ARROW ELECTRONICS, INC.
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RCA Solid State




 **INTERSIL**



Component Data Catalog 1987

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NOTE: All typical values have been characterized but are not tested.

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100S	2N5458	2N2606	2N2607	2N3332	2N5268	2N3815	IT132
100U	2N3684	2N2607	2N2607	2N3333	IT132	2N3816	IT130
102M	2N5686	2N2608	2N2608	2N3334	IT132	2N3816A	IT130A
102S	2N5457	2N2609	2N2609	2N3335	IT132	2N3817	IT130
103M	2N5457	2N2639	IT120	2N3336	IT132	2N3817A	IT130A
103S	2N5499	2N2640	IT122	2N3347	IT137	2N3819	2N5484
104M	2N5458	2N2641	IT122	2N3348	IT138	2N3820	2N2608
105M	2N5459	2N2642	IT120	2N3349	IT139	2N3821	2N3821
105U	2N4340	2N2643	IT122	2N3350	IT137	2N3822	2N3822
106M	2N5485	2N2644	IT122	2N3351	IT138	2N3823	2N3823
107M	2N5485	2N2652	IT120	2N3352	IT139	2N3824	2N3824
110U	2N3685	2N2652A	IT120	2N3365	2N4340	2N3907	IT120
120U	2N3686	2N2720	IT120	2N3366	2N4338	2N3908	IT120
125U	2N4339	2N2721	IT122	2N3367	2N4338	2N3909	2N2609
1277A	2N3822	2N2722	IT120	2N3368	2N4341	2N3909A	2N2609
1278A	2N3821	2N2802	IT139	2N3369	2N4339	2N3921	2N3921
1279A	2N3821	2N2803	IT139	2N3370	2N4338	2N3922	2N3922
1280A	2N4224	2N2804	IT139	2N3376	2N2608	2N3949	IT132
1281A	2N3822	2N2805	IT139	2N3378	2N2608	2N3950	IT132
1282A	2N4341	2N2806	IT139	2N3380	2N2609	2N3954	2N3954
1283A	2N4340	2N2807	IT139	2N3382	2N3994	2N3954A	2N3954A
1284A	2N4222	2N2841	2N2607	2N3384	2N3993	2N3955	2N3955
1285A	2N3821	2N2842	2N2607	2N3386	2N5114	2N3955A	2N3955A
1286A	2N4220	2N2843	2N2607	2N3409	IT122	2N3956	2N3956
130U	2N3687	2N2844	2N2607	2N3410	IT122	2N3957	2N3957
1325A	2N4222	2N2903	IT122	2N3411	IT122	2N3966	2N4416
135U	2N4339	2N2903A	IT120	2N3423	IT122	2N3967	2N4221
14T	2N4224	2N2910	IT122	2N3424	IT122	2N3967A	2N4221
155U	2N4416	2N2913	IT122	2N3425	IT122	2N3968	2N3968
1714A	2N4340	2N2914	IT120	2N3436	2N4341	2N3968A	2N3685
182S	2N4391	2N2915	IT120	2N3437	2N4340	2N3969	2N3686
183S	2N3823	2N2915A	IT120	2N3438	2N4338	2N3969A	2N3686
197S	2N4338	2N2916	IT120	2N3452	2N4320	2N3970	2N3970
198S	2N4340	2N2916A	IT120	2N3453	2N4338	2N3971	2N3971
199S	2N4341	2N2917	IT122	2N3454	2N4338	2N3972	2N3972
2000M	2N3823	2N2918	IT122	2N3455	2N4340	2N3993	2N3993
2001M	2N3823	2N2919	IT120	2N3456	2N4338	2N3993A	2N3993
200S	2N4392	2N2919A	IT120	2N3457	2N4338	2N3994	2N3994
200U	2N3824	2N2920	2N2920	2N3458	2N4341	2N3994A	2N3994
201S	2N4391	2N2920A	2N2920	2N3459	2N4339	2N4009	IT132
202S	2N4392	2N2936	IT120	2N3460	2N4338	2N4010	IT132
203S	2N3821	2N2937	IT120	2N3513	IT122	2N4011	IT132
204S	2N3821	2N2972	IT122	2N3514	IT122	2N4011S	IT139
2078A	2N3955	2N2973	IT122	2N3515	IT122	2N4016	IT137
2079A	2N3955	2N2974	IT120	2N3516	IT122	2N4017	IT139
2080A	2N3955A	2N2975	IT120	2N3517	IT122	2N4018	IT139
2081A	2N3955A	2N2976	IT120	2N3521	IT122	2N4019	IT139
2093M	2N3687	2N2977	IT120	2N3522	IT122	2N4020	IT139
2094M	2N3686	2N2978	IT120	2N3574	2N2607	2N4021	IT139
2095M	2N3686	2N2979	IT120	2N3575	2N2607	2N4022	IT139
2098A	2N3954	2N2980	IT121	2N3578	2N2608	2N4023	IT137
2099A	2N3955A	2N2981	IT122	2N3587	IT122	2N4024	IT137
210U	2N4416	2N2982	IT122	2N3608	3N172	2N4025	IT137
2130U	2N5452	2N3043	IT121	2N3680	IT120	2N4026	3N163
2132U	2N3955	2N3044	IT122	2N3684	2N3684	2N4038	2N4351
2134U	2N3956	2N3045	IT122	2N3684A	2N3684	2N4039	2N4351
2136U	2N3957	2N3046	IT121	2N3685	2N3685	2N4065	3N163
2138U	2N3958	2N3047	IT122	2N3685A	2N3685	2N4066	3N166
2139U	2N3958	2N3048	IT122	2N3686	2N3686	2N4067	3N166
2147U	2N3958	2N3049	IT139	2N3686A	2N3686	2N4082	2N3954
2148U	2N3958	2N3050	IT139	2N3687	2N3687	2N4083	2N3955
2149U	2N3958	2N3051	IT139	2N3687A	2N3687	2N4084	2N3954
231S	2N3954	2N3052	IT129	2N3726	IT131	2N4085	2N3955
232S	2N3955	2N3059	IT139	2N3727	IT130	2N4091	2N4091
233S	2N3956	2N3066	2N4340	2N3728	IT122	2N4091A	2N4091
234S	2N3957	2N3067	2N4338	2N3729	IT121	2N4091JAN	2N4091JAN
235S	2N3958	2N3068	2N4338	2N3800	IT132	2N4091JANTX	2N4091JANTX
241U	2N4869	2N3069	2N4341	2N3801	IT132	2N4091JANTXV	2N4091JANTXV
250U	2N4901	2N3070	2N4339	2N3802	IT132	2N4092	2N4092
251U	2N4392	2N3071	2N4338	2N3803	IT132	2N4092A	2N4092
2N2060	IT120	2N3084	2N4339	2N3804	IT130	2N4092JAN	2N4092JAN
2N2060A	IT121	2N3085	2N4339	2N3804A	IT130A	2N4092JANTX	2N4092JANTX
2N2060B	IT121	2N3086	2N4339	2N3805	IT130	2N4092JANTXV	2N4092JANTXV
2N2223	IT122	2N3087	2N4339	2N3805A	IT130A	2N4093	2N4093
2N2223A	IT121	2N3088	2N4339	2N3806	IT122	2N4093A	2N4093
2N2386	2N2608	2N3088A	2N4339	2N3807	IT122	2N4093JAN	2N4093JAN
2N2386A	2N2608	2N3089	2N4339	2N3808	IT122	2N4093JANTX	2N4093JANTX
2N2453	IT122	2N3089A	2N4339	2N3809	IT122	2N4093JANTXV	2N4093JANTXV
2N2453A	IT121	2N3113	2N2607	2N3810	2N3810	2N4100	2N4100
2N2480	IT122	2N3277	2N2606	2N3810A	2N3810A	2N4117	2N4117
2N2480A	IT121	2N3278	2N2607	2N3811	2N3811	2N4117A	2N4117A
2N2497	2N2608	2N3328	2N5265	2N3811A	2N3811A	2N4118	2N4118
2N2498	2N2608	2N3329	2N5267	2N3812	IT132	2N4118A	2N4118A
2N2499	2N2609	2N3330	2N5266	2N3813	IT132	2N4119	2N4119
2N2500	2N2608	2N3331	2N5270	2N3814	IT132	2N4119A	2N4119A

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
2N4120	3N163	2N5021	2N2607	2N5475	2N5265	2N6485	2N6485
2N4139	2N3822	2N5033	2N5460	2N5476	2N5266	2N6502	IT122
2N4220	2N4220	2N5045	2N5453	2N5484	2N5484	2N6503	IT122
2N4220A	2N4220	2N5046	2N5454	2N5485	2N5485	2N6550	2N4868A
2N4221	2N4221	2N5047	2N5454	2N5486	2N5486	2N6568	2N5432
2N4221A	2N4221	2N5078	2N5397	2N5515	2N5515	2SC294	IT122
2N4222	2N4222	2N5090	IT122	2N5516	2N5516	2S111	2N2607
2N4222A	2N4222	2N5103	2N4416	2N5517	2N5517	2S112	2N2607
2N4223	2N4223	2N5104	2N4416	2N5518	2N5518	2S113	2N5270
2N4224	2N4224	2N5105	2N4416	2N5519	2N5519	2S115	2N2607
2N4267	3N163	2N5114	2N5114	2N5520	2N5520	2S116	2N2607
2N4268	3N161	2N5114JAN	2N5114JAN	2N5521	2N5521	2S147	**
2N4302	2N4302	2N5114JANTX	2N5114JANTX	2N5522	2N5522	2S148	**
2N4303	2N5459	2N5114JANTXV	2N5114JANTXV	2N5523	2N5523	2S149	**
2N4304	2N5458	2N5115	2N5115	2N5524	2N5524	2S150	**
2N4338	2N4338	2N5115JAN	2N5115JAN	2N5545	2N3954	2S178	**
2N4339	2N4339	2N5115JANTX	2N5115JANTX	2N5546	2N3955A	2S179	**
2N4340	2N4340	2N5115JANTXV	2N5115JANTXV	2N5547	2N3955	2S180	**
2N4341	2N4341	2N5116	2N5116	2N5549	2N4093	2S111	2N5457
2N4342	2N5461	2N5116JAN	2N5116JAN	2N5555	J310	2S112	2N5457
2N4343	2N5462	2N5116JANTX	2N5116JANTX	2N5556	2N3685	2S113	2N5457
2N4351	2N4351	2N5116JANTXV	2N5116JANTXV	2N5557	2N3684	2S1132	**
2N4352	3N163	2N5117	2N5117	2N5558	2N3684	2S1133	**
2N4353	3N172	2N5118	2N5118	2N5561	U401	2S1134	**
2N4360	2N5460	2N5119	2N5119	2N5562	U402	2S1135	**
2N4381	2N2609	2N5120	IT131	2N5563	U404	2S115	2N4868
2N4382	2N5115	2N5121	IT132	2N5592	2N3822	2S117	2N5484
2N4391	2N4391	2N5122	IT132	2N5593	2N3822	2S1178	**
2N4392	2N4392	2N5123	IT131	2N5594	2N3822	2S1179	**
2N4393	2N4393	2N5124	IT132	2N5598	2N5638	2S118	2N3821
2N4416	2N4416	2N5125	IT132	2N5639	2N5639	2S1180	**
2N4416A	2N416A	2N5128	2N5434	2N5640	2N5640	2S119	ITE4416
2N4417	2N4416	2N5159	2N5433	2N5647	2N4117A	2S123	2N5459
2N4445	2N5432	2N5163	2N3822	2N5648	2N4117A	2S130	2N5458
2N4446	2N5434	2N5196	2N5196	2N5649	2N4117A	2S132	2N3822
2N4447	2N5432	2N5197	2N5197	2N5653	2N5638	2S133	2N5397
2N4448	2N5434	2N5198	2N5198	2N5654	2N5639	2S134	2N3822
2N4856	2N4856	2N5199	2N5199	2N5668	2N5484	2S137	2N5484
2N4856A	2N4856A	2N5245	ITE4416	2N5669	2N5485	2S141	2N5459
2N4856JAN	2N4856JAN	2N5246	2N5484	2N5670	2N5486	2S142	2N3822
2N4856JANTX	2N4856JANTX	2N5247	2N5486	2N5793	IT129	2S143	ITE4092
2N4856JANTXV	2N4856JANTXV	2N5248	2N5486	2N5794	IT129	2S144	ITE4416
2N4857	2N4857	2N5254	IT132	2N5795	IT139	2S146	2N5459
2N4857A	2N4857A	2N5255	IT132	2N5796	IT139	2S148	2N3821
2N4857JAN	2N4857JAN	2N5256	IT130	2N5797	2N2608	2S149	2N5484
2N4857JANTX	2N4857JANTX	2N5257	2N5457	2N5798	2N2608	2S150	ITE4416
2N4857JANTXV	2N4857JANTXV	2N5258	2N5458	2N5799	2N2608	2S154	2N3822
2N4858	2N4858	2N5259	2N5459	2N5800	2N2608	2S155	2N3822
2N4858A	2N4858A	2N5265	2N2607	2N5801	2N4393	2S156	2N5459
2N4858JAN	2N4858JAN	2N5266	2N2607	2N5802	2N4393	2S161	2N5397
2N4858JANTX	2N4858JANTX	2N5267	2N2608	2N5803	2N4392	2S165	J201
2N4858JANTXV	2N4858JANTXV	2N5268	2N2608	2N5843	IT130	2S166	2N3821
2N4859	2N4859	2N5269	2N2609	2N5844	IT130	2S168	2N3822
2N4859A	2N4859A	2N5270	2N2609	2N5870	2N5902	2S172	2N5196
2N4859JAN	2N4859JAN	2N5277	2N4341	2N5903	2N5903	3GS	2N3821
2N4859JANTX	2N4859JANTX	2N5278	2N4341	2N5904	2N5904	3N145	3N163
2N4859JTXV	2N4859JTXV	2N5358	2N4220	2N5905	2N5905	3N146	3N163
2N4860	2N4860	2N5359	2N4220	2N5906	2N5906	3N147	3N189
2N4860A	2N4860A	2N5360	2N4221	2N5907	2N5907	3N148	3N189
2N4860JAN	2N4860JAN	2N5361	2N4221	2N5908	2N5908	3N149	3N161
2N4860JANTX	2N4860JANTX	2N5362	2N4222	2N5909	2N5909	3N150	3N163
2N4860JTXV	2N4860JTXV	2N5363	2N4222	2N5911	2N5911	3N151	3N190
2N4861	2N4861	2N5364	2N4222	2N5912	2N5912	3N155	3N163
2N4861A	2N4861A	2N5391	2N4867A	2N5949	2N5486	3N155A	3N163
2N4861JAN	2N4861JAN	2N5392	2N4868A	2N5950	2N5486	3N156	3N163
2N4861JANTX	2N4861JANTX	2N5393	2N4869A	2N5951	2N5486	3N156A	3N163
2N4861JANTXV	2N4861JANTXV	2N5394	2N4869A	2N5952	2N5484	3N157	3N163
2N4867	2N4867	2N5395	2N4869A	2N5953	2N5484	3N173	3N163
2N4867A	2N4867A	2N5396	2N4869A	2N6085	IT122	3N158	3N163
2N4868	2N4868	2N5397	2N5397	2N6086	IT122	3N158A	3N163
2N4868A	2N4868A	2N5398	2N5398	2N6087	IT121	3N160	3N161
2N4868B	2N4868B	2N5432	2N5432	2N6088	IT121	3N161	3N161
2N4869A	2N4869A	2N5433	2N5433	2N6089	IT122	3N162	3N163
2N4878	2N4878	2N5434	2N5434	2N6090	IT121	3N164	3N164
2N4879	2N4879	2N5452	2N5452	2N6091	IT121	3N165	3N165
2N4880	2N4880	2N5453	2N5453	2N6092	IT121	3N166	3N166
2N4937	IT131	2N5454	2N5454	2N6441	IT122	3N167	3N161
2N4938	IT132	2N5457	2N5457	2N6442	IT122	3N168	3N161
2N4939	IT132	2N5458	2N5458	2N6443	IT122	3N169	3N170
2N4940	IT132	2N5459	2N5459	2N6444	IT122	3N170	3N170
2N4941	IT131	2N5460	2N5460	2N6445	IT121	3N171	3N171
2N4942	IT132	2N5461	2N5461	2N6446	IT121	3N172	3N172
2N4955	IT122	2N5462	2N5462	2N6447	IT121	3N173	3N173
2N4956	IT122	2N5463	2N5463	2N6448	IT121	3N174	3N163
2N4977	2N5433	2N5464	2N5464	2N6451	U310	3N175	3N170
2N4978	2N5433	2N5465	2N5465	2N6452	U310	3N176	3N170
2N4979	2N4859	2N5471	2N5265	2N6453	U310	3N177	3N171
2N5018	2N5018	2N5472	2N5265	2N6454	U310	3N178	3N172
2N5019	2N5019	2N5473	2N5265	2N6483	2N6483	3N179	3N172
2N5020	2N2843	2N5474	2N5265	2N6484	2N6484	3N180	3N172

ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT
3N181	3N161	AD7520SD	AD7520SD	AH0141D	DG141AP	BF805	2N4869
3N182	3N161	AD7520TD	AD7520TD	AH0141D/883	DG141AP/883B	BF806	2N4869
3N183	3N161	AD7520UD	AD7520UD	AH0142CD	DG142BK	BF808	2N4868
3N188	3N188	AD7521JD	AD7521JD	AH0142D	DG142AK	BF810	2N4858
3N189	3N189	AD7521JN	AD7521JN	AH0142D/883	DG142AK/883B	BF811	2N4858
3N190	3N190	AD7521KD	AD7521KD	AH0143CD	DG143BK	BF815	2N4858
3N191	3N191	AD7521KN	AD7521KN	AH0143D	DG143AK	BF816	2N4858
3N207	3N190	AD7521LD	AD7521LD	AH0143D/883	DG143AK/883B	BF817	2N4858
3N208	3N188	AD7521LN	AD7521LN	AH0144CD	DG144BK	BF818	2N4858
3SK22	2N5486	AD7521SD	AD7521SD	AH0144D	DG144AK	BFQ10	U401
3SK23	2N5397	AD7521TD	AD7521TD	AH0144D/883	DG144AK/883B	BFQ11	U401
3SK28	2N5397	AD7521UD	AD7521UD	AH0145CD	DG145BP	BFQ12	U402
42T	2N4392	AD7523AD	AD7523AD	AH0145D	DG145AP	BFQ13	U403
4360TP	2N5462	AD7523BD	AD7523BD	AH0145D/883	DG145AP/883B	BFQ14	U404
5033TP	2N5460	AD7523CD	AD7523CD	AH0146CD	DG146BP	BFQ15	U405
588U	2N4416	AD7523JN	AD7523JN	AH0146D	DG146AP	BFQ16	U406
58T	2N5457	AD7523KN	AD7523KN	AH0146D/883	DG146AP/883B	BFQ23	IT5912
59T	2N4416	AD7523LN	AD7523LN	AH0151CD	DG151BK	BFQ24	U403
703U	2N4220	AD7523SD	AD7523SD	AH0151D/883	DG151AK/883B	BFQ44	IT5912
704U	2N4220	AD7523TD	AD7523TD	AH0152CD	DG152BK	BFQ45	IT5912
705U	2N4224	AD7523UD	AD7523UD	AH0152D	DG152AK	BFQ49A	2N3055
707U	2N4860	AD7530JD	AD7530JD	AH0152D/883	DG152AK/883B	BFQ49B	2N3958
714U	2N3822	AD7530JN	AD7530JN	AH0153CD	DG153BP	BFQ49C	2N3958
734EU	2N4416	AD7530KD	AD7530KD	AH0153D	DG153AP	BF521	2N5199
734U	2N5516	AD7530KN	AD7530KN	AH0153D/883	DG153AP/883B	BF521A	2N5199
751U	2N4340	AD7530LD	AD7530LD	AH0154CD	DG154BK	BF567	2N3821
752U	2N4340	AD7530LN	AD7530LN	AH0154D	DG154AK	BF567P	2N5459
753U	2N4341	AD7531JD	AD7531JD	AH0154D/883	DG143AK/883B	BF568	2N3823
754U	2N4340	AD7531JN	AD7531JN	AH0155D	DG151AK	BF568P	2N4416
755U	2N4341	AD7531KD	AD7531KD	AH0161CD	DG161BP	BF570	2N3821
756U	2N4340	AD7531KN	AD7531KN	AH0161D	DG161AP	BF571	2N3822
A190	ITE4416	AD7531LD	AD7531LD	AH0161D/883	DG161AP/883B	BF572	2N3823
A191	ITE4416	AD7531LN	AD7531LN	AH0162CD	DG162BK	BF573	2N3821
A192	2N4416	AD7533AD	AD7533AD	AH0162D	DG162AK	BF574	2N4856
A193	2N5484	AD7533BD	AD7533BD	AH0162D/883B	DG162AK/883B	BF575	2N4857
A194	2N5484	AD7533CD	AD7533CD	AH0163CD	DG163BP	BF576	2N4858
A195	2N5484	AD7533JN	AD7533JN	AH0163D	DG163AP	BF577	2N4859
A196	ITE4416	AD7533KN	AD7533KN	AH0163D/883	DG163AP/883B	BF578	2N4860
A197	ITE4391	AD7533LN	AD7533LN	AH0164CD	DG164BK	BF579	2N4861
A198	ITE4392	AD7533SD	AD7533SD	AH0164D	DG164AK	BF580	2N4416A
A199	ITE4393	AD7533TD	AD7533TD	AH0164D/883	DG164AK/883B	BF710	2N5397
A5T3821	2N5484	AD7533UD	AD7533UD	AH5009CN	IHS009CPD	BF711	2N5019
A5T3822	2N5484	AD7541AD	AD7541AD	AH5010CN	IHS010CPD	BFW10	2N3823
A5T3823	2N4416	AD7541BD	AD7541BD	AH5012CN	IHS012CPD	BFW11	2N3822
A5T3824	2N4341	AD7541JN	AD7541JN	AH5013CN	IHS013CPD	BFW12	2N4416
A5T5460	2N5460	AD7541KN	AD7541KN	AH5014CN	IHS014CPD	BFW13	2N4867
A5T5461	2N5461	AD7541SD	AD7541SD	AH5015CN	IHS015CPE	BFW39	IT129
A5T5462	2N5462	AD7541TD	AD7541TD	AH5016CN	IHS016CPE	BFW39A	IT120
AD3954	2N3954	AD810	2N4878	ALD555	ICM7555	BFW54	2N3822
AD3954A	2N3954A	AD811	2N4878	ALD556	ICM7556	BFW55	2N3822
AD3955	2N3955	AD812	2N4878	AM5011CN	IHS011CPE	BFW56	2N4860
AD3956	2N3956	AD813	2N4878	BC264	2N5458	BFW61	2N4224
AD3958	2N3958	AD814	IT124	BC264A	2N5457	BFX11	IT132
AD589	IC18069	AD815	IT124	BC264B	2N5458	BFX15	IT122
AD590	AD590	AD816	IT120A	BC264C	2N5458	BFX36	IT131
AD5905	2N5905	AD818	IT140	BC264D	2N4416	BFX70	IT122
AD5906	2N5906	AD820	IT132	BCY87	IT121	BFX71	IT122
AD5907	2N5907	AD821	IT130A	BCY88	IT122	BFX72	IT122
AD5908	2N5908	AD822	IT130A	BCY89	IT122	BFX78	2N5397
AD5909	2N5909	AD830	2N5520	BF244	2N5486	BFX82	2N5019
AD7506/COM/CHIPS	IHE116C/D	AD831	2N5521	BF244A	2N5484	BFX83	2N5019
AD7506/MIL/CHIPS	IHE116M/D	AD832	2N5522	BF244B	2N5485	BFX99	IT120A
AD7506/JD	IHE116C/J	AD833	2N5523	BF244C	2N5486	BFY20	IT122
AD7506/JD/883B	IHE116C/J/883B	AD833A	2N5524	BF245	2N5486	BFY81	IT122
AD7506/JN	IHE116C/J	AD835	2N3954	BF245A	2N4416	BFY82	IT122
AD7506/KD	IHE116C/K	AD836	2N3955	BF245B	2N4416	BFY83	IT122
AD7506/KD/883B	IHE116C/K/883B	AD837	2N3955	BF245C	2N4416	BFY84	IT122
AD7506/L	IHE116C/L	AD838	2N3956	BF246	2N5485	BFY85	IT122
AD7506/SD	IHE116M/J	AD839	2N3957	BF246A	2N5639	BFY86	IT122
AD7506/SD/883B	IHE116M/J/883B	AD840	2N5520	BF246B	2N5638	BFY91	IT122
AD7506/TD	IHE116M/T	AD841	2N5521	BF246C	2N5638	BFY92	IT122
AD7506/TD/883B	IHE116M/T/883B	AD842	2N5523	BF247	2N4091	BN209	IT122
AD7507/COM/CHIPS	IHE1216C/D	AH0126D	DG126AP	BF247A	2N4091	BSV22	2N4416
AD7507/MIL/CHIPS	IHE1216M/D	AH0126D/883	DG126AP/883B	BF247B	2N4091	BSV78	2N4856A
AD7507/JD	IHE1216C/J	AH0129CD	DG129BK	BF247C	2N4091	BSV79	2N4857A
AD7507/JD/883B	IHE1216C/J/883B	AH0129D	DG129AK	BF256	2N5484	BSV80	2N4858A
AD7507/JN	IHE1216C/J	AH0129D/883	DG129AK/883B	BF256A	2N5484	BSX82	2N3822
AD7507/KD	IHE1216C/K	AH0133CD	DG133BK	BF256B	2N4416	C21	2N3821
AD7507/KD/883B	IHE1216C/K/883B	AH0133D	DG133AK	BF256C	2N4416	C2306	2N5196
AD7507KN	IHE1216C/P	AH0133D/883	DG133AK/883B	BF320	2N5461	C38	2N4338
AD7507SD	IHE1216M/D	AH0134CD	DG134BK	BF320A	2N5460	C413N	2N5434
AD7507SD/883B	IHE1216M/J/883B	AH0134D	DG134AK	BF320B	2N5461	C610	2N4392
AD7507TD	IHE1216M/T	AH0134D/883	DG134AK/883B	BF320C	2N5462	C611	2N4393
AD7507TD/883B	IHE1216M/J/883B	AH0139CD	DG139BK	BF346	ITE4392	C612	2N4221
AD7520JD	AD7520JD	AH0139D	DG139AK	BF347	J201	C613	2N4221
AD7520JN	AD7520JN	AH0139D/883	DG139AK/883B	BF348	J310	C614	2N4220
AD7520KD	AD7520KD	AH0140CD	DG140BP	BF800	2N4867	C615	2N4221
AD7520KN	AD7520KN	AH0140D	DG140AP	BF801	2N4867	C620	2N4220
AD7520LD	AD7520LD	AH0140D/883	DG140AP/883B	BF802	2N4338	C621	2N4220
AD7520LN	AD7520LN	AH0141CD	DG141BP	BF804	2N4338	C622	2N4220

**CONSULT FACTORY

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ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT
C623	2N4220	D123AL	D123AL	DG152AP	DG152AK	DG191AL	DG191AL
C624	2N4220	D123AP	D123AK	DG152BP	DG152BK	DG191AP	DG191AK
C625	2N4220	D123BP	D123BK	DG153AL	DG153AK	DG191AP	DG191AK
C650	2N4220	D123BP	D123BJ	DG153AP	DG153AP	DG191BP	DG191CJ
C651	2N4220	D125AL	D125AL	DG153BP	DG153BP	DG191BP	DG191BK
C652	2N4220	D125AP	D125AP	DG154AL	DG154AL	DG191BP	DG191BK
C653	2N4220	D125BP	D125BK	DG154AP	DG154AK	DG200AAA	DG200AA
C6690	2N4341	D129AL	D129AL	DG154BP	DG154BK	DG200AAL	DG200AK
C6691	2N4341	D129AP	D129AP	DG161AL	DG161AL	DG200AAL	DG200AL
C6692	2N4339	D129BP	D129BK	DG161AP	DG161AP	DG200ABA	DG200BA
C673	2N4341	D1301	2N4222	DG161BP	DG161BP	DG200ABK	DG200BK
C674	2N4341	D1302	2N4220	DG162AL	DG162AL	DG200ACJ	DG200CJ
C680	2N4338	D1303	2N4220	DG162AP	DG162AK	DG201AAK	DG201AK
C680A	2N4338	D1420	2N4868	DG162BP	DG162BK	DG201ABK	DG201BK
C681	2N4338	D1421	2N3822	DG163AL	DG163AL	DG201ACJ	DG201CJ
C681A	2N4338	D1422	2N4869	DG163AP	DG163AP	DG211CJ	DG211CJ
C682	2N4339	D2T2218	IT129	DG163BP	DG163BP	DG212CJ	DG212CJ
C682A	2N4339	D2T2218A	IT129	DG164AL	DG164AL	DG381AA	DG182AA
C683	2N4339	D2T2219	IT129	DG164AP	DG164AK	DG381AK	DG182AK
C683A	2N4339	D2T2219A	IT129	DG164BP	DG164BK	DG381AP	DG182AK
C684	2N4220	D2T2904	IT139	DG180AA	DG180AA	DG381BA	DGM181BA
C684A	2N4220	D2T2904A	IT139	DG180AL	DG180AL	DG381BK	DGM181BK
C685	2N4220	D2T2905	IT139	DG180AP	DG180AP	DG381BP	DGM181BP
C685A	2N4220	D2T2905A	IT139	DG180BA	DG180BA	DG381CJ	DGM181CJ
C80	2N4338	D2T918	IT129	DG180BP	DG180BK	DG384AK	DGM185AK
C81	2N4338	DA102	2N5196	DG181AA	DGM181AA	DG384AP	DGM185AK
C84	2N4338	DA402	2N5196	DG181AA	DG181AA	DG384BP	DGM184BK
C85	2N4338	DAC1020LCD	AD7520LD	DG181AL	DGM181AL	DG384BP	DGM184BK
C91	2N4858	DAC1020LD	AD7520LD	DG181AL	DG181AL	DG384CJ	DGM184CJ
C92	2N4091	DAC1021LCD	AD7520KD	DG181AP	DGM181AK	DG387AA	DGM188AA
C93	2N4393	DAC1021LD	AD7520TD	DG181AP	DGM181AK	DG387AK	DGM188AK
C94	2N5457	DAC1022LCD	AD7520JD	DG181BA	DGM181BA	DG387AP	DGM188AK
C94E	2N5457	DAC1022LD	AD7520SD	DG181BA	DG181BA	DG387BP	DGM187BA
C95	2N5457	DAC1218LCD	AD7541BD	DG181BP	DGM181CJ	DG387BK	DGM187BK
C95E	2N5459	DAC1218LCN	AD7541LN	DG181BP	DGM181BK	DG387BP	DGM187BK
C96E	2N5484	DAC1218LCN	AD7541KN	DG181BP	DG181BK	DG390AK	DGM191AK
C97E	2N3822	DAC1219LCD	AD7541AD	DG182AA	DGM182AA	DG390AP	DGM191AK
C98E	2N3822	DAC1219LCD	AD7541LN	DG182AA	DG182AA	DG390BP	DGM190BK
CA555	ICM7555	DAC1220LCD	AD7521LD	DG182AL	DGM182AL	DG390BP	DGM190BK
CA556	ICM7556	DAC1220LD	AD7521UD	DG182AL	DG182AL	DG390CJ	DGM190CJ
CC4445	2N5432	DAC1221LCD	AD7521KD	DG182AP	DGM182AK	DG503	AD503
CC4446	2N5434	DAC1221LD	AD7521TD	DG182AP	DG182AK	DG5040AK	IHS040MJE
CC697	2N4856	DAC1222LCD	AD7521JD	DG182BA	DGM182BA	DG5040CJ	IHS040CPE
CD22001H	ICM1424C	DAC1222LD	AD7521SD	DG182BA	DG182BA	DG5040CK	IHS040CJE
CD22015E	ICM7051A	DG123AL	DG123AL	DG182BP	DGM182CJ	DG5041AK	IHS041MJE
CF2386	2N5458	DG123AP	DG123AP	DG182BP	DGM182BK	DG5041CJ	IHS041CPE
CF24	2N3824	DG123BP	DG123BP	DG182BP	DG182BK	DG5041CK	IHS041CJE
CFM13026	2N4858	DG125AL	DG125AL	DG183AL	DG183AL	DG5042AK	IHS042MJE
CM600	2N4092	DG125AP	DG125AP	DG183AP	DG183AP	DG5042CJ	IHS042CPE
CM601	2N4091	DG125BP	DG125BP	DG183BP	DG183BP	DG5042CK	IHS042CJE
CM602	2N4091	DG126AK	DG126AP	DG184AL	DGM184AL	DG5043AK	IHS043MJE
CM603	2N4091	DG126AL	DG126AL	DG184AL	DG184AL	DG5043CJ	IHS043CPE
CM640	2N4093	DG126BP	DG126BP	DG184AP	DGM184AK	DG5043CK	IHS043CJE
CM641	2N4093	DG129AL	DG129AL	DG184AP	DG184AK	DG5044AK	IHS044MJE
CM642	2N4093	DG129AP	DG129AK	DG184BP	DGM184CJ	DG5044CJ	IHS044CPE
CM643	2N4092	DG129BP	DG129BK	DG184BP	DGM184BK	DG5044CK	IHS044CJE
CM644	2N4092	DG133AL	DG133AK	DG184BP	DG184BK	DG5045AK	IHS045MJE
CM645	2N4092	DG133AP	DG133AK	DG185AL	DGM185AL	DG5045CJ	IHS045CPE
CM646	2N4092	DG133BP	DG133BK	DG185AL	DG185AL	DG5045CK	IHS045CJE
CM647	2N4091	DG134AL	DG134AL	DG185AP	DGM185AK	DG506AAK	IHS116MJ
CM650	2N5432	DG134AP	DG134AK	DG185AP	DG185AK	DG506ABK	IHS116CJ
CM651	2N5433	DG134BP	DG134BK	DG185BP	DGM185CJ	DG506ACJ	IHS116CJE
CM652	2N5432	DG139AL	DG139AL	DG185BP	DGM185BK	DG507AAK	IHS216MJ
CM653	2N5433	DG139AP	DG139AK	DG185BP	DG185BK	DG507ABK	IHS216CJ
CM697	2N5433	DG139BP	DG139BK	DG186AA	DG186AA	DG507ACJ	IHS216CPE
CM800	2N5433	DG140AL	DG140AL	DG186AL	DG186AL	DG508AAK	IHS108MJE
CM856	2N5433	DG140AP	DG140AP	DG186AP	DG186AP	DG508ABK	IHS108CJE
CM860	2N4868A	DG140BP	DG140BP	DG186BA	DG186BA	DG508ACJ	IHS108CPE
CMX740	2N5432	DG141AL	DG141AL	DG186BP	DG186BP	DG509AAK	IHS208MJE
CP640	2N4091	DG141AP	DG141AP	DG187AA	DG187AA	DG509ABK	IHS208CJE
CP643	2N5434	DG141BP	DG141BP	DG187AL	DG187AL	DG509ACJ	IHS208CPE
CP650	2N5432	DG142AL	DG142AL	DG187AP	DG187AK	IHS140AK	IHS140MJE
CP651	2N5433	DG142AP	DG142AK	DG187BP	DG187BA	DG5140CJ	IHS140CPE
CP652	2N5433	DG142BP	DG142BK	DG187BP	DG187BK	DG5140CK	IHS140CJE
CP653	2N5433	DG143AL	DG143AL	DG188AA	DG188AA	DG5141AK	IHS141MJE
D1101	2N3821	DG143AP	DG143AK	DG188AL	DG188AL	DG5141CJ	IHS141CPE
D1102	2N4338	DG143BP	DG143BK	DG188AP	DG188AP	DG5141CK	IHS141CJE
D1103	2N4338	DG144AL	DG144AL	DG188BA	DG188BA	DG5142AK	IHS142MJE
D1177	2N3821	DG144AP	DG144AK	DG188BP	DG188BK	DG5142CJ	IHS142CPE
D1178	2N3821	DG144BP	DG144BK	DG188BP	DG188AL	DG5142CK	IHS142CJE
D1179	2N4338	DG145AL	DG145AL	DG189AP	DG189AP	DG5143AK	IHS143MJE
D1180	2N3822	DG145AP	DG145AP	DG189BP	DG189BP	DG5143CJ	IHS143CPE
D1181	2N4338	DG145BP	DG145BP	DG190AL	DGM190AL	DG5143CK	IHS143CJE
D1182	2N4338	DG146AL	DG146AL	DG190AL	DG190AL	DG5144AK	IHS144MJE
D1183	2N4341	DG146AP	DG146AP	DG190AP	DGM190AK	DG5144CJ	IHS144CPE
D1184	2N4340	DG146BP	DG146BP	DG190AP	DG190AK	DG5144CK	IHS144CJE
D1185	2N4339	DG151AL	DG151AL	DG190BP	DGM190CJ	DG5145AK	IHS145MJE
D1201	2N4339	DG151AP	DG151AP	DG190BP	DG190BK	DG5145CJ	IHS145CPE
D1202	2N3821	DG151BP	DG151BK	DG190BP	DG190BK	DG5145CK	IHS145CJE
D1203	2N4220	DG152AL	DG152AL	DG191AL	DGM191AL	DN3066A	2N3821

**CONSULT FACTORY

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ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISIL EQUIVALENT
DN3067A	2N4338	E411	IT5911	FM3956	2N3956	H11-0507A-8	IH5216MJ/883B
DN3068A	2N4338	E412	IT5911	FM3957	2N3957	H11-0508-2	IH6108MJE
DN3069A	2N3822	E413	2N5454	FM3958	2N3958	H11-0508-5	IH6108CJE
DN3070A	2N3821	E414	2N3956	FP4339	2N4339	H11-0508-8	IH6108MJ/883B
DN3071A	2N4338	E415	2N3957	FP4340	2N4340	H11-0508A-2	IH5108MJE
DN3365A	2N4220	E420	IT5911	FT0654A	2N5486	H11-0508A-5	IH5108JJE
DN3365B	2N4091	E421	IT5912	FT0654B	2N5486	H11-0508A-8	IH5108MJ/883B
DN3366A	2N3686	E430	J309(X2)	FT0654C	2N4221	H11-0509-2	IH6208MJE
DN3366B	2N4091	E431	J310(X2)	FT0654D	2N4221	H11-0509-5	IH6208CJE
DN3367A	2N3687	ESM25	U401	FT3820	2N5460	H11-0509-8	IH6208MJ/883B
DN3367B	2N4091	ESM25A	U401	FT3820	2N5019	H11-0509A-2	IH5208MJE
DN3368A	2N4341	ESM4091	2N4091	FT3909	2N5019	H11-0509A-5	IH5208JJE
DN3368B	2N4221	ESM4092	2N4092	FT7103	3N161	H11-0509A-8	IH5208MJ/883B
DN3369A	2N4339	ESM4093	2N4093	FT7104	3N163	H11-5040-2	IH5040MJE
DN3369B	2N4220	ESM4302	2N5457	G118AL	G118AL	H11-5040-5	IH5040CJE
DN3370A	2N4338	ESM4303	2N5459	G118AP	G118AK	H11-5040-8	IH5040MJ/883B
DN3370B	2N4338	ESM4304	2N5458	G123AL	G123AL	H11-5041-2	IH5041MJE
DN3436A	2N4341	ESM4445	2N5432	G123AP	G123AK	H11-5041-5	IH5041CJE
DN3436B	2N4222	ESM4446	2N5434	GET5457	2N5457	H11-5041-8	IH5041MJ/883B
DN3437A	2N4340	ESM4447	2N5432	GET5458	2N5458	H11-5042-2	IH5042MJE
DN3437B	2N4220	ESM4448	2N5434	GET5459	2N5459	H11-5042-5	IH5042CJE
DN3438A	2N4338	FE0654A	2N4386	HA2720	ICL8021	H11-5042-8	IH5142MJ/883B
DN3438B	2N4339	FE0654B	2N5485	HA7807	IT132	H11-5043-2	IH5143MJE
DN3458A	2N4341	FE100	2N3821	HA7809	IT132	H11-5043-5	IH5143CJE
DN3458B	2N4222	FE100A	2N3821	HD43871	ICM7050H	H11-5043-8	IH5143MJ/883B
DN3459A	2N4339	FE102	2N4119	HD43871	ICM7050G	H11-5044-2	IH5144MJE
DN3459B	2N4220	FE102A	2N4119	HDIG1030	3N163	H11-5044-5	IH5144CJE
DN3460A	2N4338	FE104	2N4118	HEP801	2N3822	H11-5044-8	IH5144MJ/883B
DN3460B	2N4220	FE104A	2N4118	HEP802	2N5484	H11-5045-2	IH5145MJE
DNX1	2N4338	FE1600	2N4092	HEP803	2N5019	H11-5045-5	IH5145CJE
DNX2	2N4338	FE200	2N3821	HEPF0021	2N5484	H11-5045-8	IH5145MJ/883B
DNX3	2N4869	FE201	2N3821	HEPF1035	IT176	H11-5046-2	IH5046CJE
DNX4	2N4869	FE204	2N3821	HEPF2004	2N5484	H11-5046-5	IH5046MJ/883B
DNX5	2N4868	FE300	2N3822	HEPF2005	2N5459	H11-5046-8	IH5047MJE
DNX6	2N4338	FE302	2N3821	HI0-0201-6	DG201C/D	H11-5047-2	IH5047CJE
DNX7	2N4416	FE304	2N3821	HI0-0381-6	DDM181C/D	H11-5047-5	IH5047MJ/883B
DNX8	2N4416	FE3B19	2N5484	HI0-0384-6	DGM184C/D	H11-5047-8	IH5149MJE
DNX9	2N4339	FE4302	2N5457	HI0-0387-6	DGM187C/D	H11-5049-2	IH5149CJE
DS0026	ICL7667	FE4303	2N5459	HI0-0390-6	DGM190C/D	H11-5049-5	IH5149MJ/883B
DS0026	ICL7667	FE4304	2N5458	HI0-0506-6	IH6116C/D	H11-5049-8	IH5149MJ/883B
DU4339	2N5397	FE5245	2N4416	HI0-0506A-6	IH5116C/D	H11-5050-2	IH5150MJE
DU4340	2N5398	FE5246	2N4484	HI0-0507-6	IH6216C/D	H11-5050-5	IH5150CJE
E100	2N5458	FE5247	2N5486	HI0-0507A-6	IH5216C/D	H11-5050-8	IH5150MJ/883B
E101	J204	FE5457	2N5457	HI0-0508-6	IH6108C/D	H11-5051-2	IH5151MJE
E102	2N5457	FE5458	2N5458	HI0-0508A-6	IH5108C/D	H11-5051-5	IH5151CJE
E103	2N5459	FE5459	2N5459	HI0-0509-6	IH6208C/D	H11-5051-8	IH5151MJ/883B
E105	J105	FE5484	2N5484	HI0-0509A-6	IH5208C/D	H12-0200-2	DG200AA
E106	J106	FE5485	2N5485	HI0-5040-6	IH5140C/D	H12-0200-4	DG200BA
E107	J107	FE5486	2N5486	HI0-5041-6	IH5141C/D	H12-0200-5	DG200CA
E108	J105	FF400	2N5457	HI0-5042-6	IH5142C/D	H12-0200-8	DG200AA/883B
E109	J106	FM1100	2N3954A	HI0-5043-6	IH5143C/D	H12-0381-2	DGM182AA
E110	J107	FM1100A	2N5906	HI0-5044-6	IH5144C/D	H12-0381-5	DGM181BA
E111	J111	FM1101A	2N5906	HI0-5045-6	IH5145C/D	H12-0381-8	DGM181AA/883B
E1115	ICL1115A	FM1102	2N5906	HI0-5046-6	IH5046C/D	H13-0200-2	DG200AJ
E111A	J111	FM1102A	2N5906	HI0-5047-6	IH5047C/D	H13-0201-5	DG201CJ
E112	J112	FM1103	2N3955	HI0-5049-6	IH5149C/D	H13-0381-5	DGM181CJ
E112A	J112	FM1103A	2N5906	HI0-5050-6	IH5150C/D	H13-0384-5	DGM184CJ
E113	J113	FM1104	2N3957	HI0-5051-6	IH5051C/D	H13-0390-5	DGM190CJ
E113A	J113	FM1104A	2N5909	HI1-0200-2	DG200AK	H13-0506-5	IH6116CPI
E114	J204	FM1105	2N3954A	HI1-0200-4	DG200BK	H13-0506A-5	IH5116CPI
E1151	ICM1115B	FM1105A	IT500	HI1-0200-5	DG200BK	H13-0507-5	IH6216CPI
E1426	ICM7050U	FM1106	2N3954A	HI1-0200-6	DG200C/D	H13-0507A-5	IH5216CPI
E174	J174	FM1106A	IT500	HI1-0200-8	DG200AK/883B	H13-0508-5	IH6108CPE
E175	J175	FM1107	2N3954	HI1-0201-2	DG201AK	H13-0508A-5	IH5108CPE
E176	J176	FM1107A	IT500	HI1-0201-4	DG201BK	H13-0509-5	IH6208CPE
E177	J177	FM1108	2N3955	HI1-0201-5	DG201BK	H13-0509A-5	IH5208CPE
E201	J201	FM1108A	IT502	HI1-0201-8	DG201AK/883B	ICL7611	ICL7611
E202	J202	FM1109	2N3957	HI1-0381-2	DGM182AK	ICL7612	ICL7612
E203	J203	FM1109A	IT503	HI1-0381-5	DGM181BK	ICL7621	ICL7621
E204	J204	FM1110	2N3955	HI1-0381-8	DGM182AK/883B	ICL7631	ICL7631
E210	2N5397	FM1110A	2N5908	HI1-0384-2	DGM185AK	ICL7641	ICL7641
E211	2N5397	FM1111	2N3957	HI1-0384-5	DGM184BK	ICL7642	ICL7642
E212	2N5397	FM1111A	2N5909	HI1-0384-8	DGM185AK/883B	ICL7650	ICL7650
E230	2N4867	FM1112	2N5196	HI1-0387-2	DGM188AK	ICL7652	ICL7652
E231	2N4868	FM11200	2N3954	HI1-0387-5	DGM187BK	ICL7660	ICL7660
E232	2N4869	FM11201	2N3954	HI1-0387-8	DGM188AK/883B	ICL7663	ICL7663
E270	J270	FM11202	2N3954	HI1-0390-2	DGM191AK	ICL7665	ICL7665
E271	J271	FM11203	2N3955A	HI1-0390-5	DGM190BK	ICL8069	ICL8069
E300	2N5397	FM11204	2N3955	HI1-0390-8	DGM191AK/883B	ICM7240	ICM7240
E304	2N5486	FM11205	2N3954	HI1-0506-2	IH6116MJ	ICM7242	ICM7242
E305	2N5484	FM11206	2N3954	HI1-0506-5	IH6116CJ	ICM7250	ICM7250
E308	J308	FM11207	2N3954	HI1-0506-8	IH6116MJ/883B	ICM7553	ICM7553
E309	J309	FM11208	2N3955A	HI1-0506A-2	IH5116MJ	ICM7556	ICM7556
E310	J310	FM11209	2N3955	HI1-0506A-5	IH5116JJI	ICN00M7555	ICM7555
E311	J310	FM11210	2N3955A	HI1-0506A-8	IH5116MJ/883B	ID100	ID100
E312	2N5397	FM11211	IT5911	HI1-0507-2	IH6216MJ	ID101	ID101
E400	2N3955	FM3954	2N3954	HI1-0507-5	IH6216CJ	IMF3954	2N3954
E401	2N3955	FM3954A	2N3954A	HI1-0507-8	IH6216MJ/883B	IMF3954A	2N3954A
E402	2N3957	FM3955	2N3955	HI1-0507A-2	IH5216MJ	IMF3955	2N3955
E410	2N3955	FM3955A	2N3955A	HI1-0507A-5	IH5216JJI	IMF3955A	2N3955A

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
IMF3956	2N3956	ITE2913	IT122	J113A	J113	J4869	2N4869
IMF3957	2N3957	ITE2914	IT122	J113A-18	J113	J4869A	2N4869A
IMF3958	2N3958	ITE2915	IT120	J114	2N5555	J4869RR	2N4869
IMF5911	IMF5911	ITE2916	IT120	J1401	IT501	J5103	2N5484
IMF5912	IMF5912	ITE2917	IT122	J1402	IT502	J5104	2N5485
IMF6485	IMF6485	ITE2918	IT122	J1403	IT503	J5105	2N5486
IT100	IT100	ITE2919	IT120	J1404	IT503	J5163	2N5486
IT101	IT101	ITE2920	IT120	J1405	IT504	K114-18	2N5555
IT108	ITE4416	ITE2936	IT120	J1406	IT505	K210-18	2N5397
IT109	ITE4416	ITE2937	IT120	J174	J174	K211-18	2N5397
IT120	IT120	ITE2972	IT122	J174-18	J174	K212-18	2N5397
IT120A	IT120A	ITE2973	IT122	J175	J175	K300-18	2N5397
IT121	IT121	ITE2974	IT120	J175-18	J175	K304-18	2N5486
IT122	IT122	ITE2975	IT120	J176	J176	K305-18	2N5484
IT126	IT126	ITE2976	IT120	J176-18	J176	K308-18	2N5484
IT127	IT127	ITE2977	IT120	J177	J177	K309-18	J309
IT128	IT128	ITE2978	IT120	J177-18	J177	K310-18	J310
IT129	IT129	ITE2979	IT120	J201	J201	KE3684	2N3684
IT130	IT130	ITE3066	2N3685	J201-18	J201	KE3685	2N3685
IT130A	IT130A	ITE3067	2N3686	J202	J202	KE3686	2N3686
IT131	IT131	ITE3068	2N3687	J202-18	J202	KE3687	2N3687
IT132	IT132	ITE3347	IT137	J203	J203	KE3823	2N3823
IT136	IT136	ITE3348	IT138	J203-18	J203	KE3970	ITE4391
IT137	IT137	ITE3349	IT138	J204	J204	KE3971	ITE4392
IT138	IT138	ITE3350	IT137	J204-18	J204	KE3972	ITE4393
IT139	IT139	ITE3351	IT138	J210	2N5397	KE4091	ITE4091
IT140	IT140	ITE3800	IT132	J211	2N5397	KE4092	ITE4092
IT1700	IT1700	ITE3800	IT132	J212	2N5397	KE4093	ITE4093
IT1701	3N172	ITE3802	IT132	J230	2N4867	KE4220	2N5457
IT1702	3N163	ITE3804	IT130	J231	2N4868	KE4221	2N5459
IT1750	IT1750	ITE3806	IT132	J232	2N4869	KE4222	2N5459
IT2700	3N165	ITE3807	IT132	J270	J270	KE4223	J204
IT2701	3N165	ITE3808	IT132	J270-18	J270	KE4391	ITE4391
IT400	2N4392	ITE3809	IT132	J271	J271	KE4392	ITE4392
IT500	IT500	ITE3810	IT130	J271-18	J271	KE4393	ITE4393
IT500P	IT500	ITE3811	IT130	J300	2N5397	KE4416	ITE4416
IT501	IT501	ITE3907	IT120	J304	2N5486	KE4856	ITE4391
IT501P	IT501	ITE3908	IT120	J305	2N5484	KE4857	ITE4392
IT502	IT502	ITE4017	IT139	J308	J308	KE4858	ITE4393
IT502P	IT502	ITE4018	IT139	J309	J309	KE4859	ITE4391
IT503	IT503	ITE4019	IT139	J310	J310	KE4860	ITE4392
IT503P	IT503	ITE4020	IT139	J315	2N5397	KE4861	ITE4393
IT504	IT504	ITE4021	IT139	J316	U309	KE510	ITE4393
IT505	IT505	ITE4022	IT139	J317	U310	KE5103	J204
IT550	IT550	ITE4023	IT137	J3970	ITE4391	KE5104	ITE4416
IT5911	IT5911	ITE4024	IT137	J3971	ITE4392	KE5105	ITE4416
IT5912	IT5912	ITE4025	IT137	J3972	ITE4393	KE511	ITE4392
ITC2972	IT122	ITE4091	ITE4091	J401	IT501	KH5196	2N5196
ITC2973	IT122	ITE4092	ITE4092	J402	IT502	KH5197	2N5197
ITC2974	IT120	ITE4093	ITE4093	J403	IT503	KH5198	2N5198
ITC2975	IT120	ITE4117	2N4117	J404	IT503	KH5199	2N5199
ITC2976	IT120	ITE4118	2N4118	J405	IT504	KS5183	ICM7259
ITC2977	IT120	ITE4119	2N4119	J406	IT505	KS5240B01H	ICM7245B
ITC2978	IT120	ITE4338	2N4338	J4091	ITE4091	KS5240B01J	ICM7245A
ITC2979	IT120	ITE4339	2N4339	J4092	ITE4092	KS5240B10H	ICM7245D
ITC3347	IT137	ITE4340	2N4340	J4093	ITE4093	KS5240B12H	ICM7245E
ITC3348	IT138	ITE4341	2N4341	J410	IT502	KS5240B20H	ICM7245F
ITC3349	IT139	ITE4391	ITE4391	J411	IT503	KS5240U01E	ICM7245U
ITC3350	IT137	ITE4392	ITE4392	J412	IT503	LDP603	2N4221
ITC3351	IT138	ITE4393	ITE4393	J420	IT5911	LDP604	2N4221
ITC3352	IT139	ITE4416	ITE4416	J421	IT5912	LDP605	2N4221
ITC3800	IT132	ITE4867	2N4867	J4220	J204	LF11201D	DG201AK
ITC3802	IT132	ITE4868	2N4868	J4221	J202	LF11201D/883	DG201AK/883B
ITC3804	IT130	ITE4869	2N4869	J4222	J203	LF11508D	IH6108MJ
ITC3806	IT132	J100	2N5458	J4223	J202	LF11508D/883	IH6108MJE/883B
ITC3807	IT132	J101	2N4338	J4224	J202	LF11509D	IH6208MJ
ITC3808	IT132	J102	2N4337	J430	J309(X2)	LF11509D/883	IH6208MJE/883B
ITC3809	IT132	J103	2N5459	J4302	2N4302	LF13201D	DG201BK
ITC3810	IT130	J105	J105	J4303	2N5459	LF13201M	DG201CJ
ITC3811	IT130	J105-18	J105	J4304	2N5458	LF13508D	IH6108CJE
ITC4017	IT139	J106	J106	J431	J310(X2)	LF13508N	IH6108CPE
ITC4018	IT139	J106-18	J106	J433	2N5457	LF13509D	IH6208CJE
ITC4019	IT139	J107	J107	J4338	2N5457	LF13509M	IH6208CPE
ITC4020	IT139	J107-18	J107	J4339	2N5457	LM113	ICL8069
ITC4021	IT139	J108	J105	J4391	ITE4391	LM114	IT120
ITC4022	IT139	J108-18	J105	J4392	ITE4392	LM114A	IT120A
ITC4023	IT137	J109	J106	J4393	ITE4393	LM114B	IT120A
ITC4024	IT137	J109-18	J106	J4416	ITE4416	LM114H	IT120
ITC4025	IT137	J110	J107	J4856	ITE4856	LM115	IT120
ITE2453	IT120	J110-18	J107	J4857	ITE4857	LM115A	IT120A
ITE2639	IT120	J111	J111	J4858	ITE4858	LM115AH	IT120A
ITE2640	IT122	J111-18	J111	J4859	ITE4859	LM115H	IT120
ITE2641	IT122	J111A	J111	J4860	ITE4860	LM185	ICL8069
ITE2642	IT120	J111A-18	J111	J4861	ITE4861	LM194	IT120A
ITE2643	IT122	J112	J112	J4867	2N4867	LM394	IT120A
ITE2644	IT122	J112-18	J112	J4867A	2N4867A	LM4250	LM4250
ITE2720	IT120	J112A	J112	J4867RR	2N4867	LM4250	ICL8021
ITE2721	IT122	J112A-18	J112	J4868	2N4868	LM555	ICM7555
ITE2722	IT120	J113	J113	J4868A	2N4868A	LM556	ICM7556
ITE2903	IT122	J113-18	J113	J4868RR	2N4868	LMC555	ICM7555

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
LMC556	ICM7556	M511	3N172	MD8002	IT120	MEM955B	3N190
LMC668	ICL7650	M511A	3N172	MD8003	IT122	MF510	2N4092
LS3069	2N5458	M517	3N163	MD918	IT122	MF803	2N4338
LS3070	2N5458	M58434P	ICM7038D	MD918A	IT122	MF818	2N4858
LS3071	2N5458	M58435P	ICM1115B	MD918B	IT122	MFE2000	2N4416
LS3458	J204	M58436-001P	ICM7050G	MD982	IT139	MFE2001	2N4416
LS3459	J204	M58437-001P	ICM7070L	MD984	IT139	MFE2004	2N4093
LS3460	J204	MA7807	IT132	MEF103	2N5457	MFE2005	2N4092
LS3684	2N3684	MA7809	IT132	MEF104	2N5459	MFE2006	2N4091
LS3685	2N3685	MAT-01AH	IT140	MEF3069	2N4341	MFE2007	2N4860
LS3686	2N3686	MAT-01FH	IT140	MEF3070	2N4339	MFE2008	2N4859
LS3687	2N3687	MAT-01GH	IT140	MEF3458	2N4341	MFE2009	2N4859
LS3819	2N5484	MAT-01H	IT140	MEF3459	2N4339	MFE2010	2N4859
LS3821	2N5457	MAX232	ICL232	MEF3460	2N4338	MFE2011	2N5433
LS3822	2N5458	MAX420	ICL420	MEF3684	2N3684	MFE2012	2N5434
LS3823	2N5458	MAX665	ICL7663	MEF3685	2N3685	MFE2012	2N5433
LS3921	2N3921	MAX665	ICL7665	MEF3686	2N3686	MFE2093	2N4338
LS3922	2N3922	MAX8211	ICL8211	MEF3687	2N3687	MFE2094	2N4339
LS3966	ITE4416	MAX8212	ICL8212	MEF3821	2N3821	MFE2095	2N4340
LS3967	ITE4416	MB101	ICM7245B	MEF3822	2N3822	MFE2133	2N4860
LS3968	ITE4416	MB103	ICM7245E	MEF3823	2N3823	MFE2912	2N5433
LS3969	ITE4416	MB105	ICM7245U	MEF3954	2N3954	MFE3002	3N170
LS4220	J204	MB107	ICM7245D	MEF3955	2N3955	MFE3003	3N170
LS4221	J203	MB108	ICM7245E	MEF3956	2N3956	MFE3020	3N166
LS4222	J203	MB143	ICM7245A	MEF3957	2N3957	MFE3021	3N166
LS4223	J202	MB144	ICM7245F	MEF3958	2N3958	MFE4007	2N3686
LS4224	J202	MB510	ICM1115B	MEF4223	2N4223	MFE4008	2N3686
LS4338	2N5457	MB511	ICM7050H	MEF4224	2N4224	MFE4009	2N3685
LS4339	2N5457	MB512	ICM7050H	MEF4391	ITE4391	MFE4010	2N2608
LS4340	2N5457	MB513	ICM7050G	MEF4392	ITE4392	MFE4011	2N2608
LS4341	2N5458	MB521	ITS9068	MEF4393	ITE4393	MFE4012	2N2609
LS4391	ITE4391	MB522	ITS9068	MEF4416	ITE4416	MFE823	IT1700
LS4392	ITE4392	MB531	ICM7050H	MEF4857	2N4856	MHW590	AD590
LS4393	ITE4393	MB533	ICM7050H	MEF4857	2N4857	MJ41	ICM1424C
LS4416	ITE4416	MB541	ICM7052	MEF4858	2N4858	MJ6	ICM7220
LS4856	ITE4091	MB542	ICM7052	MEF4859	2N4859	MK10	2N4416
LS4857	ITE4092	MB78	ICM7245U	MEF4860	2N4860	MM450H	MM450H
LS4858	ITE4093	MCCI14440	ICM1424C	MEF4861	2N4861	MM451H	MM451H
LS4859	ITE4091	MCCI14483	ICM7210	MEF5103	ITE4416	MM452D	MM452J
LS4860	ITE4092	MD1120	IT122	MEF5104	ITE4416	MM452F	MM452F
LS4861	ITE4093	MD1121	IT122	MEF5105	ITE4416	MM455H	MM455H
LS5103	2N5484	MD1122	IT122	MEF5245	ITE4416	MM550H	MM550H
LS5104	2N5485	MD1123	IT139	MEF5246	2N5484	MM551H	MM551H
LS5105	2N5486	MD1129	IT129	MEF5247	2N5486	MM552D	MM552J
LS5245	ITE4416	MD1130	IT139	MEF5248	2N5486	MM552F	MM552F
LS5246	2N5484	MD2218	IT129	MEF5284	2N5484	MM555H	MM555H
LS5247	2N5486	MD2218A	IT129	MEF5285	2N5485	MMF1	2N5197
LS5248	2N5486	MD2219	IT129	MEF5286	2N5486	MMF2	2N3921
LS5358	J204	MD2219A	IT129	MEF5561	U401	MMF3	2N5198
LS5359	J204	MD2369	IT129	MEF5562	U402	MMF4	2N3922
LS5360	J202	MD2369A	IT129	MEF5563	U403	MMF5	2N5199
LS5361	J202	MD2369B	IT122	MEM511	3N172	MMF6	2N3955A
LS5362	J203	MD2904	IT139	MEM511A	3N172	MMT3823	2N3823
LS5363	J203	MD2904A	IT139	MEM511C	3N172	MN6091	ICM7038B
LS5364	J203	MD2905	IT139	MEM517	3N172	MN6092A	ICM7038E
LS5391	2N4867A	MD2905A	IT139	MEM517A	3N172	MN6093	ICM7051A
LS5392	2N4868A	MD2974	IT120	MEM517B	3N172	MN6252	ICM7050G
LS5393	2N4869A	MD2975	IT120	MEM517C	3N172	MP301	IT124
LS5394	2N4869A	MD2976	IT120	MEM550	3N189	MP302	IT124
LS5395	2N4869A	MD2979	IT120	MEM550C	3N189	MP303	IT124
LS5396	2N4869A	MD3008	IT120	MEM550F	3N189	MP310	2N4045
LS5457	2N5457	MD3250	IT132	MEM551	3N190	MP311	2N4045
LS5458	2N5458	MD3250A	IT131	MEM551C	3N189	MP312	2N4044
LS5459	2N5459	MD3251	IT132	MEM556	3N172	MP313	IT124
LS5484	2N5484	MD3251A	IT131	MEM556C	3N172	MP318	IT20A
LS5485	2N5485	MD3409	IT129	MEM560	3N161	MP350	IT132
LS5486	2N5486	MD3410	IT129	MEM560C	3N161	MP351	IT130
LS5556	2N3685	MD3467	IT139	MEM561	3N163	MP352	IT130
LS5557	2N3684	MD3725	IT129	MEM561C	3N163	MP358	IT130A
LS5558	2N3684	MD3762	IT139	MEM562	2N4351	MP360	IT132
LS5638	2N5638	MD4957	IT132	MEM562C	2N4351	MP361	IT130A
LS5639	2N5639	MD5000	IT132	MEM563	2N4351	MP362	IT130A
LS5640	2N5640	MD5000A	IT132	MEM563C	2N4351	MP3954	2N3954
LTC1044	ICL7650	MD5009	IT132	MEM711	M116	MP395A	2N3954A
LTC1052	ICL7652	MD7000	IT129	MEM712	M116	MP3955	2N3955
LTC1052	ICL7650	MD7001	IT139	MEM712A	M116	MP3956	2N3956
LTC1652	ICL7652	MD7002	IT122	MEM713	3N170	MP3957	2N3957
M103	3N161	MD7002A	IT122	MEM806	3N163	MP3958	2N3958
M104	3N161	MD7002B	IT122	MEM806A	3N163	MP5905	2N5905
M106	3N166	MD7003	IT132	MEM807	3N172	MP5906	2N5906
M107	3N189	MD7003A	IT132	MEM807A	3N172	MP5907	2N5907
M108	3N191	MD7003B	IT132	MEM814	3N161	MP5908	2N5908
M113	3N161	MD7004	IT129	MEM816	3N172	MP5909	2N5909
M114	3N161	MD7007	IT129	MEM817	3N172	MP5911	2N5911
M116	M116	MD7007A	IT129	MEM823	MFE823	MP5912	2N5912
M117	2N4351	MD7007B	IT129	MEM954	3N188	MP7520JD	AD7520JD
M119	3N161	MD708	IT129	MEM954A	3N188	MP7520JN	AD7520JN
M163	3N163	MD708A	IT129	MEM954B	3N186	MP7520KD	AD7520KD
M164	3N164	MD708B	IT129	MEM955	3N190	MP7520KN	AD7520KN
M5001	ICM7269	MD8001	IT120	MEM955A	3N190	MP7520LD	AD7520LD

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ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
MP7520LN	AD7520LN	NF5101	2N4867	PN3687	2N3687	SJM187BCC	JM38510/11105BCC
MP7520SD	AD7520SD	NF5102	2N4867	PN4091	ITE4091	SJM187BIC	JM38510/11105BIC
MP7520TD	AD7520TD	NF5103	2N4867	PN4092	ITE4092	SJM188BCC	JM38510/11106BCC
MP7520UD	AD7520UD	NF5111	2N4860	PN4093	ITE4093	SJM188BIC	JM38510/11106BIC
MP7521JD	AD7521JD	NF5163	2N4341	PN4220	J204	SJM190BEC	JM38510/11107BEC
MP7521JN	AD7521JN	NF520	2N3684	PN4221	J202	SJM191BEC	JM38510/11108BEC
MP7521KD	AD7521KD	NF521	2N3685	PN4222	J203	SL301AT	IT129
MP7521KN	AD7521KN	NF522	2N3686	PN4223	J204	SL301BT	IT129
MP7521LD	AD7521LD	NF523	2N3685	PN4224	J202	SL301CT	IT129
MP7521LN	AD7521LN	NF530	2N4341	PN4342	2N5461	SL301ET	IT129
MP7521SD	AD7521SD	NF5301	2N4118A	PN4360	2N5460	SL3600	IT129
MP7521TD	AD7521TD	NF5301-1	2N4117A	PN4391	ITE4391	SL362C	IT129
MP7521UD	AD7521UD	NF5301-2	2N4118A	PN4392	ITE4392	SM5011	ICM7050G
MP7523JN	AD7523JN	NF5301-3	2N4118A	PN4416	ITE4416	SM5510	ICM1115B
MP7523KN	AD7523KN	NF531	2N4339	PN4856	2N4856	SM5530B	ICM7070P
MP7523LN	AD7523LN	NF532	2N4341	PN4857	2N4857	SU2000	2N4340
MP7621AD	AD7541AD	NF533	2N4339	PN4858	2N4858	SU2020	2N3954
MP7621BD	AD7541BD	NF5457	2N5457	PN4859	2N4859	SU2021	2N3954
MP7621JN	AD7541JN	NF5458	2N5458	PN4860	2N4860	SU2022	2N3954
MP7621KN	AD7541KN	NF5459	2N5459	PN4861	2N4861	SU2023	2N3954
MP7621SD	AD7541SD	NF5484	2N5484	PN5033	2N5460	SU2024	2N3954
MP7621TD	AD7541TD	NF5485	2N5485	PTC151	2N5485	SU2025	2N3954
MP804	2N5520	NF5486	2N5486	PTC152	2N5486	SU2026	2N3954
MP830	2N5520	NF555	2N5484	RC595	ICM7555	SU2027	2N3954
MP831	2N5521	NF5638	2N5638	RC556	ICM7556	SU2028	2N3954
MP832	2N5522	NF5639	2N5639	S1424	ICM1424C	SU2029	2N5197
MP833	2N5523	NF5640	2N5640	SA2253	IT122	SU2029B	2N3954
MP835	2N3954	NF5653	2N4860	SA2254	IT122	SU2030	2N3955
MP836	2N3955	NF5654	2N4861	SA2255	IT122	SU2030	2N3954
MP837	2N3955	NF580	2N5432	SA2644	IT120	SU2031	2N5198
MP838	2N3956	NF581	2N5432	SA2648	IT120	SU2031	2N3954
MP839	2N3957	NF582	2N5433	SA2710	IT120	SU2032	2N3954
MP840	2N5520	NF583	2N5434	SA2711	IT120	SU2033	2N3954
MP841	2N5521	NF584	2N5433	SA2712	IT121	SU2034	2N3955
MP842	2N5523	NF585	2N4859	SA2713	IT121	SU2034	2N3954
MPF102	2N5486	NF6451	U310	SA2714	IT122	SU2035	2N3955
MPF103	2N5457	NF6452	U310	SA2715	IT120	SU2035	2N3954
MPF104	2N5458	NF6453	U310	SA2716	IT120	SU2074	2N3954
MPF105	2N5459	NF6454	U310	SA2717	IT121	SU2075	2N3954
MPF106	2N5485	NKT80111	2N4220	SA2718	IT122	SU2076	2N3954
MPF107	2N5486	NKT80112	2N4220	SA2719	IT120	SU2077	2N3955
MPF108	2N5486	NKT80113	2N4220	SA2720	IT121	SU2077B	2N3954
MPF109	2N5484	NKT80211	2N4339	SA2721	IT122	SU2078	2N3955
MPF111	2N5458	NKT80212	2N4339	SA2722	IT120	SU2079	2N3955
MPF112	2N5458	NKT80213	2N4339	SA2723	IT121	SU2080	U404
MPF161	2N5398	NKT80214	2N4339	SA2724	IT122	SU2081	U404
MPF208	2N3821	NKT80215	2N4339	SA2726	IT122	SU2098	2N5197
MPF209	2N3821	NKT80216	2N4339	SA2727	IT122	SU2098A	2N5197
MPF256	ITE4416	NKT80421	2N4220	SA2738	IT120A	SU2098B	2N5196
MPF4391	ITE4391	NKT80422	2N4220	SA2739	IT120A	SU2099	2N5197
MPF4392	ITE4392	NKT80423	2N4220	SCL54301	ICM1424C	SU2099A	2N5197
MPF4393	ITE4393	NKT80424	2N4220	SCL5478	ICM7269	SU2365	2N3954
MPF920	J310	NPC103	2N4338	SDF1001	2N5432	SU2365A	2N3954
MPF970	J175	NPC211N	2N4338	SDF1002	2N5433	SU2366	2N3955
MPF971	J175	NPC212N	2N4338	SDF1003	2N5434	SU2366A	2N3955
MS5010	ICL8069	NPC213N	2N4338	SDF500	2N5520	SU2367	2N3955
MSM5001	ICM7269	NPC214N	2N4339	SDF501	2N5520	SU2367A	2N3955
MSM5011	ICM1424C	NPC215N	2N4339	SDF502	2N5520	SU2368	2N3956
MSM5977	ICM1424C	NPC216N	2N4339	SDF503	2N5520	SU2368A	2N3956
MTF101	2N5484	NPB8301	2N3954	SDF504	2N5520	SU2369	2N3957
MTF102	2N5484	NPB8302	2N3955	SDF505	2N5520	SU2369A	2N3957
MTF103	2N5457	NPB8303	2N3956	SDF506	2N5520	SU2410	2N5907
MTF104	2N5459	OT3	2N4338	SDF507	2N5520	SU2411	2N5908
ND5700	IT120A	PI004	2N5116	SDF508	2N5520	SU2412	2N5909
ND5701	IT120A	PI005	2N5115	SDF509	2N5520	SU2652	U401
ND5702	IT120	PI027	2N5267	SDF510	2N3954	SU2652M	U401
NDF9401	IT500	PI028	2N5270	SDF511	2N3954	SU2653	U401
NDF9402	IT501	PI029	2N5270	SDF513	2N3954	SU2653M	U401
NDF9403	IT502	PI069E	2N2609	SDF514	2N3954	SU2654	U401
NDF9404	IT503	PI086E	2N5115	SDF661	IT122	SU2654M	U401
NDF9405	IT504	PI087E	2N5516	SDF662	IT122	SU2655	U402
NDF9406	IT500	PI117E	2N5640	SDF663	IT122	SU2655M	U402
NDF9407	IT501	PI118E	2N5641	SE555	ICM7555	SU2656	U404
NDF9408	IT502	PI119E	2N5640	SE556	ICM7556	SU2656M	U404
NDF9409	IT503	PF510	2N5115	SE53819	2N5484	SX3819	2N5484
NDF9410	IT504	PF5101	2N4867	SFT601	2N4338	SX3820	2N2608
NE555	ICM7955	PF5102	2N4867	SFT602	2N4338	TC8031P	ICM7038A
NE556	ICM7956	PF5103	2N4867	SFT603	2N4339	TC8032P	ICM7038B
NE590	AD590	PF511	2N5114	SFT604	2N4339	TC8051P	ICM7038B
NF3819	2N5484	PF5301	2N4118A	SG4250	LM4250	TC8052P	ICM7038E
NF4302	2N5457	PF5301-1	2N4117A	SI7135CPI	ICL7135CPI	TC8056PA	ICM1115B
NF4303	2N5459	PF5301-2	2N4118A	SI7652	ICL7652	TC8057P	ICM7038D
NF4304	2N5458	PF5301-3	2N4118A	SI7660	ICL7660	TD100	IT129
NF4445	2N5432	PLI091	2N3823	SI7661	ICL7662	TD101	IT129
NF4446	2N5433	PLI092	2N3823	SJM181BCC	JM38510/11101BCC	TD102	IT129
NF4447	2N5433	PLI093	2N3823	SJM181BIC	JM38510/11101BIC	TD200	IT129
NF4448	2N5433	PLI094	2N3823	SJM182BCC	JM38510/11102BCC	TD201	IT129
NF500	2N4224	PN3684	2N3684	SJM182BIC	JM38510/11102BIC	TD202	IT129
NF501	2N4416	PN3685	2N3685	SJM184BEC	JM38510/11103BEC	TD219	IT129
NF506	2N4416	PN3686	2N3686	SJM185BEC	JM38510/11104BEC	TD224	IT122

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ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERISL EQUIVALENT
TD225	IT122	TIS69	2N3955A	U1179	2N3821	U300	2N5114
TD226	IT122	TIS70	2N3956	U1180	2N4221	U3000	2N4341
TD227	IT122	TIS73	ITE4391	U1181	2N4220	U3001	2N4339
TD228	IT122	TIS74	ITE4392	U1182	2N3821	U3002	2N4338
TD229	IT122	TIS75	ITE4393	U1277	2N3684	U301	2N5115
TD230	IT121	TIS88	2N4416	U1278	2N3685	U3010	2N4341
TD231	IT121	TIS88A	2N4416	U1279	2N3686	U3011	2N4340
TD232	IT122	TIXS33	2N4392	U1280	2N3684	U3012	2N4338
TD233	IT122	TIXS35	2N4857	U1281	2N3822	U304	U304
TD234	IT122	TIXS36	2N4391	U1282	2N4341	U305	U305
TD235	IT122	TIXS41	2N4859	U1283	2N4340	U306	U306
TD236	IT122	TIXS42	2N5639	U1284	2N4341	U308	U308
TD237	IT122	TIXS59	2N5459	U1285	2N4220	U309	U309
TD238	IT122	TIXS78	2N4341	U1286	2N4341	U310	U310
TD239	IT122	TIXS79	2N4341	U1287	2N4092	U311	U310
TD240	IT121	TL182CL	DGM182BA	U1321	2N4860	U312	2N5397
TD241	IT121	TL182CN	DGM182CJ	U1322	2N3822	U314	2N5397
TD242	IT120A	TL182IL	DGM182BA	U1323	2N3822	U315	2N5397
TD243	IT120A	TL182IN	DGM182CJ	U1324	2N3687	U316	U309
TD244	IT129	TL182ML	DGM182AA	U1325	2N3686	U317	U310
TD245	IT129	TL185CJ	IHS045CJE	U133	2N2608	U320	2N5433
TD246	IT129	TL185CN	IHS045CPE	U1420	2N3821	U321	2N5434
TD247	IT129	TL185JL	IHS045CJE	U1421	2N3822	U322	2N5433
TD248	IT129	TL185IN	IHS045CPE	U1422	2N3822	U328	**
TD250	IT120A	TL185MJ	IHS045MJE	U146	2N2608	U329	**
TD2905	IT139	TL188CL	IHS042CTW	U147	2N2608	U330	**
TD400	IT139	TL188CN	IHS042CPE	U148	2N2608	U331	**
TD401	IT139	TL188IL	IHS042CTW	U149	2N2609	U350	**
TD402	IT139	TL188IN	IHS042CPE	U168	2N2609	U401	U401
TD500	IT139	TL188ML	IHS042MTW	U1714	2N4340	U402	U402
TD501	IT139	TL191CJ	IHS043CJE	U1715	2N4340	U403	U403
TD502	IT139	TL191CN	IHS043CPE	U182	2N4857	U404	U404
TD509	IT132	TL191JL	IHS043CJE	U183	2N3824	U405	U405
TD510	IT132	TL191IN	IHS043CPE	U1837E	2N5486	U406	U406
TD511	IT132	TL191MJ	IHS043MJE	U184	2N5397	U410	2N3955
TD512	IT132	TLC251	ICL7612	U1897E	U1897	U411	2N3956
TD513	IT132	TLC251	ICL7611	U1898E	U1898	U412	2N3958
TD514	IT132	TLC252	ICL7621	U1899E	U1899	U421	2N5908
TD517	IT132	TLC254	ICL7642	U191	2N4338	U422	2N5908
TD518	IT132	TLC271	ICL7612	U198	2N4340	U423	2N5909
TD519	IT132	TLC271	ICL7611	U199	2N4341	U424	2N5908
TD520	IT139	TLC272	ICL7621	U194E	2N4416	U425	2N5908
TD521	IT139	TLC274	ICL7642	U200	2N4861	U426	2N5909
TD522	IT139	TLC274	ICL7641	U201	2N4860	U430	J309(X2)
TD523	IT139	TLC555	ICM7555	U202	2N4859	U431	J310(X2)
TD524	IT139	TLC556	ICM7556	U2047E	2N4416	U440	IT5911
TD525	IT132	TN4117	2N4117	U221	2N4391	U441	IT5912
TD526	IT132	TN4117A	2N4117A	U222	2N4391	UA555	ICM7555
TD527	IT131	TN4118	2N4118	U231	U231	UA556	ICM7556
TD528	IT131	TN4118A	2N4118A	U232	U232	UC100	2N3684
TD5432	2N5432	TN4119	2N4119	U233	U233	UC110	2N3685
TD5433	2N5433	TN4119A	2N4119A	U234	U234	UC115	2N4340
TD5434	2N5434	TN4339	2N4339	U235	U235	UC120	2N3686
TD550	IT129	TN4339	2N4339	U240	2N5432	UC130	2N3687
TD5902	2N5902	TN4340	2N4340	U241	2N5433	UC155	2N4416
TD5902A	2N5902	TN4341	2N4341	U242	2N5432	UC1700	3N163
TD5903	2N5903	TN5277	2N4341	U243	2N5433	UC1764	3N163
TD5903A	2N5903	TN5278	2N4341	U244	2N5433	UC20	2N3686
TD5904	2N5904	TP5114	2N5114	U248	2N5902	UC200	2N3824
TD5904A	2N5904	TP5115	2N5115	U248A	2N5906	UC201	2N3824
TD5905	2N5905	TP5116	2N5116	U249	2N5903	UC21	2N3687
TD5905A	2N5905	TSC426	ICL7667	U249A	2N5907	UC210	2N4416
TD5906	2N5906	TSC7106CJL	ICL7106CJL	U250	2N5904	UC2130	2N5452
TD5906A	2N5906	TSC7106CPL	ICL7106CPL	U250A	2N5908	UC2132	2N5453
TD5907	2N5907	TSC7106RCPL	ICL7106RCPL	U251	2N5905	UC2134	2N5454
TD5907A	2N5907	TSC7107CJL	ICL7107CJL	U251A	2N5909	UC2136	2N5454
TD5908	2N5908	TSC7107CPL	ICL7107CPL	U252	IT5911	UC2138	2N5454
TD5908A	2N5908	TSC7107RCPL	ICL7107RCPL	U253	IT5912	UC2139	2N3958
TD5909	2N5909	TSC7109CJL	ICL7109CJL	U254	2N4859	UC2147	2N3958
TD5909A	2N5909	TSC7109JL	ICL7109JL	U255	2N4860	UC2148	2N3958
TD5911	IT5911	TSC7109MJL	ICL7109MJL	U256	2N4861	UC2149	2N3958
TD5911A	IT5911	TSC7116CJL	ICL7116CJL	U257	U257	UC220	2N3822
TD5912	IT5912	TSC7116CPL	ICL7116CPL	U257/TO-71	U257/TO-71	UC240	2N4869
TD5912A	IT5912	TSC7117CJL	ICL7117CJL	U266	2N4856	UC241	2N4869
TD700	IT122	TSC7117CPL	ICL7117CPL	U273	2N4118A	UC250	2N4091
TD701	IT122	TSC7126CJL	ICL7126CJL	U273A	2N4118A	UC251	2N4392
TD709	IT122	TSC7126RCPL	ICL7126RCPL	U274	2N4119A	UC2766	3N166
TD710	IT122	TSC7135CJL	ICL7135CJL	U274A	2N4119A	UC300	2N2608
TD711	IT122	TSC7135CPI	ICL7135CPI	U275	2N4119A	UC310	2N2607
TD713	IT122	TSC7650	ICL7650	U275A	2N4119A	UC320	2N2607
TIS14	2N4340	TSC7660	ICL7660	U280	2N5452	UC330	2N2607
TIS20	2N3954	TSC9491	ICL8069	U281	2N5453	UC340	2N2607
TIS26	2N3954	TT-590	AD590	U282	2N5453	UC40	2N2608
TIS27	2N3955	U110	2N2608	U283	2N5453	UC400	2N5270
TIS34	2N5486	U111	2N2608	U284	2N5454	UC401	2N5116
TIS41	2N4859	U112	2N2608	U285	2N5454	UC41	2N2608
TIS42	2N4393	U113	2N2608	U290	2N5432	UC410	2N5268
TIS58	2N5484	U114	2N2608	U291	2N5434	UC420	2N5267
TIS59	2N5486	U1177	2N4220	U295	2N5432	UC450	2N5114
TIS68	2N3955A	U1178	2N3821	U296	2N5434	UC451	2N5116

**CONSULT FACTORY

XXIX

ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT	ALTERNATE SOURCE PRODUCT	INTERSIL EQUIVALENT
UC588 UC703 UC704 UC705 UC707	2N4416 2N4220 2N4220 2N4224 2N4860						
UC714 UC714E UC734 UC734E UC751	2N3822 2N4341 2N4416 2N4416 2N4340						
UC752 UC753 UC754 UC755 UC756	2N4340 2N4341 2N4340 2N4341 2N4340						
UC805 UC807 UC814 UC851 UC853	2N5270 2N5115 2N5270 2N2608 2N2608						
UC854 UC855 UCN-4111M UCN-4112M UCN-4113M	2N2608 2N2609 ICM7038C ICM7051A ICM7038B						
UPD1952P UPD1962C UPD1963C UPD815C UPD816C	ICM7220MFA ICM7050G ICM7050 ICM7038E ICM7038B						
UPD820C UPD833G UT100 UT101 UXC2910	ICM1115B ICM7223 2N5397 2N5397 IT126						
VCR10N VCR11N VCR12N VCR13N VCR20N	2N4869 VNR11N 2N3958 2N3958 2N4341						
VCR2N VCR3P VCR4N VCR5P VCR6P	VCR2N VCR2P VCR4N VCR5P VCR6P						
VCR7N VF28 VF811 VF815 VFW40	VCR7N 2N4392 2N4858 2N4858 IT122						
VFW40A VR-8069 W245A W245B W245C	IT120 ICL8069 ITE4416 ITE4416 ITE4416						
W300 W300A W300B W300C W300D	2N5398 2N5397 2N5397 2N5397 2N5398						
WG-8038 WK5457 WK5458 WK5459 XR555	ICL8038 2N5457 2N5458 2N5459 ICM7555						
XR556 XR8038 ZDT40 ZDT41 ZDT42	ICM7556 ICL8038 IT129 IT129 IT129						
ZDT44 ZDT45	IT129 IT129						

Section 1 — Selector Guides

INTERSIL YOUR COMPLETE SOURCE FOR INTEGRATED SIGNAL PROCESSING COMPONENTS

Intersil, founded in 1967, is a wholly owned subsidiary of General Electric Company U.S.A., and a component of the GE/RCA Solid State Division, headquartered in Somerville, New Jersey.

Intersil's Semiconductor Business charter has been the development of an extensive analog/digital component complement focusing on the commercial, industrial, instrumentation and military markets. Based on the most advanced innovations in CMOS technology, it has established itself as a frontrunner in products serving the explosive data conversion and digital signal processing marketplace.

Intersil's expanding product line is headed by a respected portfolio of data converters, analog switches and multiplexers, display drivers, digital controls and sophisticated linear circuitry. Technology innovations include an operational 130-volt CMOS process with 3μ and 4μ feature sizes, and a 5-inch wafer fabrication system. Intersil's new digital signal processing products use advanced very large scale integration (AVLSI) processes with a 1.5μ feature size, and a 1.25μ process is in the final stages of development. Intersil's next-generation MOS/bipolar (BiMOS) process that combines the best attributes of MOS and bipolar processing on a single chip.

Product quality and reliability are fundamental considerations in Intersil's manufacturing facilities. Clean-room environments, Class 100 in critical wafer processing areas and Class 5000 in manufacturing areas, easily meet recommended standards. A high degree of factory automation has phased out slower and less reliable manual operations.

And, overall, a high dedication to customer service reflects the Intersil commitment to be one of the most respected semiconductor suppliers in the industry.

The proliferation of microprocessors and the general swing to digital signal processing has caused an explosion in the need for data acquisition products. In turn, the associated data translation requirements from the analog world to digital format, and vice versa, have spurred considerable effort toward making A/D-D/A converters progressively smaller, cheaper, and more reliable. Toward that end, Intersil has developed a family of integrated circuits designed to meet the varying requirements of the system designer.

All of Intersil's converters are fabricated using CMOS technology, which equates, inherently, to extremely low power consumption. All maximize on-chip componentry for the intended application in order to reduce the external component requirements to a minimum.

To facilitate acquaintance with Intersil products, a number of A/D converters are available in the form of low-cost Eval-

uation Kits. The Kits combine the specified converter with a number of additional components required to assemble a functional subsystem. They include components PC board and appropriate assembly instructions.

Content:

- A/D Converter Systems
 - Digital Multimeter Instrumentation Bargraph
- A/D Converters
 - Display Type μ P Type
- Evaluation Kits
- D/A Converters

Analog To Digital Converters

A/D Converters with Display Drivers

Integrating A/D Converters are characterized by high inherent accuracy, excellent noise rejection, non-critical associated components and low cost. They are relatively slow with conversion rates up to 30 conversions per second. All Intersil integrating converters provide fully precise Auto-Zero, Auto-Polarity (including \pm null indication), single reference operation, very high input impedance, true input integration over a constant period (for maximum EMI rejection), fully ratiometric operation, overrange indication and a medium-quality built-in reference.

3 $\frac{3}{4}$ Digit LCD 7-Segment Displays **ICL7139** For Low-Cost Autoranging Digital Multimeters **ICL7149**

These monolithic autoranging multimeter circuits always display the results of a conversion on the correct range. Measure AC and DC voltage, DC current and resistance in the following ranges:

- DC Voltage — 400mV, 4V, 40V, 400V
- AC Voltage — 400V (ICL7139)
- (Optional ac circuit with 2 ranges (ICL7149))
- DC Current — 4mA, 40mA, 400mA, 4A
- Resistance — 4K, 40K, 400K, 4M

On-chip duplex display drive includes three decimal points and 11 annunciators. Less than 20mW power dissipation provides 1000 hours typical battery life. Continuity output drives piezoelectric beeper. Guaranteed zero reading for 0 Volts input on all ranges.

101-Segment LCD Bargraph A-D Converter **ICL7182**

The ICL7182 is a complete analog-to-digital converter that directly drives a multiplexed liquid crystal display. Included are a charge-balance A/D converter, a 2.56V bandgap reference, display decode and driver, and a 50KHz oscillator. A complete analog bargraph generator requires only the addition of an external display, two passive components and a 350 μ A, 5V power source.

4 $\frac{1}{2}$ Digit LCD 7-Segment Displays **ICL7129** For High Quality Battery Operated Instruments

Very high performance A/D Converter for direct drive of multiplexed LCDs. Ideal for high-resolution, hand-held digital multimeters and other battery powered (9V) instruments. Accuracy is better than 0.005% of full scale, with resolution down to 10 μ V per count. Overrange and underange outputs permit design of autoranging instruments with 10:1 range changing input. Instant continuity check gives both visual indication and a logic-level output for enabling an external audible transducer. Provisions for detection and indication of Low Battery condition.

For 3 $\frac{1}{2}$ Digit LCD/LED 7-Segment Displays **ICL7106/7116, ICL7136/7126** **ICL7137-7107, ICL7117**

These 3 $\frac{1}{2}$ -digit A/D Converters contain all the necessary active devices on a single CMOS integrated circuit. Included are A/D Converters, 7-segment decoders, display drivers, a reference and a clock. All feature auto-zero to less than 10 μ V, zero-input drift of less than 1 μ V/ $^{\circ}$ C, input bias current of 10pA max., and rollover and linearity errors of less than one count. True differential inputs and reference provide wide applications versatility over a temperature range from 0 to +70 $^{\circ}$ C.

For Liquid Crystal Displays	ICL7106 — Direct drive; 0.1 to 15 conversions per second; supply current = 1.8mA max.
	ICL7116 — Similar to above, but features a Hold Reading input which allows indefinite retention of a display reading
	ICL7136 — Low-power version of ICL7106, but with maximum supply current of only 100 μ A gives 8000 hours typical 9V battery life. 0.1 to 4 conversions per second.
	ICL7126 — Earlier version of ICL7136. Recommended for exact replacement requirement only.
For LED Displays	ICL7137 — Low-power, direct drive ADC for common-anode, 7-segment LED displays. Requires positive and negative 5V supply voltages, with supply current of less than 200 μ A. 0.1 to 4 conversions per second.
	ICL7107 — Earlier version of ICL7137. Recommended for exact replacement requirements only.
	ICL7117 — Similar to ICL7137, but requires 1.8mA (max.) of supply current and provides up to 15 conversions per second. Hold Reading allows indefinite retention of display reading.

μP Compatible A/D Converters

Integrating

Intersil integrating μP-Compatible A/D Converters contain both monolithic versions and 2-chip sets, with up to 16-bit resolution. All utilize CMOS processing for lowest power consumption, and all have a guaranteed accuracy of 1 count.

4½ Digit A/D Converter with Multiplexed BCD Output

ICL7135

This precision A/D Converter is suitable for display applications as well as microprocessor and UART interface. Count accuracy of ±1 in 20,000 makes it ideal for the visual display DVM/DPM market, while added functions such as Strobe, Run/Hold, Busy, Overrange and Underrange allow operation in more sophisticated systems. Chip contains all necessary active devices except display drivers, reference and clock. All outputs are TTL compatible.

12-Bit μP-Compatible A/D Converter

ICL7109

This monolithic 12-bit binary A/D converter may be directly accessed under control of two byte-Enable inputs, and a Chip Select input, for a simple parallel-bus interface. A UART handshake mode operates in conjunction with industry-standard UARTs to provide serial data transmission. Operates at up to 30 conversions per second. Available in three temperature ranges: -55°C to +125°C, -25°C to +85°C, and 0°C to +70°C.

14/16-Bit μP-Compatible Two-Chip A/D Converter Sets

**ICL8052/ICL7104
ICL8068/ICL7104**

Available with 14-bit and 16-bit resolution, this two-chip set performs the analog signal processing on one chip (ICL8052 or ICL8068) and the switching and digital functions on the other (ICL7104). A combination of chips may be ordered for either 14-bit or 16-bit operation and for low-noise or low-leakage alternatives. All combinations, however, offer three-state, latched, binary outputs plus Polarity and Overrange. All combinations operate over a temperature range of 0°C to +70°C.

ICL7104-14	14-Bit ADC
ICL7104-16	16-Bit ADC
ICL8052	Low input leakage current (30pA max.) analog processing circuit. Typical noise = 30μV.
ICL8068	Low noise (2μV typical) analog processing circuit. Input leakage current = 165pA.

Successive Approximation

Successive Approximation Converters are generally associated with high speed, ranging up to 100,000 conversions per second. All Intersil Successive Approximation Converters are μP compatible.

8-Bit A/D Converters for 8080A MPU Interface

**ADC0802
ADC0803
ADC0804**

This Successive Approximation A/D Converter was designed to operate with the 8080A or Z-80 microprocessor control bus via three-state outputs with no additional interfacing requirements, but permits easy interface to most other microprocessors. Differential analog input range is 0 to 5V with a single +5V supply. With a conversion time of less than 100 μs, it provides up to 8888 conversions per second with a clock frequency of 640KHz.

ADC0802	Total unadjusted error = ± 1/2LSB
ADC0803	Total full-scale adjust error = ± 1/2LSB
ADC0804	Total unadjusted error = ± 1LSB

14-Bit High-Speed A/D Converter

ICL7115

With a conversion speed of 40μs (max), this 14-bit ADC has a byte organized digital output for bus interface to 8 and 16-bit microprocessor systems. CMOS circuitry, thin-film resistors and an on-chip PROM calibration table combine to achieve 13-bit linearity (without laser trimming) and a very low (60mW) power dissipation. Available in three temperature ranges: 0°C to +70°C, -25°C to +85°C, and -55°C to +125°C.

Digital to Analog Converters

Intersil supplies digital-to-analog converters (D/A converters) with 8-bit, 10-bit, 12-bit, 14-bit and 16-bit resolution. All are four-quadrant multiplying D/A converters using thin-film

resistors and CMOS circuitry for high accuracy and low power dissipation. All are microcomputer compatible, with input protection against damage from electrostatic discharge.

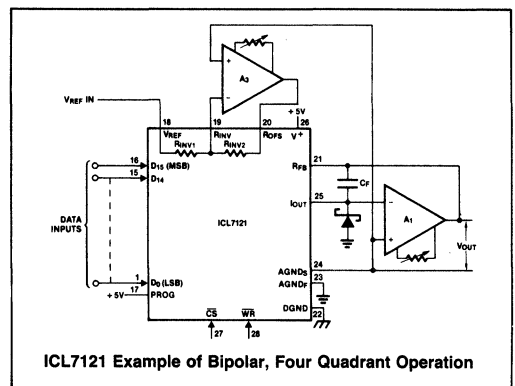
Type	Digital Input Format	Settling Time (To 0.05% FS)	Output Current (Max)	Non Linearity% FS (Suffix)	Gain Error (% FS)	Gain Linearity Tempo PPM/°C	Power Supply $\frac{V(TYP)}{I(Max)}$
8-BIT							
AD7523	Binary/Offset Binary	200 ns (Max)	$\pm \frac{V_{REFA}}{10K\Omega}$	0.2% (J) 0.1% (K) 0.05% (L)	1.5% (Max)	10 2	$\frac{+15V}{100\mu A}$
10-BIT							
AD7520* AD7530	Binary/Offset Binary	500 ns (Typ)	$\pm \frac{V_{REFA}}{10K\Omega}$	0.2% (J) 0.1% (K) 0.05% (L)	0.3% (Max)	10 2	$\frac{+15V}{2mA}$
AD7533	Binary/Offset Binary	600 ns (Typ)	$\pm \frac{V_{REFA}}{10K\Omega}$	0.2% (J) 0.1% (K) 0.05% (L)	1.4% (Max)	10 2	$\frac{+15V}{2mA}$
12-BIT							
AD7521* AD7531	Binary/Offset Binary	500 ns (Typ)	$\pm \frac{V_{REFA}}{10K\Omega}$	0.2% (J) 0.1% (K) 0.05% (L)	0.3% (Typ)	10 2	$\frac{+15V}{2mA}$
AD7541	Binary/Offset Binary	1 μ s (Max)	$\pm \frac{V_{REFA}}{10K\Omega}$	0.02% (J) 0.01% (K) 0.01% (L)	0.3% (Max)	— 2	$\frac{+15V}{2mA}$
14-BIT							
ICL7134	Binary μ 2's Complement B	3 μ s (Max)	$\pm \frac{V_{REFA}}{10K\Omega}$	0.1% (J) 0.006% (K) 0.003% (L)	0.02% (J) 0.012% (K) 0.006% (L)	5 1	$\frac{+15V}{0.5mA}$

*AD7530 and AD7531 are identical to AD7520 and AD7521, respectively, except for output leakage current and feed-through specifications.

ICL7121 16-Bit μ P-Compatible D/A Converter

This high-performance 16-bit D/A converter achieves 0.003% linearity without laser trimming by combining the converter with a unique on-chip PROM-controlled correction circuit. This insures long-term stability and accuracy even over the full military temperature range. Silicon-gate CMOS circuitry keeps the power dissipation to a very low 25 mW.

Designed and programmed for bipolar operation, it can be connected to provide a true 2's complement input transfer function without any external resistors. Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. The device is available in a 28-pin CERDIP package in both 0°C to +70°C, and -55°C to +125°C temperature ranges.



A/D Converter Evaluation Kits

The following Evaluation Kits are available to permit rapid assembly, testing and evaluation of specific A/D converters. Each Kit comes complete with a prewired printed circuit board and all necessary components (except batteries) for a suitable demonstration circuit. Assembly and operating instruction are supplied.

ICL7129EV/Kit

This Kit permits evaluation of the Intersil ICL7129 4½ digit, LCD, 7-segment display in a functional DC digital voltmeter circuit. It includes the A/D converter IC, a liquid crystal display, a 120KHz crystal, a voltage reference IC and all necessary passive components and hardware items.

- ICL7139EV/Kit
- ICL7106/07EV/Kit
- ICL7136EV/Kit

ICL7106EV/Kit, ICL7107EV/Kit

To ease evaluation of these unique circuits, Intersil offers kits which contain all the necessary components to build a 3½ digit panel meter. Two kits are offered, the ICL7106EV/Kit and the ICL7107EV/Kit. Both contain the appropriate IC, a circuit board, a display (LCD for the ICL7106EV/Kit, LEDs for the ICL7107EV/Kit), passive components, and miscellaneous hardware.

ICL7136EV/Kit

Intersil's ICL7136 is a low-power version of the 3½ digit LCD A/D converters. This Kit contains all the components necessary to build a battery-operated 3½ digit panel meter. It includes the A/D converter IC, a circuit board, liquid crystal display, passive components, and miscellaneous hardware.

ICL7139EV/Kit

This Kit uses the Intersil ICL7139 to build a complete 3¾ digit autoranging multimeter, capable of directly measuring voltage, current, and resistance. Included in the Kit are the ICL7139 IC, circuit board, liquid crystal display, and all necessary passive components and hardware.

ICL7182EV/Kit

With this Kit, the user can easily evaluate a 101 segment LCD bargraph A/D converter using Intersil's ICL7182. Everything necessary to build the completed circuit is included in the Kit: The ICL7182 IC, circuit board, 101 segment LCD, passive components, and miscellaneous hardware.

GRAPHICS

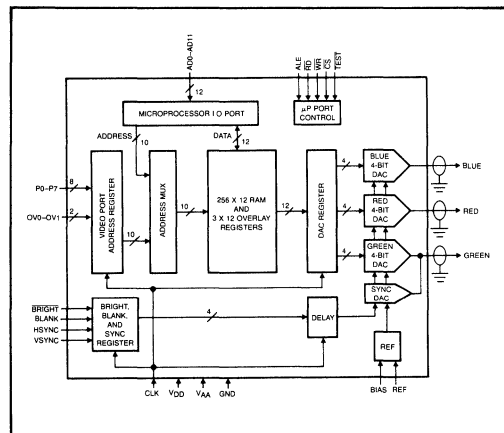
IM2110 256 x 12 Color Lookup Table and DAC

The IM2110 is designed specifically for color graphics, and integrates a 256 x 12 color lookup table, three 4-bit DACs, and a microprocessor interface.

The color lookup table is stored in a RAM and may be written asynchronously by an 8- or 16-bit microprocessor. Three overlay registers are provided for overlaying cursors, grids, text, etc. The chip is capable of simultaneously displaying 256 out of 4096 colors at a 25 MHz rate, for a 640 x 480 non-interlaced display.

The IM2110 generates RS-343-A compatible red, green and blue analog signals, and is capable of driving doubly-terminated 75 Ω coaxial cables directly.

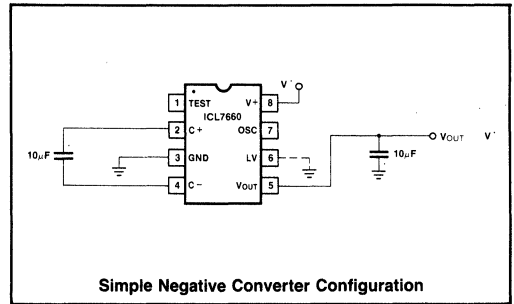
The circuit is available in a 40-pin plastic package and operates over a temperature range of 0°C to +70°C.



ICL7660S/ICL7662S
Voltage Converters

These voltage converters transform a positive (+) input voltage from a power supply to a corresponding negative (-) output, resulting in complementary output voltages of -1.5V to -12.0V for the ICL7660, and -4.5V to -20V for the ICL7662. Only two non-critical external capacitors are needed to perform the conversions. The converters can also be connected as voltage doublers and will generate output voltages of +18.6V and 22.6V, respectively.

Available in two temperature ranges, 0°C to 70°C and -55°C to +125°C, and three packages, TO-99, 8-pin MiniDIP (ICL7660S only) and SOIC.



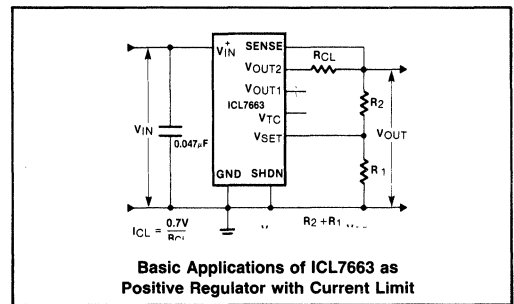
Simple Negative Converter Configuration

ICL7663S
Programmable Micropower Voltage Regulators

The ICL7663 (positive) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 16V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4µA, regardless of load.

Output current sensing and remote shutdown are available, thereby providing protection for the regulators and the circuits they power.

The ICL7663 is available in 8-pin plastic, TO-99 metal can, CERDIP, and SOIC packages, in two temperature ranges — 0°C to +70°C and -25°C to +85°C.

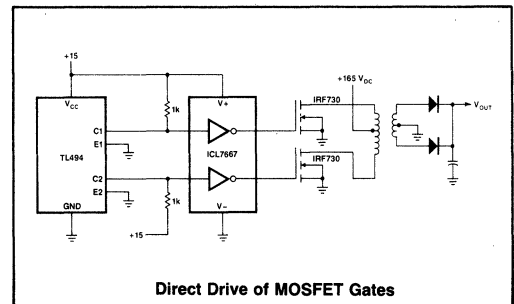


Basic Applications of ICL7663 as Positive Regulator with Current Limit

ICL7667
Dual Power MOSFET Driver

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters.

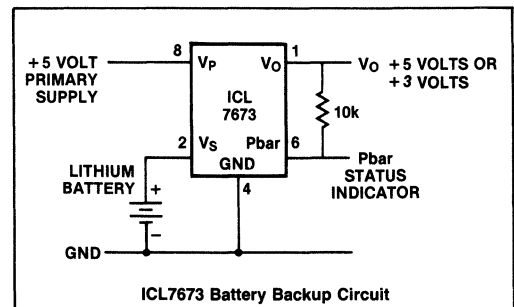
Available in commercial and military temperature ranges, and in 8-pin plastic DIP, SOIC, CERDIP and TO-99 metal packages.



Direct Drive of MOSFET Gates

ICL7673
Automatic Battery Back-Up Switch

The ICL7673 automatically switches from the main power supply to a battery back-up supply in the event of power loss, and back again when power is restored. Ideal for on-board battery back-up for real-time clocks, timers, volatile RAMs, or portable instruments. Available in 8-pin MiniDIP and TO-99 packages.



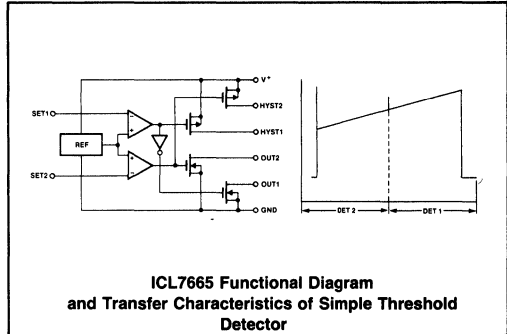
ICL7673 Battery Backup Circuit

ICL7665

Micropower Under/Over Voltage Detector

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only 3µA, typical, for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and corrections.

Available in 8-lead CERDIP, MiniDIP, TO-99 metal can and SOIC packages with a temperature range from 0°C to 70°C.



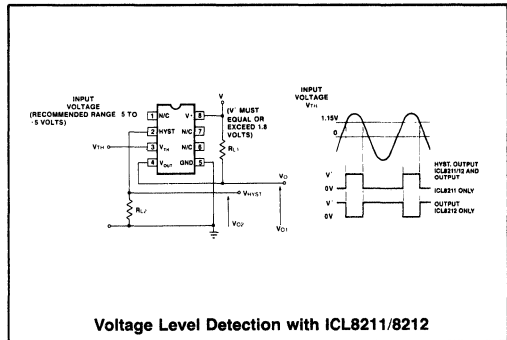
ICL8211/ICL8212

Programmable Voltage Detector

These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

The ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminals is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Available in 8-lead MiniDip, TO-99 metal can and SOIC packages, in commercial and military temperature ranges.



ICL8069

Low Voltage Reference

ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50µA. Applications include analog-to-digital converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

Available in TO-92 plastic and TO-52 metal packages with 0°C to 70°C and -55°C to +125°C temperature ranges (metal only) and with temperature coefficients of 0.005 and 0.01°C.

ICL7677

Power Fail Detector

ICL7677 is a Power Fail Detector which can be incorporated either into the primary or the secondary side of a power supply to give the fastest possible power-fail indication. On the primary side, it can simultaneously monitor AC line voltage, the reservoir capacitor voltage, primary side current and ambient temperature. On the secondary side, it can simultaneously monitor up to two DC voltages, one load current and the ambient temperature. The circuit has an on-chip bandgap-voltage reference to conveniently program the detection thresholds.

ICL7675/ICL7676

Switched-Mode Power Supply Controller Set

The ICL7675/7676 two-chip set provides the necessary control circuitry for regulation of an isolated flyback type switching power supply. Specifically designed to operate in this type of configuration, the Intersil controller chip-set is trimmed to provide a regulated 5V output. The isolated flyback converter is the most widely used configuration for switched-mode power supplies in 50W to 150W range because of its simplicity. The chip-set features soft-start and power switch over-current protection.

ICL7680

5V to ±15V Voltage Converter

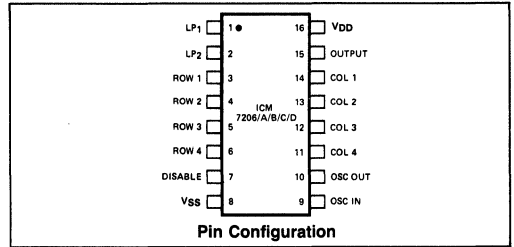
The ICL7680 is a simple boost-type switched-mode converter/inverter chip using minimal external components to convert +5V to ±15V regulated outputs. An internal oscillator is user programmable to optimize efficiency for various load conditions. The device features current limiting protection together with external shut-down.

ICM7206

Touch-Tone Encoder

The ICM7206 is a 2-of-8 sinewave DTMF generator for use in telephone dialing systems. Requires a 3.58 MHz crystal and will operate with both 3x4 and 4x4 keypads. This low-cost circuit has a high current bipolar output driver providing low harmonic distortion. Supply voltage range is 3 to 6 volts with power dissipation of less than 5.5mW at 5.5 volts. Single and dual tone capability.

Available in 16-pin plastic DIP with a temperature range from -40°C to +85°C.

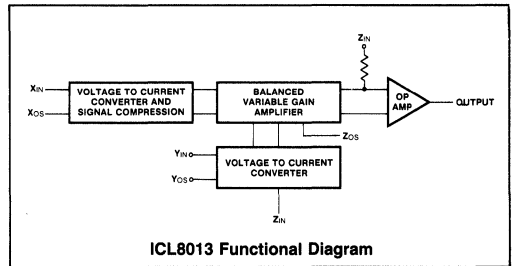


ICL8013

Four Quadrant Analog Multiplier

The ICL8013 is a bipolar, four-quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to time gain accuracy, offset voltage and feedthrough performance.

Available in 10-pin TO-100 metal package in both commercial and military temperature ranges.

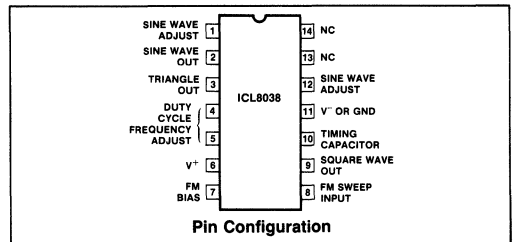


ICL8038

Precision Waveform Generator/Voltage Controlled Oscillator

The ICL8038 Waveform Generator is capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300KHz using either resistors or capacitors, and frequency modulation, and sweeping can be accomplished with an external voltage.

The 14-pin CERDIP package is available with 0°C to +70°C, and -55°C to +125°C temperature ranges.



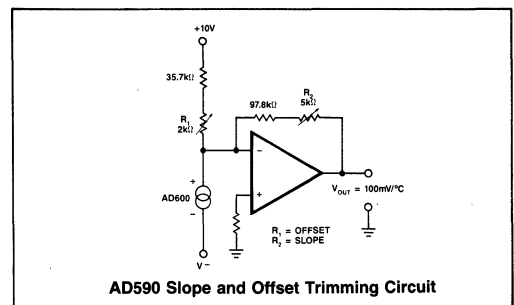
AD590

2-Wire, Current-Output Temperature Transducer

The AD590 is a 2-wire integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1 μA/K for supply voltages between +4V and +30V. Laser trimming of the chip's thin-film resistors is used to calibrate the device to 298.2 μA output at 298.2°K (+25°C).

The AD590 could be used in any temperature-sensing application between -55°C and +150°C in which conventional electrical temperature sensors are currently employed.

Plastic (TO-92) packaged device covers temperature ranges from 0°C to +70°C; Metal packaged device (TO-52) covers -55°C to +150°C range. With slope and offset trimming circuit it is possible to adjust devices to give less than 0.1% error over the temperature range from 0°C to 90°C.



Special Purpose Amplifiers

ICL420/421 ± 15V Chopper Stabilized Operational Amplifier

These chopper-stabilized CMOS operational amplifiers are designed for signal conditioning, precision and instrumentation type applications. They offer a wide input and operating supply range, allowing virtual plug-in replacements for conventional lower-performance amplifiers, requiring only two additional external capacitors.

The ICL420 (8-pin) and ICL421 (14-pin) devices draw a maximum supply current of 2 mA and are available in all temperature ranges.

ICL7605/7606 Commutating Auto-Zero (CAZ) Instrumentation Amplifier, CMOS

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

Available in three temperature ranges.

ICL8048/ICL8049 Log/Antilog Amplifier

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change in the input.

ICL8063 Power Transistor Driver/Amplifier

The ICL8063 is a monolithic transistor driver and amplifier primarily intended for driving complementary output stages.

The ICL8063 takes the output levels (typical $\pm 11V$) from an op amp and boosts them to $\pm 30V$ to drive power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 supply up to 100mA to the base leads of the external power transistors.

Content:

- Special Purpose Amplifiers
 - Instrumentation Amplifiers
 - Log/Antilog Amplifiers
 - Drive Amplifier for Power Transistors
- Operational Amplifiers
 - General Purpose
 - Low Power
 - Low Input Offset Voltage
 - Low Input Bias Current

Features:

- Input Offset Voltage — $2\mu V$
- Input Offset Voltage Drift — $0.2\mu V/Year$
- Common Mode Input Voltage Range — 0.3V Above Supply Rail
- Common Mode Rejection Ratio — 100 dB
- Operates at Supply Voltages As Low As $\pm 2V$
- Short Circuit Protection On Outputs
- Compensated (ICL7605) or Uncompensated (ICL7606) Versions

Features:

- $\frac{1}{2}\%$ Full Scale Accuracy
- Temperature Compensated for $0^{\circ}C$ to $+70^{\circ}C$
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual JFET-Input Op-Amps

Features:

- When Used in Conjunction with General-Purpose Op Amps and External Complementary Power Transistors, System Can Deliver >50 Watts to External Loads
- Built-In Safe Area Protection and Short-Circuit Protection
- Built-In $\pm 13V$ Regulators to Power Op Amps or Other External Functions

Operational Amplifiers

Intersil offers a range of single and multiple monolithic operational amplifiers suitable for a number of specific applications categories. Included are bipolar Super-Beta and Chopper-Stabilized CMOS devices for very low input offset requirement, a selection of PMOS and JFET-input devices

for very low bias currents, as well as general-purpose and low-power amplifiers for a broad range of applications.

All monolithic operational amplifiers are available in a variety of packages and in die form.

Operational Amplifiers: General Purpose

Type	Description	V _{OS} (mV Max)	I _{BIAS} (pA Max)	Slew Rate (V/μs)	GBW (MHz)	Compensation	V _{SUPPLY} (V Max)	Temperature Range (°C)
SINGLES								
ICL7611	CMOS, Selectable I _Q	2, 5, 15	50	1.6	1.4	INT	±9	0 to +70 -55 to +125
ICL8007M	JFET Input Op-Amp	20	20	6	1.0	INT	±18	-55 to +125
ICL8007C	JFET Input Op-Amp	50	50	6	1.0	INT	±18	0 to +70
DUALS								
ICL7621	CMOS, Fixed I _Q	2, 5, 15	50	0.16	0.48	INT	±9	0 to +70 -55 to +125
ICL8043M	JFET Input Op-Amp	20	20	6	1.0	INT	±18	-55 to +125
ICL8043C	JFET Input Op-Amp	50	50	6	1.0	INT	±18	0 to +70
TRIPLES								
ICL7631	CMOS, Selectable I _Q	5, 10, 20	50	1.6	1.4	INT	±9	0 to +70 -55 to +125
QUADS								
ICL7641	CMOS, Fixed I _Q	5, 10, 20	50	1.6	1.4	INT	±9	0 to +70 -55 to +125

Low Power

Type	Description	I _{QUIESCENT} (Per Channel) (μA Typ)	V _{SUPPLY} (V Max)	V _{OS} (mV Max)	I _{BIAS} (nA Max)	GBW (MHz)	Compensation	Temperature Range (°C)
SINGLES								
ICL7611	CMOS, Selectable I _Q	10	±9	2, 5, 15	0.05	0.044	INT	0 to +70 & -55 to +125
ICL7612	CMOS, Extended CMVR	10	±9	2, 5, 15	0.05	0.044	INT	-55 to +125
ICL8021M	Bipolar, Selectable I _Q	30	±18	3	20	0.27	INT	-55 to +125
ICL8021C	Bipolar, Selectable I _Q	30	±18	6	30	0.27	INT	0 to +70
TRIPLES								
ICL7631	CMOS, Selectable I _Q	10	±9	5, 10, 20	0.05	0.044	INT	0 to +70 & -55 to +125
ICL8023M	Triple 8021M	30	±18	3	20	0.27	INT	-55 to +125
ICL8023C	Triple 8021C	30	±18	6	30	0.27	INT	0 to +70
QUADS								
ICL7642	CMOS, Fixed I _Q	10	±9	5, 10, 20	0.05	0.044	INT	0 to +70 & -55 to +125

Operational Amplifiers: Special Purpose

Low/Ultra-low Input Offset Voltage

Type	Description	V _{OS} (μ V Max)	Δ V _{OS} / Δ T (μ V/ $^{\circ}$ C) (Max)	Δ V _{OS} / Δ t (nV/month) (Typ)	I _{BIAS} (pA Max)	GBW (MHz)	V _{SUPPLY} (V Max)	Temperature Range ($^{\circ}$ C)
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SINGLES

ICL7650C	CMOS, Chopper-stabilized	± 8	± 0.02	100	20	2.0	± 9	0 to +70
ICL7650I	CMOS, Chopper-stabilized	± 10	± 0.02	100	50	2.0	± 9	-25 to +85
ICL7650M	CMOS, Chopper-stabilized	± 20	± 0.03	100	500	2.0	± 9	-55 to +125
ICL7652C	Low-noise 7650C	± 7	± 0.01	100	30	0.5	± 9	0 to +70
ICL7652I	Low-noise 7650I	± 10	± 0.02	100	30	0.5	± 9	-25 to +85
ICL7652M	Low-noise 7650M	± 50	± 0.1	100	500	0.5	± 9	-55 to +125

Low Input Bias Current

Type	Description	I _{BIAS} (pA Max)	I _{OS} (pA Typ)	V _{OS} (mV Max)	GBW (MHz)	Compensation	V _{SUPPLY} (V Max)	Temperature Range ($^{\circ}$ C)
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SINGLES

ICL7611	CMOS, Selectable I _Q	50	0.5	2, 5, 15	1.4	INT	± 9	0 to +70 &
ICL7612	CMOS, Extended CMVR	50	0.5	2, 5, 15	1.4	INT	± 9	-55 to +125
ICL8007M	JFET Input Op-Amp	20	0.5	20	1.0	INT	± 18	-55 to +125
ICL8007AM	JFET Input, Low Bias	4.0	0.2	30	1.0	INT	± 18	-55 to +125
ICL8007C	JFET Input Op-Amp	50	0.5	50	1.0	INT	± 18	0 to +70
ICL8007AC	JFET Input, Low Bias	4.0	0.2	30	1.0	INT	± 18	0 to +70
ICH8500	PMOS Input	0.1	—	50	0.7	INT	± 18	-25 to +85
ICH8500A	PMOS Input, Low Bias	0.01	—	50	0.7	INT	± 18	-25 to +85

DUALS

ICL7621	CMOS, Fixed I _Q	50	0.5	2, 5, 15	0.48	INT	± 9	0 to +70 & -55 to +125
ICL8043M	JFET Input Op-Amp	20	0.5	20	1.0	INT	± 18	-55 to +125
ICL8043C	JFET Input Op-Amp	50	0.5	50	1.0	INT	± 18	0 to +70

TRIPLES

ICL7631	CMOS, Selectable I _Q	50	0.5	5, 10, 20	1.4	INT	± 9	0 to +70 & -55 to +125
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QUADS

ICL7641	CMOS, Fixed I _Q	50	0.5	5, 10, 20	1.4	INT	± 9	0 to +70 &
ICL7642	CMOS, Fixed I _Q	50	0.5	5, 10, 20	0.044	INT	± 9	-55 to +125

Content:

General Purpose Analog Switches
 Drivers for FET Switches
 Low Cost, Virtual Ground Switch Family
 RF/Video Switch Family
 Multiplexers

General Purpose Analog Switches

Intersil offers two general-purpose switch lines, each with various switch configurations. The first consists of bipolar drivers controlling an associated set of field-effect switching transistors in a multi-chip structure that provides a wide choice of parameters at low cost. The second is a monolithic CMOS structure capable of improved performance and

greater reliability. All have break-before-make switch action.

All switches are available in commercial and military temperature ranges. Package options include Plastic DIP, CER-DIP, Flat Pack and Metal Can (not all options are available for all device types).

General Purpose Analog Switches

Switch Family	Special Features	Switch Type	Switch Parameters				Analog Voltage Range (V _{SUPPLY} = ±15V)
			R _{DS(ON)} (Ω Max)	I _{D(OFF)} (nA Max)	t _{ON} (ns Max)	t _{OFF} (ns Max)	

Multichip

DG123-125	Inverting/non-inverting logic inputs	PMOS	600	4	300	1000	—
DG126-154 DG139-164	Dual Channel Single Channel	N-JFET	10 15 30 50 80	10 10 1 1 1	1000 1000 600 600 600	2500 2500 1600 1600 1600	—
DG180-191	Mature, Industry-standard switch, JAN38510 Approved	N-JFET	10 30 75	10 1 1	300 150 250	250 130 130	-7.5 to +15 -7.5 to +15 -10 to +15

Monolithic

DGM181-191	Monolithic replacement for DG180 family	CMOS	50 75	2.0 0.5	250 450	200 250	-15 to +15 -15 to +15
DG200/201	Industry-standard low cost	CMOS	70/80	2.0	1000	500	-15 to +15
DG211 DG212	Inverting Noninverting	CMOS	175	5.0	1000	500	-15 to +15
DG300A-303A	TTL compatible, low power	CMOS	50	1.0	300	250	-15 to +15
IH311 IH312	High Speed Inverting Noninverting	CMOS CMOS	175	100	300	150	-15 to +15
IH5040-47 IH5048-51 IH5052-53	Low quiescent current Low R _{DS(ON)}	CMOS	75 40 75	1.0 1.0 1.0	750 500 500	350 250 250	-10 to +10 -10 to +10 -11 to +11
IH5140-45	High speed, low power, low leakage	CMOS	50	0.5	100	75	-11 to +11
IH5148-51	Low R _{DS(ON)} , high speed, low power	CMOS	25	0.5	250 350 500	200 250 250	-14 to +14

Separate Driver/Switch Combinations

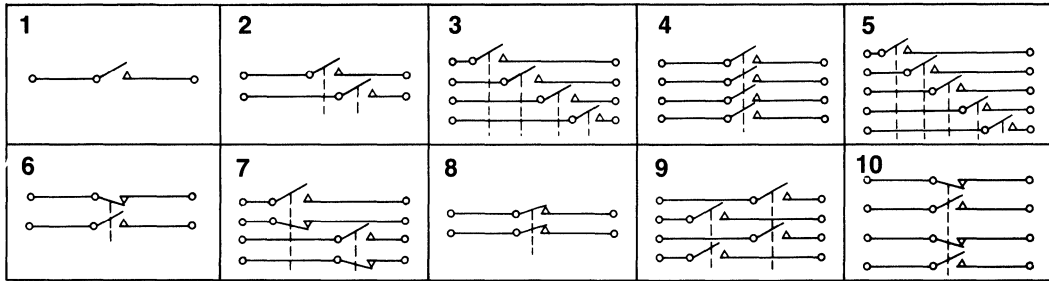
IH6201	TTL level translator/driver	N-JFET	30	0.5	50 (Typ)	150 (Typ)	15 p-p (Min)
IH401/A	Low charge injection switch		30/50	0.5	50 (Typ)	150 (Typ)	20 p-p (Min)

Drivers for FET Switches

Monolithic bipolar drivers convert low-level positive logic to high-level positive and negative voltages necessary to drive FET switches.

Type	Number of Channels	Output Swing		t _{ON} ns Max	t _{OFF} ns Max
		Positive (V Max)	Negative (V Max)		
D123	6 TTL/DTL	V _{Supply}	-19.7	250	400-800
D125	6 TTL	V _{Supply}	-19.7	250	400-800
D129	4 TTL/DTL	V _{Supply}	-19.3	250	1000
IH6201	2 TTL	+14.0	-14.0	200	300

Switch Configurations



Switch Configuration (Diagram)

SPST (1)	Dual SPST (2)	Quad SPST (3)	4PST (4)	Five SPST (5)	SPDT (6)	Dual SPDT (7)	DPST (8)	Dual DPST (9)	DPDT (10)
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				DG123 DG125					
	DG141 DG151 DG133 DG152 DG134				DG146 DG161 DG144 DG162 DG143			DG140 DG153 DG129 DG154 DG126	DG145 DG163 DG139 DG164 DG142
	DG180 DG181 DG182				DG186 DG187 DG188	DG189 DG190 DG191		DG183 DG184 DG185	

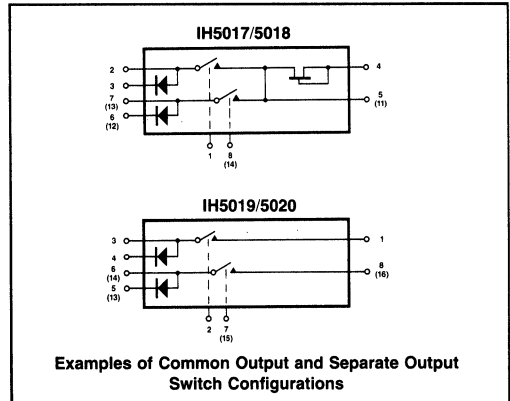
	DGM182					DGM190 DGM191		DGM184 DGM185	
	DG200	DG201							
		DG211 DG212							
DG301A	DG300A					DG303A		DG302A	
		IH311 IH312							
IH5040	IH5041 IH5048	IH5052/53	IH5047		IH5042 IH5050	IH5043 IH5051	IH5044	IH5045 IH5049	IH5046
IH5140	IH5141				IH5142	IH5143	IH5144	IH5145	
	IH5148				IH5150	IH5151		IH5149	

		IH401/A							
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Virtual Ground Switches, JFETs (P-Channel)

Each package contains up to four channels of analog gating designed to eliminate the need for external drivers. The odd-numbered devices are designed to be driven directly from TTL open-collector logic (15V). Each channel simulates a SPDT switch. The parts are intended for high-performance multiplexing and commutating use. All have turn-on/turn-off times of 500 ns and a leakage current ($I_{D(off)}$) of 0.2 nA.

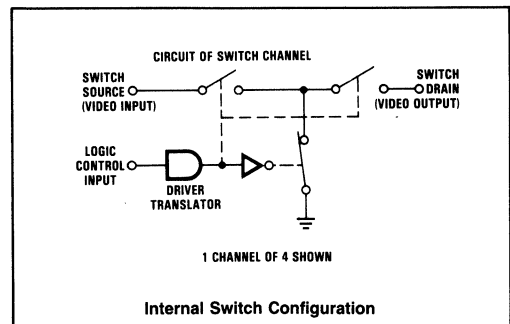
Switch Configuration				Special Features	Switch Type	$r_{DS(on)}$ (Ω Max)
SPST	Dual SPST	Triple SPST	Quad SPST			
IH5021	IH5017	IH5013	IH5009	Common Output	P-JFET	100
IH5022	IH5018	IH5014	IH5010			150
IH5023	IH5019	IH5015	IH5011	Separate Output	P-JFET	100
IH5024	IH5020	IH5016	IH5012			150



RF/Video Switches, CMOS

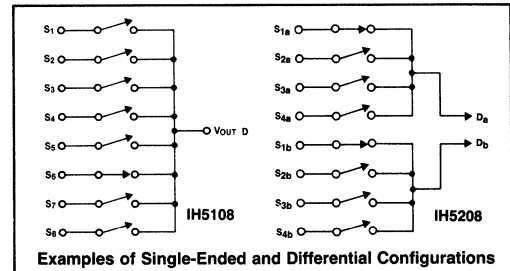
Designed for high-frequency operation, these switches utilize a "T" configuration where a shunt switch is closed when the switch is open. This provides superior isolation between input and output and greatly improves performance in the video and RF region. Switch attenuation varies less than 3 dB from dc to 100 MHz. Available in three (commercial and military) temperature ranges and in 14-pin plastic DIP and 10-pin TO-100 metal package.

Switch Configuration		$r_{DS(on)}$ (Ω Max)	$I_{D(off)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)
Dual SPST	Quad SPST				
IH5341	IH5352	75	1.0	300	150



Multiplexers

Intersil provides three multiplexer families — a standard IH6000 Family featuring low $r_{DS(ON)}$; an equivalent fault-protected IH5000 series which ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ± 25 V, even with the supply voltage at zero; a multiplex/demultiplex unit with on-board data latches and control pins for microprocessor interface. All utilize CMOS technology for extremely low quiescent operating current.



Switch Family	Special Features	$r_{DS(ON)}$ (Ω Max)	$I_{D(OFF)}$ (nA Max)	t_{ON} (ns Max)	t_{OFF} (ns Max)	Analog Voltage Range $V_{Supply} = (\pm 15V)$	Configuration			
							8 Channel Single Ended	4 Channel Differential	16 Channel Single Ended	8 Channel Differential
IH5000 Series	Industry standard pinouts, fault protection up to $\pm 25V$ input, low leakage, low input current	900	1.0	1500	1000	-25 to +25 (Input)	IH5108	IH5208		
		1000	1.0	1500	1000	-25 to +25 (Input)			IH5116	IH5216
IH6000 Series	Industrial standard pinouts, low leakage, low $r_{DS(ON)}$ break before make switching	300	2.0	1500	1000	-14 to +14	IH6108	IH6208		
		600	2.0	1500	1000	-14 to +14			IH6116	IH6216
IH9108	Multiplexer/Demultiplexer with latches for μP based systems	120	2.5	2000	1000	-50 to +50	IH9108			



Switching Transistors

Junction FETs — N-Channel

PART NUMBER	PACKAGE**	$r_{DS(ON)}$ Ω		V_p V		I_{GSS} pA	BV_{GSS} V	$I_{D(OFF)}$ pA	I_{DSS} mA		t_{ap} ns	C_{rss} pF	C_{iss} pF	COMMENTS
		Max	Min	Max	Max	Min	Max	Min	Max	Max	Max	Max	Max	
2N3824	TO-72	250		8.0	-100	-50						3	6	High Isolation
2N3970	TO-18	30	-4.0	-10.0	-250	-40		250	50	150	50	6	25	High Isolation
2N3971	TO-18	60	-2.0	-5.0	-250	-40		250	25	75	90	6	25	High Isolation
2N3972	TO-18	100	-0.5	-3.0	-250	-40		250	5	30	180	6	25	High Isolation
* 2N4091	TO-18	30	-5.0	-10.0	-200	-40		200	30		65	5	16	High Isolation
2N4091A	TO-18	30	-5.0	-10.0	-40	-50		200	30		65	5	16	High Isolation
* 2N4092	TO-18	50	-2.0	-7.0	-200	-40		200	15		95	5	16	High Isolation
2N4092A	TO-18	50	-2.0	-7.0	40	-50		200	15		95	5	16	High Isolation
* 2N4093	TO-18	80	-1.0	-5.0	-200	-40		200	8		140	5	16	High Isolation
2N4093A	TO-18	80	-1.0	-5.0	40	-50		200	8		140	5	16	High Isolation
2N4391	TO-18	30	-4.0	-10.0	-100	-40		100	50	150	55	3.5	14	High Isolation
2N4392	TO-18	60	-2.0	-5.0	-100	-40		100	25	75	75	3.5	14	High Isolation
2N4393	TO-18	100	-0.5	-3.0	-100	-40		100	5	30	100	3.5	14	High Isolation
* 2N4856	TO-18	25	-4.0	-10.0	-250	-40		250	50		34	8	18	High Isolation
* 2N4857	TO-18	40	-2.0	-6.0	-250	-40		250	20	100	60	8	18	High Isolation
* 2N4858	TO-18	60	-0.8	-4.0	-250	-40		250	8	80	120	8	18	High Isolation
* 2N4859	TO-18	25	-4.0	-10.0	-250	-30		250	50		34	8	18	High Isolation
* 2N4860	TO-18	40	-2.0	-6.0	-250	-30		250	20	100	60	8	18	High Isolation
* 2N4861	TO-18	60	-0.8	-4.0	-250	-30		250	8	80	120	8	18	High Isolation
2N4978	TO-18	20	-2.0	-8.0	-500	-30		500	15		55	8	35	Low $r_{DS(ON)}$
2N5432	TO-52	5	-4.0	-10.0	-200	-25		200	150		41	15	30	Low $r_{DS(ON)}$
2N5433	TO-52	7	-3.0	-9.0	-200	-25		200	100		41	15	30	Low $r_{DS(ON)}$
2N5434	TO-52	10	-1.0	-4.0	-200	-25		200	30		41	15	30	Low $r_{DS(ON)}$
2N5555	TO-92	150		-10.0	-1nA	-25	10nA	15			35	1.2	5	Low Cost
2N5638	TO-92	30		-12.0	-1nA	-30	1nA	50			24	4	10	Low Cost
2N5639	TO-92	60		-8.0	-1nA	-30	1nA	25			44	4	10	Low Cost
2N5640	TO-92	100		-6.0	-1nA	-30	1nA	5			63	4	10	Low Cost
2N5653	TO-92	50		-12.0	-1nA	-30	1nA	40			24	3.5	10	Low Cost
2N5654	TO-92	100		-8.0	-1nA	-30	1nA	15			44	3.5	10	Low Cost
ITE4091	TO-92	30	-5.0	-10.0	-200	-40		200	30		65	5	16	Low Cost
ITE4092	TO-92	50	-2.0	-7.0	-200	-40		200	15		95	5	16	Low Cost
ITE4093	TO-92	80	-1.0	-5.0	-200	-40		200	8		140	5	16	Low Cost
ITE4391	TO-92	30	-4.0	-10.0	-100	-40		100	50	150	55	3.5	14	Low Cost
ITE4392	TO-92	60	-2.0	-5.0	-100	-40		100	25	75	75	3.5	14	Low Cost
ITE4393	TO-92	100	-0.5	-3.0	-100	-40		100	5	30	100	3.5	14	Low Cost

*Also available as JAN/JANTX & JANTXV

(Continued Next Page)

**Most TO-92's are available lead formed to a TO-18 or TO-5 pinout. Also available in tape and reel (EIA STD RS-468).

Switching Transistors (Continued)

Junction FETs — N-Channel (Continued)

PART NUMBER	PACKAGE**	$r_{DS(ON)}$ Ω		V_p V		I_{GSS} pA	BV_{GSS} V	$I_{D(OFF)}$ pA		I_{DSS} mA		t_{ap} ns	C_{rss} pF	C_{iss} pF	COMMENTS
		Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	Max	Max		
J105	TO-92	3	-4.5	-10.0	-3nA	-25	3nA	500	20						Lowest $r_{DS(ON)}$
J106	TO-92	6	-2.0	-6.0	-3nA	-25	3nA	200	20						Lowest $r_{DS(ON)}$
J107	TO-92	8	-0.5	-4.5	-3nA	-25	3nA	100	20						Lowest $r_{DS(ON)}$
J108	TO-92	8	-3.0	-10.0	-3nA	-25	3nA	80	41						Low Cost
J109	TO-92	12	-2.0	-6.0	-3nA	-25	3nA	40	41						Low Cost
J110	TO-92	18	-0.5	-4.0	-3nA	-25	3nA	10	41						Low Cost
J111	TO-92	30	-3.0	-10.0	-1nA	-35	1nA	20	48						Lowest Cost
J112	TO-92	50	-1.0	-5.0	-1nA	-35	1nA	5	48						Lowest Cost
J113	TO-92	100	-0.5	-3.0	-1nA	-35	1nA	2	48						Lowest Cost
J114	TO-92	150		-10.0	-1nA	-25	1nA	15	26						Low Cost
PN4091	TO-92	30	-5.0	-10.0	-200	-40	200	30	65	5	16				Low Cost
PN4092	TO-92	50	-2.0	-7.0	-200	-40	200	15	95	5	16				Low Cost
PN4093	TO-92	80	-1.0	-5.0	-200	-40	200	8	140	5	16				Low Cost
PN5432	TO-92	5	-4.0	-10.0	-200	-25	200	150	41	15	30				Lowest $r_{DS(ON)}$
PN5433	TO-92	7	-3.0	-9.0	-200	-25	200	100	41	15	30				Lowest $r_{DS(ON)}$
PN5434	TO-92	10	-1.0	-4.0	-200	-25	200	30	41	15	30				Lowest $r_{DS(ON)}$
U200	TO-18	150	-0.5	-3.0	-1nA	-30	1nA	3	25		8	30			Low Cost
U201	TO-18	75	-1.5	-5.0	-1nA	-30	1nA	15	75		8	30			Low Cost
U202	TO-18	50	-3.5	-10.0	-1nA	-30	1nA	30	150		8	30			Low Cost
U1897	TO-92	30	-5.0	-10.0	-400	-40	200	30	65	5	16				Low Cost
U1898	TO-92	50	-2.0	-7.0	-400	-40	200	15	95	5	16				Low Cost
U1899	TO-92	80	-1.0	-5.0	-400	-40	200	8	140	5	16				Low Cost

Junction FETs — P-Channel

2N3382	TO-72	300	1.0	5.0	15nA	30	-2nA	-3	-30			16 typ			Low $r_{DS(ON)}$
2N3384	TO-72	180	4.0	5.0	15nA	30	-2nA	-15	-30			16 typ			Low $r_{DS(ON)}$
2N3386	TO-72	150	4.0	9.5	15nA	30	-2.5nA	-15	-50			16 typ			Low $r_{DS(ON)}$
2N3993	TO-72	150	4.0	9.5	1.2nA	25	-1.2nA	-10			4.5	16			
2N3994	TO-72	300	1.0	5.5	1.2nA	25	-1.2nA	-2			4.5	16			
2N5018	TO-18	75		12.0	2nA	30	-10nA	-10		100	10	45			Low $r_{DS(ON)}$
2N5019	TO-18	150		7.0	2nA	30	-10nA	-5		215	10	45			Low $r_{DS(ON)}$
* 2N5114	TO-18	75	5.0	10.0	500	30	-500	-30	-90	37	7	25			Low $r_{DS(ON)}$
* 2N5115	TO-18	100	3.0	6.0	500	30	-500	-15	-60	66	7	25			Low $r_{DS(ON)}$
* 2N5116	TO-18	150	1.0	4.0	500	30	-500	-5	-25	102	7	25			Low $r_{DS(ON)}$
IT100	TO-18	75	2.0	4.5	200	35	-100	-10			12	35			TTL Compatible
IT101	TO-18	60	4.0	10.0	200	35	-100	-20			12	35			TTL Compatible
J174	TO-92	85	5.0	10.0	1nA	30	-1nA	-20	-100	22					Low Cost
J175	TO-92	125	3.0	6.0	1nA	30	-1nA	-7	-60	45					Low Cost
J176	TO-92	250	1.0	4.0	1nA	30	-1nA	-2	-25	70					Low Cost
J177	TO-92	300	0.8	2.25	1nA	30	-1nA	-1.5	-20	90					TTL Compatible
PN5114	TO-92	75	5.0	10.0	500	30	-500	-30	-90	37	7	25			Low Cost
PN5115	TO-92	100	3.0	6.0	500	30	-500	-15	-60	68	7	25			Low Cost
PN5116	TO-92	150	1.0	4.0	500	30	-500	-5	-25	102	7	25			Low Cost
U304	TO-18	85	5.0	10.0	500	30	-500	-30	-90	70	7	27			High Off Isolation
U305	TO-18	110	3.0	6.0	500	30	-500	-15	-60	105	7	27			High Off Isolation
U306	TO-18	175	1.0	4.0	500	30	-500	-5	-25	140	7	27			High Off Isolation

*Also available as JAN/JANTX & JANTXV

**Most TO-92's are available lead formed to a TO-18 or TO-5 pinout. Also available in tape and reel (EIA STD RS-468).

Amplifier Transistors

Junction FETs — N-Channel

PART NUMBER	PACKAGE**	f_{fs} μmho		I_{DSS} mA		V_p V		I_{GSS} pA	BV_{GSS} V	C_{iss} pF	C_{rss} pF	e_n nV/ $\sqrt{\text{Hz}}$	COMMENTS
		Min	Max	Min	Max	Min	Max	Max	Min	Max	Max		
N-Channel:													
2N3684	TO-72	2000	2.5	7.5	-2.0	-5.0	-100	-50	4	1.2		150 @ 20Hz	Low Noise
2N3685	TO-72	1500	1.0	3.0	-1.0	-3.5	-100	-50	4	1.2		150 @ 20Hz	Low Noise
2N3686	TO-72	1000	0.4	1.2	-0.6	-2.0	-100	-50	4	1.2		150 @ 20Hz	Low Noise
2N3687	TO-72	500	0.1	0.5	-0.3	-1.2	-100	-50	4	1.2		150 @ 20Hz	Low Noise
* 2N3821	TO-72	1500	0.5	2.5		-4.0	-100	-50	6	3		200 @ 10Hz	GPA
2N3822	TO-72	3000	2.0	10.0		-6.0	-100	-50	6	3		200 @ 10Hz	GPA
2N3823	TO-72	3500	4.0	20.0	-1.0	-7.5	-500	-30	6	2		2.5dB @ 100MHz	VHF Amp
2N4117	TO-72	70	0.03	0.09	-0.6	-1.8	-10	-40	3	1.5			Low Leakage
2N4117A	TO-72	70	0.03	0.09	-0.6	-1.8	-1	-40	3	1.5			Low Leakage
2N4118	TO-72	80	0.08	0.24	-1.0	-3.0	-10	-40	3	1.5			Low Leakage
2N4118A	TO-72	80	0.06	0.24	-1.0	-3.0	-1	-40	3	1.5			Low Leakage
2N4119	TO-72	100	0.2	0.6	-2.0	-6.0	-10	-40	3	1.5			Low Leakage
2N4119A	TO-72	100	0.2	0.6	-2.0	-6.0	-1	-40	3	1.5			Low Leakage
2N4220	TO-72	1000	0.5	3.0		-4.0	-100	-30	6	2			Low Cost
2N4220A	TO-72	1000	0.5	3.0		-4.0	-100	-30	6	2		2.5dB @ 100Hz	GPA
2N4221	TO-72	2000	2.0	6.0		-6.0	-100	-30	6	2			Low Cost
2N4221A	TO-72	2000	2.0	6.0		-6.0	-100	-30	6	2		2.5dB @ 100Hz	GPA
2N4222	TO-72	2500	5.0	15.0		-8.0	-100	-30	6	2			Low Cost
2N4222A	TO-72	2500	5.0	15.0		-8.0	-100	-30	6	2		2.5dB @ 100Hz	GPA
2N4223	TO-72	3000	3.0	18.0	-0.1	-8.0	-250	-30	6	2			Low Cost
2N4224	TO-72	2000	2.0	20.0	-0.1	-0.8	-150	-30	6	2			Low Cost
2N4338	TO-18	600	0.2	0.6	-0.3	-1.0	-100	-50	7	3		65 @ 1kHz	General Purpose Amp
2N4339	TO-18	800	0.5	1.5	-0.6	-1.8	-100	-50	7	3		65 @ 1kHz	General Purpose Amp
2N4340	TO-18	1300	1.2	3.6	-1.0	-3.0	-100	-50	7	3		65 @ 1kHz	General Purpose Amp
2N4341	TO-18	2000	3.0	9.0	-2.0	-6.0	-100	-50	7	3		65 @ 1kHz	General Purpose Amp
2N4416	TO-72	4500	5.0	15.0		-6.0	-100	-30	4	2			High Gain
2N4867	TO-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5		10 @ 1kHz	Audio Amp
2N4867A	TO-72	700	0.4	1.2	-0.7	-2.0	-250	-40	25	5		5 @ 1kHz	Low Noise/GPA
2N4868	TO-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5		10 @ 1kHz	Audio Amp
2N4868A	TO-72	1000	1.0	3.0	-1.0	-3.0	-250	-40	25	5		5 @ 1kHz	Low Noise/GPA
2N4869	TO-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5		10 @ 1kHz	Audio Amp
2N4869A	TO-72	1300	2.5	7.5	-1.8	-5.0	-250	-40	25	5		5 @ 1kHz	Low Noise/GPA
2N5397	TO-72	6000	10.0	30.0	-1.0	-6.0	-100	-25	5.0	1.2		3.5dB @ 450MHz	VHF Amp
2N5398	TO-72	5500	5.0	40.0	-1.0	-6.0	-100	-25	5.5	1.3			VHF Amp
2N5457	TO-92	1000	1.0	5.0	-0.5	-6.0	-1nA	-25	7	3		3dB @ 1kHz	Low Cost/GPA
2N5458	TO-92	1500	2.0	9.0	-1.0	-7.0	-1nA	-25	7	3		3dB @ 1kHz	Low Cost/GPA
2N5459	TO-92	2000	4.0	16.0	-2.0	-8.0	-1nA	-25	7	3		3dB @ 1kHz	Low Cost/GPA
2N5484	TO-92	3000	1.0	5.0	-0.3	-0.3	-1nA	-25	5	1		120 @ 1kHz	Low Cost RF Amp
2N5485	TO-92	3500	4.0	10.0	-0.5	-4.0	-1nA	-25	5	1		120 @ 1kHz	Low Cost RF Amp
2N5486	TO-92	4000	8.0	20.0	-2.0	-6.0	-1nA	-25	5	1		120 @ 1kHz	Low Cost RF Amp
ITE4416	TO-92	4500	5.0	15.0		-6.0	100	-30	4	2			Low Cost RF Amp

*Also available as JAN/JANTX & JANTXV

(Continued Next Page)

**Most TO-92's are available lead formed to a TO-18 or TO-5 pinout. Also available in tape and reel (EIA STD RS-468).

Amplifier Transistors (Continued)

Junction FETs — N-Channel (Continued)

PART NUMBER	PACKAGE**	g_{fs} μmho		I_{DSS} mA		V_p V		I_{GSS} pA	BV_{GSS} V	C_{iss} pF	C_{rss} pF	e_n nV/ $\sqrt{\text{Hz}}$	COMMENTS
		Min	Max	Min	Max	Min	Max	Max	Min	Max	Max	Max	
J201	TO-92	500	1.0	0.2	1.0	-0.3	-1.5	-100	-40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J202	TO-92	1000	0.9	4.5	4.5	-0.8	-4.0	-100	-40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J203	TO-92	1500	4.0	20.0	20.0	-2.0	-10.0	-100	-40	4typ.	1typ.	5typ. @ 1kHz	GPA/Low Cost
J204	TO-92					-0.5	-2.0	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J210	TO-92	4000	2.0	15.0	15.0	-1.0	-3.0	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J211	TO-92	7000	7.0	20.0	20.0	-2.5	-4.5	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J212	TO-92	7000	15.0	40.0	40.0	-4.0	-6.0	-100	-25	4typ.	1typ.	10typ. @ 1kHz	GPA/Low Cost
J300	TO-92	4500	4.0	45.0	45.0	-1.5	-7.0	-500	-25	5.5	1.7		VHF AMP/Low Cost
J308	TO-92	8000	12.0	60.0	60.0	-1.0	-6.5	-1nA	-25			2.7dB @ 450MHz	VHF Amp/Low Cost
J309	TO-92	10,000	12.0	30.0	30.0	-1.0	-4.0	-1nA	-25			2.7dB @ 450MHz	VHF Amp/Low Cost
J310	TO-92	8000	24.0	60.0	60.0	-2.0	-6.5	-1nA	-25			2.7dB @ 450MHz	VHF Amp/Low Cost
PN4302	TO-92	1000	0.5	5.0	5.0		-4.0	-1nA	-30	6	2	2dB @ 1kHz	GPA/Low Cost
PN4303	TO-92	2000	4.0	10.0	10.0		-6.0	-1nA	-30	6	2	2dB @ 1kHz	GPA/Low Cost
PN4304	TO-92	1000	0.5	15.0	15.0		-10.0	-1nA	-30	6	2	3dB @ 1kHz	GPA/Low Cost
PN4338	TO-92	600	0.2	0.6	0.6	-0.3	-1.0	-100	-50	7	3	1dB @ 1kHz	GPA/VCR
PN4339	TO-92	800	0.5	1.5	1.5	-0.6	-1.8	-100	-50	7	3	1dB @ 1kHz	GPA/VCR
PN4340	TO-92	1300	1.2	3.6	3.6	-1.0	-3.0	-100	-50	7	3	1dB @ 1kHz	GPA/VCR
PN4341	TO-92	2000	3.0	9.0	9.0	-2.0	-6.0	-100	-50	7	3	1dB @ 1kHz	GPA/VCR
PN4416	TO-92	4500	5.0	15.0	15.0		-6.0	-100	-30	4	2		High Gain/Low Cost
PN5163	TO-92	2000	1.0	40.0	40.0	-0.4	-8.0	-10nA	-25	20	5	50 @ 1kHz	Low Cost
U308	TO-52	10,000	12.0	60.0	60.0	-1.0	-6.0	-150	-25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp
U309	TO-52	10,000	12.0	30.0	30.0	-1.0	-4.0	-150	-25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp
U310	TO-52	10,000	24.0	60.0	60.0	-2.5	-6.0	-150	-25	7typ.	4.0typ.	2.7dB @ 450MHz	VHF Amp

**Most TO-92's are available lead formed to a TO-18 or TO-5 pinout. Also available in tape and reel (EIA STD RS-468).

Amplifier Transistors (Continued)

Junction FETs — P-Channel

PART NUMBER	PACKAGE**	g_{fs}	I_{DSS}		V_p		I_{GSS}	BV_{GSS}	C_{iss}	C_{rss}	e_n	COMMENTS
		μmho	Min	Max	Min	Max	nA	V	pF	pF	nV/ \sqrt{Hz}	
2N2606	TO-18	110	0.1	-0.5	0.5	4.0	1nA	30	6		3dB@1kHz	VP Min Waiver
2N2607	TO-18	330	-0.3	-1.5	1.0	4.0	3nA	30	10		400@1kHz	Low Noise/GPA
2N2608	TO-18	1000	-0.9	-4.5	1.0	4.0	10nA	30	17		180@1kHz	Low Noise/GPA
2N2609	TO-18	2500	-2.0	-10.0	1.0	4.0	30nA	30	30		180@1kHz	Low Noise/GPA
2N2609JAN	TO-18	2500	-2.0	-10.0	1.0	4.0	30nA	30	30		3dB@1kHz	Low Noise/GPA
2N3328	TO-72	100		-1.0		6.0	1nA	20	4		400@1kHz	GPA
2N3329	TO-72	1000	-1.0	-3.0		5.0	10nA	20	20		3db@1kHz	GPA
2N3330	TO-72	1500	-2.0	-6.0		6.0	10nA	20	20		3db@1kHz	GPA
2N3331	TO-72	2000	-5.0	-15.0		8.0	10nA	20	20		4db@1kHz	GPA
2N3332	TO-72	1000	-1.0	-6.0		6.0	10nA	20	20		1db@1kHz	GPA
2N5265	TO-72	900	-0.5	-1.0	0.3	1.5	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5266	TO-72	1000	-0.8	-1.6	0.4	2.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5267	TO-72	1500	-1.5	-3.0	1.0	4.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5268	TO-72	2000	-2.5	-5.0	1.0	4.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5269	TO-72	2200	-4.0	-8.0	2.0	6.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5270	TO-72	2500	-7.0	-14.0	2.0	6.0	2nA	60	7	2	115@100Hz	Low Noise/GPA
2N5460	TO-92	1000	-1.0	-5.0	0.75	6.0	5nA	40	7	2	115@100Hz	Low Noise/Low Cost
2N5461	TO-92	1500	-2.0	-9.0	1.0	7.5	5nA	40	7	2	115@100Hz	Low Noise/Low Cost
2N5462	TO-92	2500	-4.0	-16.0	1.8	9.0	5nA	40	7	2	115@100Hz	Low Noise/Low Cost
2N5463	TO-92	1000	-1.0	-5.0	0.75	6.0	5nA	60	7	2	115@100Hz	Low Noise/Low Cost
2N5464	TO-92	1500	-2.0	-9.0	1.0	7.5	5nA	60	7	2	115@100Hz	Low Noise/Low Cost
2N5465	TO-92	2500	-4.0	-16.0	1.8	9.0	5nA	60	7	2	115@100Hz	Low Noise/Low Cost
J270	TO-92	6000	-2.0	-15.0	0.5	2.0	0.200	30	32typ	4typ	6typ@1kHz	Low Noise/Low Cost
J271	TO-92	8000	-6.0	-50.0	1.5	4.5	0.200	30	31typ	4typ	6typ@1kHz	Low Noise/Low Cost
PN4342	TO-92	2000	-4.0	-12.0	0.7	5.0	10nA	25	20	5	80@100Hz	Low Noise/Low Cost
PN4343	TO-92	3000	-10.0	-30.0	1.8	9.0	10nA	25	20	5	80@100Hz	Low Noise/Low Cost

**Most TO-92's are available lead formed to a TO-18 or TO-5 pinout. Also available in tape and reel (EIA STD RS-468).

Switching/Amplifier Transistors

MOSFETs — N-Channel

PART NUMBER	PACKAGE	$V_{GS(TH)}$ V		BV_{DSS} V	I_{DSS} pA	I_{GSS} pA	g_{fs} μmho	$r_{DS(ON)}$ Ω	$I_{D(ON)}$ mA	$I_{D(ON)}$ mA	COMMENTS
		Min	Max								
2N4351	TO-72	1.0	5.0	25	10nA	10	1000	300	3		High Input Z
3N170	TO-72	1.0	2.0	25	10nA	10	1000	200	10		High Input Z
3N171	TO-72	1.5	3.0	25	10nA	10	1000	200	10		High Input Z
IT1750	TO-72	0.5	3.0	25	10nA	10	3000	50	10		Low $r_{DS(ON)}$
M116	TO-72	1.0	5.0	30	10nA	100		100			Diode Protected
M117	TO-72	1.0	5.0	30	10nA	1		100			High Input Z

MOSFETs — P-Channel

Generally used where max. isolation between signal source and logic drive is required: switch "On" resistance varies with signal amplitude.

PART NUMBER	PACKAGE	$V_{GS(TH)}$ V		BV_{DSS} V	I_{DSS} pA	I_{GSS} pA	g_{fs} μmho	$r_{DS(ON)}$ Ω	$I_{D(ON)}$ mA	$I_{D(ON)}$ mA	COMMENTS
		Min	Max								
2N4352	TO-72	-1.0	-5.0	-25	-10nA	10	1000	600	-3		High Input Z
3N155	TO-72	-1.5	-3.2	-35	-1nA	10	1000	600	-5		High Input Z
3N155A	TO-72	-1.5	-3.2	-35	-250	10	1000	300	-5		High Input Z
3N157	TO-72	-1.5	-3.2	-35	-1nA	10	1000		-5		High Input Z
3N157A	TO-72	-1.5	-3.2	-50	-250	10	1000		-5		High Input Z
3N161	TO-72	-1.5	-5.0	-25	-10nA	-100	3500		-40	-120	Diode Protected
3N163	TO-72	-2.0	-5.0	-40	-200	-10	2000	250	-5	-30	High Input Z
3N164	TO-72	-2.0	-5.0	-30	400	10	1000	300	-3	-30	High Input Z
3N172	TO-72	-2.0	-5.0	-40	-400	-200		250	-5	-30	Diode Protected
3N173	TO-72	-2.0	-5.0	-30	-10nA	-500		350	-5	-30	Diode Protected
IT1700	TO-72	-2.0	-5.0	-40	200		2000	400	-2		High Input Z
IT1701	TO-72	-2.0	-5.0	-40	200	100	2000	400	-2		Diode Protected

Diodes, Low Leakage Used to protect the inputs of MOSFETs such as 3N163, while maintaining input leakage < 0.1 pA.

PART NUMBER	PACKAGE	$I_R @ 1V$	$I_R @ 10V, 125^\circ C$	$BV_R @ 1\mu A$	$V_F @ 10mA$		COMMENTS
		(pA) Typ	(nA) Max	(V) Min	(V) Min	(V) Max	
ID100	TO-78	0.1	10	30	0.8	1.1	(Note 1)
ID101	TO-71	0.1	10	30	0.8	1.1	(Note 1)

Note 1. Used to protect the inputs of MOSFETs such as 3N163, while maintaining input leakage < 0.1pA.

Differential Amplifier Transistors — Monolithic Duals

Junction FETs — N-Channel

PART NUMBER	PACKAGE	V_{GS1-2}	ΔV_{GS}	I_G	BV_{GSS}	V_p		g_{fs}		I_{DSS}		e_n	COMMENTS
		Max	$\mu V/^\circ C$ Max	pA	V	Min	Max	Min	Max	Min	Max	nV/ \sqrt{Hz} Max	
2N3921	TO-71	5	10	250	-50		-3.0	1.5	7.5	1	10.0	2dB @ 1kHz	GP Diff Amp
2N3922	TO-71	5	25	250	-50		-3.0	1.5	7.5	1	10.0	2dB @ 1kHz	GP Diff Amp
2N3954	TO-71	5	10	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N3954A	TO-71	5	5	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N3955	TO-71	10	25	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N3955A	TO-71	5	15	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N3956	TO-71	15	50	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N3957	TO-71	20	75	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N3958	TO-71	25	100	-50	-50	-1.0	-4.5	1	3	0.5	5.0	160 @ 100Hz	General Purpose
2N5045	TO-71	5	65		-50	-0.5	-4.5	1.5	6.0	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5046	TO-71	10	133		-50	-0.5	-4.5	1.5	6.0	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5047	TO-71	15	200		-50	-0.5	-4.5	1.5	6.0	0.5	8.0		GP Diff Amp
2N5196	TO-71	5	5	-15	-50	-0.7	-4.0	0.7 @ 200 μA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5197	TO-71	5	10	-15	-50	-0.7	-4.0	0.7 @ 200 μA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5198	TO-71	10	20	-15	-50	-0.7	-4.0	0.7 @ 200 μA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5199	TO-71	15	40	-15	-50	-0.7	-4.0	0.7 @ 200 μA		0.7	7.0	20 @ 1kHz	Low Noise, GPA
2N5515	TO-71	5	5	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5516	TO-71	5	10	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5517	TO-71	10	20	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5518	TO-71	15	40	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5519	TO-71	15	80	-100	-40	-0.7	-4.0	1	4	0.5	7.5	30 @ 10Hz	GP Diff Amp
2N5520	TO-71	5	5	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5521	TO-71	5	10	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5522	TO-71	10	20	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5523	TO-71	15	40	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5524	TO-71	15	80	-100	-40	-0.7	-4.0	1	4	0.5	7.5	15 @ 10Hz	Lowest Noise
2N5545	TO-71	5	10	-50	-50	-0.5	-4.5	1.5	6	0.5	8.0	180 @ 10Hz	GP Diff Amp
2N5546	TO-71	10	20	-50	-50	-0.5	-4.5	1.5	6	0.5	8.0	200 @ 10Hz	GP Diff Amp
2N5547	TO-71	15	40	-50	-50	-0.5	-4.5	1.5	6	0.5	8.0		GP Diff Amp
2N5902	TO-78	5	5	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5903	TO-78	5	10	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5904	TO-78	10	20	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5905	TO-78	15	40	-3	-40	-0.6	-4.5	0.07	.250	0.03	0.50	100 @ 1kHz	Low Leakage
2N5906	TO-99	5	5	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5907	TO-99	5	10	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5908	TO-99	10	20	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5909	TO-99	15	40	-1	-40	-0.6	-4.5	0.07	0.25	0.03	0.50	100 @ 1kHz	Low Leakage
2N5911	TO-99	10	20	-100	-25	-1.0	-5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
2N5912	TO-99	15	40	-100	-25	-1.0	-5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz	RF Amplifier
2N6483	TO-71	5	5	-100	-50	-0.7	-4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
2N6484	TO-71	10	10	-100	-50	-0.7	-4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
2N6485	TO-71	15	25	-100	-50	-0.7	-4.0	1	4	0.5	7.5	10 @ 10Hz	Low Noise
IT500	TO-52	5	5	-5	-50	-0.7	-4.0	0.7/1.6 @ 200 μA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT501	TO-52	5	10	-5	-50	-0.7	-4.0	0.7/1.6 @ 200 μA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT502	TO-52	10	20	-5	-50	-0.7	-4.0	0.7/1.6 @ 200 μA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT503	TO-52	15	40	-5	-50	-0.7	-4.0	0.7/1.6 @ 200 μA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT504	TO-52	25	100	-5	-25	-0.7	-4.0	0.7/1.6 @ 200 μA		0.7	7.0	35 @ 10Hz	Cascode RF Amp
IT505	TO-52	50	200	-5	-25	-0.7	-4.0	0.7/1.6 @ 200 μA		0.7	7.0	35 @ 10Hz	Cascode RF Amp

* @ I_{DSS}

(Continued Next Page)

Differential Amplifiers (Continued)

Junction FETs — N-Channel (Continued)

PART NUMBER	PACKAGE	V_{GS1-2} mV		ΔV_{GS} $\mu V/^\circ C$	I_G pA	BV_{GSS} V		V_p V		g_{fs} mmho*		I_{DSS} mA		e_n nV/ \sqrt{Hz}	COMMENTS
		Max	Max	Max	Min	Min	Max	Min	Max	Min	Max	Min	Max	Max	
IT5911	TO-71	10	20	-100	-25	-1.0	-5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz		RF Amplifier	
IT5912	TO-71	15	40	-100	-25	-1.0	-5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz		RF Amplifier	
ITC5911	TO-99	10	20	-100	-25	-1.0	-5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz		RF Amplifier	
ITC5912	TO-99	15	40	-100	-25	-1.0	-5.0	5/10 @ 5mA		7.0	40.0	20 @ 10kHz		RF Amplifier	
U231	TO-71	5	10	-50	-50	-0.5	-4.5	1	5	0.5	5.0	80 @ 100Hz		GP Diff Amp	
U232	TO-71	10	25	-50	-50	-0.5	-4.5	1	5	0.5	5.0	80 @ 100Hz		GP Diff Amp	
U233	TO-71	15	50	-50	-50	-0.5	-4.5	1	5	0.5	5.0	80 @ 100Hz		GP Diff Amp	
U234	TO-71	20	75	-50	-50	-0.5	-4.5	1	5	0.5	5.0	80 @ 100Hz		GP Diff Amp	
U235	TO-71	25	100	-50	-50	-0.5	-4.5	1	5	0.5	5.0	80 @ 100Hz		GP Diff Amp	
U257	TO-78	100			-25	-1.0	-5.0	4.5	10	5.0	40.0	30 @ 10kHz		Low Cost	
U426	TO-78	25	40	-0.5	-40	-0.4	-3.0	0.3	1.5	.06	1.8	70 @ 10Hz		Low Cost	
U440	TO-71	10			-25	-1.0	-6.0	4.5/9 @ 5 μ A		6	30			High Gain	
U441	TO-71	20			-25	-1.0	-6.0	4.5/9 @ 5 μ A		6	30			High Gain	

MOSFETs — Monolithic Dual P-Channel (Enhancement)

PART NUMBER	PACKAGE	$V_{GS(TH)}$ V		BV_{DSS} V	I_{DSS} pA	I_{GSS} pA	g_{fs} μ mho	$I_{D(ON)}$ mA		$r_{DS(ON)}$ Ω	V_{GS1-2} mV	COMMENTS
		Min	Max	Min/Max	Max	Max	Min	Min	Max	Max	Max	
3N165	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	100	Low Leakage
3N166	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300		Low Leakage
3N188	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300	100	Diode Protected
3N189	TO-99	-2	-5	-40	-200	-200	1500	-5.0	-30	300		Diode Protected
3N190	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300	100	High Input Z
3N191	TO-99	-2	-5	-40	-200	-10	1500	-5.0	-30	300		High Input Z

*@ I_{DSS}

Differential Amplifiers (Continued)

Bipolar Monolithic Dual Transistors — NPN

PART NUMBER	PACKAGE	V_{BE} 1-2	ΔV_{BE}	h_{FE}	I_{B1-2}	V_{CE0}	I_{CBO}	NF dB	f_t	C_{obo} pF	COMMENTS
		Max	Max	(Note 1) Min	(Note 1) nA	V Min	nA Max		MHz @ I_C Min		
2N2453	TO-78	3	10	80		30	5	7 typ.			Audio Amp
2N2453A	TO-78	3	5	80		60	5	4 typ.			Audio Amp
2N2920	TO-78	3	10	150		60	2	3 typ.	60 @ 0.5mA	6	High Gain, Low Noise
2N2920A	TO-78	1.5	5	150		60	2	3 typ.	60 @ 0.5mA	6	High Gain, Low Noise
2N4044	TO-78	3	3	200	5	60	0.1	2	200 @ 1mA	0.8	Low Capacitance
2N4045	TO-78	5	10	80	25	45	0.1	3	150 @ 1mA	0.8	Low Capacitance
2N4100	TO-78	5	5	150	10	55	0.1	3	150 @ 1mA	0.8	Low Capacitance
2N4878	TO-71	3	3	200	5	60	0.1	2 typ.	200 @ 1mA	0.8	Low Capacitance
2N4879	TO-71	5	5	150	10	55	0.1	3 typ.	150 @ 1mA	0.8	Low Capacitance
2N4880	TO-71	5	10	80	25	45	0.1	3 typ.	150 @ 1mA	0.8	Low Capacitance
IT120	TO-78 TO-71	2	5	200	5	45	1.0	2 typ.	150 @ 1mA	2	Low Cost, Low V_{OS}
IT120A	TO-78 TO-71	1	3	200	2.5	45	1.0	2 typ.	150 @ 1mA	2	Low Cost, Low V_{OS}
IT121	TO-78 TO-71	3	10	80	25	45	1.0	2 typ.	180 @ 1mA	2	Low Cost
IT122	TO-78 TO-71	5	20	80	25	45	1.0	2 typ.	180 @ 1mA	2	Low Cost
IT124	TO-78	5	15	1500	0.6A	2	0.1	3	100 @ 100 μ A	0.8	Super β for Log Amps
IT126	TO-78 TO-71	1	3	150	2.5	60	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
IT127	TO-78 TO-71	2	5	150	5	60	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
IT128	TO-78 TO-71	3	10	100	10	55	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
IT129	TO-78 TO-71	10	20	70	20	45	0.1	1 typ.	250 @ 10mA	3	Low V_{OS}
LM114	TO-71	2.0	10	250	10	45	0.050				Low V_{OS}
LM114A	TO-71	0.5	2	500	2	45	0.010				Low V_{OS}
LM114AH	TO-78	0.5	2	500	2	45	0.010				Low V_{OS}
LM114B	TO-71	1.0	5	250	10	45	0.050				Low V_{OS}
LM114BH	TO-78	1.0	5	250	10	45	0.050				Low V_{OS}
LM114H	TO-78	2.0	10	250	10	45	0.050				Low V_{OS}

NOTE:

1. $I_C = 10\mu A$

(Continued Next Page)

Differential Amplifiers (Continued)

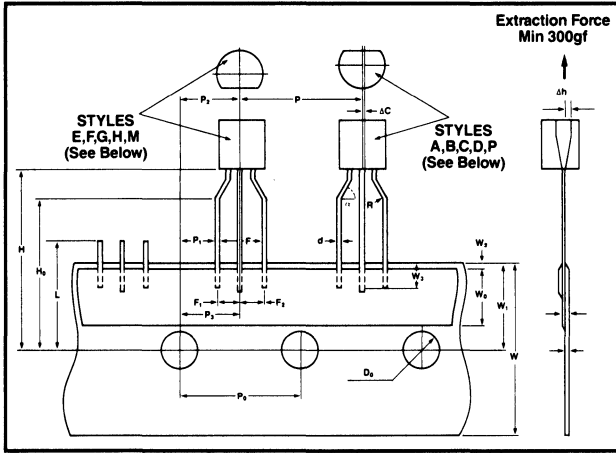
Bipolar Dual Transistors — PNP

PART NUMBER	PACKAGE	V_{BE} 1-2	ΔV_{BE}	h_{FE}	I_{B1-2}	BV_{CEO}	I_{CBO}	NF	f_t	C_{obo}	COMMENTS
		mV	$\mu V/^\circ C$	(Note 1)	(Note 1)	V	nA	dB	MHz @ I_C	pF	
		Max	Max	Min	Max	Min	Max	Max	Min	Max	
2N3810	TO-78	3	10	100		-60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N3810A	TO-78	1.5	5	100		-60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N3811	TO-78	3	10	225		-60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N3811A	TO-78	1.5	5	225		-60	10	3 typ.	100 @ 1mA	4	Low V_{OS}
2N5117	TO-78	3	3	100	10	-45	0.1	4 typ.	100 @ 0.5mA	0.8	Low V_{OS}
2N5118	TO-78	5	5	100	15	-45	0.1	4 typ.	100 @ 0.5mA	0.8	Low Cost
2N5119	TO-78	5	10	50	40	-45	0.1	4 typ.	100 @ 0.5mA	0.8	Low Cost
IT130	TO-78 TO-71	2	5	200	5	-45	1.0	2 typ.	150 @ 1mA	2	Low V_{OS}
IT130A	TO-78 TO-71	1	3	200	2.5	-45	1.0	2 typ.	150 @ 1mA	2	Low V_{OS}
IT131	TO-78 TO-71	3	10	80	25	-45	1.0	2 typ.	150 @ 1mA	2	Low Cost
IT132	TO-78 TO-71	5	20	80	25	-45	1.0	2 typ.	150 @ 1mA	2	Low Cost
IT136	TO-78 TO-71	1	3	150	2.5	-60	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}
IT137	TO-78 TO-71	2	5	150	5	-60	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}
IT138	TO-78 TO-71	3	10	100	10	-55	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}
IT139	TO-78 TO-71	5	20	70	20	-45	0.1	2 typ.	250 @ 10mA	4	Low V_{OS}

Note:

1. $I_C = 10\mu A$, $V_{CE} = 5V$

TO-92 Taping Specifications and Winding Styles



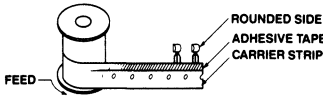
(EIA STD RS468)

P	12.7 ± 0.5	H_0	16 ± 0.5
P_0	12.7 ± 0.2	F	$5^{+0.08}_{-0.02}$
P_1	3.85 ± 0.5	$F_1 - F_2$	± 0.3
P_2	6.35 ± 0.5	D_0	4 ± 0.2
P_3	6.35	t	0.7 ± 0.2
W	$8^{+1.0}_{-0.5}$	Δh	0 ± 1
W_0	6 ± 1	d	$0.050^{+0.006}_{-0.005}$ dia.
W_1	9 ± 0.5	R	0.8
W_2	Max. 0.5	α	$45^\circ C - 60^\circ C$
W_3	Min. 4.5	L	Max. 11
H	19.5 ± 0.5	ΔC	0 ± 0.5

All Dimensions in Millimeter

STYLE A

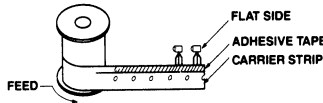
STYLE A IS PREFERRED



ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

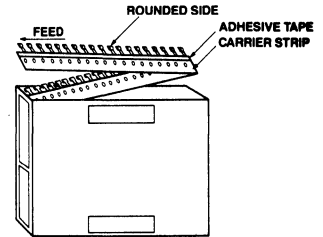
STYLE E

STYLE E IS A PREFERRED STYLE



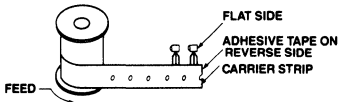
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE P



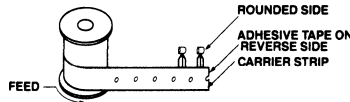
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE
STYLE P IS EQUIVALENT TO STYLES A, B, C, D OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

STYLE B



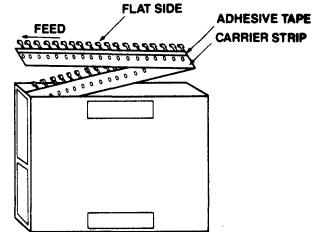
FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE F



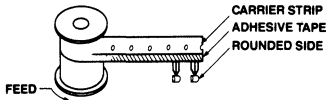
ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE M



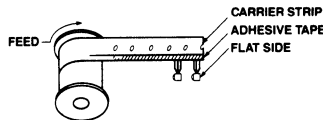
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE
STYLE M AMMO PACK IS EQUIVALENT TO STYLES E, F, G, H OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

STYLE C



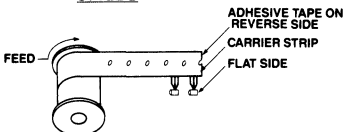
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE G



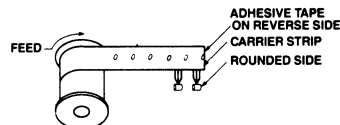
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE D



FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

STYLE H



ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE
(ADHESIVE TAPE ON REVERSE SIDE)

Microperipheral and Interface Circuits

IM6402/IM6403

Universal Asynchronous Receiver Transmitter (UART)

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. CMOS/LSI technology permits clock frequencies up to 6.0 MHz (250K Baud).

Variations include the following:

Device	Fc (MHz)	Device	Fc (MHz)
IM6402	1	IM6403	2.46
IM6402-1	2	IM6403-1	3.58
IM6402A	4	IM6403A	6.00

The IM6403 Series differs from the IM6402 Series primarily by having an on-board crystal oscillator and baud rate generator. Available in plastic and ceramic packages, in commercial and military temperature ranges.

IM4702/4712

Baud Rate Generator

The IM4702/12 Baud Rate Generators provide necessary clock signals for digital data transmission systems, such as UARTs, using a 2.4576 MHz crystal oscillator as an input. They control up to 8 output channels and can be cascaded for output expansion.

Multi-channel operation allows up to eight simultaneous Baud rates to be generated. Provides 14 most commonly used baud rates from zero through 9600 Baud. In addition, 19200 Baud is possible via hardwiring.

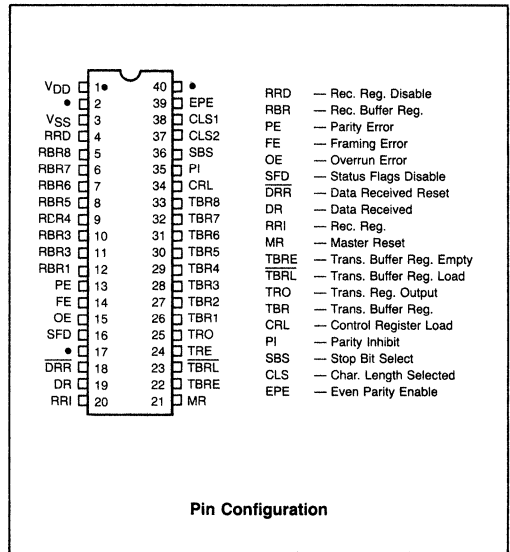
IM4712 integrates oscillator feedback resistor and two load capacitors on-chip.

Available in 16-pin plastic DIP and CERDIP packages with a temperature range from -40°C to +85°C.

ICL232

+5V Powered Dual RS-232 Transmitter/Receiver

The ICL232 requires only a few non-critical external components to perform the RS-232 driver/receiver function with either CMOS or TTL inputs. It features two on-board charge-pump voltage converters which generate the required $\pm 10V$ supplies from a single 5V power supply. The ICL232 meets all EIA RS-232C specifications. It is available in a variety of packages (including the 16-pin SOIC) and operating temperature ranges.



IM26C91

Universal Asynchronous Receiver/Transmitter (UART)

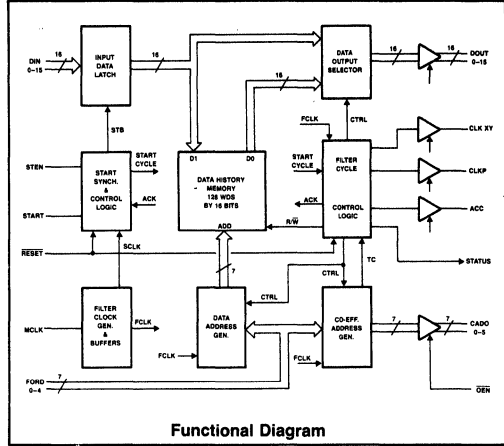
The IM26C91 is a high-performance Universal Asynchronous Receiver/Transmitter that provides full duplex operation. Operating speed can be selected from 18 fixed baud rates ranging from 50 to 38.4K baud, or from an internal programmable counter/timer (16 x clock speed), or from an external 1X or 16X clock. The ability to program the operating speed independently makes the UART particularly well suited for dual-speed channel applications, e.g. clustered terminal systems.

The quadruple buffered receiver minimizes potential receiver overrun and reduces interrupt overhead in interrupt driven systems. Handshaking capability disables a remote UART transmitter when the receiver buffer is full.

The IM26C91 UART is fabricated with high-density, low-power CMOS technology which permits monolithic construction and encapsulation in a 24-pin DIP. The device is TTL compatible and operates from a single +5V power supply.

IM29C128 Finite Impulse Response Filter Controller

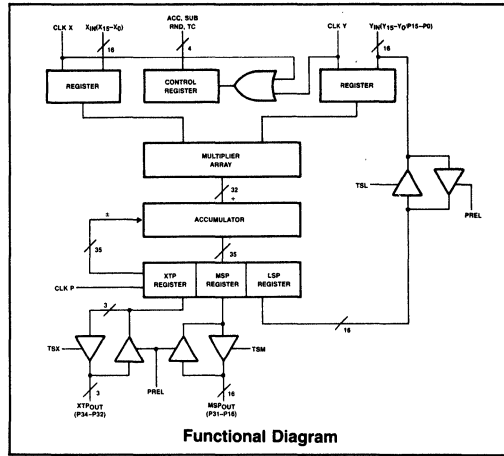
The 16-bit FIR Filter Controller (FFC) provides all the data history, storage and programmable filter cycle control logic required to implement FIR filters of up to 128 filter points. When used in conjunction with an external filter coefficient memory of up to 128 words by 16 bits and an industry standard 16 bit Multiplier-Accumulator (MAC), the FFC provides the system designer with the ability to implement a powerful FIR filter with only three ICs. The FFC provides all the control signals required to operate the MAC and the coefficient memory as tri-stateable devices, allowing multiplexed use of these resources. The FFC's asynchronous interface enables easy integration of the FIR filter in any system environment. It incorporates a 16 bit data I/O path, a 128 word by 16 bit RAM memory, and programmable filter control logic capable of handling filter order lengths of up to 128 points. Available in 64-lead DIP and 68-contact PLCC packages, with 0°C to +70°C and -55°C to +125°C temperature ranges.



IM29C510 16 x 16 Bit Multiplier/Accumulator, CMOS

The IM29C510 is a high-speed 16 x 16 Bit Parallel Multiplier/Accumulator which operates at a 65 ns clock rate (more than 15 MHz Multiply/Accumulate rate). The 2 input registers, x and y, accept 16 bit two's complement or unsigned magnitude operands and produce a 32 bit product, with accumulation up to 35 bits. The IM29C510 16 x 16 Bit Multiplier/Accumulator is pin and function compatible with the industry-standard TDC1010. Depending on the multiply-accumulate rate, it operates with the same speed at one-sixth or less power dissipation than the bipolar versions. (Worst case CMOS power consumption decreases with decreasing clock rate.)

The IM29C510 can operate as a 16 x 16 Bit Multiplier only, as well as a 16 x 16 Bit Multiplier/Accumulator. It is available in 64-lead DIP and 68-contact PLCC packages, with 0°C to +70°C and -40°C to +85°C temperature ranges. Full MIL screening is available.

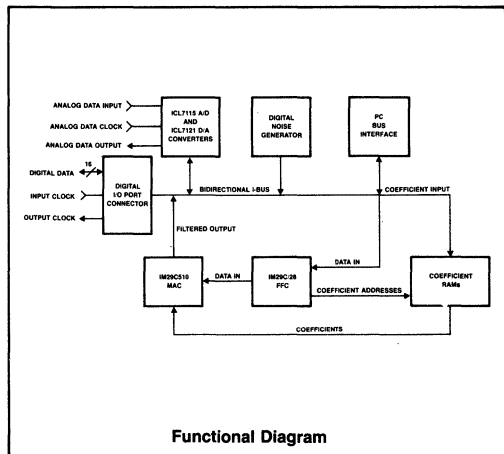


EVK-128 Data Conversion and FIR Filtering System

The Intersil EVK-128 provides a moderate speed data acquisition, conversion, and digital filtering system for the IBM PC and most compatibles. Consisting of a board which occupies a single slot on the PC, the card digitally filters data with a filter length of 0 (unfiltered) to 128 taps. Throughput is a function of required filter length, with an 80 ns per tap processing rate.

The ICL7115 converts analog signals to 14 bit words at up to 32.727 kHz rate, while the ICL7121 converts a 16 bit digital data stream to analog. The A/D and/or D/A converters may be bypassed for processing of digital data. This allows non-real time processing or storage of data to or from a disk, for example.

Also included is a floppy disk with an easy-to-use menu driven FIR filter design program for the PC, including coefficient calculations, time and frequency calculations and plotting capabilities.



DISPLAY DRIVERS



Intersil's complete complement of monolithic Display Driver circuits provides a suitable interface for virtually any display application.

- Choice of Displays:
LED, LCD, Vacuum Fluorescent
- Choice of Characters or Digits:
4, 8 or 10 7-Segment Digits
14, 16 or 18-Segment Characters
- Choice of Font:
Hexadecimal, Code B, ASCII

- Choice of Interface:
Multiplexed or Direct Drive; BCD, Random Access, Serial or Parallel

All Intersil Drivers are fabricated with CMOS technology for low power dissipation, and most are available in CERDIP and Plastic Dual In-line packages, as well as in die form. All are completely self-contained, requiring few, if any, external components to accomplish their intended basic functions.

The following table offers a quick-glance overview of available functions for a first-order selection.

TYPE	# OF CHARACTERS OR DIGITS					DISPLAY TYPE	FONT	INTERFACE			FEATURES AND COMMENTS												
	# of 7-Segment Digits	# of Decimal Points or Annunciators	# of Alphanumeric 14 Segments + D.P.	# of Alphanumeric 16 Segments + D.P.	# of Alphanumeric 18 Segments			# of Dot Matrix	LED, Common Anode Non-MUX	LED, Common Cathode MUX		LED, Common Anode MUX	LCD, Direct Drive	LCD, # of Ways MUX'D	Vacuum Fluorescent	Hexadecimal (0-9, A-F)	Code B (0-9, H, E, L, P, , and Blank)	ASCII	MUX BCD (BCD + Digit Select Strokes)	Random Access (Data + Address + WR)	Bit Parallel, Digit Serial	Bit Serial	Cycle Time (ns)
ICM7211	4																				1000	Drives Conventional LCD Displays. Includes RC Oscillator, Divider Chain, Latches, Interface and LCD Drivers. Evaluation Kit Available.	
ICM7211A	4																						1000
ICM7211M	4																						200
ICM7211AM	4																						200
ICM7212	4																					1000	Drives Common Anode LED Displays. 28 Current Controlled Outputs. Includes Latches, Interface and Brightness Control. Evaluation Kit Available.
ICM7212A	4																					1000	
ICM7212M	4																					200	
ICM7212AM	4																					200	
ICM7218A	8	8																				550	
ICM7218B	8	8																				550	
ICM7218C	8	8																				500	
ICM7218D	8	8																				500	
ICM7218E	8	8																				500	
ICM7228A	8	8																				550	
ICM7228B	8	8																				550	
ICM7228C	8	8																				500	
ICM7228D	8	8																				500	
ICM7231A	8	16																				500	8 Digits, 16 Annunciators on COM, Hexadecimal
ICM7231B	8	16																				500	
ICM7231C	8	16																				500	
ICM7232A	10	20																				350	
ICM7232B	10	20																				350	
ICM7232C	10	20																				350	
ICM7233A				4																		500	
ICM7233B				4																		500	
ICM7243A			8																			250	
ICM7243B			8																			250	

Available with and without on-board display drivers, Intersil's broad range of Timer/Counters circuits serves a

wide variety of control functions. For separate Display Driver circuits, see separate section.

Timer/Counters With Display Drivers

TYPE	DISPLAY			FUNCTIONS														MAX COUNT SPEED (MHz)	Evaluation Kit Available	TYPICAL APPLICATIONS AND COMMENTS																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
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	Common Anode, Non-MUX	Common Cathode, MUX	Common Anode, MUX	Direct Drive, Non-MUX	Non-MUX	Up/Down	Up Only	Decade	Modulo 60 (Hr/Min/Sec)	Frequency	Period	Frequency Ratio	Time Interval	MUX BCD Outputs	Display Latch	Display Blanking	Count Enable	Leading Zero Blanking	Preset Count	Comparison Register	Equal and Zero Output																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
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ICM7249			•			•	•						•						•				Event timer/counter, hour meter. 14 programmable modes. Selectable input filtering.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
ICM7215		•				•	•					•			•	•							4 functions: start/stop/reset, split, Taylor, time out. 1/100's seconds and low battery.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
ICM7208		•				•	•		■						•	•	•					2.5	Use with ICM7207/A for a 7-digit frequency counter.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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ICM7226A			•			•	•		•	•	•	•	•	•	•	•						10		Same as ICM7216 plus period and time interval averaging, BDC outputs, µP PIA compatible.																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
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■ These counters will measure frequency when used with the ICM7207 (0.01 and 0.1 second timebase) or the ICM7207A (0.1 and 1.0 second timebase)

Timers/Counters Without Display Drivers

Type	Special Features	Description
ICM7555		Low power CMOS equivalent of industry standard 555 timer — only 80 μ A supply current. ICM7555 does not have the large supply current transients of the bipolar 555 and does not require the large bypassing capacitors needed by the 555. Low leakage threshold and trigger inputs allow use of higher impedance RC timing components for extra long time delays.
ICM7556		An ICM7556 is a dual ICM7555, a CMOS, low power equivalent of the Bipolar 556 Timer.
ICM7240 ICM7250	Binary 0–225 BCD 0–99	Programmable CMOS counter/timer. Uses on-board RC oscillator or an external clock. The count is programmed by wire-AND connection of the outputs. Excellent for ON/OFF delay timers, \div N counters, and long period delays.
ICM7242	Fixed 128/255	RC oscillator + 8-bit counter, similar to ICM7240 but with fixed 256 count. Used for extremely long time delays. Cascadable.

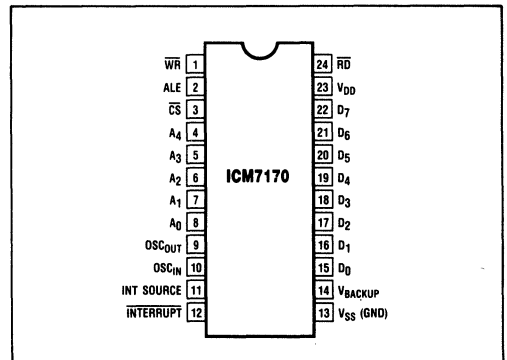
Oscillator/Divider Selector Guide

Type	Output Frequency	Supply Voltage (V)	Typical Current (μ A)	Pulse Width (ms)	Crystal Frequency	Other Outputs/Comments
ICM7213	1 Pulse/Min	2–4	100	125, 1000	4.19 MHz	1 Pulse/Sec., 2048, 1024, 34.133, 16 Hz
	1 Hz	2–4	100	7.8	4.19 MHz	1 Pulse/Min., 2048, 1024, 34.133, 16 Hz
	16 Hz	2–4	100	Sq. Wave	4.19 MHz	1 Pulse/Min., 2048, 1024, 34.133, 1 Hz
	1000 Hz 1024 Hz	2–4 2–4	100 100	Sq. Wave Sq. Wave	4.096 MHz 4.19 MHz	2000, 2000 Pulses/Min. 1 Pulse/Min., 2048, 34.133, 16, 1 Hz
	2048 Hz	2–4	100	Sq. Wave	4.19 MHz	1 Pulse/Min., 1024, 34.133, 16, 1 Hz
ICM7209	250 kHz– 10 MHz	4.5–5.5	11,000	Sq. Wave	1–10 MHz	Two buffered outputs — Crystal Frequency and \div 8 output. Drives up to 5 TTL loads.

ICM7170

μ P-Compatible Real-Time Clock, CMOS

This real-time clock circuit is set or read by accessing eight internal separately addressable and programmable counters from 1/100 seconds to 99 years. An 8-bit bidirectional bus is used for the data I/O circuitry. Access time of 300 ns eliminates the need for mpu wait states or software overhead. An Address Latch Enable input is provided to permit both multiplexed and direct addressing. These features allow easy interface with any available microprocessor. Other features include full calendar with automatic leap-year correction, on-chip battery backup switch over circuit and on-chip alarm comparator and RAM. Available in 24-pin plastic DIP and Cerdip package with temperature range from -40°C to $+85^{\circ}\text{C}$.



Section 2 — A/D Converters Display Type

ICL7106.....	2-1
ICL7107.....	2-1
ICL7116.....	2-13
ICL7117.....	2-13
ICL7126.....	2-24
ICL7129.....	2-35
ICL7136.....	2-47
ICL7137.....	2-58
ICL7139.....	2-67
ICL7149.....	2-81
ICL7182.....	2-95

ICL7106/ICL7107

3½-Digit LCD/LED

Single-Chip A/D Converter



ICL7106/ICL7107

2

GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, a reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10 pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. Finally, the true economy of single power supply operation (7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

FEATURES

- Guaranteed Zero Reading for 0 Volts Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct Display Drive — No External Components Required — LCD ICL7106 — LED ICL7107
- Low Noise — Less Than 15µV p-p
- On-Chip Clock and Reference
- Low Power Dissipation — Typically Less Than 10mW
- No Additional Active Circuits Required
- New Small Outline Surface Mount Package Available
- Evaluation Kit Available

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7106CPL	0°C to +70°C	40 pin plastic DIP
ICL7106CJL	0°C to +70°C	40 pin CERDIP
ICL7106CM44	0°C to +70°C	44 pin Surface Mount
ICL7107CJL	0°C to +70°C	40 pin CERDIP
ICL7107CPL	0°C to +70°C	40 pin plastic DIP
ICL7106EV/Kit ICL7107EV/Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.	

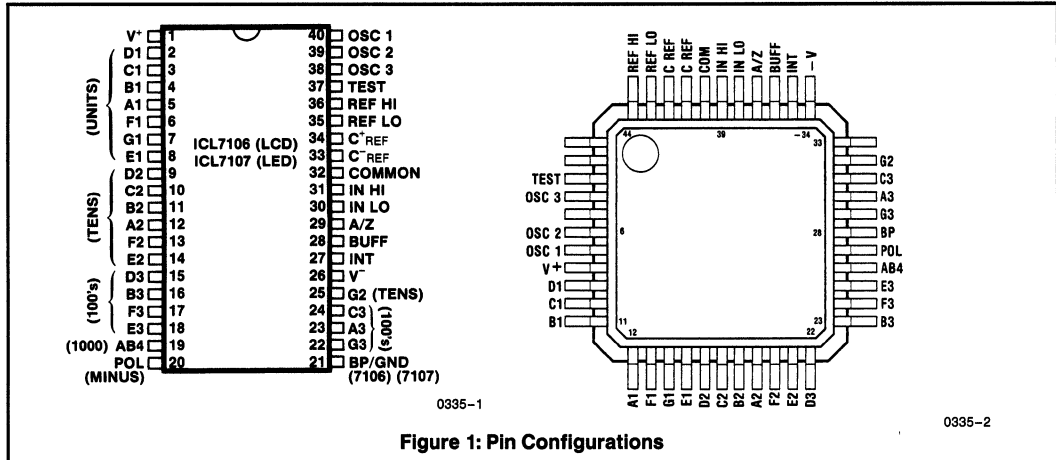


Figure 1: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

ICL7106/ICL7107



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
ICL7106, V ⁺ to V ⁻	15V
ICL7107, V ⁺ to GND	+6V
ICL7107, V ⁻ to GND	-9V
Analog Input Voltage (either input)(Note 1)	V ⁺ to V ⁻
Reference Input Voltage (either input)	V ⁺ to V ⁻
Clock Input	
ICL7106	TEST to V ⁺
ICL7107	GND to V ⁺

Power Dissipation (Note 2)

Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100\mu\text{A}$.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V _{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} V _{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	-V _{IN} = +V _{IN} \cong 200.0mV	-1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200.0mV or full scale = 2.000V (Note 6)	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V _{CM} = ±1V, V _{IN} = 0V Full Scale = 200.0mV		50		$\mu\text{V}/\text{V}$
Noise (Pk-Pk value not exceeded 95% of time)	V _{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current Input	V _{IN} = 0 (Note 6)		1	10	pA
Zero Reading Drift	V _{IN} = 0 0° < T _A < 70°C (Note 6)		0.2	1	$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	V _{IN} = 199.0mV 0° < T _A < 70°C (Ext. Ref. Oppm/°C) (Note 6)		1	5	ppm/°C
V ⁺ Supply Current (Does not include LED current for 7107)	V _{IN} = 0		0.8	1.8	mA
V ⁻ Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25k Ω between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25k Ω between Common & Pos. Supply		80		ppm/°C

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

Characteristics	Test Conditions	Min	Typ	Max	Unit
7106 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ \text{ to } V^- = 9V$	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19 & 20)	$V^+ = 5.0V$ Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
(Pin 20 only)		4	7		mA

NOTES: 3. Unless otherwise noted, specifications apply to both the 7106 and 7107 at $T_A = 25^\circ C$, $f_{clock} = 48kHz$. 7106 is tested in the circuit of Figure 2. 7107 is tested in the circuit of Figure 3.

4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. Not tested, guaranteed by design.



TEST CIRCUITS

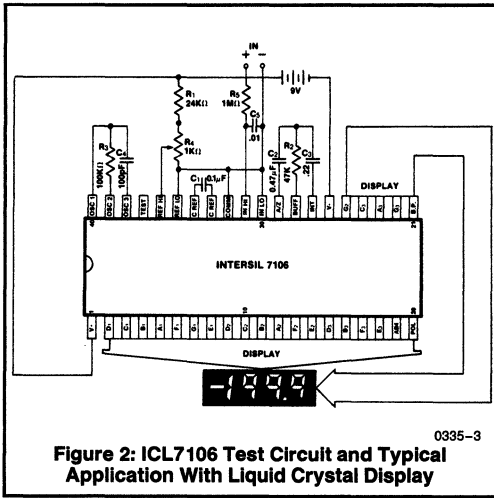


Figure 2: ICL7106 Test Circuit and Typical Application With Liquid Crystal Display

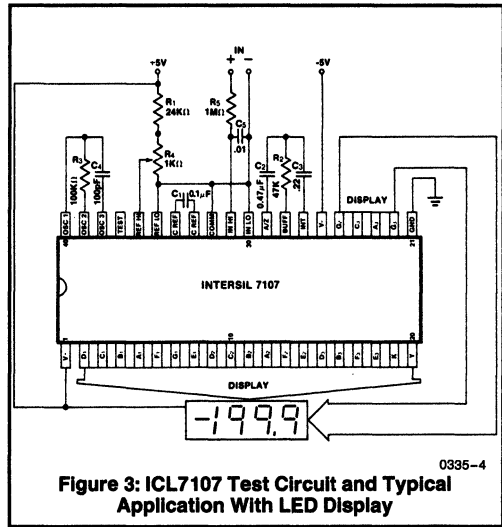


Figure 3: ICL7107 Test Circuit and Typical Application With LED Display

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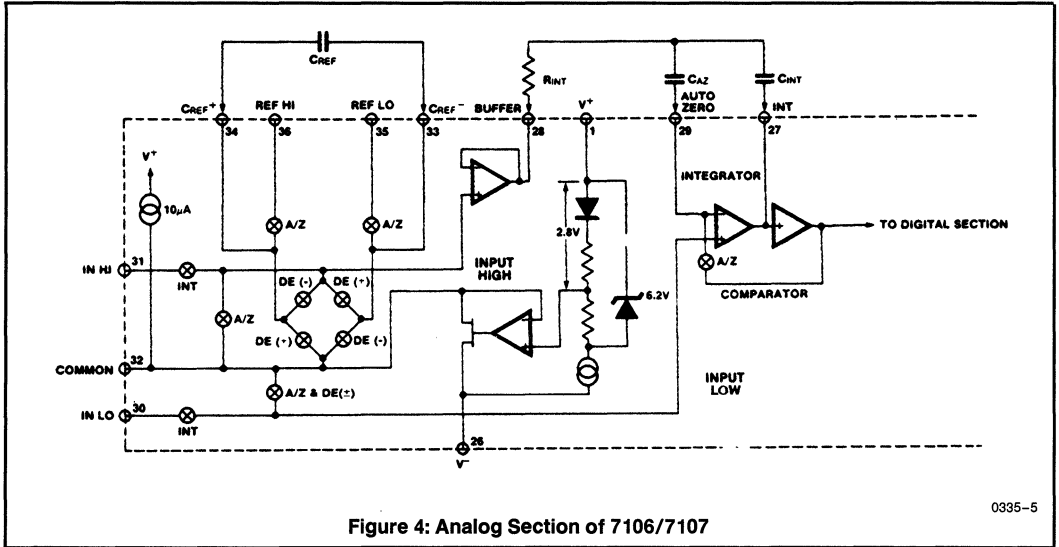


Figure 4: Analog Section of 7106/7107

0035-5

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to one volt from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the

capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000 \left(\frac{V_{IN}}{\sqrt{V_{REF}}} \right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range, the system has a CMRR of 86 dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See Application Note A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is

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NOTE: All typical values have been characterized but are not tested.

large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($>7V$), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance ($\approx 15\Omega$), and a temperature coefficient typically less than 80ppm/ $^{\circ}C$.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μV -p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overrange condition. This is because overrange is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overrange and a nonoverrange count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

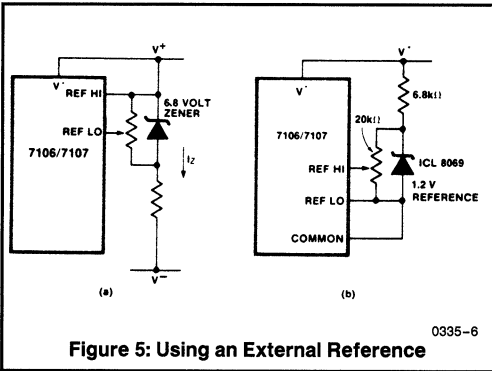


Figure 5: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 30mA of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.

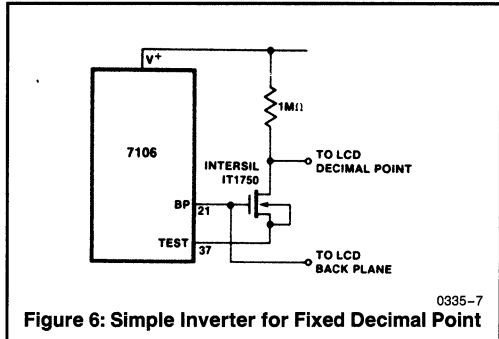


Figure 6: Simple Inverter for Fixed Decimal Point

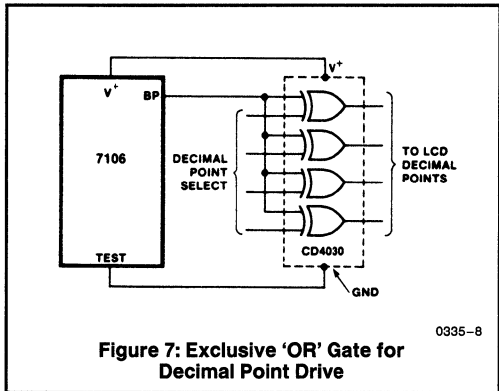


Figure 7: Exclusive 'OR' Gate for Decimal Point Drive

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DISPLAY FONT

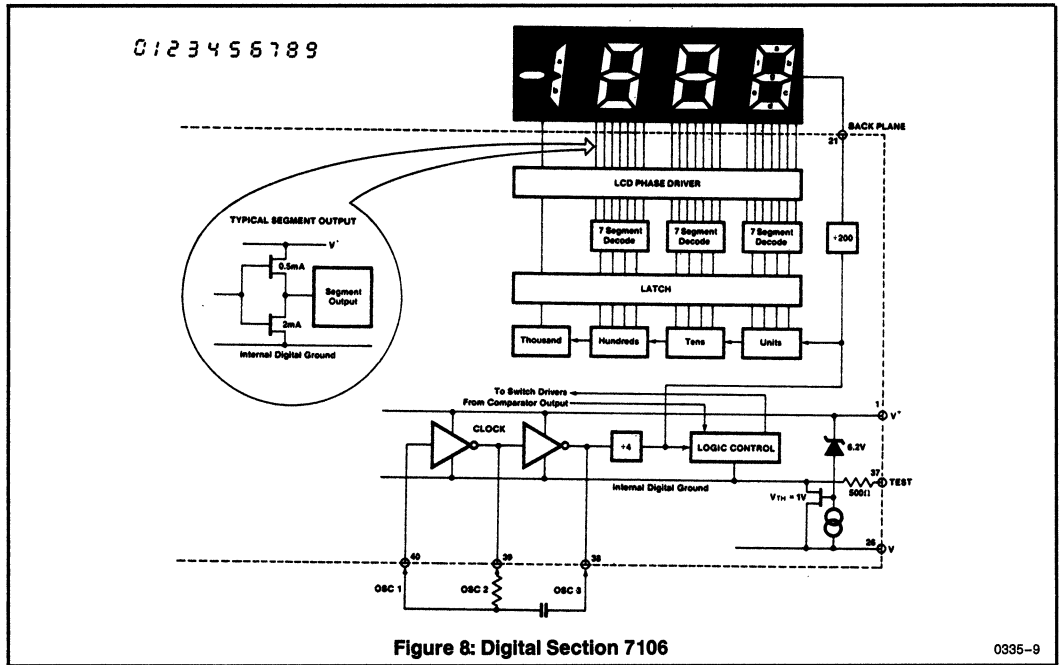


Figure 8: Digital Section 7106

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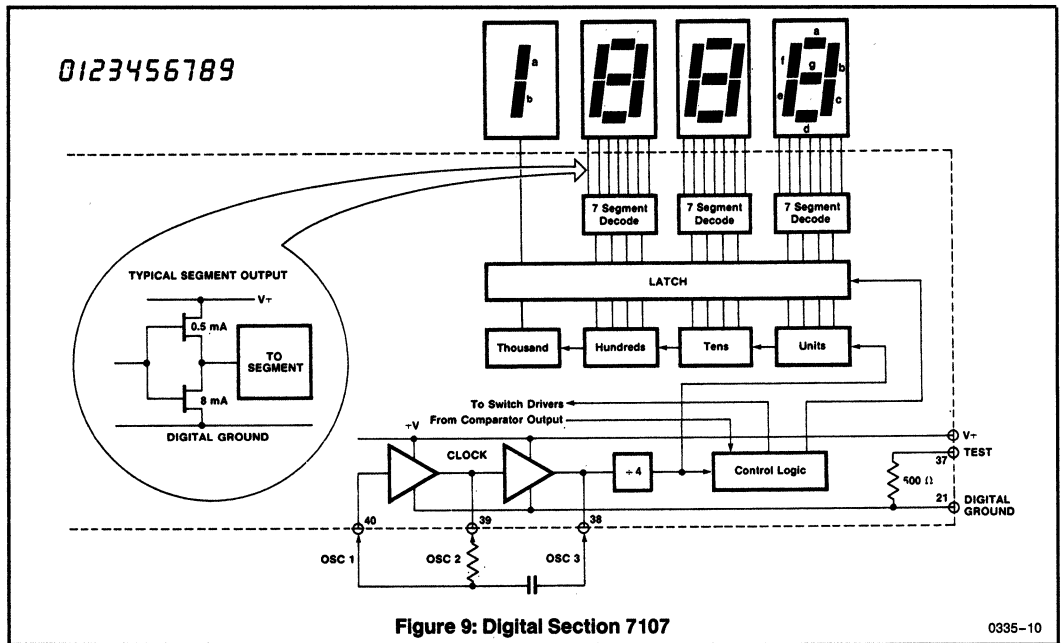


Figure 9: Digital Section 7107

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The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

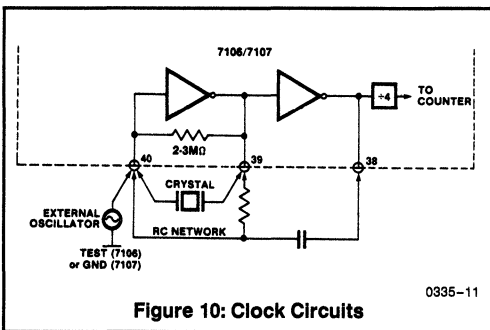
Figure 9 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Figure 10 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.



The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 $\frac{1}{3}$ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 $\frac{2}{3}$ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μ A of quiescent current. They can supply 20 μ A of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470k Ω is near optimum and similarly a 47k Ω for a 200.0 mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ± 2 volt full scale integrator swing is fine. For the 7107 with ± 5 volt supplies and analog COMMON tied to supply ground, a ± 3.5 to ± 4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22 μ F and 0.10 μ F, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable error at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47 μ F capacitor is recommended. On the 2 volt scale, a 0.047 μ F capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

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NOTE: All typical values have been characterized but are not tested.

ICL7106/ICL7107



Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, V_{ref} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

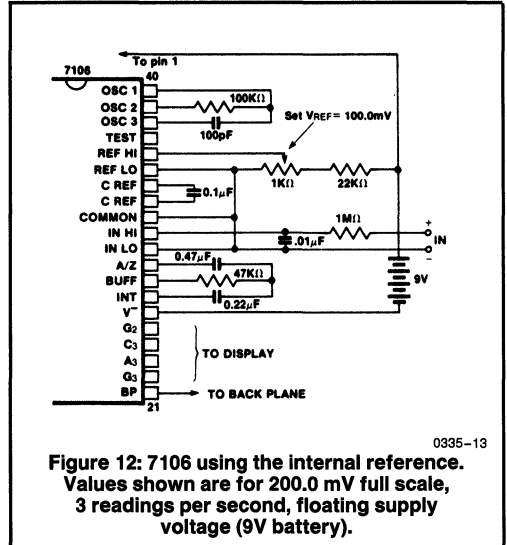


Figure 12: 7106 using the internal reference.
 Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

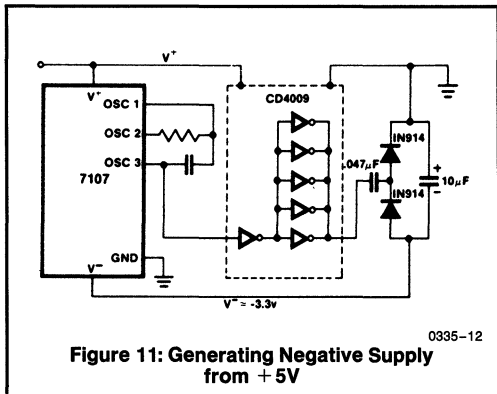
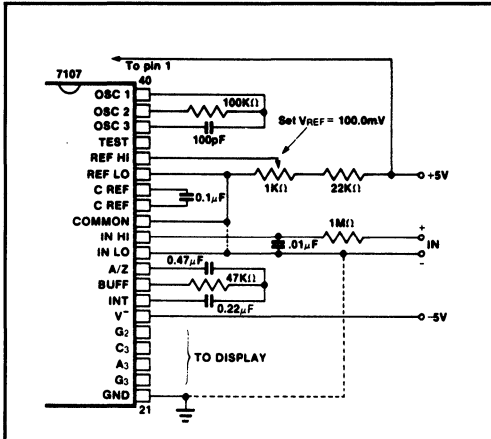


Figure 11: Generating Negative Supply from +5V

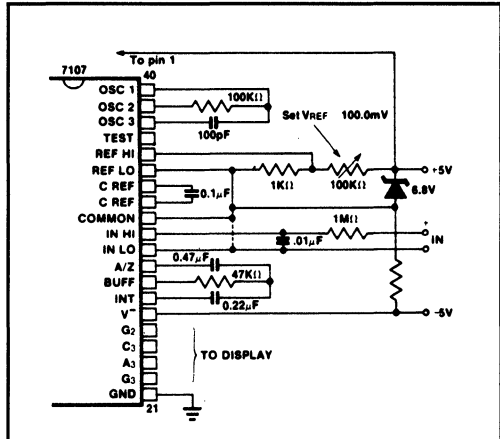
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NOTE: All typical values have been characterized but are not tested.



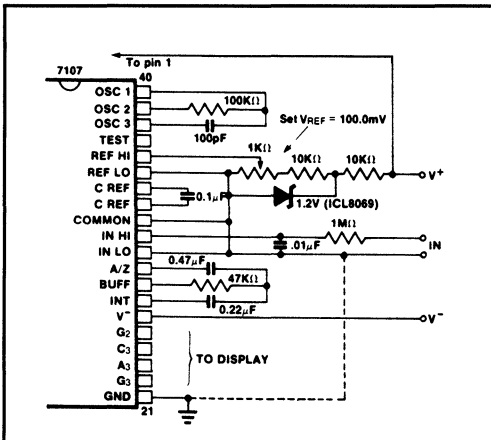
0335-14

Figure 13: 7107 using the internal reference.
 Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)



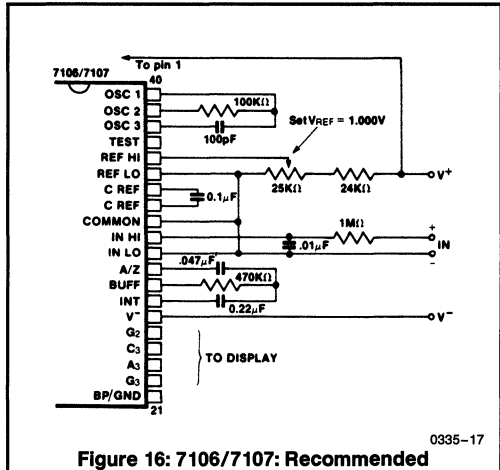
0335-16

Figure 15: 7107 with Zener diode reference.
 Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 15, IN LO may be tied to either COMMON or GND.



0335-15

Figure 14: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-riden.

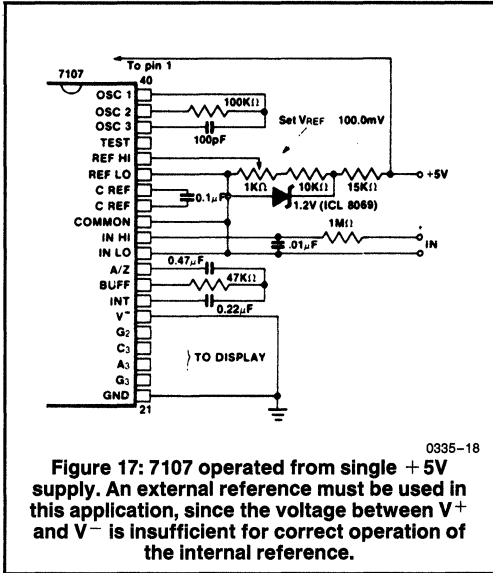


0335-17

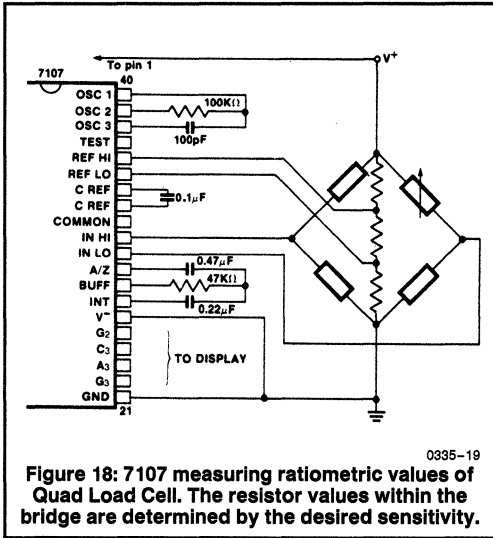
Figure 16: 7106/7107: Recommended component values for 2.000V full scale.

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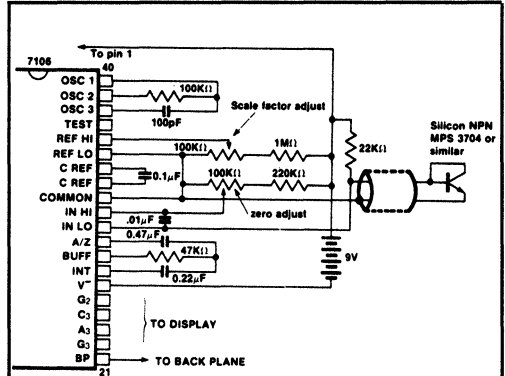
NOTE: All typical values have been characterized but are not tested.



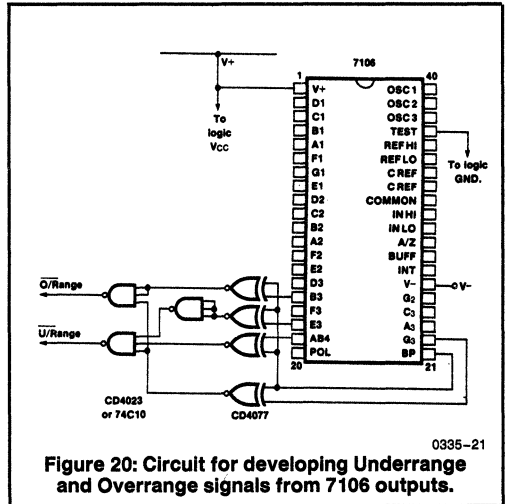
0335-18
Figure 17: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.



0335-19
Figure 18: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.



0335-20
Figure 19: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.



0335-21
Figure 20: Circuit for developing Underrange and Overrange signals from 7106 outputs.

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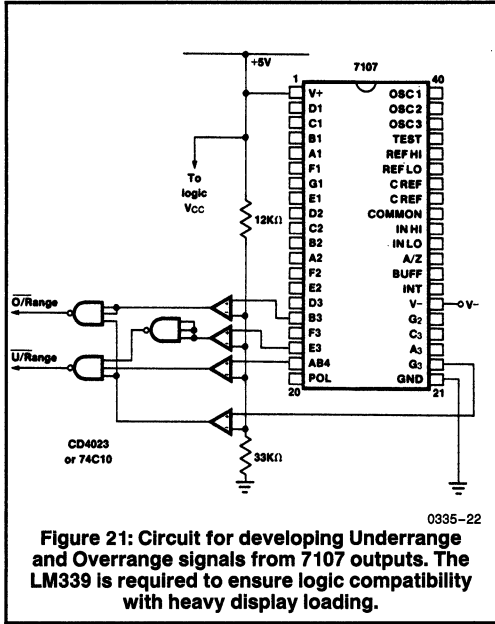


Figure 21: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of addition-

al components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

- A016 "Selecting A/D Converters", by David Fullagar.
- A017 "The Integrating A/D Converter", By Lee Evans.
- A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
- A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
- A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

2

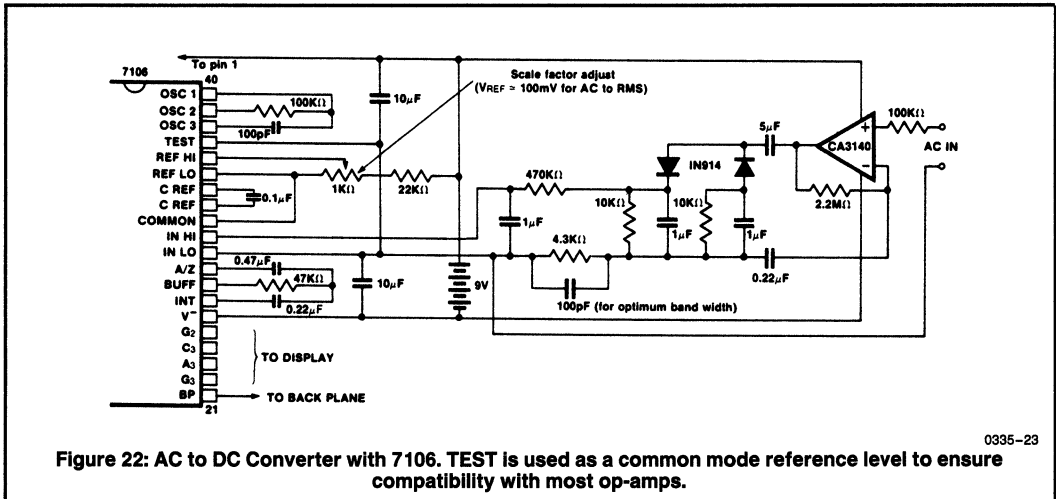
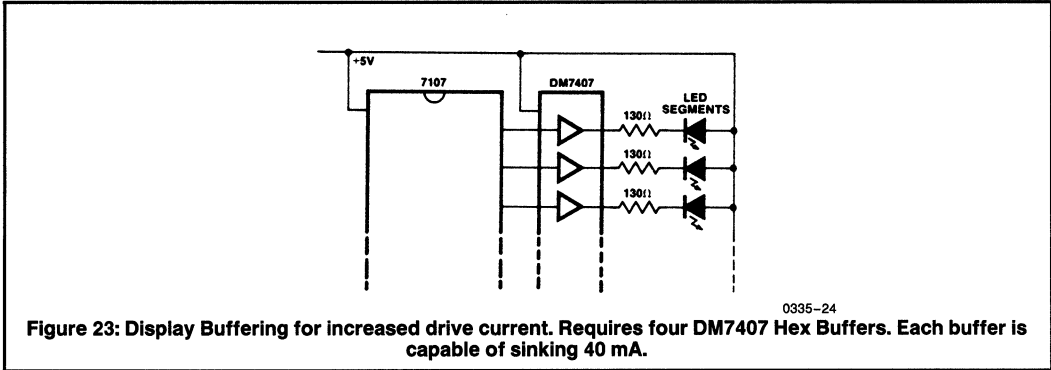


Figure 22: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

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NOTE: All typical values have been characterized but are not tested.

ICL7116/7117

3½-Digit LCD/LED

Single-Chip A/D Converter with Display Hold



ICL7116/7117

GENERAL DESCRIPTION

The Intersil ICL7116 and 7117 are high performance, low power 3-½ digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HoLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. They feature auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

FEATURES

- HoLD Reading Input Allows Indefinite Display Hold
- Guaranteed Zero Reading for 0 Volts Input
- True Polarity at Zero for Precise Null Detection
- 1pA Input Current Typical
- True Differential Input
- Direct Display Drive — No External Components Required — LCD ICL7116 — LED ICL7117
- Low Noise — Less Than 15µV pk-pk Typical
- On-Chip Clock and Reference
- Low Power Dissipation — Typically Less Than 10mW
- No Additional Active Circuits Required
- New Small Outline Surface Mount Package Available

2

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7116CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7116CM44	0°C to +70°C	44-Pin Surface Mount
ICL7117CPL	0°C to +70°C	40-Pin Plastic DIP

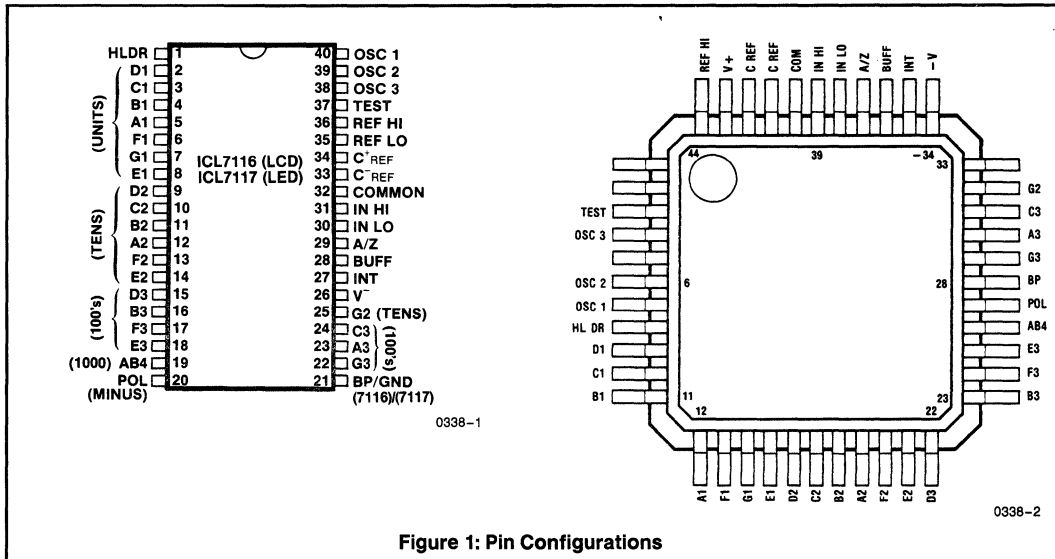


Figure 1: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V ⁺ to V ⁻)	15V
Analog Input Voltage (either input) (Note 1)	V ⁺ to V ⁻
Reference Input Voltage (either input)	V ⁺ to V ⁻
HILDR, Clock Input	Test to V ⁺
Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

ICL7117

Supply Voltage V ⁺	+6V
V ⁻	-9V
Analog Input Voltage (either input) (Note 1)	V ⁺ to V ⁻
Reference Input Voltage (either input)	V ⁺ to V ⁻
HILDR, Clock Input	Grnd to V ⁺
Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100\mu\text{A}$.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V _{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} V _{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	V _{IN} \cong 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V (Note 7)	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V _{CM} = $\pm 1\text{V}$, V _{IN} = 0V, Full Scale = 200.0mV		50		$\mu\text{V}/\text{V}$
Noise (Pk — Pk value not exceeded 95% of time)	V _{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V _{IN} = 0V (Note 7)		1	10	pA
Zero Reading Drift	V _{IN} = 0 0°C < T _A < 70°C (Note 7)		0.2	1	$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	V _{IN} = 199.0mV 0°C < T _A < 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V ⁺ Supply Current (Does not include LED current for 7117)	V _{IN} = 0		0.8	1.8	mA
V ⁻ Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25k Ω between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25k Ω between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		k Ω
V _{IL} , Pin 1 (7116 only)				TEST + 1.5	V

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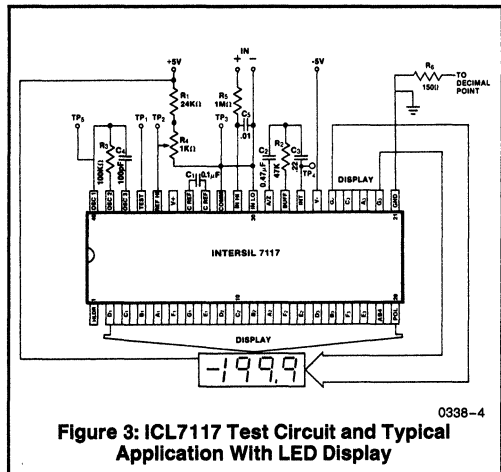
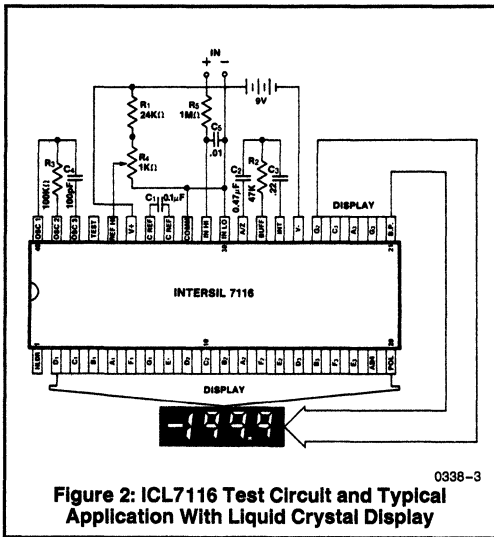
ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL} , Pin 1 (7117 only)				GND+ 1.5	V
V_{IH} , Pin 1 (Both)		$V^+ - 1.5$			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	$V^+ - V^- = 9V$	4 4	5 5	6 6	V
7117 ONLY Segment Sinking Current (Except Pin 19 and 20) (Pin 19 only) (Pin 20 only)	$V^+ = 5.0V$ Segment Voltage = 3V	5 10 4	8.0 16 7		mA

NOTES: 3. Unless otherwise noted, specifications apply to both the 7116 and 7117 at $T_A = 25^\circ C$, $f_{clock} = 48kHz$. 7116 is tested in the circuit of Figure 2. 7117 is tested in the circuit of Figure 3.

4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.
7. Not tested, guaranteed by design.

TEST CIRCUITS



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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10\mu V$.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and

low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$1000 \left(\frac{V_{in}}{V_{ref}} \right)$$

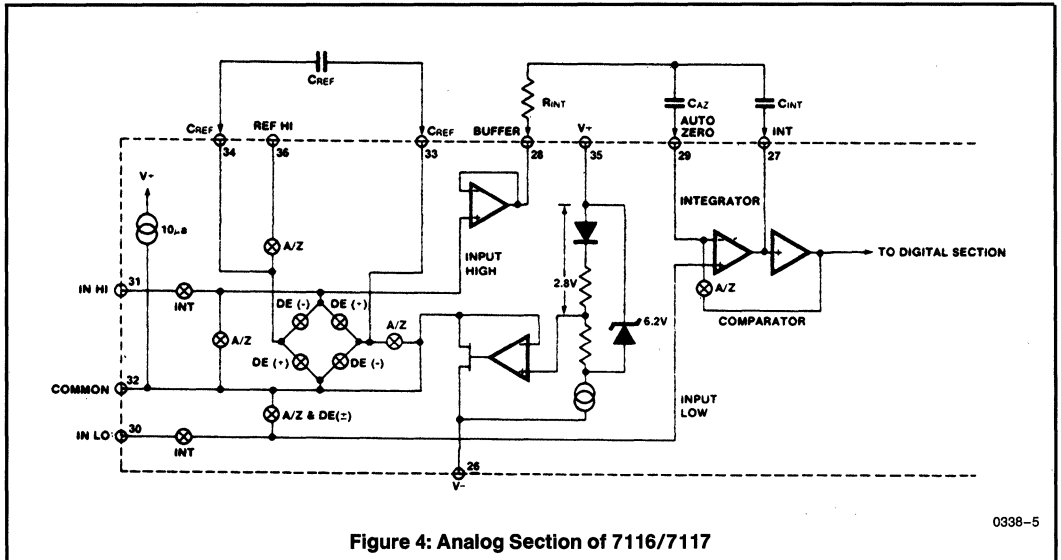


Figure 4: Analog Section of 7116/7117

0338-5

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Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of typically 86dB. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See Application Note A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts less than the positive supply. This is selected to provide proper operation with a minimum end-of-life battery voltage of about 6V. However, analog COMMON does have some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($> 7V$), the COMMON voltage will have a low voltage coefficient ($.001\%/V$), low output impedance ($\approx 15\Omega$), and a temperature coefficient typically less than $80\text{ppm}/^\circ\text{C}$.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from $25\mu\text{V}$ to $80\mu\text{Vpk-pk}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.

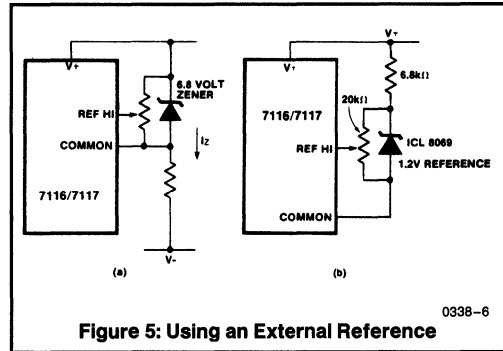


Figure 5: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only $10\mu\text{A}$ of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.

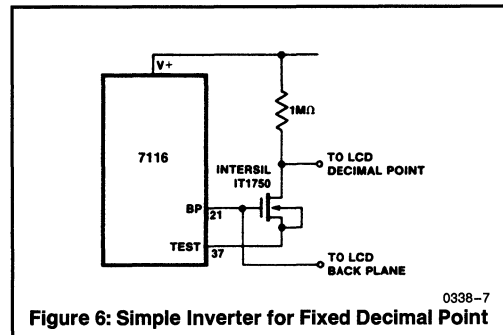
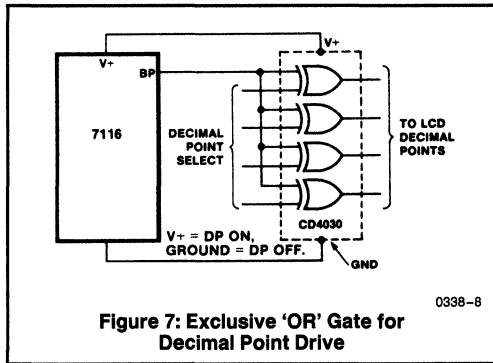


Figure 6: Simple Inverter for Fixed Decimal Point

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NOTE: All typical values have been characterized but are not tested.



The second function is a "lamp test". When TEST is pulled to high (to V^+) all segments will be turned on and the display should read - 1888. [Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7117. It is identical to that of the 7116 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

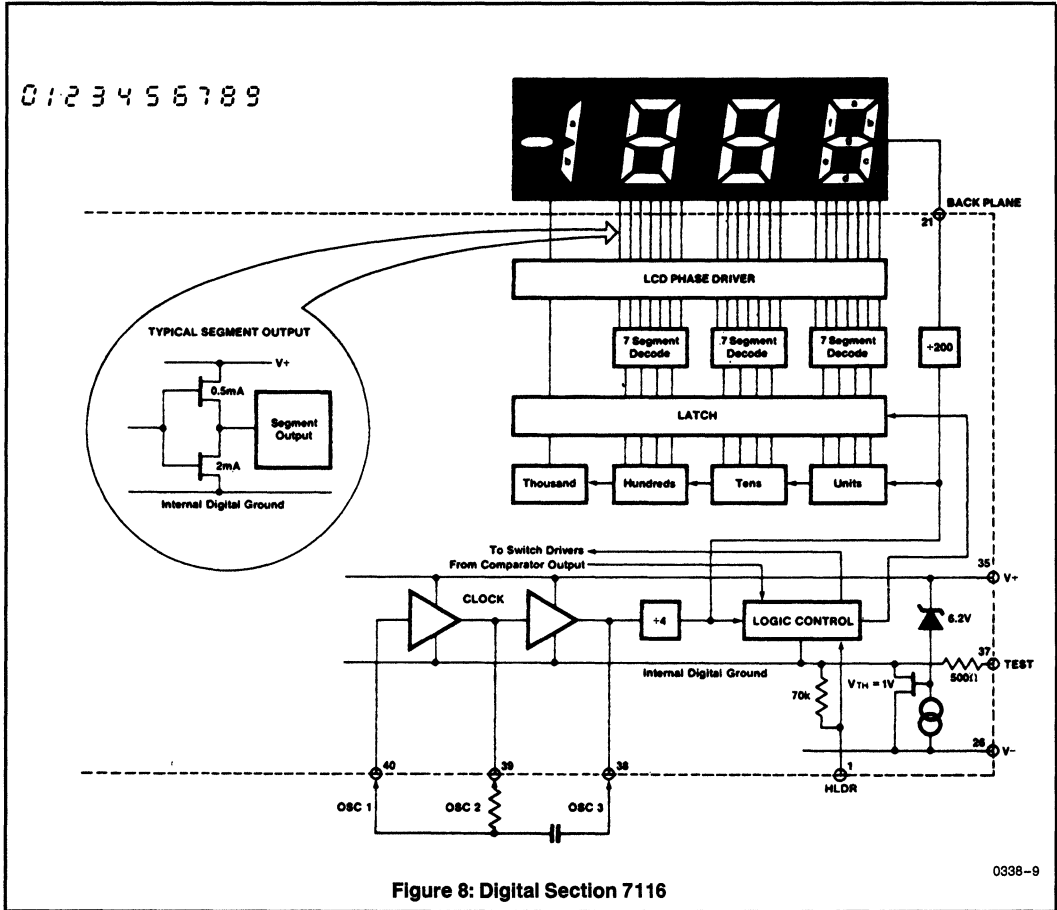
In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70k Ω typical resistance to either TEST (7116) or GROUND (7117).

DISPLAY FONT

2



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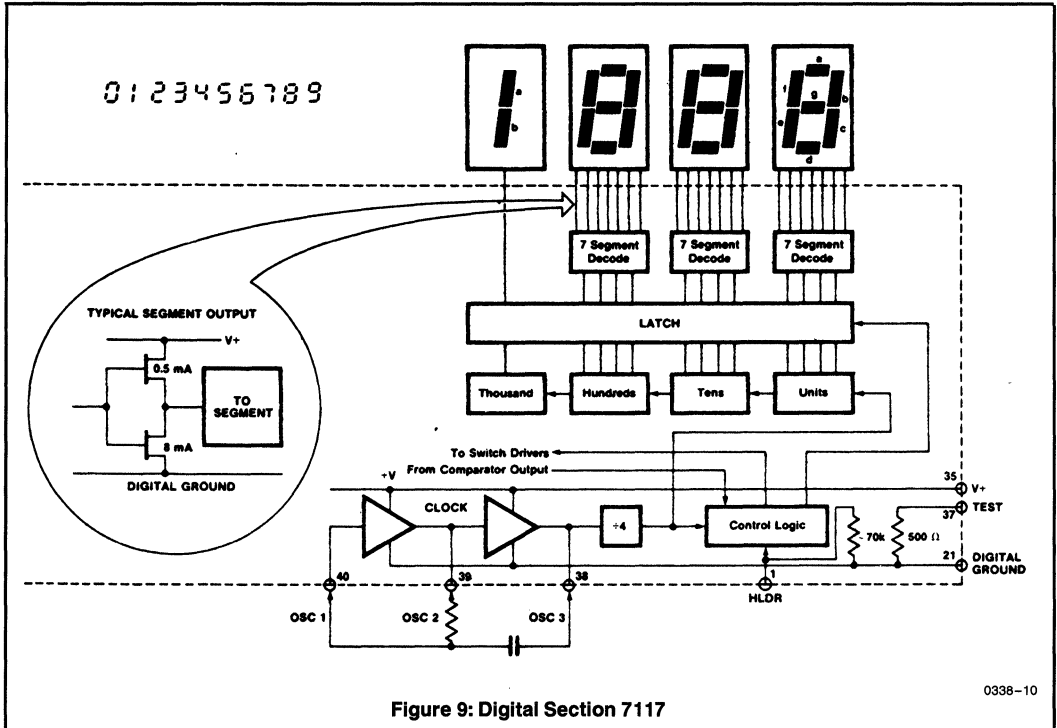


Figure 9: Digital Section 7117

0338-10

System Timing

Figure 10 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

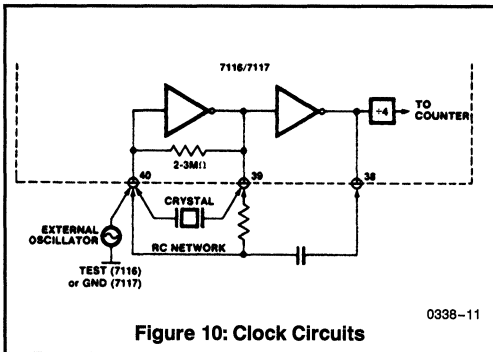


Figure 10: Clock Circuits

0338-11

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 $\frac{1}{3}$ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 $\frac{2}{3}$ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

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COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μ A of quiescent current. They can supply 20 μ A of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volts full scale, 470k Ω is near optimum and similarly a 47k Ω resistor is optimum for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ± 2 volt full scale integrator swing is fine. For the 7117 with ± 5 volt supplies and analog common tied to supply ground, a ± 3.5 to ± 4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are 0.22 μ F and 0.10 μ F, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47 μ F capacitor is recommended. On the 2 volt scale, a 0.047 μ F capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μ F capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0 μ F may be required.

Oscillator Components

For all ranges of frequency a 100k Ω resistor is recommended and the capacitor is selected from the equation $f \approx \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, V_{REF} should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the

digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. Suitable values for integrating resistor and capacitor would be 120k Ω and 0.22 μ F. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ± 5 volts supplies can accept input signals up to ± 4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7117 Power Supplies

The 7117 is designed to work from ± 5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.

2

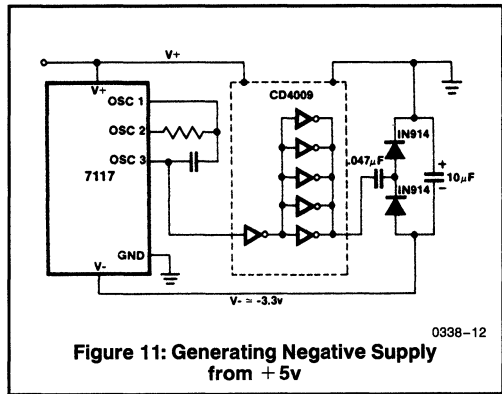


Figure 11: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

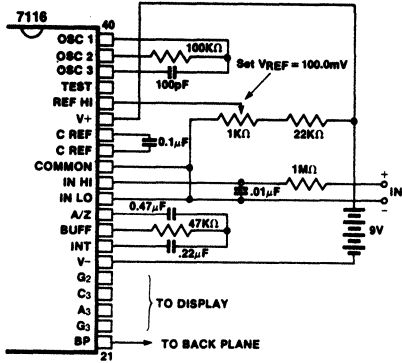
1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ± 1.5 volts in magnitude.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

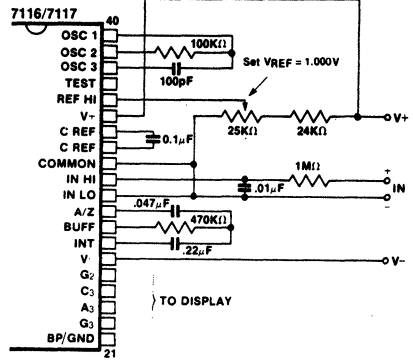
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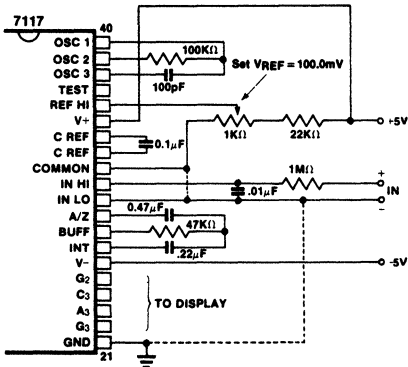
0338-13

Figure 12: 7116 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).



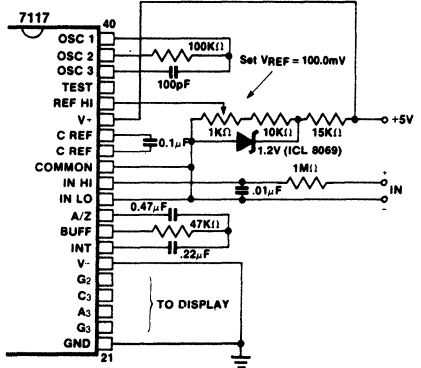
0338-15

Figure 14: 7116/7117: Recommended component values for 2.000V full scale.



0338-14

Figure 13: 7117 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)



0338-16

Figure 15: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

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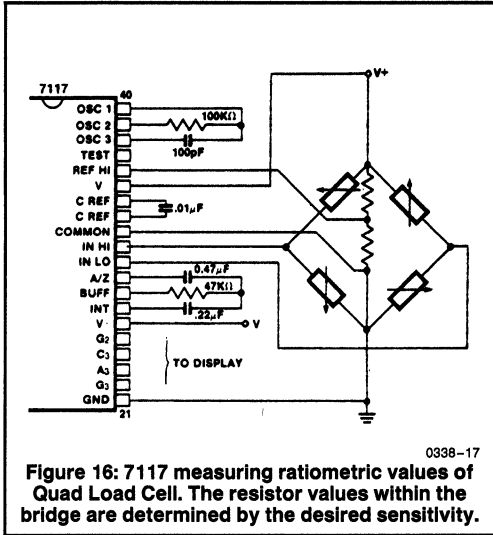


Figure 16: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

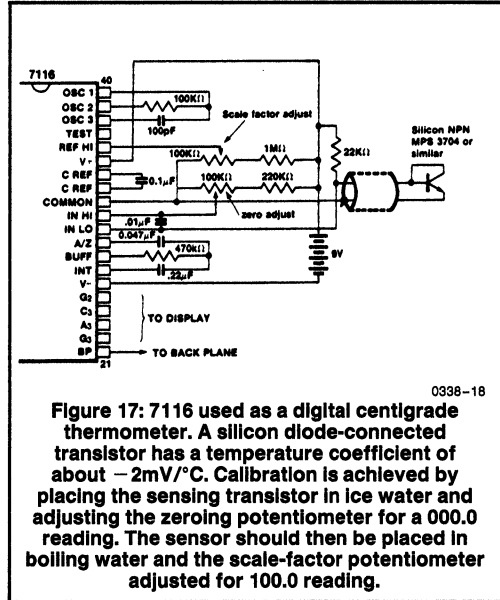


Figure 17: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about $-2\text{mV}/^\circ\text{C}$. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

APPLICATION NOTES

- A016 "Selecting A/D Converters," by David Fullagar.
- A017 "The Integrating A/D Converter," by Lee Evans.
- A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047 "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
- A052 "Tips for Using Single-Chip $3\frac{1}{2}$ -Digit A/D Converters," by Dan Watson.

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ICL7126

3 1/2-Digit Low-Power Single-Chip A/D Converter



GENERAL DESCRIPTION

The Intersil ICL7126 is a high performance, very low power 3 1/2-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is 100µA, ideally suited for 9V battery operation.

The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

FEATURES

- 8,000 Hours Typical 9 Volt Battery Life
- Guaranteed Zero Reading for 0 Volts Input On All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LCD Display Drive — No External Components Required
- Pin Compatible With The ICL7106
- Low Noise — Less Than 15µVp-p
- On-Chip Clock and Reference
- Low Power Dissipation Guaranteed Less Than 1mW
- No Additional Active Circuits Required
- Evaluation Kit Available (ICL7126EV/KIT)

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7126CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7126CM44	0°C to +70°C	40-Pin Surface Mount
ICL7126RCPL	0°C to +70°C	40-Pin Plastic DIP

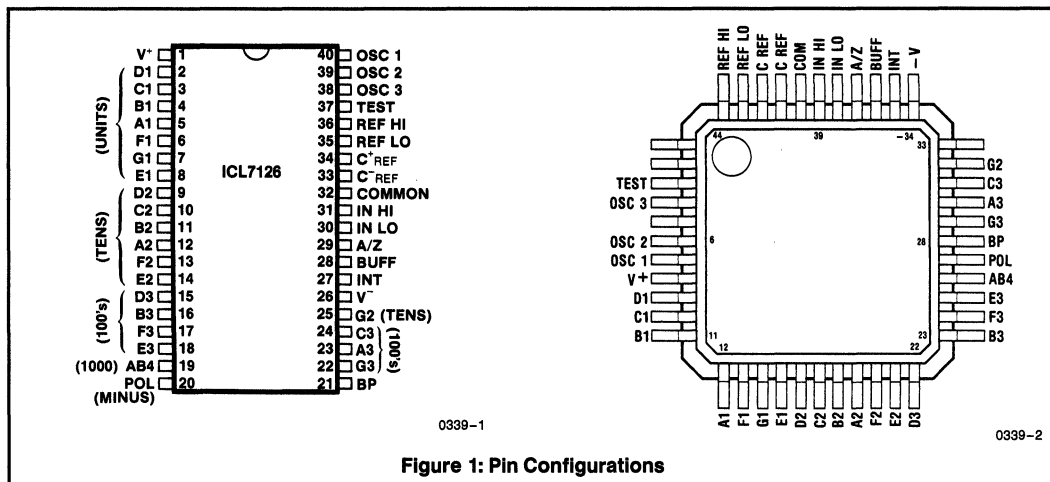


Figure 1: Pin Configurations

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V⁺ to V⁻) 15V
 Analog Input Voltage (Either Input) (Note 1) V⁺ to V⁻
 Reference Input Voltage (Either Input) V⁺ to V⁻
 Clock Input TEST to V⁺

Power Dissipation (Note 2)
 Ceramic Package 1000mW
 Plastic Package 800mW
 Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.

NOTE 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V _{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} V _{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	-V _{IN} = +V _{IN} ≈ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V _{CM} = ±1V, V _{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk - Pk value not exceeded 95% of time)	V _{IN} = 0V Full Scale = 200.0mV		15		µV
Leakage Current @ Input	V _{IN} = 0V		1	10	pA
Zero Reading Drift	V _{IN} = 0 0°C < T _A < 70°C		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V _{IN} = 199.0mV 0°C < T _A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V _{IN} = 0 (Note 6)		70	100	µA
Analog COMMON Voltage (With respect to pos. supply)	250kΩ between Common & pos. Supply	2.4	2.8	3.2	V

2

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ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250kΩ between Common & pos. Supply		150		ppm/°C
PK-Pk Segment Drive Voltage (Note 5)	V+ to V- = 9V	4	5	6	V
PK-Pk Backplane Drive Voltage (Note 5)	V+ to V- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.

4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 5, increases current by 8μA (typ).
7. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

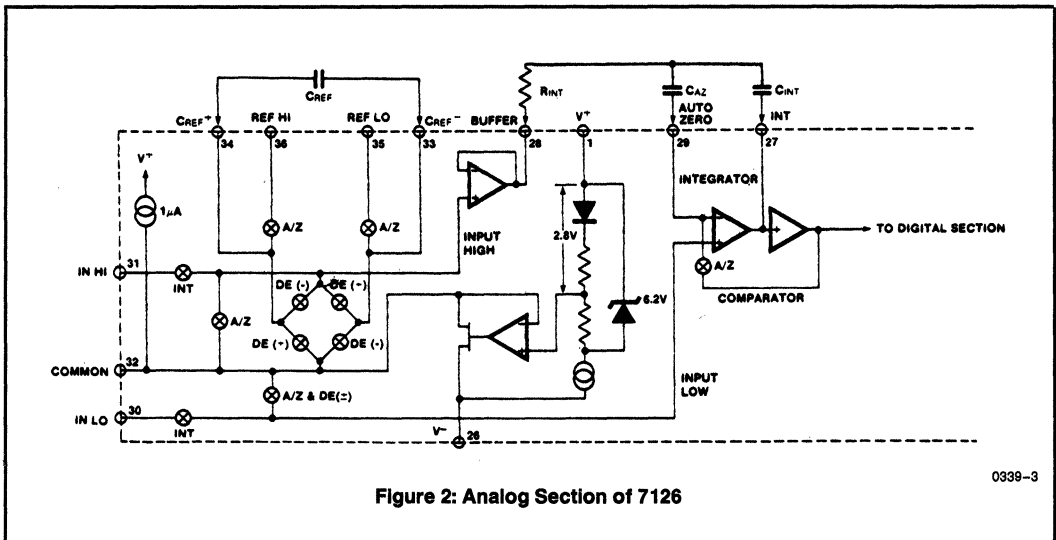


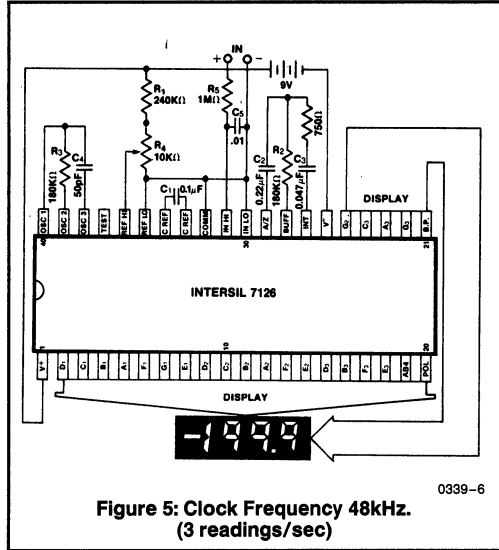
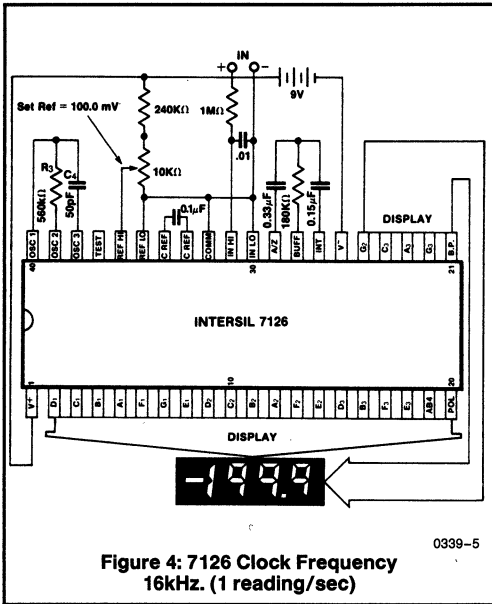
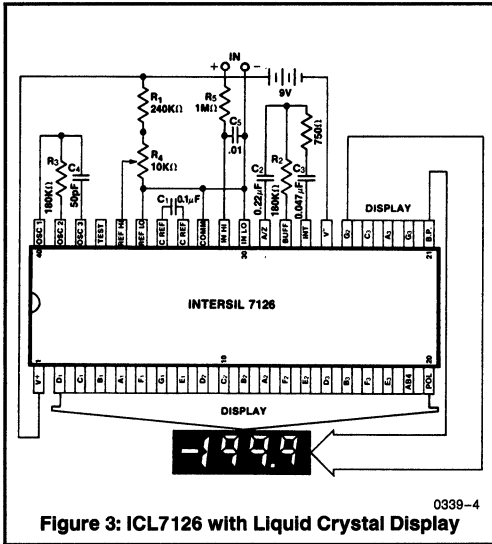
Figure 2: Analog Section of 7126

0939-3

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TEST CIRCUITS



2

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and in-

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put high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000 \left(\frac{V_{IN}}{V_{REF}} \right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\approx 15\Omega$), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temper-

ature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

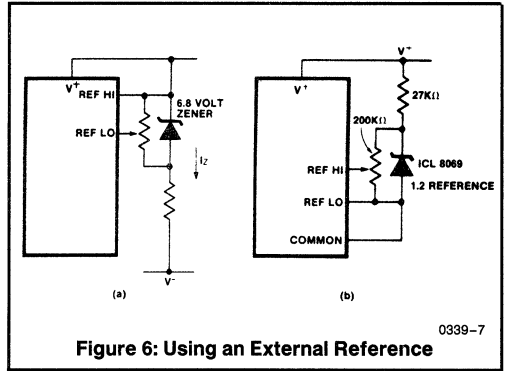


Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 3mA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1µA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

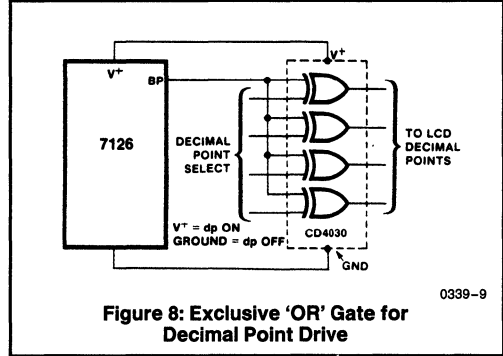
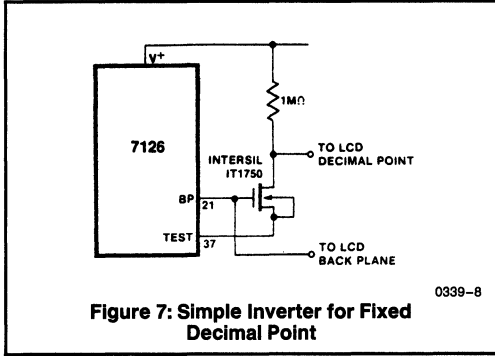
The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

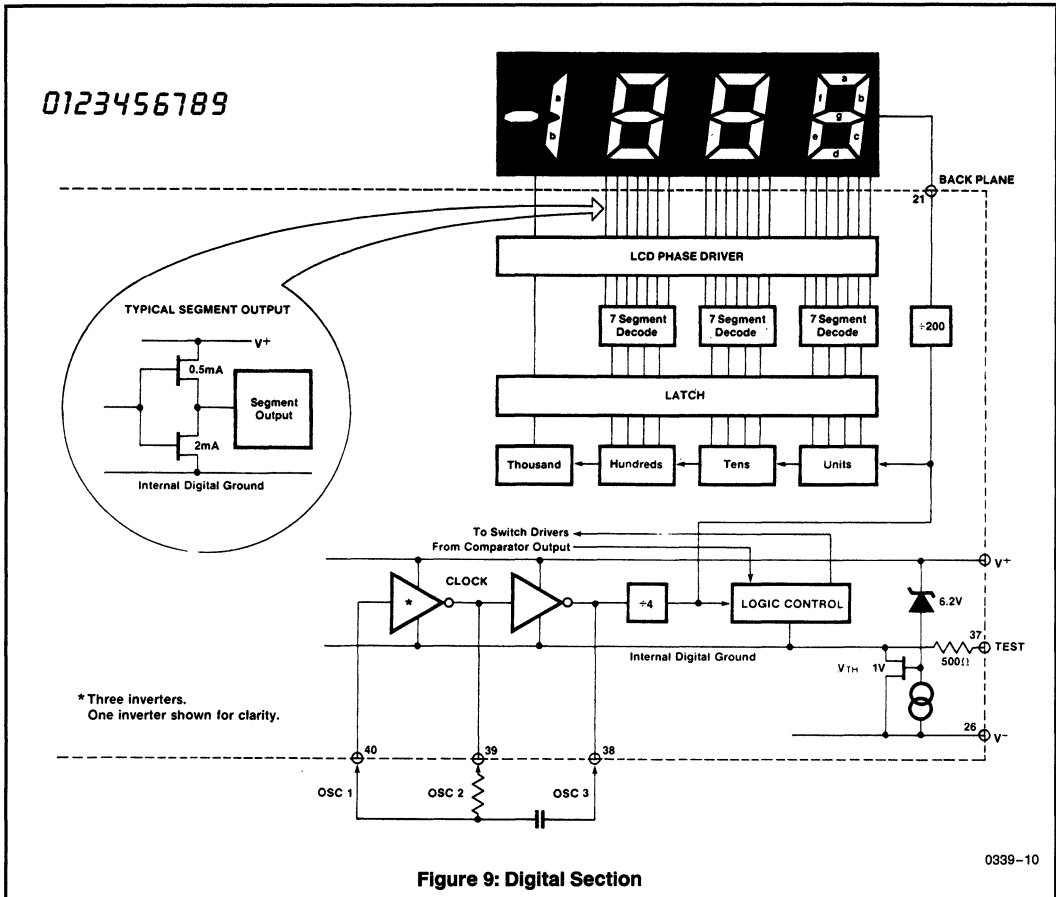
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NOTE: All typical values have been characterized but are not tested.



DISPLAY FONT

2



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NOTE: All typical values have been characterized but are not tested.

DIGITAL SECTION

Figure 9 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Figure 10 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

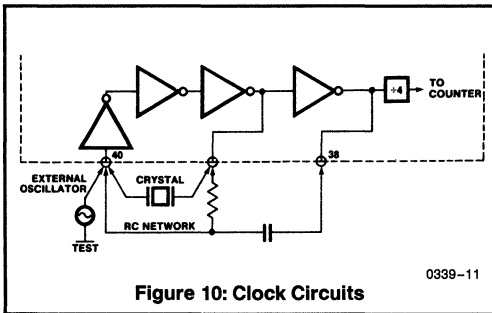


Figure 10: Clock Circuits

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8mΩ is near optimum and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), R = 180kΩ.

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NOTE: All typical values have been characterized but are not tested.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 Volt scale, V_{REF} should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for integrating resistor would be 330k Ω . This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

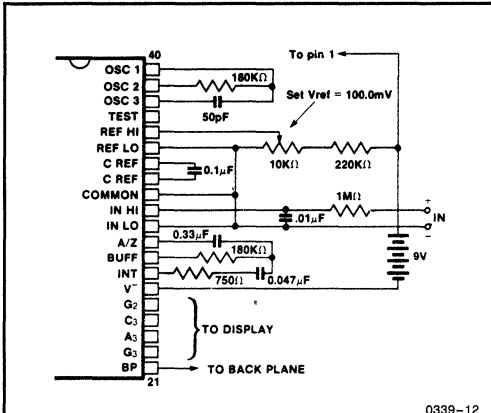


Figure 11: 7126 using the internal reference.

Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).

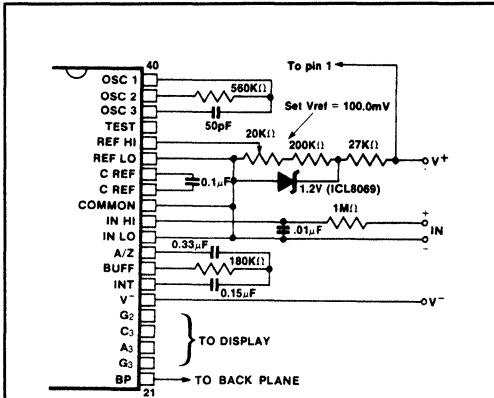


Figure 12: 7126 with an external band-gap reference (1.2V type).

IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.

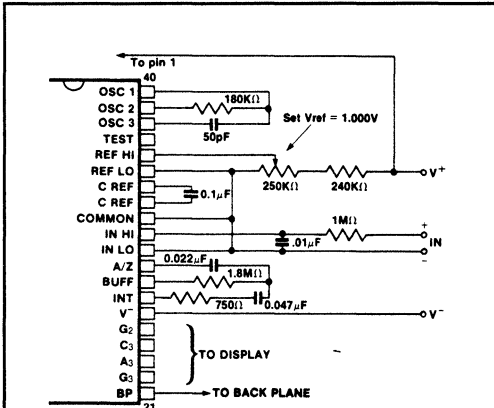
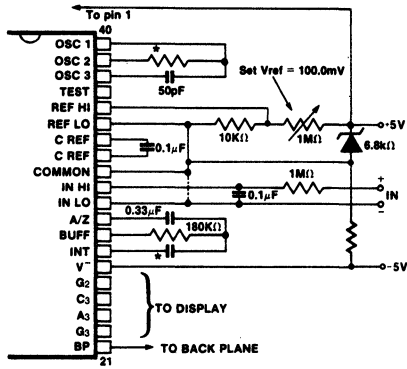


Figure 13: Recommended component values for 2.000V full scale, 3 readings per second.

For 1 reading per second, delete 750 Ω resistor, change C_{INT} , R_{OSC} to values of Figure 12.

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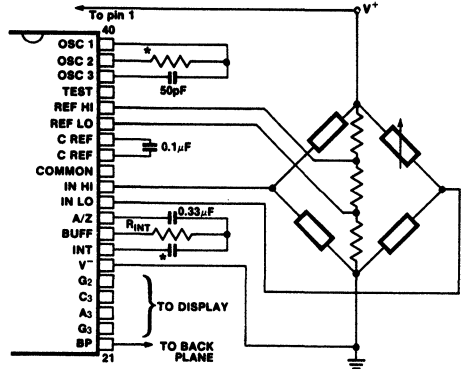
NOTE: All typical values have been characterized but are not tested.



0339-15

Figure 14: 7126 with Zener diode reference.

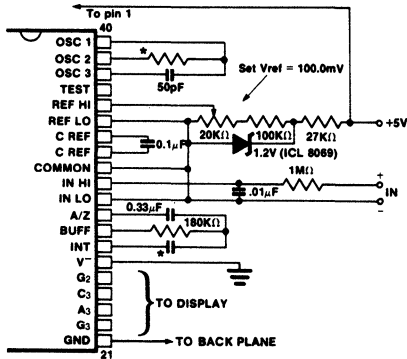
Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



0339-17

Figure 16: 7126 measuring ratiometric values of Quad Load Cell.

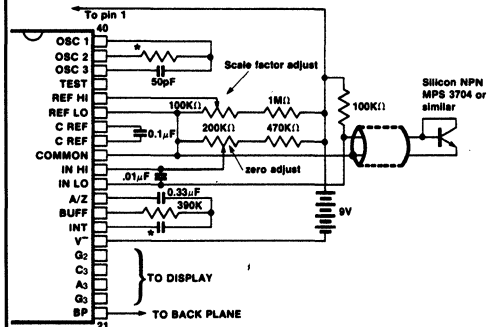
The resistor values within the bridge are determined by the desired sensitivity.



0339-16

Figure 15: 7126 operated from single +5V supply.

An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.



0339-18

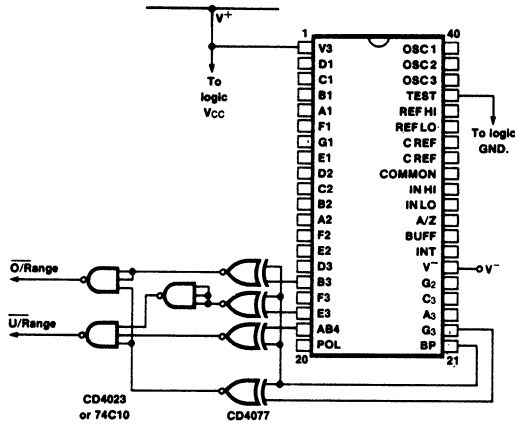
Figure 17: 7126 used as a digital centigrade thermometer.

A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

*Values depend on clock frequency. See Figures 11, 12, 13.

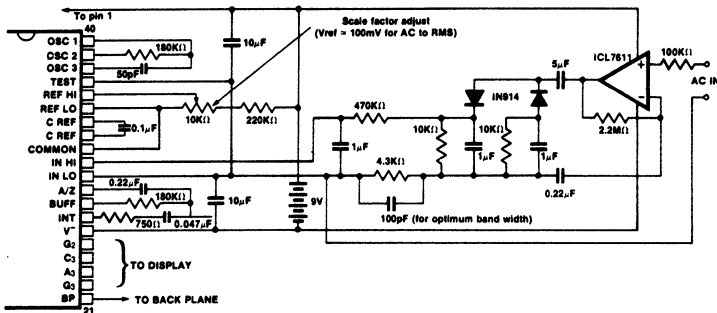
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NOTE: All typical values have been characterized but are not tested.



0339-19

Figure 18: Circuit for developing Underrange and Overrange signals from 7126 outputs.



0339-20

Figure 19: AC to DC Converter with 7126. Test is used as a common mode reference level to ensure compatibility with most op-amps.

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NOTE: All typical values have been characterized but are not tested.

APPLICATION NOTES

- A016** "Selecting A/D Converters", by David Fullagar.
- A017** "The Integrating A/D Converter", by Lee Evans.
- A018** "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.
- A023** "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.
- A032** "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.
- A046** "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.
- A052** "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

7126 EVALUATION KIT

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

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NOTE: All typical values have been characterized but are not tested.

ICL7129

4 1/2 Digit LCD Single-Chip A/D Converter



ICL7129

GENERAL DESCRIPTION

The Intersil ICL7129 is a very high-performance 4 1/2-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high-resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10µV/count.

The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

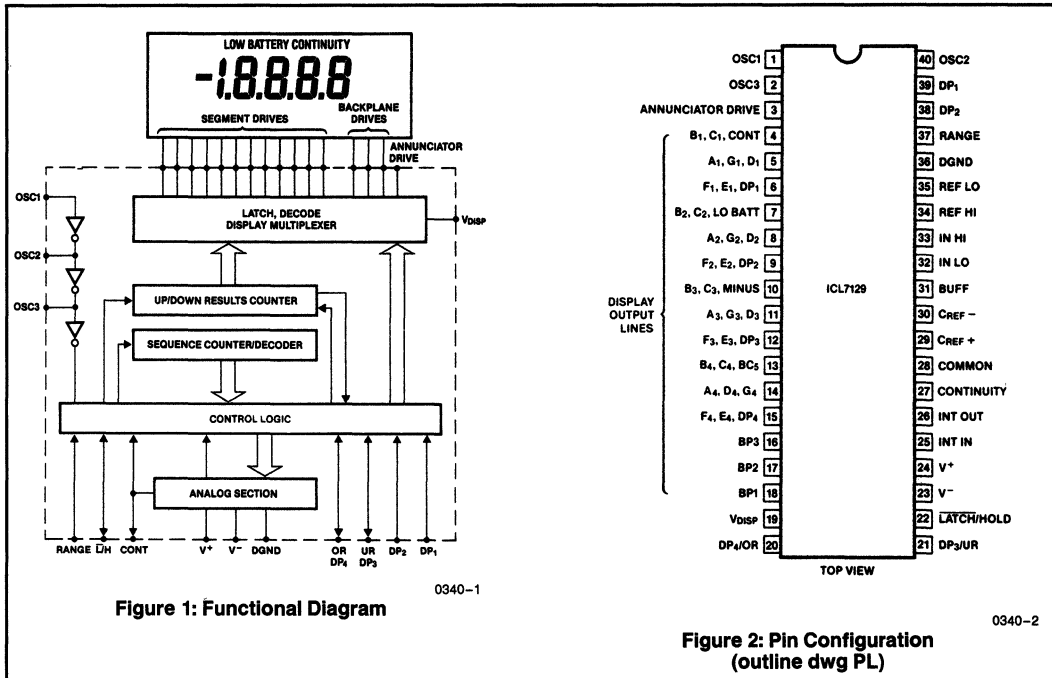
FEATURES

- ± 19,999 Count A/D Converter Accurate to ± 4 Count
- 10µV Resolution On 200mV Scale
- 110dB CMRR
- Direct LCD Display Drive
- True Differential Input and Reference
- Low Power Consumption
- Decimal Point Drive Outputs
- Overrange and Underrange Outputs
- Low Battery Detection and Indication
- 10:1 Range Change Input

ORDERING INFORMATION

Part Number	Temperature	Package
ICL7129CPL	0°C to +70°C	40-Pin Plastic
ICL7129EV/KIT	—	Evaluation Kit

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V^+ to V^-)	15V
Reference Voltage (REF HI or REF LO)	V^+ to V^-
Input Voltage (Note 1)	V^+ to V^-
(IN HI or IN LO)	V^+ to V^-
V_{DISP}	DGND $-0.3V$ to V^+
Digital Input Pins	
1, 2, 19, 20, 21, 22, 27,	
37, 38, 39, 40	DGND to V^+

Power Dissipation (Note 2)	
Plastic package	800mW
Operating Temperature	0°C to $+70^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to $\pm 400\mu\text{A}$. Currents above this value may result in invalid display readings but will not destroy the device if limited to $\pm 1\text{mA}$.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V^- to $V^+ = 9V$, $V_{REF} = 1.00V$, $T_A = +25^\circ\text{C}$, $f_{CLK} = 120\text{kHz}$, unless otherwise noted.

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	$V_{IN} = 0V$ 200mV Scale	-0000	0000	+0000	Counts
Zero Reading Drift	$V_{IN} = 0V$ $0^\circ\text{C} < T_A < +70^\circ\text{C}$		± 0.5		$\mu\text{V}/^\circ\text{C}$
Ratiometric Reading	$V_{IN} = V_{REF} = 1000\text{mV}$ RANGE = 2V	9996	9999	10000	Counts
Range Change Accuracy	$V_{IN} = 0.10000V$ on Low Range \approx $V_{IN} = 1.0000V$ on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN} = +V_{IN} = 199\text{mV}$		1.5	3.0	Counts
Linearity Error	200mV Scale		1.0		
Input Common-Mode Rejection Ratio	$V_{CM} = 1.0V$, $V_{IN} = 0V$ 200mV Scale		110		dB
Input Common-Mode Voltage Range	$V_{IN} = 0V$ 200mV Scale		$(V^-) + 1.5$ $(V^+) - 1.0$		V
Noise (p-p Value not Exceeding 95% of Time)	$V_{IN} = 0V$ 200mV Scale		14		μV
Input Leakage Current	$V_{IN} = 0V$, Pin 32, 33		1	10	pA
Scale Factor Tempco	$V_{IN} = 199\text{mV}$ $0^\circ\text{C} < T_A < +70^\circ\text{C}$ External $V_{REF} = 0\text{ppm}/^\circ\text{C}$		2	7	ppm/ $^\circ\text{C}$
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	$\Delta\text{Common} = +0.1V$		0.6		mA
COMMON Source Current	$\Delta\text{Common} = -0.1V$		10		μA
DGND Voltage	V^+ to Pin 36 V^+ to $V^- = 9V$	4.5	5.3	5.8	V
DGND Sink Current	$\Delta\text{DGND} = +0.5V$		1.2		mA
Supply Voltage Range	V^+ to V^- (Note 1)	6	9	12	V

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

V^- to $V^+ = 9V$, $V_{REF} = 1.00V$. $T_A = +25^\circ C$, $f_{CLK} = 120kHz$, unless otherwise noted. (Continued)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Supply Current Excluding COMMON Current	V^+ to $V^- = 9V$		1.0	1.5	mA
Clock Frequency	(Note 1)		120	360	kHz
V_{DISP} Resistance	V_{DISP} to V^+		50		k Ω
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	400	mV
Pull-Down Current	Pins 37, 38, 39		2	10	μA
"Weak Output" Current Sink/Source	Pin 20, 21 Sink/Source		3/3		μA
	Pin 27 Sink/Source		3/9		
Pin 22 Source Current			40		μA
Pin 22 Sink Current			3		

2

NOTES: 1. Device functionality is guaranteed at the stated Min/Max limits. However, accuracy can degrade under these conditions.

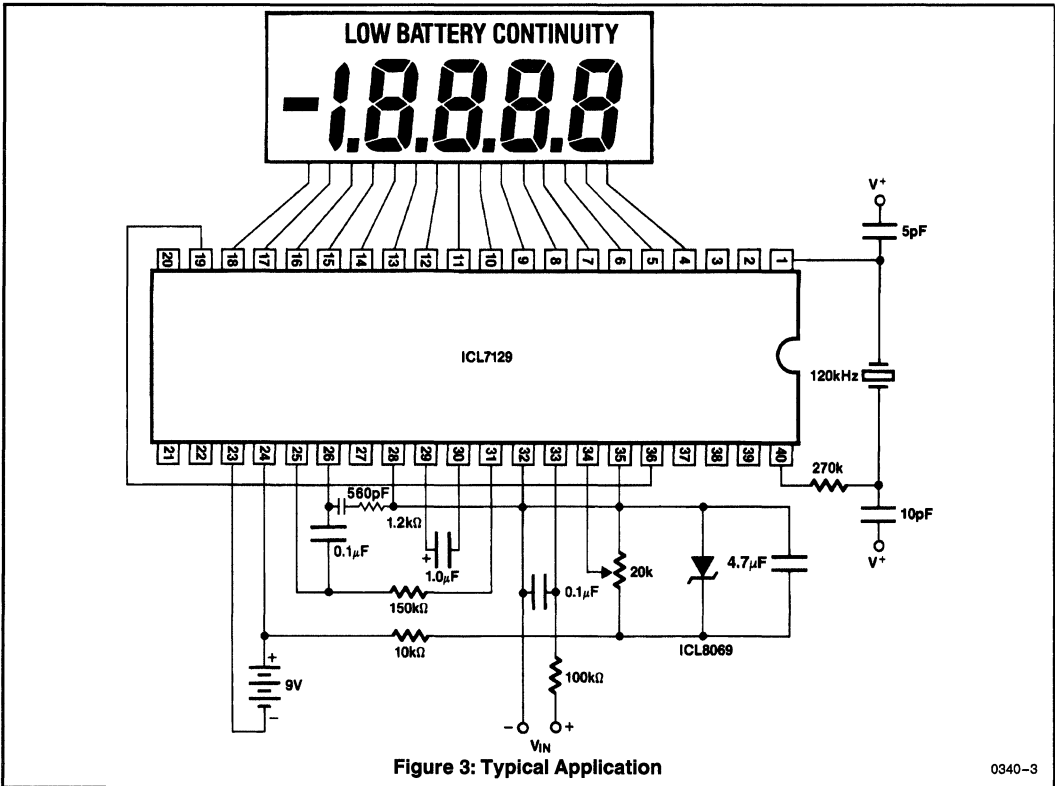


Figure 3: Typical Application

0340-3

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Table 1. Pin Descriptions

Pin	Name	Function
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B ₁ , C ₁ , CONT	Output to display segments.
5	A ₁ , G ₁ , D ₁	Output to display segments.
6	F ₁ , E ₁ , DP ₁	Output to display segments.
7	B ₂ , C ₂ , LO BATT	Output to display segments.
8	A ₂ , G ₂ , D ₂	Output to display segments.
9	F ₂ , E ₂ , DP ₂	Output to display segments.
10	B ₃ , C ₃ , MINUS	Output to display segments.
11	A ₃ , G ₃ , D ₃	Output to display segments.
12	F ₃ , E ₃ , DP ₃	Output to display segments.
13	B ₄ , C ₄ , BC ₅	Output to display segments.
14	A ₄ , D ₄ , G ₄	Output to display segments.
15	F ₄ , E ₄ , DP ₄	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V _{DISP}	Negative rail for display drivers.
20	DP ₄ /OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP ₃ /UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	LATCH/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.

Pin	Name	Function
23	V ⁻	Negative power supply terminal.
24	V ⁺	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V ⁺ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	C _{REF} ⁺	Positive side of external reference capacitor.
30	C _{REF} ⁻	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference point voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP ₂	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP ₁	Internal 3μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Intersil's ICL7129 is a uniquely designed single-chip A/D converter. It features a new "successive integration" technique to achieve 10 μ V resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are cancelled using digital techniques instead. Savings in external parts cost are realized as well as improved noise performance and elimination of a source of electromagnetic and electrostatic pick-up.

The overall functional diagram of the ICL7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps

track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 4 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 5 illustrates a typical waveform on the integrator output. INT, INT₁, and INT₂ all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

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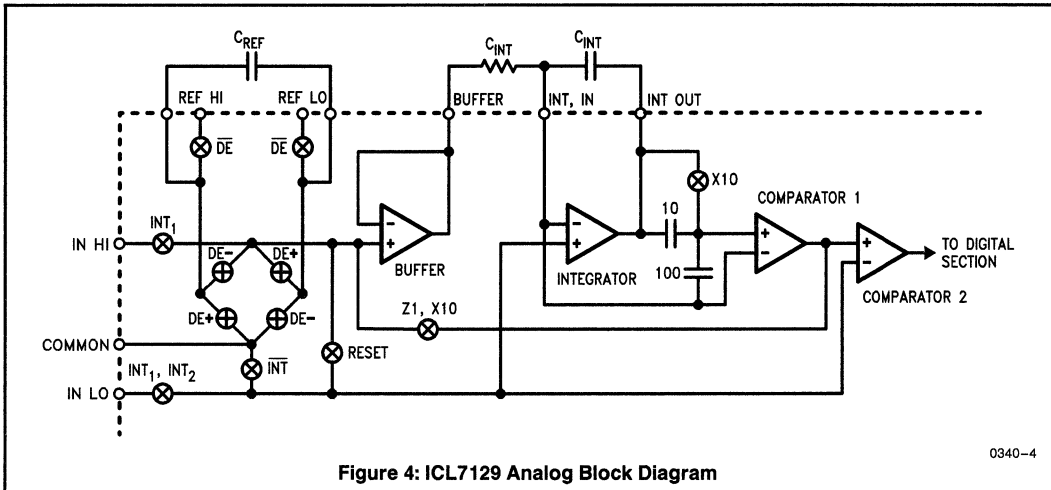
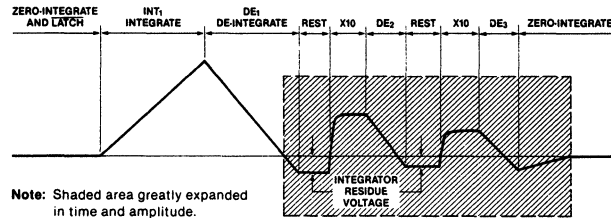


Figure 4: ICL7129 Analog Block Diagram

0340-4

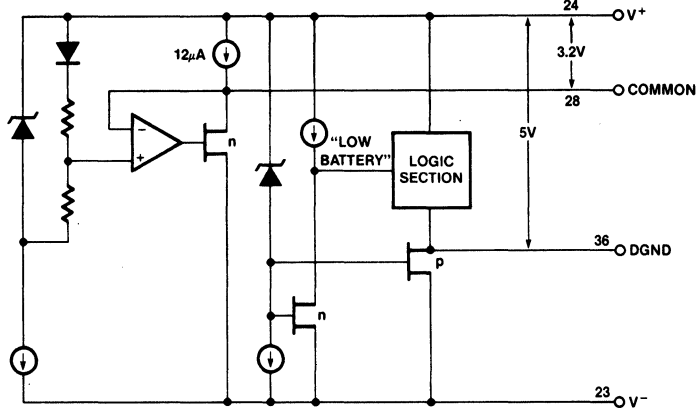
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NOTE: All typical values have been characterized but are not tested.



0340-5

Figure 5: Integrator Waveform for Negative Input Voltage Showing Successive Integration Phases and Residue Voltage



0340-6

Figure 6: Biasing Structure for COMMON and DGND

DE₁, DE₂, and DE₃ are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE₂ begins. Similarly DE₂'s overshoot is amplified by 10 and DE₃ begins. At the end of DE₃ the results counter holds a number with 5½ digits of resolution. This was obtained by feeding counts into the results counter at the 3½ digit level during DE₁, into the 4½ digit level during DE₂ and the 5½ digit level for DE₃. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT₂ switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.02% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, AND "LOW BATTERY"

The COMMON and DGND (Digital Ground) outputs of the ICL7129 are generated from internal zener diodes (Figure 6). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V⁺ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 7 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 8 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12µA while DGND has no source capability.

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NOTE: All typical values have been characterized but are not tested.

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V^+ and V^- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V^- rail in Figure 6. As the supply voltage decreases, the n-channel transistor connected to the V^- rail eventually turns off and the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

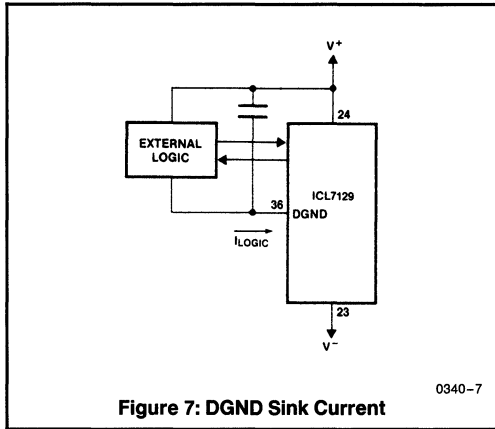


Figure 7: DGND Sink Current

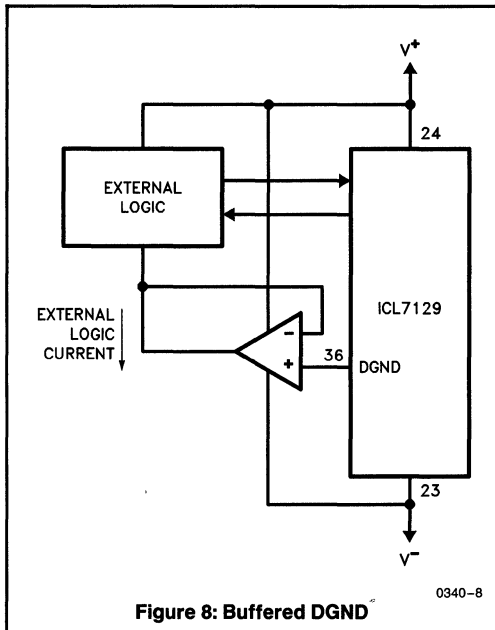


Figure 8: Buffered DGND

I/O PORTS

Four pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described in the Pin Description table (Table 1). If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V^+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 9. Since there is approximately 500k Ω in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3 μ A, nominally, and the input switching threshold is typically DGND + 2V.

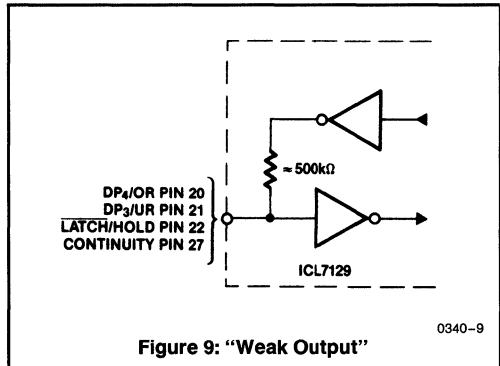


Figure 9: "Weak Output"

LATCH/HOLD, OVERRANGE, AND UNDERANGE TIMING

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) an UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Description table.

INSTANT CONTINUITY

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 10). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability.

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NOTE: All typical values have been characterized but are not tested.

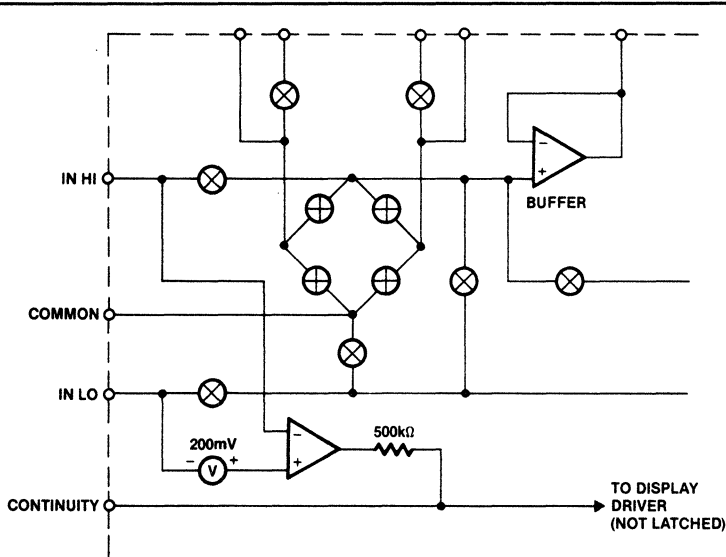


Figure 10: "Instant Continuity" Comparator and Output Structure

0340-10

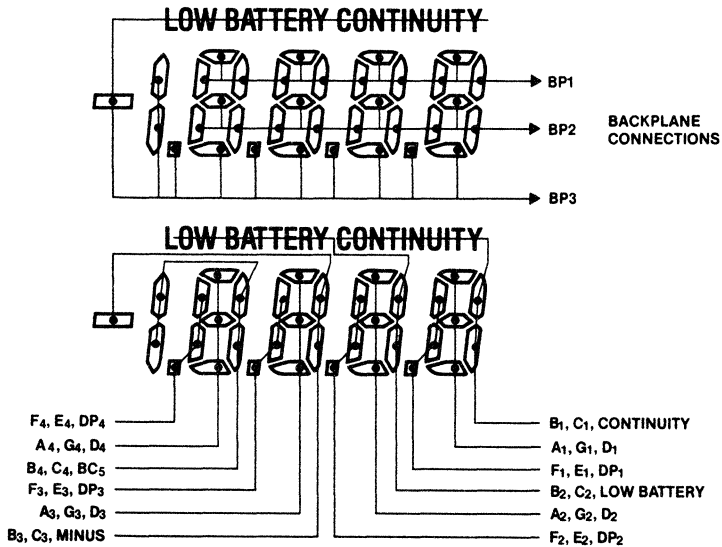


Figure 11: Triplexed Liquid Crystal Display Layout for ICL7129

0340-11

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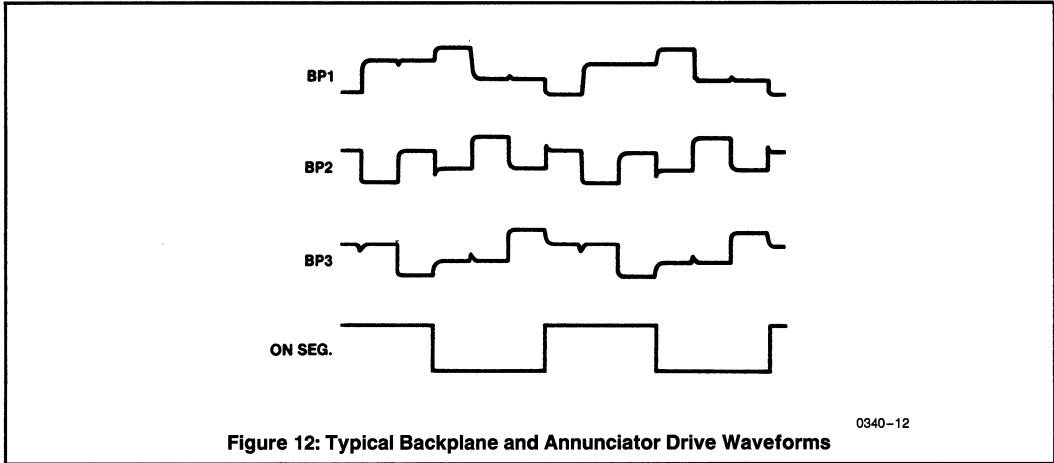


Figure 12: Typical Backplane and Annunciator Drive Waveforms

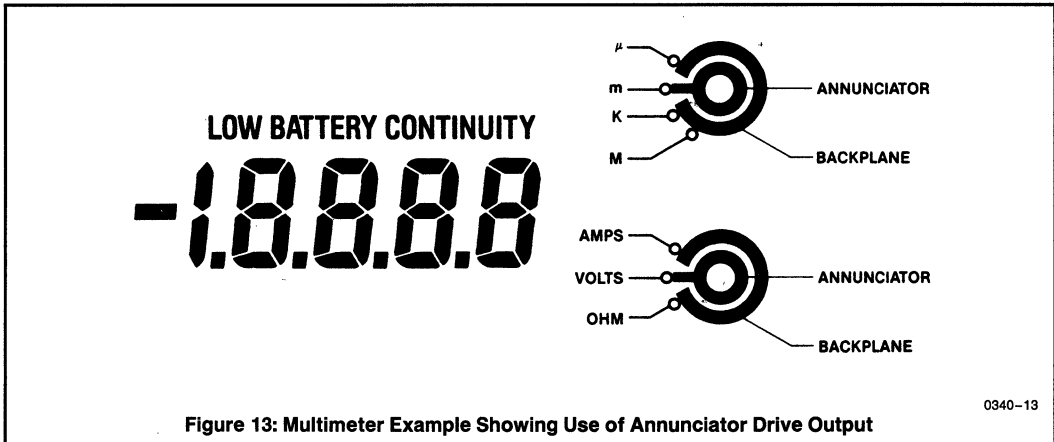


Figure 13: Multimeter Example Showing Use of Annunciator Drive Output

Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

DISPLAY CONFIGURATION

The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 11. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of

the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

ANNUNCIATOR DRIVE

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DjSP} to V^+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 12 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 13.

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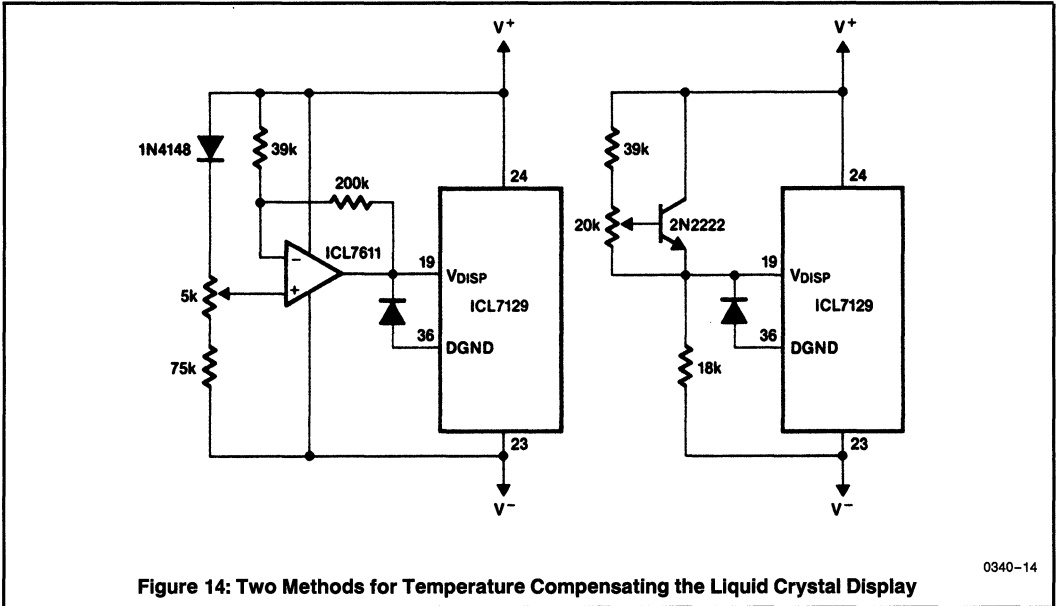


Figure 14: Two Methods for Temperature Compensating the Liquid Crystal Display

0340-14

DISPLAY TEMPERATURE COMPENSATION

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 14 shows two circuits that can be adjusted to give a temperature compensation of $\approx +10\text{mV}/^\circ\text{C}$ between V^+ and V_{DISP} . The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected into the chip if V_{DISP} is more negative than DGND.

COMPONENT SELECTION

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is no auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected to be high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of $150\text{k}\Omega$ should be optimum for most applications. The integrator capacitor is selected to give an

optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail ($\approx 0.7\text{V}$). This gives an optimum swing of $\approx 2.5\text{V}$ at full-scale. For a $150\text{k}\Omega$ integrating resistor and 2 conversions per second the value is $0.10\mu\text{F}$. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a $1.0\mu\text{F}$ value is recommended.

CLOCK OSCILLATOR

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

In low resolution applications, where the converter uses only $3\frac{1}{2}$ digits and $100\mu\text{V}$ resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from $f_{OSC} = 0.45/RC$. However, when the converter is used to its full potential ($4\frac{1}{2}$ digits and $10\mu\text{V}$ resolution) a crystal oscillator is recom-

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NOTE: All typical values have been characterized but are not tested.

mended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 15.

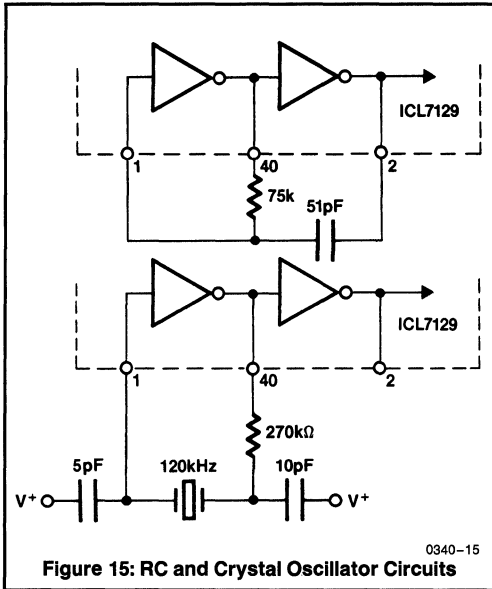


Figure 15: RC and Crystal Oscillator Circuits

POWERING THE ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 16, 17, and 18 show various powering modes that may be used with the ICL7129.

The standard supply connection using a 9V battery is shown in Figure 3.

The power connection for systems with +5V and -5V supplies available is shown in Figure 16. Notice that measurements are with respect to ground. COMMON is also tied to INLO to remove any common-mode voltage swing on the integrator amplifier inputs.

It is important to notice that in Figure 16, digital ground of the ICL7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 7 and 8. In Figure 7, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 8. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

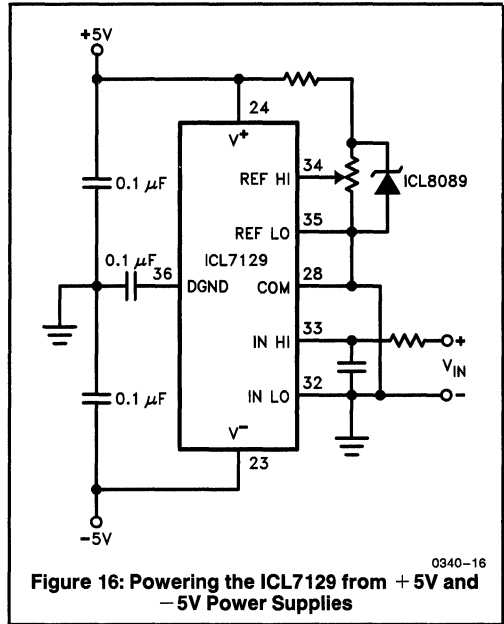


Figure 16: Powering the ICL7129 from +5V and -5V Power Supplies

When a battery voltage between 3.8V and 7V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 17.

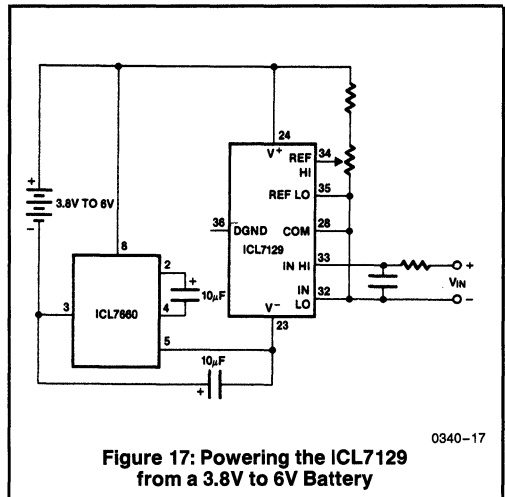


Figure 17: Powering the ICL7129 from a 3.8V to 6V Battery

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Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 18 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

VOLTAGE REFERENCES

The COMMON output of the ICL7129 has a temperature coefficient of $\pm 80\text{ppm}/^\circ\text{C}$ typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram in Figures 3 and 18 show the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129, and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.

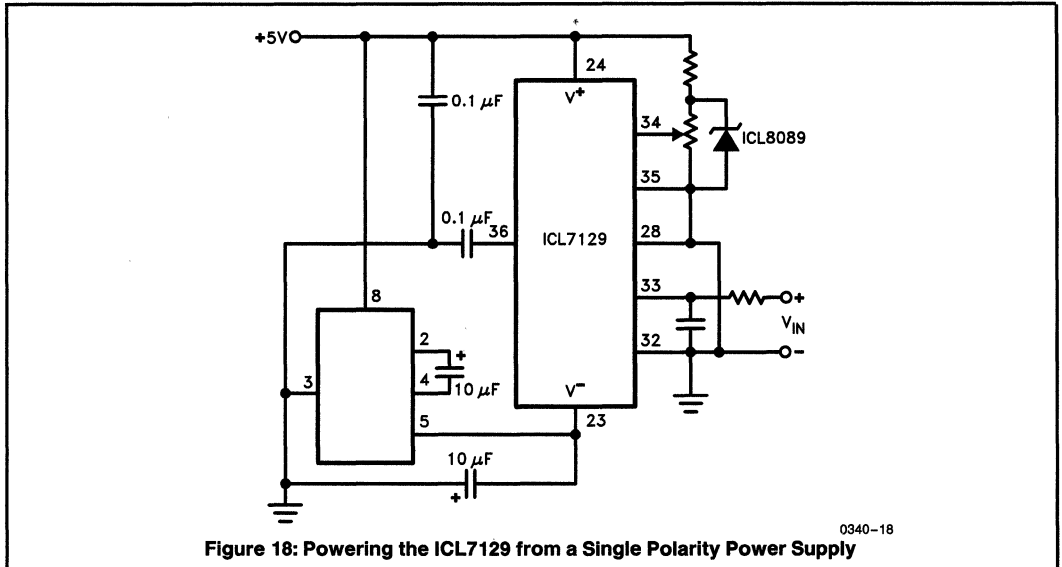


Figure 18: Powering the ICL7129 from a Single Polarity Power Supply

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NOTE: All typical values have been characterized but are not tested.

ICL7136

3½-Digit LCD Low Power A/D Converter



ICL7136

GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100µA, ideally suited for 9V battery operation.

The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

FEATURES

- First-Reading Recovery From Overrange Gives Immediate "OHMS" Measurement
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LCD Display Drive — No External Components Required
- Pin Compatible With The ICL7106, ICL7126
- Low Noise — 15µVp-p Without Hysteresis or Overrange Hangover
- On-Chip Clock and Reference
- Low Power Dissipation, Guaranteed Less Than 1mW — Gives 8,000 Hours Typical 9V Battery Life
- No Additional Active Circuits Required
- Evaluation Kit Available (ICL7136EV/Kit)

2

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7136CM44	0°C to +70°C	44-Pin Surface Mount
ICL7136CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7136RCPL	0°C to +70°C	40-Pin Plastic DIP
ICL7136EV/KIT		EVALUATION KIT

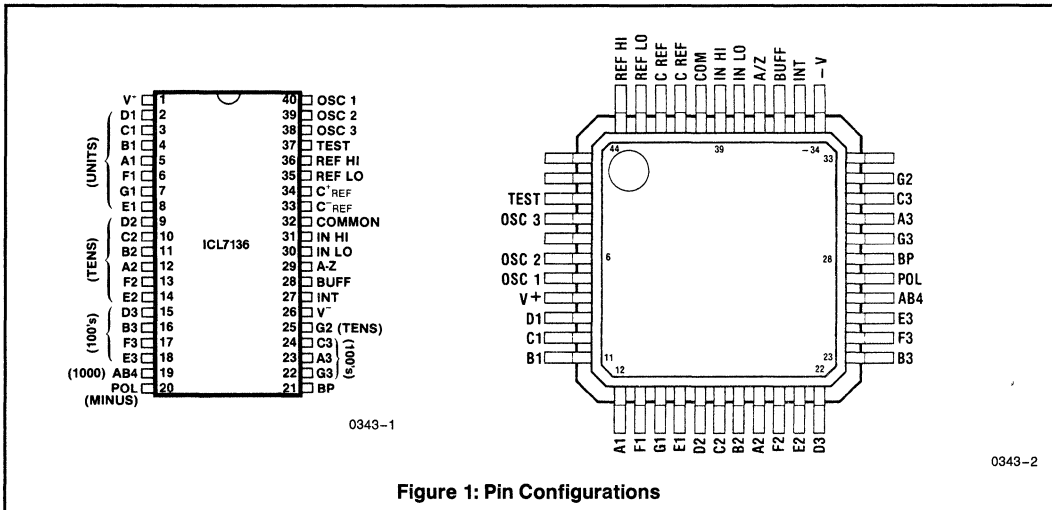


Figure 1: Pin Configurations

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
 Analog Input Voltage (either input)(Note 1) V^+ to V^-
 Reference Input Voltage (either input) V^+ to V^-
 Clock Input TEST to V^+

Power Dissipation (Note 2)
 Ceramic Package 1000mW
 Plastic Package 800mW
 Operating Temperature 0°C to $+70^\circ\text{C}$
 Storage Temperature -65°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to $\pm 100\mu\text{A}$.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

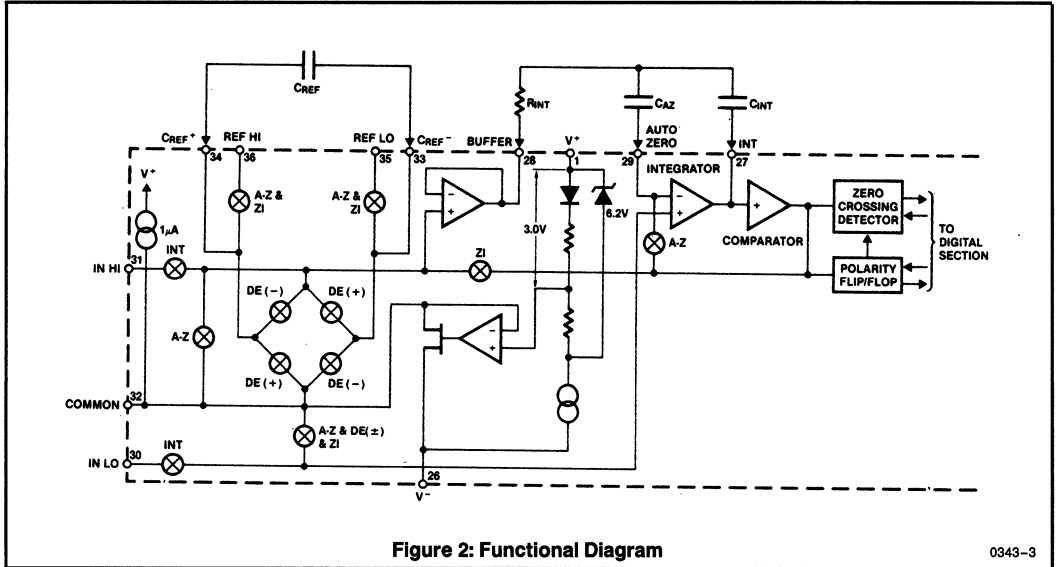


Figure 2: Functional Diagram

0343-3

ELECTRICAL CHARACTERISTICS (Notes 3, 7)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	$V_{IN} = 0.0V$ Full-Scale = 200.0mV	-000.0	± 000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, $V_{REF} = 100mV$	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \cong 200.0mV$	-1	± 0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	-1	± 0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1V$, $V_{IN} = 0V$ Full-Scale = 200.0mV		50		$\mu V/V$
Noise (Pk-Pk value not exceeded 95% of time)	$V_{IN} = 0V$, Full Scale = 200.0mV		15		μV
Leakage Current @ Input	$V_{IN} = 0V$		1	10	pA

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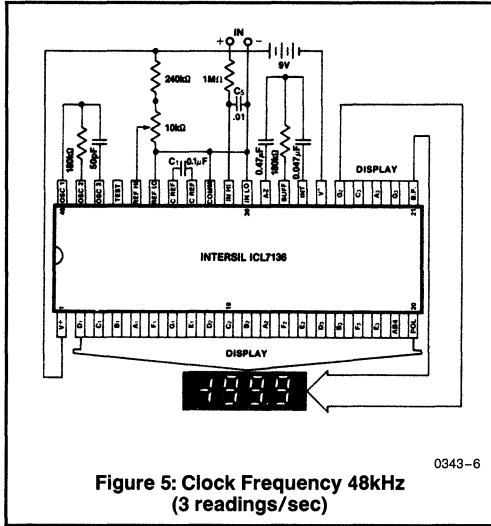


Figure 5: Clock Frequency 48kHz
(3 readings/sec)

DETAILED DESCRIPTION (Analog Section)

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ} , to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10\mu\text{V}$.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the

capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is $1000 (V_{IN}/V_{REF})$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($>7\text{V}$), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\approx 35\Omega$), and a temperature coefficient typically less than $150\text{ppm}/^\circ\text{C}$.

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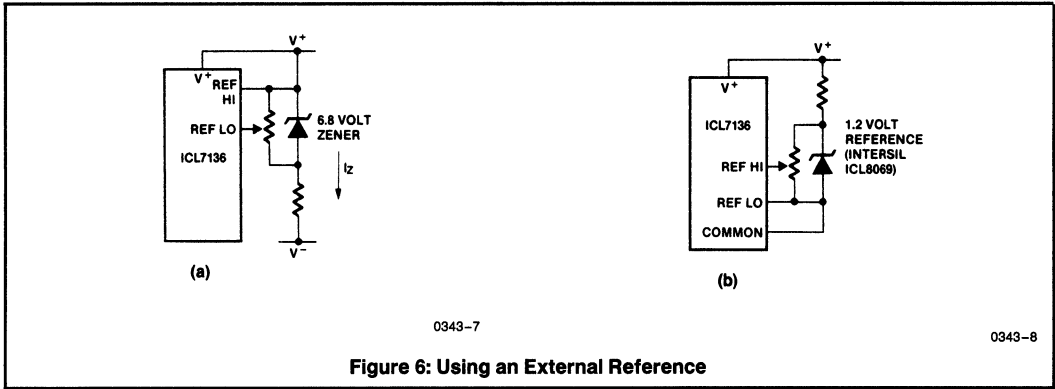


Figure 6: Using an External Reference

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 3mA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1µA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

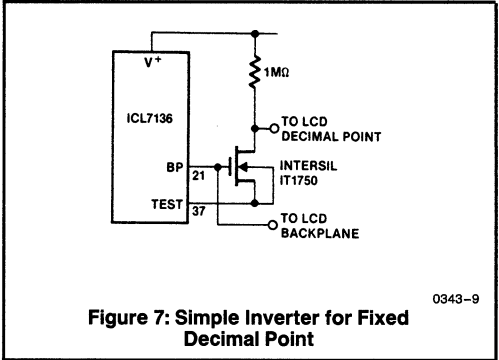


Figure 7: Simple Inverter for Fixed Decimal Point

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

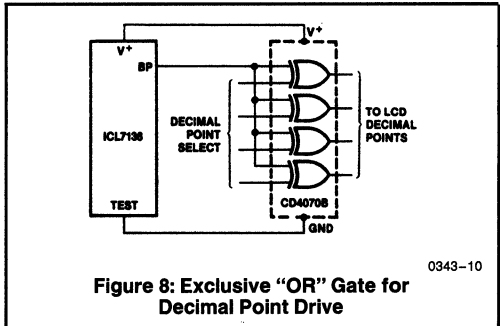


Figure 8: Exclusive "OR" Gate for Decimal Point Drive

DETAILED DESCRIPTION (Digital Section)

Figure 9 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and

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NOTE: All typical values have been characterized but are not tested.

DISPLAY FONT

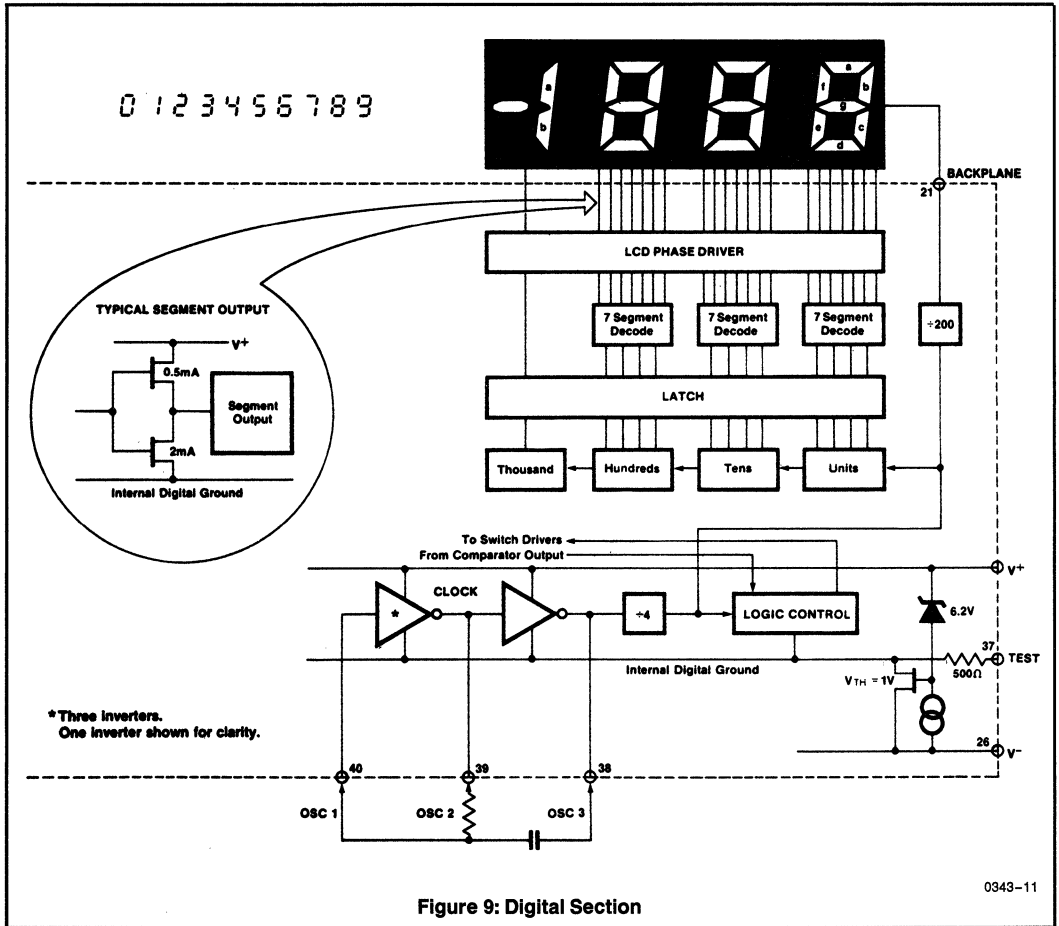


Figure 9: Digital Section

0343-11

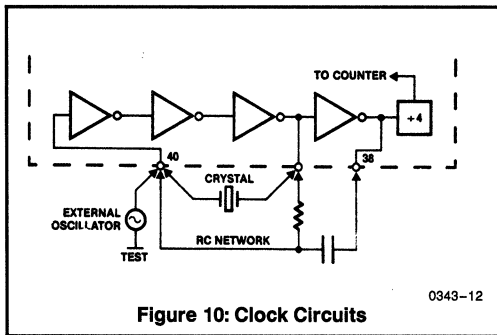


Figure 10: Clock Circuits

0343-12

amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Figure 10 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the

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four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33 $\frac{1}{3}$ kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66 $\frac{2}{3}$ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

COMPONENT VALUE SELECTION

(See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μ A of quiescent current. They can supply $\sim 1\mu$ A of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8M Ω is near optimum, and similarly 180k Ω for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal $\pm 2V$ full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047 μ F, for 1 reading/second (16kHz) 0.15 μ F. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47 μ F capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

Reference Capacitor

A 0.1 μ F capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0 μ F will hold the roll-over error to 0.5 count in this instance.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

Oscillator Components

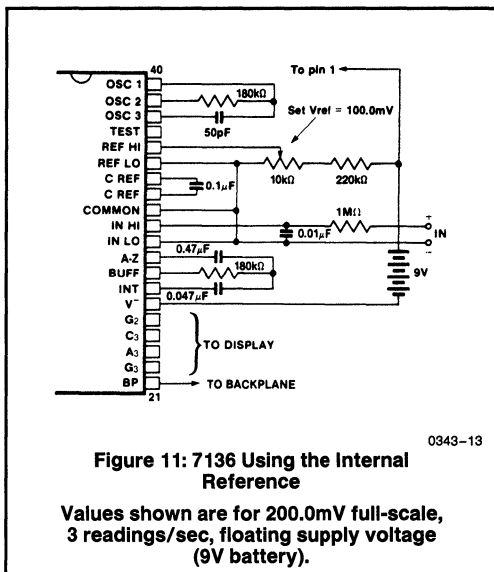
For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim 0.45/RC$. For 48kHz clock (3 readings/second), $R = 180k\Omega$, for 16kHz, $R = 560k\Omega$.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330k Ω . This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

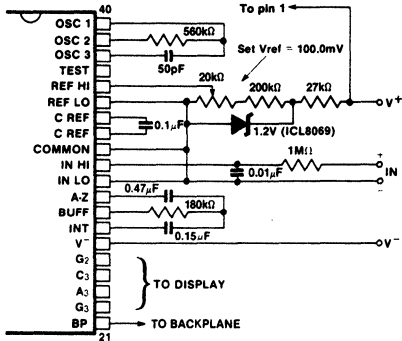
TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.



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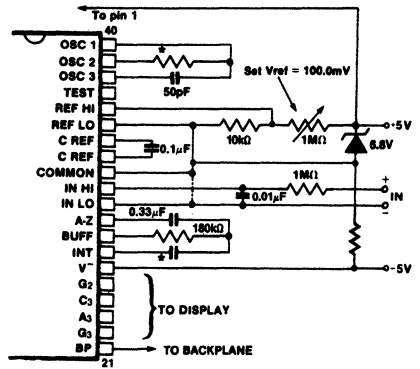
NOTE: All typical values have been characterized but are not tested.



0343-14

Figure 12: 7136 with an External Band-Gap Reference (1.2V Type)

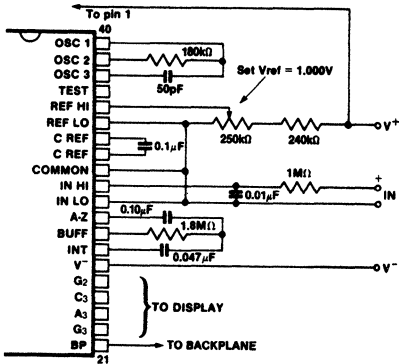
IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.



0343-16

Figure 14: 7136 with Zener Diode Reference

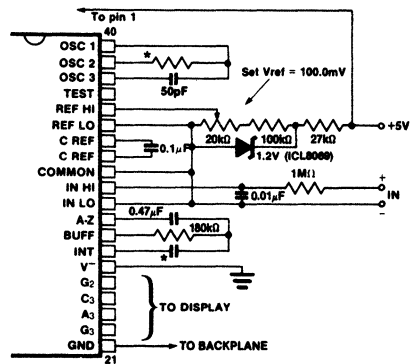
Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



0343-15

Figure 13: Recommended Component Values for 2,000V Full-Scale, 3 Readings/Sec

For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 12.



0343-17

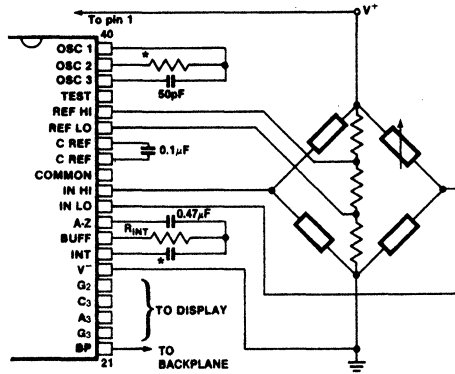
Figure 15: 7136 Operated from Single +5V Supply

An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.

*Values depend on clock frequency. See Figures 11, 12, 13.

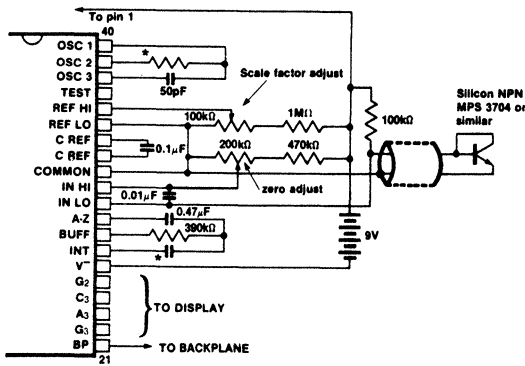
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0343-18

Figure 16: 7136 Measuring Ratiometric Values of Quad Load Cell
 The resistor values within the bridge are determined by the desired sensitivity.



0343-19

Figure 17: 7136 used as a Digital Centigrade Thermometer

A silicon diode-connected transistor has a temperature coefficient of about $-2\text{mV}/^\circ\text{C}$. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL807 $\frac{3}{4}$ and AD590 data sheets for alternative circuits.

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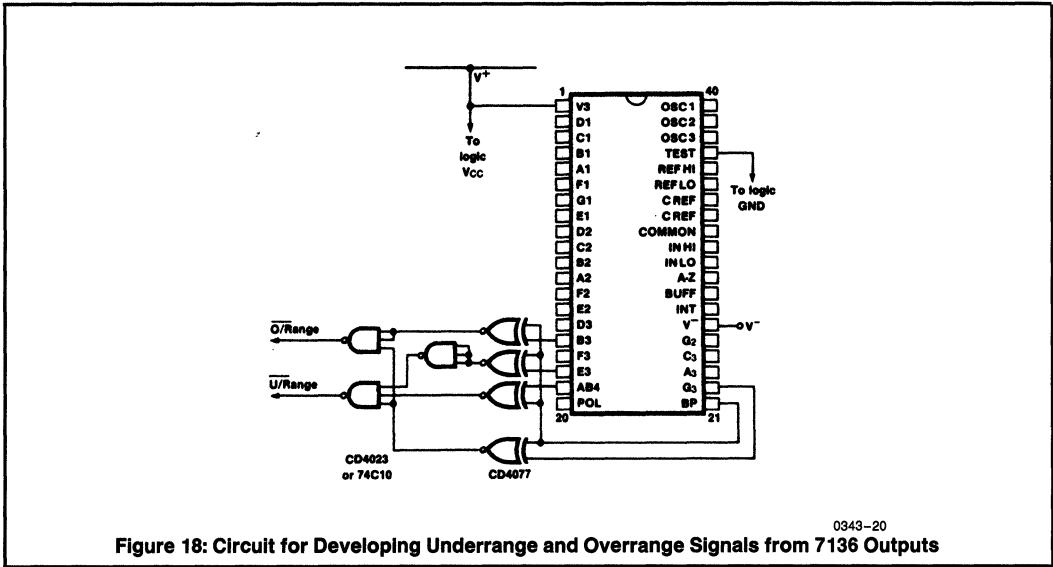


Figure 18: Circuit for Developing Underrange and Overrange Signals from 7136 Outputs

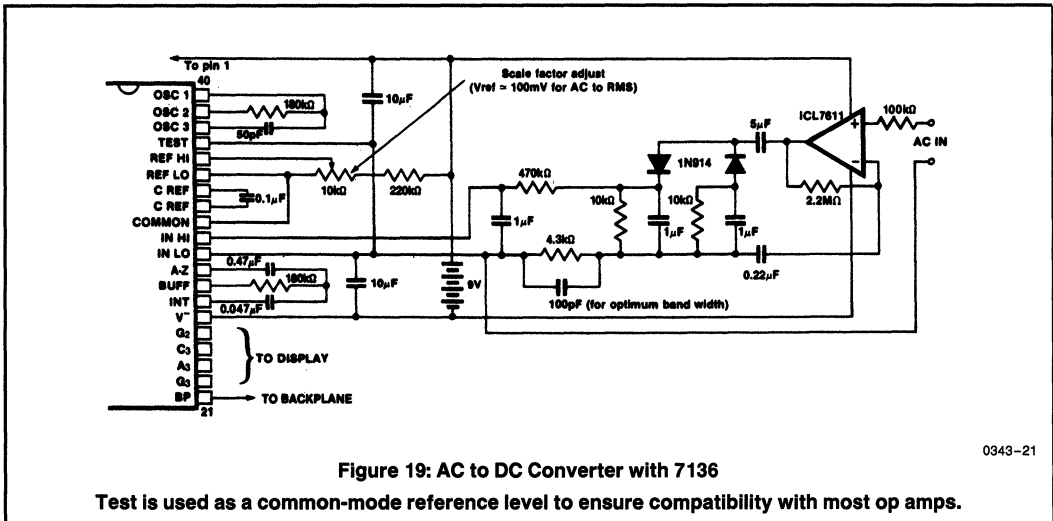


Figure 19: AC to DC Converter with 7136

Test is used as a common-mode reference level to ensure compatibility with most op amps.

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APPLICATION NOTES

- A016** "Selecting A/D Converters," by David Fullagar.
- A017** "The Integrating A/D Converter," by Lee Evans.
- A018** "Do's and Don't's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A023** "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032** "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046** "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047** "Games People Play with Intersil's A/D Converters," edited by Peter Bradshaw.
- A052** "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

7136 EVALUATION KIT

After purchasing a sample of the 7136, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7136EV/Kit and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

ICL7137

3 1/2-Digit LED Low Power Single-Chip A/D Converter



GENERAL DESCRIPTION

The Intersil ICL7137 is a high performance, very low power 3 1/2-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200µA, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. The device features auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

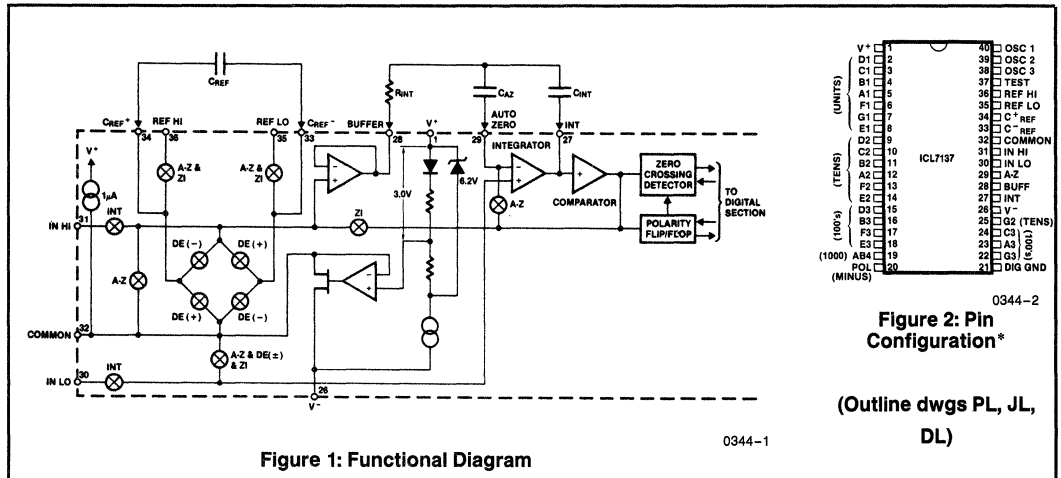
The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

FEATURES

- First-Reading Recovery From Overrange allows Immediate "OHMS" Measurement
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference
- Direct LED Display Drive — No External Components Required
- Pin Compatible With The ICL7107
- Low Noise — 15µVp-p Without Hysteresis or Overrange Hangover
- On-Chip Clock and Reference
- Improved Rejection of Voltage On COMMON Pin
- No Additional Active Circuits Required
- Evaluation Kit Available ICL7137EV/KIT

ORDERING INFORMATION*

Part Number	Temperature Range	Package
ICL7137CPL	0°C to +70°C	40-Pin Plastic
ICL7137RCPL	0°C to +70°C	40-Pin Plastic
ICL7137EV/KIT		EVALUATION KIT



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V ⁺	+6V
V ⁻	-9V
Analog Input Voltage (either input)(Note 1)	V ⁺ to V ⁻
Reference Input Voltage (either input)	V ⁺ to V ⁻
Clock Input	GND to V ⁺

Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to $\pm 100\mu\text{A}$.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V _{IN} = 0.0V Full-Scale = 200.0mV	-000.0	± 000.0	+000.0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} , V _{REF} = 100mV	998	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	-V _{IN} = +V _{IN} \approx 200.0mV	-1	± 0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	-1	± 0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V _{CM} = $\pm 1\text{V}$, V _{IN} = 0V Full-Scale = 200.0mV		30		$\mu\text{V}/\text{V}$
Noise (Pk-Pk value not exceeded 95% of time)	V _{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V _{IN} = 0V		1	10	pA
Zero Reading Drift	V _{IN} = 0V, 0°C < T _A < +70°C		0.2	1	$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	V _{IN} = 199.0mV, 0°C < T _A < +70°C (Ext. Ref. Oppm/°C)		1	5	ppm/°C
V ⁺ Supply Current (Does not include LED current)	V _{IN} = 0V (Note 5)		70	200	μA
V ⁻ Supply current			40		
Analog COMMON Voltage (With respect to positive supply)	250k Ω between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250k Ω between Common and Positive Supply		150		ppm/°C
Segment Sinking Current (Except Pins 19 & 20) (Pin 19 only) (Pin 20 only)	V ⁺ = 5.0V Segment Voltage = 3V	5 10 4	8.0 16 7		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.

4. Refer to "Differential Input" discussion.

5. 48kHz oscillator, Figure 5, increases current by 35 μA (typ).

6. Extra capacitance of CERDIP package changes oscillator resistor value to 470k Ω or 150k Ω (1 reading/sec or 3 readings/sec).

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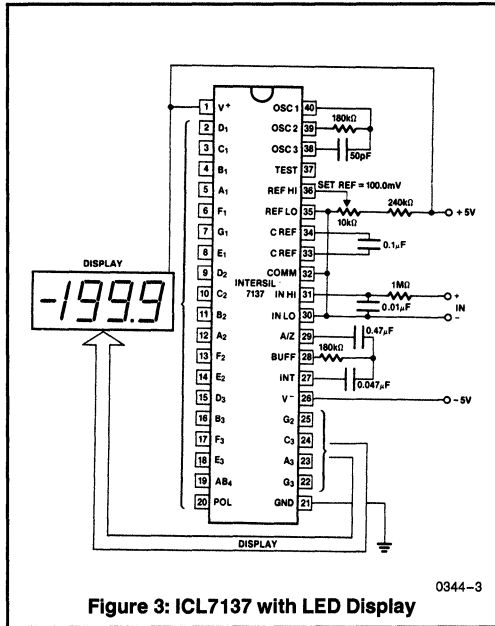


Figure 3: ICL7137 with LED Display 0344-3

TEST CIRCUITS

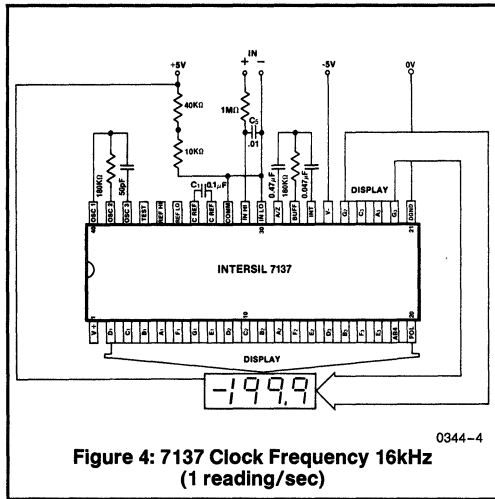


Figure 4: 7137 Clock Frequency 16kHz (1 reading/sec) 0344-4

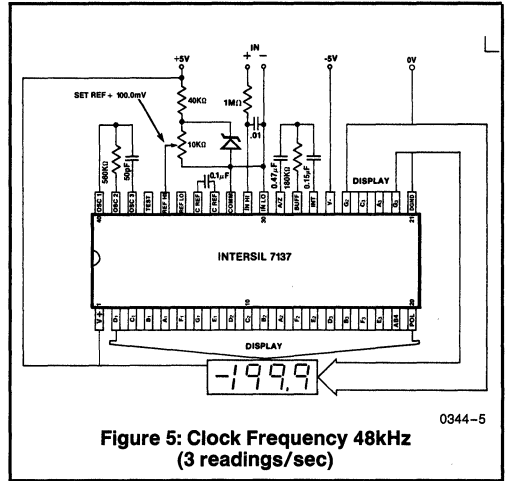


Figure 5: Clock Frequency 48kHz (3 readings/sec) 0344-5

DETAILED DESCRIPTION (Analog Section)

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero-integrator (Z).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ} , to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10\mu V$.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

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NOTE: All typical values have been characterized but are not tested.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically; the digital reading displayed is $1000(V_{IN}/V_{REF})$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V.

However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($>7V$), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\approx 35\Omega$), and a temperature coefficient typically less than 150ppm/ $^{\circ}C$.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of $2^{\circ}C$ to $8^{\circ}C$, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate ($<7V$). These problems are eliminated if an external reference is used, as shown in Figure 6.

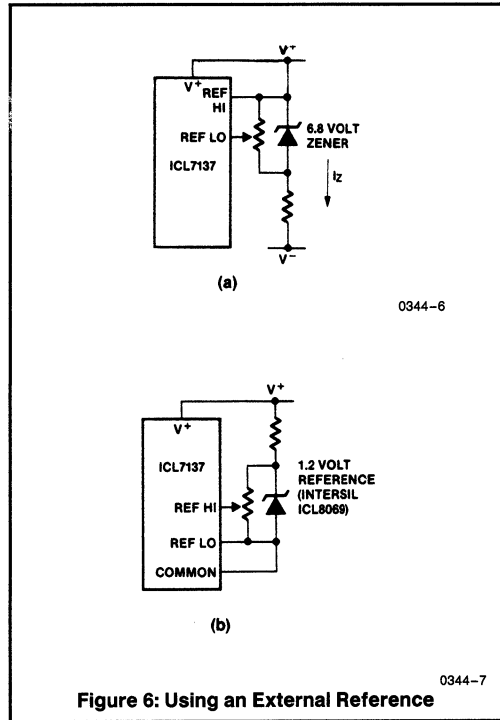


Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

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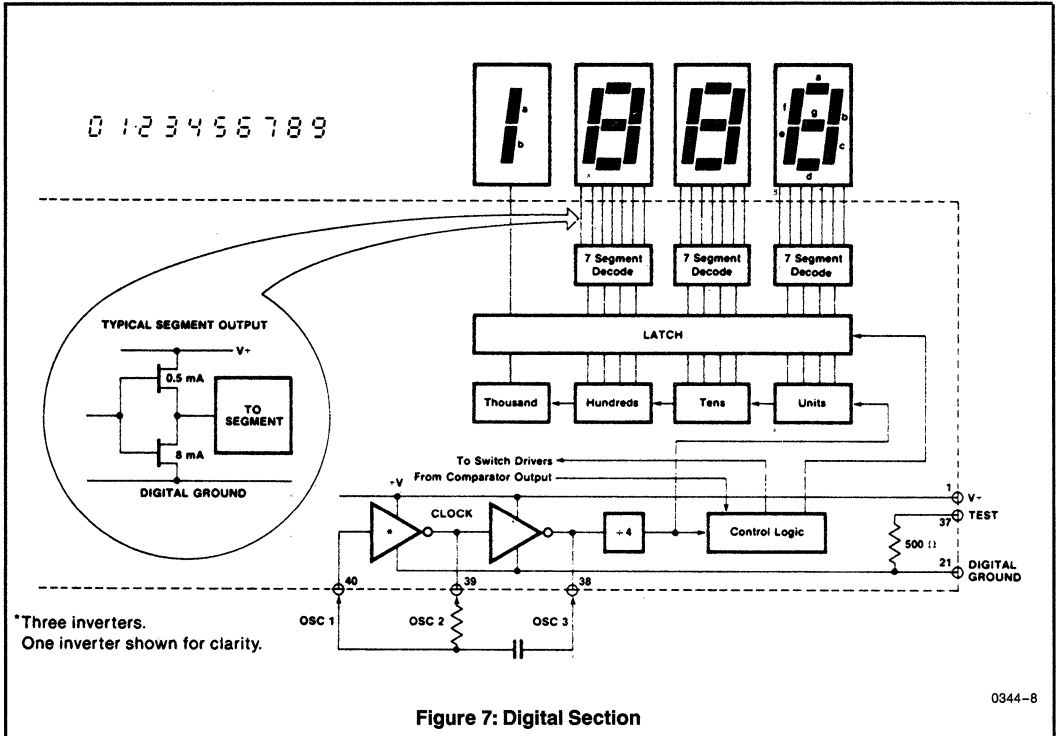
NOTE: All typical values have been characterized but are not tested.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100 μ A or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1 μ A of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

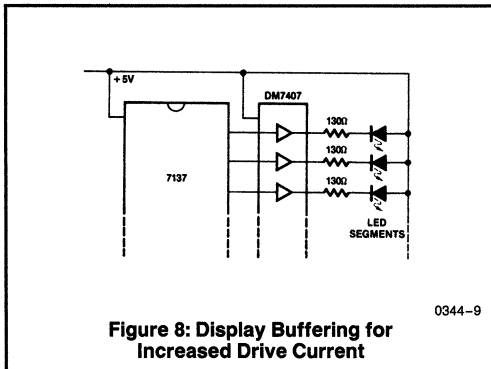
TEST

The TEST pin is coupled to the internal digital supply through a 500 Ω resistor, and functions as a "lamp test." When TEST is pulled high (to V⁺) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

DISPLAY FONT



0344-8



0344-9

DETAILED DESCRIPTION (Digital Section)

Figure 7 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 8 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

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NOTE: All typical values have been characterized but are not tested.

System Timing

Figure 9 shows the clock oscillator provided in the 7137. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

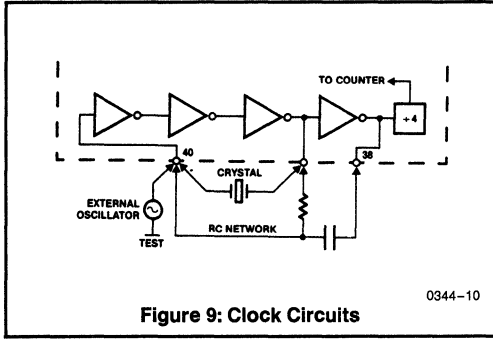


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33¹/₃kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66²/₃kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz.) See also A052.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

COMPONENT VALUE SELECTION

(See Application Note A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μ A of quiescent current. They can supply ~ 1 μ A of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8M Ω is near optimum, and similarly 180k Ω for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either

supply). When the analog COMMON is used as a reference, a nominal $\pm 2V$ full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047 μ F, for 1 reading/second (16kHz) 0.15 μ F. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47 μ F capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (See Application Note A032).

Reference Capacitor

A 0.1 μ F capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0 μ F will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), $R = 180k\Omega$, while for 16kHz (1 reading/sec), $R = 560k\Omega$.

Reference Voltage

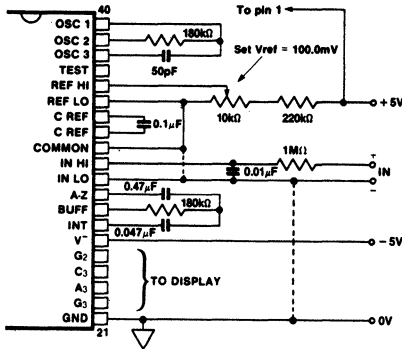
The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2,000V scale, V_{REF} should equal 100.0mV and 1,000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330k Ω . This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

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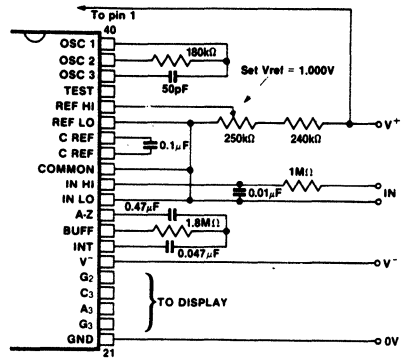
NOTE: All typical values have been characterized but are not tested.



0344-11

Figure 10: 7137 Using the Internal Reference.

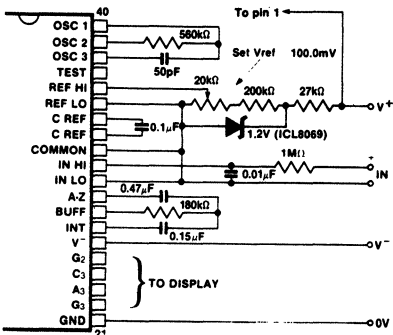
Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)



0344-13

Figure 12: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec.

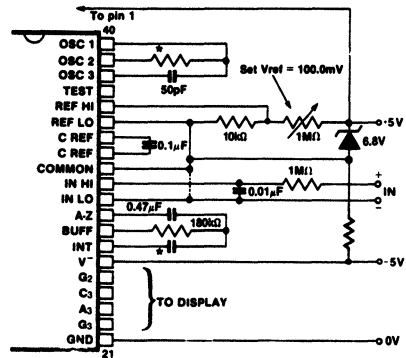
For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 11.



0344-12

Figure 11: 7137 with an External Band-Gap Reference (1.2V Type).

IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.



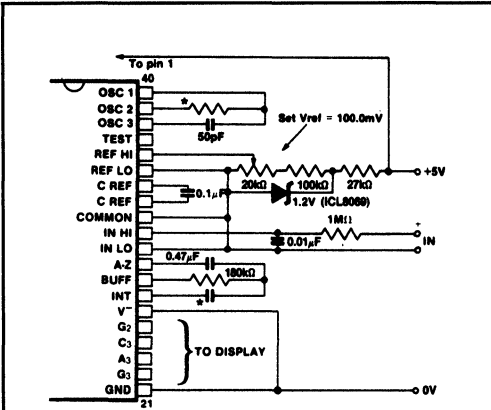
0344-14

Figure 13: 7137 with Zener Diode Reference.

Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

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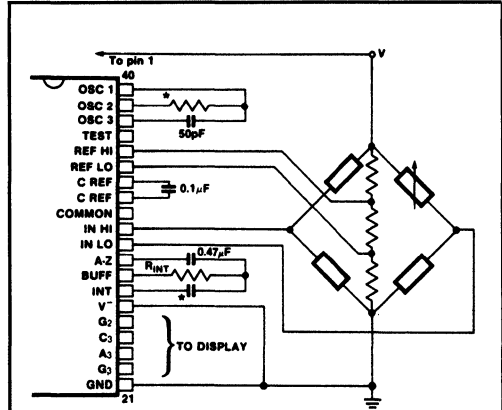
NOTE: All typical values have been characterized but are not tested.



0344-15

Figure 14: 7137 Operated from Single +5V Supply.

An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.

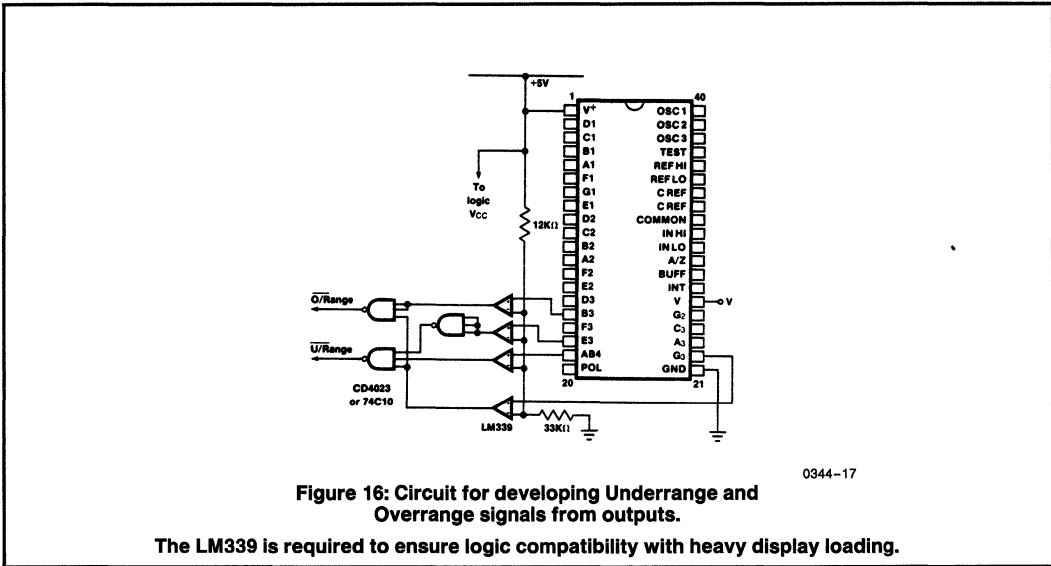


0344-16

Figure 15: Measuring Ratiometric Values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.

2



0344-17

Figure 16: Circuit for developing Underrange and Overrange signals from outputs.

The LM339 is required to ensure logic compatibility with heavy display loading.

*Values depend on clock frequency. See Figures 10, 11, and 12.

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NOTE: All typical values have been characterized but are not tested.

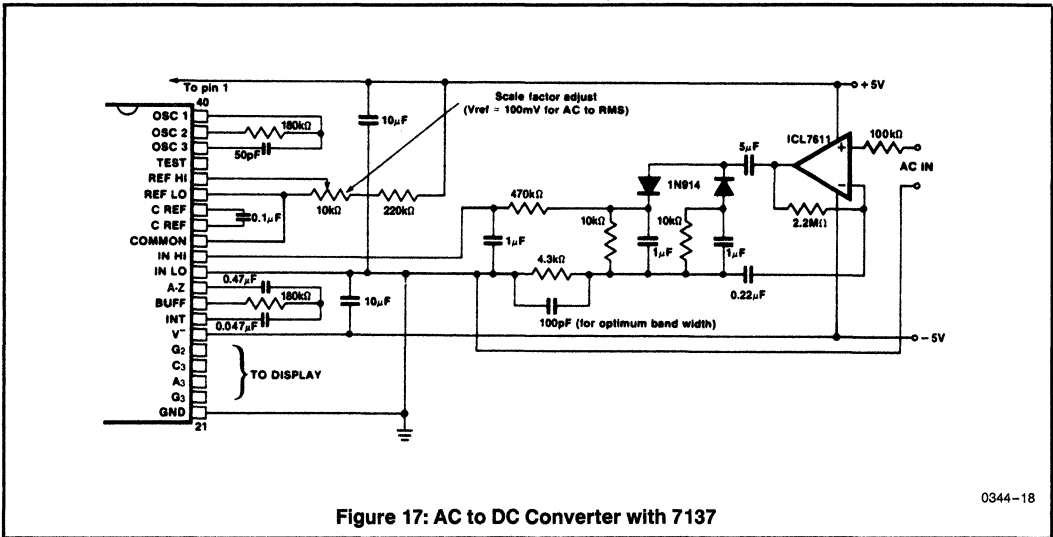


Figure 17: AC to DC Converter with 7137

0344-18

APPLICATION NOTES

- A016 "Selecting A/D converters," by David Fullagar.
- A017 "The Integrating A/D Converter," by Lee Evans.
- A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.
- A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.
- A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.
- A047 "Games People Play with Intersil's A/D Converters" edited by Peter Bradshaw.
- A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

ICL7137 EVALUATION KITS

After purchasing a sample of the 7137, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7137EV/Kit, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, LED display, passive components, and miscellaneous hardware.

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NOTE: All typical values have been characterized but are not tested.

ICL7139

3³/₄-Digit Autoranging Multimeter



ICL7139

GENERAL DESCRIPTION

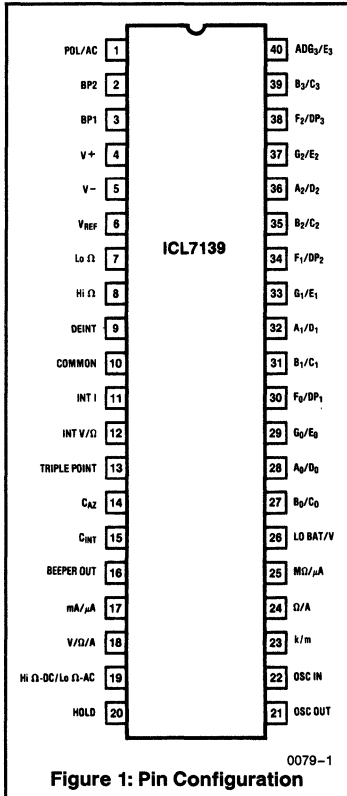
The Intersil ICL7139 is a high performance, low power, auto-ranging digital multimeter IC. Unlike other autoranging multimeter ICs, the ICL7139 always displays the result of a conversion on the correct range. There is no "range hunting" noticeable in the display. The unit will autorange between the four different ranges. A manual switch is used to select the 2 high group ranges. DC current ranges are 4 mA and 40 mA in the low current group, 400 mA and 4A in the high current group. Resistance measurements are made on 4 ranges, which are divided into two groups. The low resistance ranges are 4/40 kilohms. High resistance ranges are 0.4/4 megohms. Resolution on the lowest range is 1 ohm.

PRELIMINARY
Subject To Change Without Notice

FEATURES

- **13 Ranges:**
 - 4 DC Voltage—400 mV, 4V, 40V, 400V
 - 1 AC Voltage—400V
 - 4 DC Current—4 mA, 40 mA, 400 mA, 4A
 - 4 Resistance—4 K Ω , 40 K Ω , 400 K Ω , 4 M Ω
- **Autoranging—First Reading is Always on Correct Range**
- **On-Chip Duplex LCD Display Drive Including Three Decimal Points and 11 Annunciators**
- **No Additional Active Components Required**
- **Low Power Dissipation—Less than 20 mW—1000 Hour Typical Battery Life**
- **Average Responding Converter for Sinewave Inputs**
- **Display Hold Input**
- **Continuity Output Drives Piezoelectric Beeper**
- **Low Battery Annunciator with On-Chip Detection**
- **Guaranteed Zero Reading for 0 Volts Input on All Ranges**

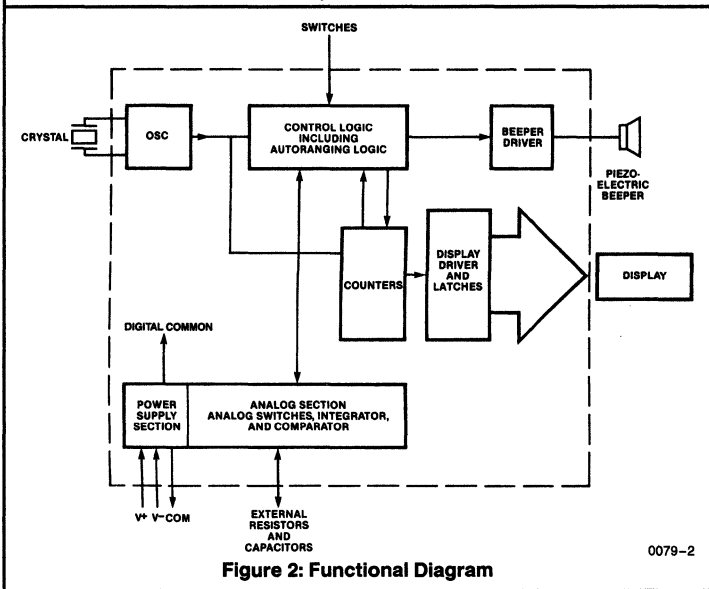
2



ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7139CPL	0°C to +70°C	40 Pin Plastic DIP
*ICL7139CM44	0°C to +70°C	44 Pin Surface Mount

*Consult Factory for Details.



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-)	15V
Reference Input Voltage (V_{REF} to COM)	3V
Analog Input Current (I_N + Current or I_N + Voltage)	100 μ A
Clock Input Swing	V^+ to V^+ - 3
Power Dissipation (Plastic Package)	800 mW
Operating Temperature Range	0°C to +70°C

Storage Temperature Range	-65°C to +130°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V^+ = +9.0V$, $T_A = +25^\circ C$, V_{REF} adjusted for -3.700 reading on DC volts, test circuit as shown in Figure 3. Crystal = 120 kHz.

Parameter	Test Conditions	Min	Typ	Max	Units
Zero Input Reading	V_{IN} or I_{IN} or $R_{IN} = 0.00$	-00.0		+00.0	V, I, Ohms
Rollover Error (Note 1)	V_{IN} or $I_{IN} = \pm$ Full Scale ¹		4		Counts
Linearity (Best Straight Line) (Note 6)		-1		+1	Counts
Accuracy DC V, 400 Volt Range Only				± 1	% of RDG + 1
Accuracy DC V, 400 Volt Range Excluded				± 0.2	% of RDG + 1
Accuracy Ohms, 4K and 400K Range				± 0.5	% of RDG + 8
Accuracy Ohms, 40K and 4 Meg Range				± 1	% of RDG + 9
Accuracy DC I, Unadjusted for FS				± 0.5	% of RDG + 1
Accuracy DC I, Adjusted for FS				± 0.2	% of RDG + 1
Accuracy AC V (Note 5)	@60 Hz		± 2		% of RDG
Open Circuit Voltage for Ohms Measurements	$R_{UNKNOWN} = \text{Infinity}$		V_{REF}		V
Noise (Note 2, 95% of Time)	$V_{IN} = 0$, DC Volts		0.1		LSB
Noise (Note 2, 95% of Time)	$V_{IN} = 0$, AC Volts		4		LSB
Supply Current	$V_{IN} = 0$, DC Voltage Range		1.5	2.4	mA
Analog Common (with Respect to V^+)	$I_{COMMON} < 10 \mu A$	2.7	2.9	3.1	V
Temperature Coefficient of Analog Common	$I_{COMMON} < 10 \mu A$, Temp = 0-70°C		-100		ppm/°C
Output Impedance of Analog Common	$I_{COMMON} < 100 \mu A$		1	10	Ohms
Backplane/Segment Drive Voltage	Average DC < 50 mV	2.8	3.0	3.2	V
Backplane/Segment Display Frequency			75		Hz
Switch Input Current (Note 3)	$V_{IN} = V^+$ to V^-	-50		+50	μA
Switch Input Levels (High Trip Point)		$V^+ - 0.5$		V^+	V
Switch Input Levels (Mid Trip Point)		$V^- + 3$		$V^+ - 2.5$	V
Switch Input Levels (Low Trip Point)		V^-		$V^- + 0.5$	V
Beeper Output Drive (Rise or Fall Time)	$C_{LOAD} = 10 \text{ nF}$		25	100	μs
Beeper Output Frequency			2		kHz
Continuity Detect	Range = Low Ohms, $V_{REF} = 1.00V$	500		2000	Counts
Power Supply Functional Operation	V^+ to V^-	7	9	11	V
Low Battery Detect (Note 4)	V^+ to V^-	6.5	7	7.5	V

NOTE 1: Rollover is defined as absolute value of negative reading minus absolute value of positive reading.

2: Noise is defined as the width of the uncertainty window (where the display will flicker) between two adjacent codes.

3: Applies to pins 17-20.

4: Analog Common falls out of regulation when the Low Battery Detect is asserted, however the ICL7139 will continue to operate correctly with a supply voltage above 7 volts and below 11 volts.

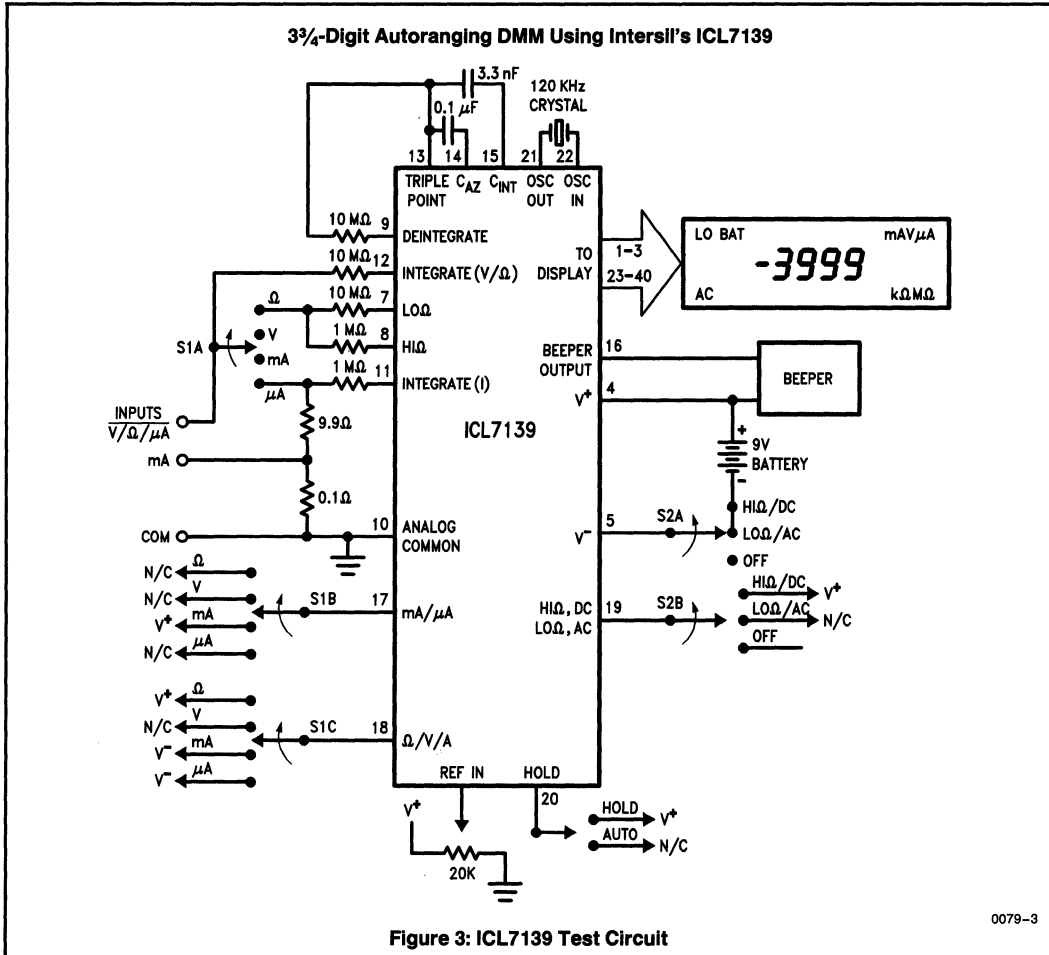
5: For 50 Hz use a 100 kHz crystal.

6: Guaranteed by design, not tested.

RDG = Reading

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NOTE: All typical values have been characterized but are not tested.



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2

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NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Numbers and Function

I/O	Pin Number	Pin Function
O	1	Segment Driver POL/AC
O	2	Backplane 2
O	3	Backplane 1
I	4	V ⁺
I	5	V ⁻
I	6	Reference Input
O	7	Lo Ohms
O	8	Hi Ohms
I/O	9	Deintegrate
I/O	10	Analog Common
I	11	Int I
I	12	Int V/Ohms
I	13	Triple Point
I	14	Auto Zero Capacitor (C _{AZ})
I	15	Integrate Capacitor (C _{INT})
O	16	Beeper Output
I	17	mA/μA
I	18	Ohms/V/A
I	19	Hi Ohms DC/Lo Ohms AC
I	20	Hold
O	21	Oscillator Out
I	22	Oscillator In
O	23	Segment DRIVER k/m
O	24	Segment Driver Ohms/A
O	25	Segment Driver M Ohms/μA
O	26	Segment Driver Lo Bat/V
O	27	Segment Driver B ₀ /C ₀
O	28	Segment Driver A ₀ /D ₀
O	29	Segment Driver G ₀ /E ₀
O	30	Segment Driver F ₀ /DP ₁
O	31	Segment Driver B ₁ /C ₁
O	32	Segment Driver A ₁ /D ₁
O	33	Segment Driver G ₁ /E ₁
O	34	Segment Driver F ₁ /DP ₁
O	35	Segment Driver B ₂ /C ₂
O	36	Segment Driver A ₂ /D ₂
O	37	Segment Driver G ₂ /E ₂
O	38	Segment Driver F ₂ /DP ₃
O	39	Segment Driver B ₃ /C ₃
O	40	Segment Driver ADG ₃ /E ₃

NOTE: For segment drivers, segments are listed as (segment for backplane 1)/(segment for backplane 2). Example: pin 27; segment B₀ is on backplane 1, segment C₀ is on backplane 2.

DETAILED DESCRIPTION

General

Figure 2 is a simplified block diagram of the ICL7139. The digital section includes all control logic, counters, and display drivers. The digital section is powered by V⁺ and Digital Common, which is about 3V below V⁺. The oscillator is also in the digital section. Normally 120 kHz for rejection of 60 Hz AC interference and 100 kHz for rejection of 50 Hz AC, the oscillator output is divided by two to generate the internal master clock. The analog section contains the integrator, comparator, reference section, analog buffers, and several analog switches which are controlled by the digital logic. The analog section is powered from V⁺ and V⁻.

DC VOLTAGE MEASUREMENT

Autozero

Only those portions of the analog section which are used during DC voltage measurements are shown in Figure 5. As shown in the timing diagram (Figure 6), each measurement starts with an autozero (AZ) phase. During this phase, the integrator and comparator are configured as unity gain buffers and their non-inverting inputs are connected to Common. The output of the integrator, which is equal to its offset, is stored on C_{AZ}—the autozero capacitor. Similarly, the offset of the comparator is stored in C_{INT}. The autozero cycle equals 1000 clock cycles which is one 60 Hz line cycle with a 120 kHz oscillator or one 50 Hz line cycle with a 100 kHz crystal.

Range 1 Integrate

The ICL7139 performs a full autorange search for each reading, beginning with range 1. During the range 1 integrate period, internal switches connect the INT V/Ohm terminal to the Triple Point (Pin 13). The input signal is integrated for 10 clock cycles, which are gated out over a period of 1000 clock cycles to ensure good normal mode rejection of AC line interference.

Range 1 Deintegrate

At the beginning of the deintegrate cycle, the polarity of the voltage on the integrator capacitor (C_{INT}) is checked, and either the DEINT⁺ or DEINT⁻ is asserted. The integrator capacitor C_{INT} is then discharged with a current equal to V_{REF}/R_{DEINT}. The comparator monitors the voltage on C_{INT}. When the voltage on C_{INT} is reduced to zero (actually to the V_{OS} of the comparator), the comparator output switches, and the current count is latched. If the C_{INT} voltage zero-crossing does not occur before 4000 counts have elapsed, the overload flag is set. "OL" (overload) is then displayed on the LCD. If the latched result is between 360 and 3999, the count is transferred to the output latches and is displayed. When the count is less than 360, an under-range has occurred, and the ICL7139 then switches to range 2—the 40V scale.

Range 2

The range 2 measurement begins with an autozero cycle similar to the one that preceded range 1 integration. Range 2 cycle length however, is one AC line cycle, minus 360 clock cycles. When performing the range 2 cycle, the signal is integrated for 100 clock cycles, distributed throughout

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NOTE: All typical values have been characterized but are not tested.

one line cycle. This is done to maintain good normal mode rejection. Range 2 sensitivity is ten times greater than range 1 (100 vs. 10 clock cycle integration) and the full scale voltage of range 2 is 40V. The range 2 deintegrate cycle is identical to the range 1 deintegrate cycle, with the result being displayed only for readings greater than 360 counts. If the reading is below 360 counts, the ICL7139 again asserts the internal underrange signal and proceeds to range 3.

Range 3

The range 3 or 4V full scale measurement is identical to the range 2 measurement, except that the input signal is integrated during the full 1000 clock cycles (one line frequency cycle). The result is displayed if the reading is greater than 360 counts. Underrange is asserted, and a range 4 measurement is performed if the result is below 360 counts.

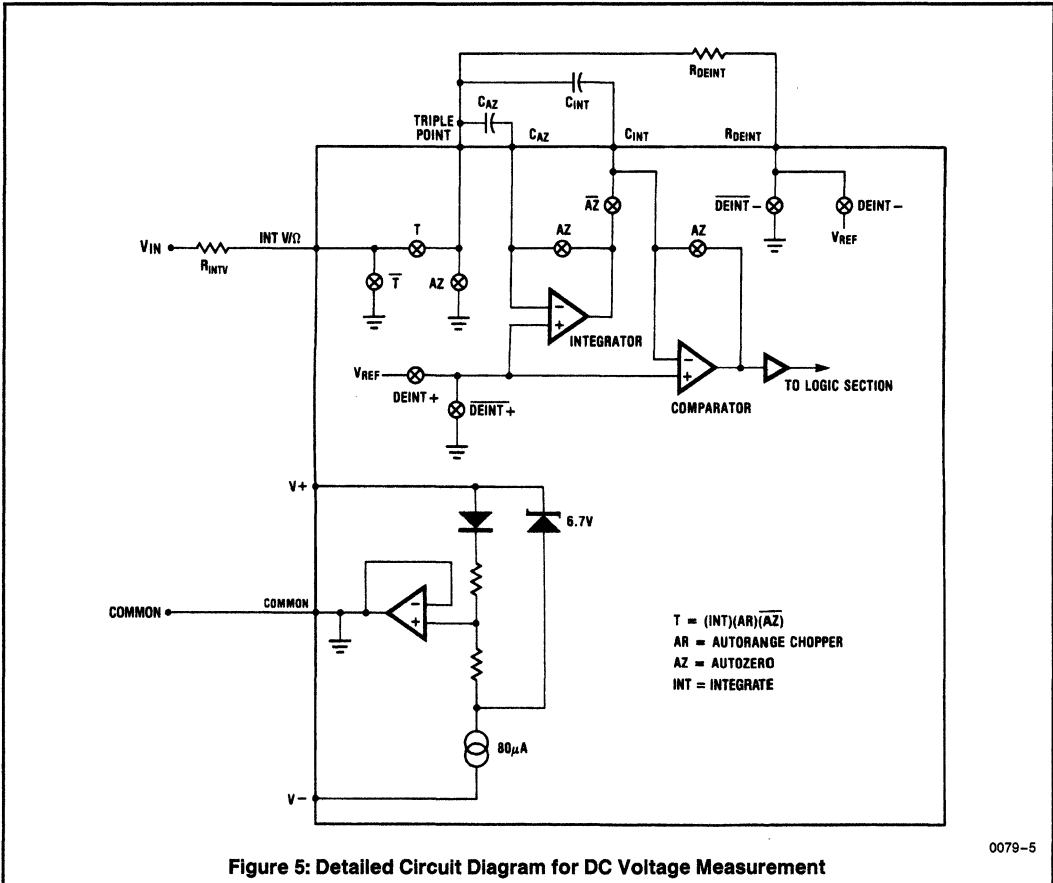
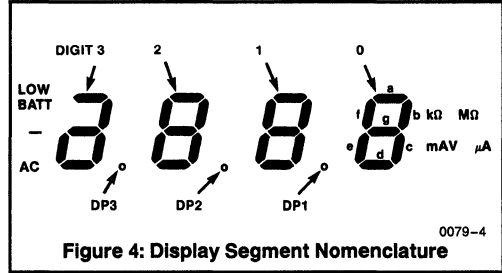
Range 4

This measurement is similar to the range 1, 2 and 3 measurements, except that the integration period is 10,000 clock cycles (10 line cycles) long. The result of this mea-

surement is transferred to the output latches and displayed even if the reading is less than 360.

Autozero

After finding the first range for which the reading is above 360 counts, the display is updated and an autozero cycle is entered. The length of the autozero cycle is variable which results in a fixed measurement period of 24,000 clock cycles (24 line cycles).



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NOTE: All typical values have been characterized but are not tested.

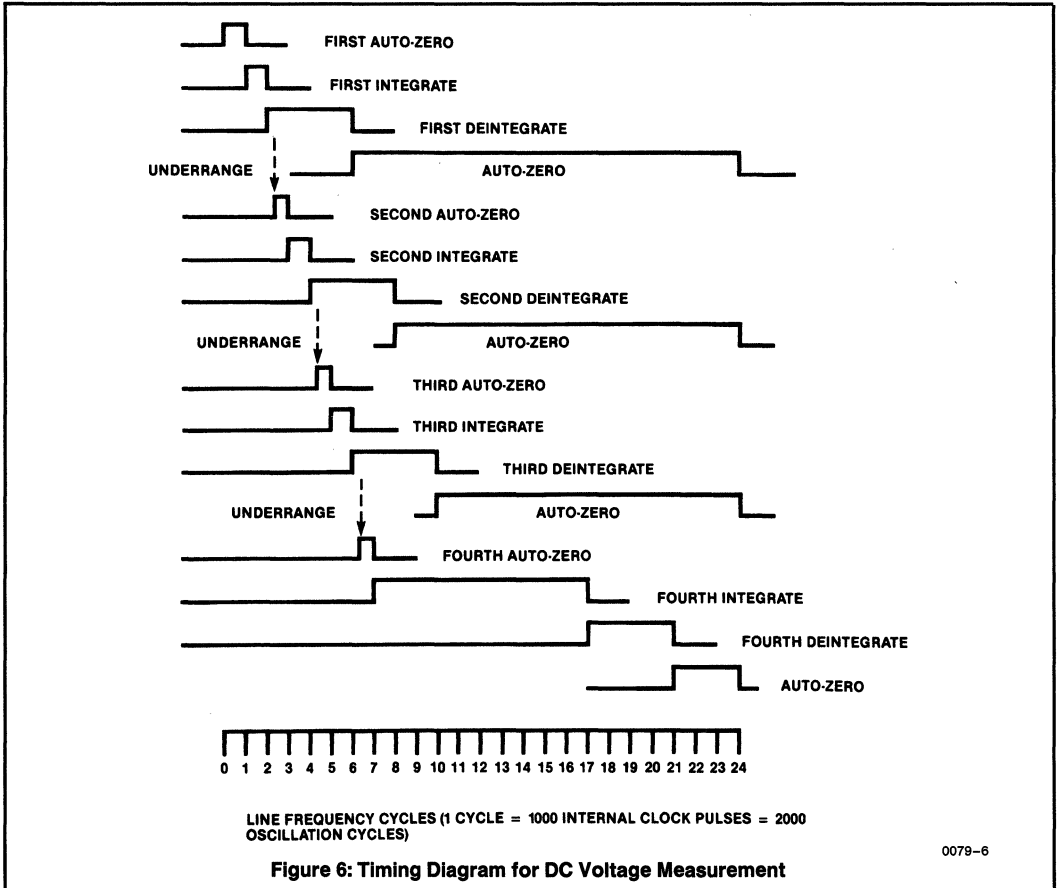


Figure 6: Timing Diagram for DC Voltage Measurement

0079-6

DC CURRENT

Figure 7 shows a simplified block diagram of the analog section of the ICL7139 during DC current measurement. The DC current measurements are very similar to DC voltage measurements except: 1) The input voltage is developed by passing the input current through a 0.1 ohm (HI current ranges), or 9.9 ohm (LOW current ranges) current sensing resistor; 2) Only those ranges with 1000 and 10,000 clock cycles of integration are used; 3) The R_{INT} resistor is 1 megohm, rather than the 10 megohm value used for the R_{INT} ν resistor.

By using the lower value integration resistor, and only the 2 most sensitive ranges, the voltage drop across the current sensing resistor is 40 mV maximum on the 4 mA and 400 mA ranges; 400 mV maximum on the 40 mA and 4A scales. With some increase in noise, these "burden" voltages can be reduced by lowering the value of both the current sense resistors and the R_{INT} resistor proportionally. The DC current measurement timing diagram is similar to the DC voltage measurement timing diagram, except in the DC current timing diagram, the first and second integrate and deintegrate phases are skipped.

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NOTE: All typical values have been characterized but are not tested.

AC VOLTAGE MEASUREMENT

As shown in Figure 8, the AC input voltage is applied directly to the ICL7139 input resistor. No separate AC to DC conversion circuitry is needed. The AC measurement cycle is begun by disconnecting the integrator capacitor and using the integrator as an autozeroed comparator to detect the positive-going zero crossing. Once synchronized to the AC input, the autozero loop is closed and a normal integrate/deintegrate cycle begins. The ICL7139 resynchronizes itself to the AC input prior to every reading. Because diode D4 is in series with the integrator capacitor, only positive current from the integrator flows into the integrator capacitor, C_{INT}. Since the voltage on C_{INT} is proportional to the half-wave rectified average AC input voltage, a conversion factor must be applied to convert the reading to RMS. This conversion factor is $\pi/\sqrt{2} = 1.107$, and the system clock is manipulated to perform the RMS conversion. As a result the deintegrate and autozero cycle times are reduced by 10%.

Ratiometric Ohms Measurement

The ratiometric ohms measurement is performed by first integrating the voltage across an unknown resistor, R_x, then

effectively deintegrating the voltage across a known resistor (R_{KNOWN1} or R_{KNOWN2} of Figure 9). The shunting effect of R_{INTV} does not affect the reading because it cancels exactly between integration and deintegration. Like the current measurements, the ohm measurements are split into two sets of ranges. LO ohms measurements use a 10 kilohm reference resistor, and the full scale ranges are 4 and 40 kilohms. HI ohms measurements use a 1 megohm reference resistor, and the full scale ranges are 0.4 and 4 megohms. The measurement phases and timing are the same as the measurement phases and timing for DC current except: 1) During the integrate phases the input voltage is the voltage across the unknown resistor R_x, and; 2) During the deintegrate phases, the input voltage is the voltage across the reference resistor R_{KNOWN1} or R_{KNOWN2}.

Continuity Indication

When the ICL7139 is in the LO ohms measurement mode, the continuity circuit of Figure 10 will be active. When the voltage across R_x is less than approximately 100 mV, the beeper output will be on. When R₃ is 10 kilohms, the beeper output will be on when R_x is less than 1 kilohm.

2

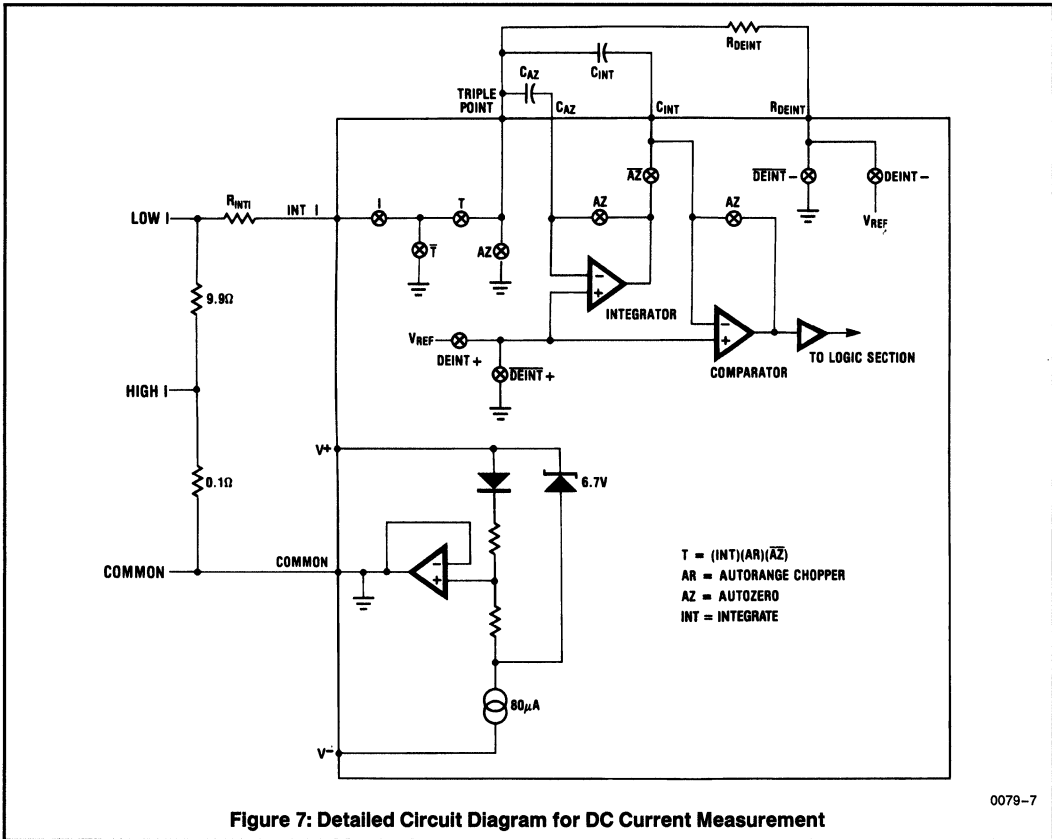


Figure 7: Detailed Circuit Diagram for DC Current Measurement

0079-7

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Common Voltage

The analog and digital common voltages of the ICL7139 are generated by an on-chip resistor/zener/diode combination, shown in Figure 11. The resistor values are chosen so the coefficient of the diode voltage cancels the positive temperature coefficient of the zener voltage. This voltage is then buffered to provide the analog common and the digital common voltages. The nominal voltage between V⁺ and analog common is 3V. The analog common buffer can sink about 20 mA, or source 0.01 mA, with an output impedance of 10 ohms. A pullup resistor to V⁺ may be used if more sourcing capability is desired. Analog common may be used to generate the reference voltage, if desired.

Oscillator

The ICL7139 uses a parallel resonant-type crystal in a Pierce oscillator configuration, as shown in Figure 12, and requires no other external components. The crystal eliminates the need to trim the oscillator frequency. An external signal may be capacitively coupled in OSC IN, with a signal level between 0.5 and 3V pk-pk. Because the OSC OUT

pin is not designed to drive large external loads, loading on this pin should not exceed a single CMOS input. The oscillator frequency is internally divided by two to generate the ICL7139 clock. The frequency should be 120 kHz to reject 60 Hz AC signals, and 100 kHz to reject 50 Hz signals.

Display Drivers

Figure 13 shows typical LCD Drive waveforms, RMS ON, and RMS OFF voltage calculations. Duplex multiplexing is used to minimize the number of connections between the ICL7139 and the LCD. The LCD has two separate backplanes. Each drive line can drive two individual segments, one referenced to each backplane. The ICL7139 drives 3¾ 7-segment digits, 3 decimal points, and 11 annunciators. Annunciators are used to indicate polarity, low battery condition, and the range in use. Peak drive voltage across the display is approximately 3V. An LCD with approximately 1.4V RMS threshold voltage should be used. The third voltage level needed for duplex drive waveforms is generated through an on-chip resistor string. The DC component of the drive waveforms is guaranteed to be less than 50 mV.

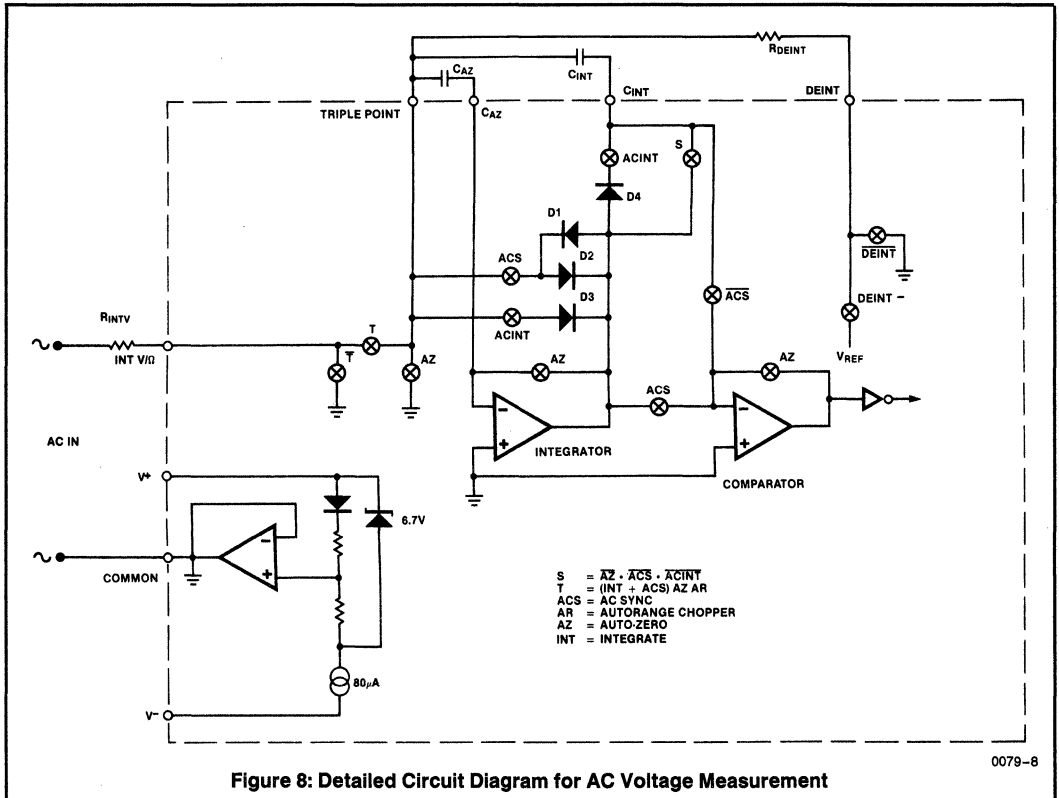


Figure 8: Detailed Circuit Diagram for AC Voltage Measurement

0079-8

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Ternary Input

The Ohms/Volts/Amps logic input is a ternary, or 3-level input. This input is internally tied to the common voltage through a high-value resistor, and will go to the middle, or "Volts" state, when not externally connected. When connected to V^- , approximately $5 \mu\text{A}$ of current flows out of the input. In this case, the logic level is the "Amps", or low state. When connected to V^+ , about $5 \mu\text{A}$ of current flows into the input. Here, the logic level is the "Ohms", or high state. For other pins, see Table 2.

Table 2: Ternary Inputs Connections

Pin Number	V^+	OPEN or COM	V^-
17	mA	μA	Test
18	Ohms	Volts	Amps
19	Hi Ω /DC	Lo Ω /AC	Test
20	Hold	Auto	Test

COMPONENT SELECTION

For optimum performance while maintaining the low-cost advantages of the ICL7139, care must be taken when selecting external components. This section reviews specifications and performance effects of various external components.

Integrator Capacitor, C_{INT}

As with all dual-slope integrating convertors, the integration capacitor must have low dielectric absorption to reduce linearity errors. Polypropylene capacitors add undetectable errors at a reasonable cost, while polystyrene and polycarbonate may be used in less critical applications. The

ICL7139 is designed to use a 3.3 nF ($0.0033 \mu\text{F}$) C_{INT} with an oscillator frequency of 120 kHz and an R_{INTV} of 10 megohms. With a 100 kHz oscillator frequency (for 50 Hz line frequency rejection), C_{INT} and R_{INTV} affects the voltage swing of the integrator. Voltage swing should be as high as possible without saturating the integrator. Saturation occurs when the integrator output is within 1V of either V^+ or V^- . Integrator voltage swing should be about $\pm 2\text{V}$ when using standard component values. For different R_{INTV} and oscillator frequencies the value of C_{INT} can be calculated from:

$$C_{INT} = \frac{(\text{Integrate Time}) \times (\text{Integrate Current})}{(\text{Desired Integrator Swing})}$$

$$= \frac{(10,000 \times 2 \times \text{Oscillator Period}) \times 0.4\text{V}/R_{INTV}}{(2\text{V})}$$

Integrator Resistors

The normal values of the R_{INTV} and R_{INTI} resistors are 10 megohms and 1 megohm respectively. Though their absolute values are not critical, unless the value of the current sensing resistors are trimmed, their ratio should be 10:1, within 0.05%. Some carbon composition resistors have a large voltage coefficient which will cause linearity errors on the 400V scale. Also, some carbon composition resistors are very noisy. The class "A" output of the integrator begins to have nonlinearities if required to sink more than $70 \mu\text{A}$ (the sourcing limit is much higher). Because R_{INTV} drives a virtual ground point, the input impedance of the meter is equal to R_{INTV} .

Deintegration Resistor, R_{DEINT}

Unlike most dual-slope A/D converters, the ICL7139 uses different resistors for integration and deintegration. R_{DEINT} should normally be the same value as R_{INTV} , and have the same temperature coefficient. Slight errors in matching may be corrected by trimming the reference voltage.

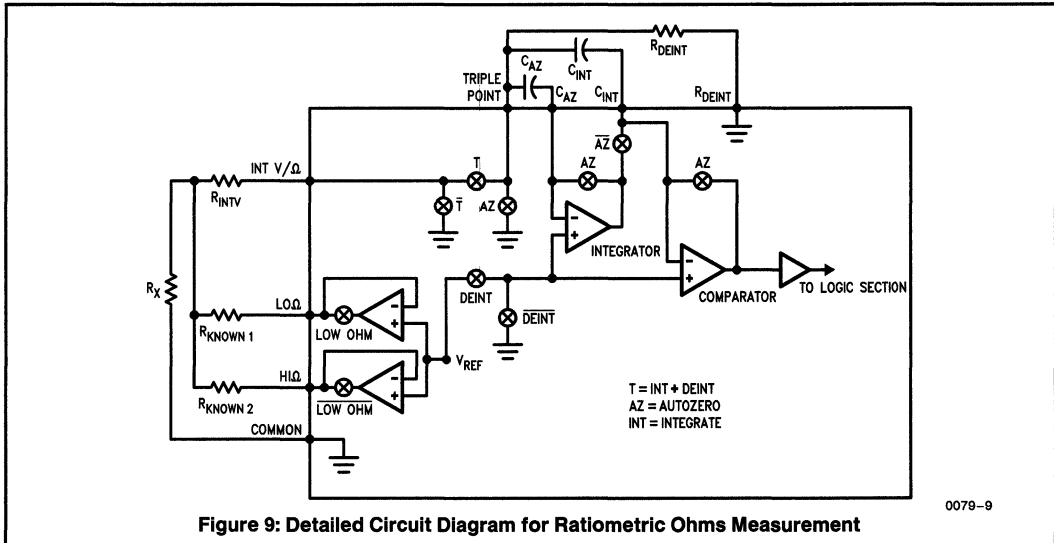


Figure 9: Detailed Circuit Diagram for Ratiometric Ohms Measurement

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Autozero Capacitor, C_{AZ}

The C_{AZ} is charged to the integrator's offset voltage during the autozero phases, and subtracts that voltage from the input signal during the integrate phases. The integrator thus appears to have zero offset voltage. Minimum C_{AZ} value is determined by: 1) Circuit leakages; 2) C_{AZ} self-discharge; 3) Charge injection from the internal autozero switches. To avoid errors, the C_{AZ} voltage change should be less than $1/10$ of a count during the 10,000 count clock cycle integration period for the 400 mV range. These requirements set a lower limit of 0.047 μF for C_{AZ} but 0.1 μF is the preferred value. The upper limit on the value of C_{AZ} is set by the time constant of the autozero loop, and the 1 line cycle time period allotted to autozero. C_{AZ} may be several 10s of microfarads before approaching this limit.

The ideal C_{AZ} is a low leakage polypropylene or Teflon capacitor. Other film capacitors such as polyester, polystyrene, and polycarbonate introduce negligible errors. If a few seconds of settling time upon power-up is acceptable, the C_{AZ} may be a ceramic capacitor, provided it does not have excessive leakage.

Ohms Measurement Resistors

Because the ICL7139 uses a ratiometric ohms measurement technique, the accuracy of ohms reading is primarily determined by the absolute accuracy of the $R_{K\text{KNOWN}1}$ and $R_{K\text{KNOWN}2}$. These should normally be 10 kilohms and 1 megohm, with an absolute accuracy of at least 0.5%.

Current Sensing Resistors

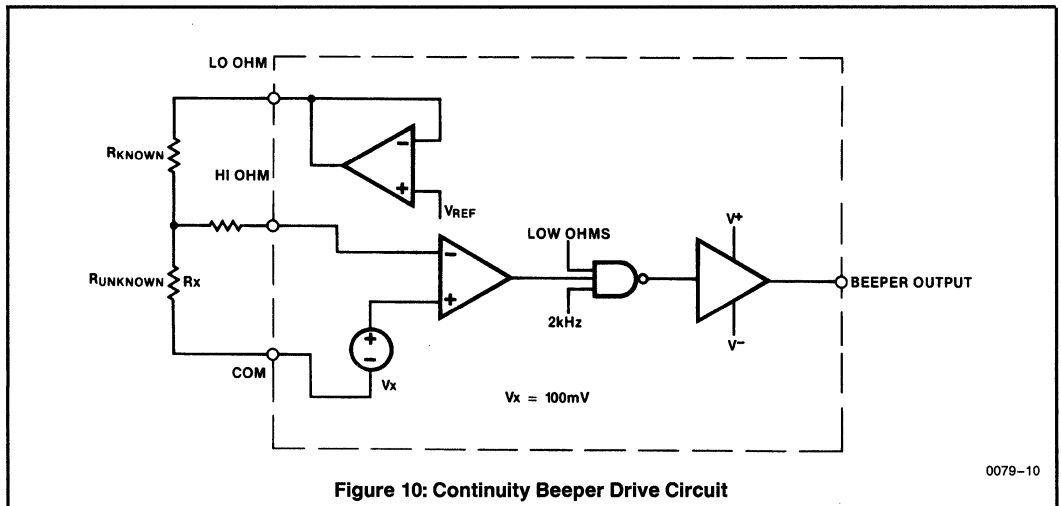
The 0.1 ohm and 9.9 ohm current sensing resistors convert the measured current to a voltage, which is then measured using $R_{\text{INT}1}$. The two resistors must be closely matched, and the ratio between $R_{\text{INT}1}$ and these two resistors must be accurate—normally 0.5%. The 0.1 ohm resistor must be capable of handling the full scale current of 4 amps, which requires it to dissipate 1.6 watts.

Continuity Beeper

The Continuity Beeper output is designed to drive a piezoelectric transducer at 2 kHz (using a 120 kHz crystal), with a voltage output swing of V^+ to V^- . The beeper output off state is at the V^+ rail. When crystals with different frequencies are used, the frequency needed to drive the transducer can be calculated by dividing the crystal frequency by 60.

Display

The ICL7139 uses a custom, duplexed drive display with range, polarity, and low battery annunciators. With a 3 volt peak display voltage, the RMS ON voltage will be 2.37V minimum; RMS OFF voltage will be 1.06V maximum. Because the display voltage is not adjustable, the display should have a 10% ON threshold of about 1.4V. Most display manufacturers supply a graph that shows contrast versus RMS drive voltage. This graph can be used to determine what the contrast ratio will be when driven by the ICL7139. Most display thresholds decrease with increasing temperature. The threshold at the maximum operating temperature should be checked to ensure that the "off" segments will not be turned "on" at high temperatures.



NOTE 1: The ICL7139 contains a comparator that is enabled on the lowest ohms range. It trips at approximately $1/4$ of the full scale value of that range and enables the beeper driver to oscillate (between V^- and V^+) at 2 kHz. The beeper driver is capable of driving a piezo-electric transducer. The beeper output response is independent of the state of the conversion; therefore appears instantaneous to the user. Some applications may require a 150 pF capacitor between pin 4 and pin 8 to insure a sharp on/off continuity detection.

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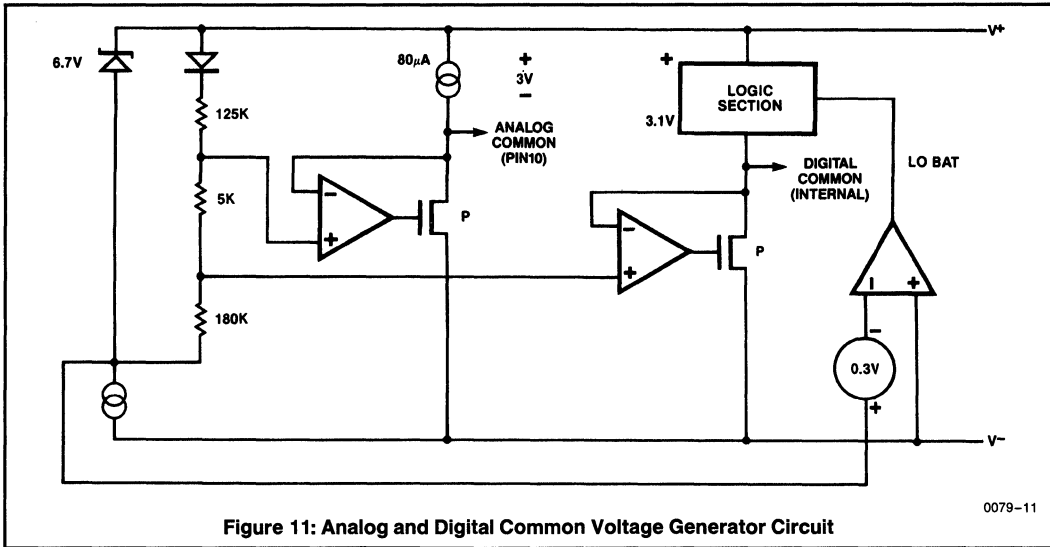


Figure 11: Analog and Digital Common Voltage Generator Circuit

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Crystal

The ICL7139 is designed to use a parallel resonant 120 kHz or 100 kHz crystal with no additional external components. The R_S parameter should be less than 25 kilohms to ensure oscillation. Initial frequency tolerance of the crystal can be a relatively loose 0.05%.

Switches

Because the logic input draws only about 5 μ A, switches driving these inputs should be rated for low current, or "dry" operations. The switches on the external inputs must be able to reliably switch low currents, and be able to handle voltages in excess of 400V AC.

Reference Voltage Source

A voltage divider connected to V^+ and Common is the simplest source of reference voltage. While minimizing external component count, this approach will provide the same voltage tempco as the ICL7139 Common—about 100 PPM/ $^{\circ}$ C. To improve the tempco, an ICL8069 bandgap reference may be used (see Figure 14). The reference voltage source output impedance must be $\leq R_{DEINT}/4000$.

Applications, Examples, and Hints

A complete autoranging 3 $\frac{3}{4}$ digit multimeter is shown in Figure 15. The following sections discuss the functions of specific components and various options.

Meter Protection

The ICL7139 and its external circuitry should be protected against accidental application of 110/220V AC line voltages on the ohms and current ranges. Without the necessary precautions, both the 7139 and its external components could be damaged under such fault conditions. For the current ranges, fast-blow fuses should be used between S5A in Figure 15 and the 0.1 ohm and 9.9 ohm shunt resistors. For the ohms ranges, no additional protection circuitry is required. However, the 10 kilohm resistor connected to pin 7 must be able to dissipate 1.2W or 4.8W for short periods of time during accidental application of 110V or 220V AC line voltages respectively.

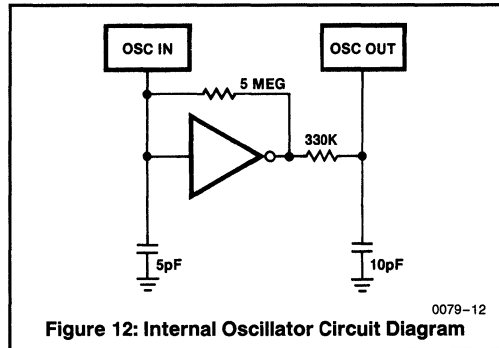


Figure 12: Internal Oscillator Circuit Diagram

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Printed Circuit Board Layout Considerations

Particular attention must be paid to rollover performance, leakages, and guarding when designing the PCB for a ICL7139-based multimeter.

Rollover Performance, Leakages, and Guarding

Because the ICL7139 system measures very low currents, it is essential that the PCB have low leakage. Boards should be properly cleaned after soldering. Areas of particular importance are: 1) The INT V/ Ω and INT I Pins; 2) The Triple Point; 3) The R_{DEINT} and the C_{AZ} pins.

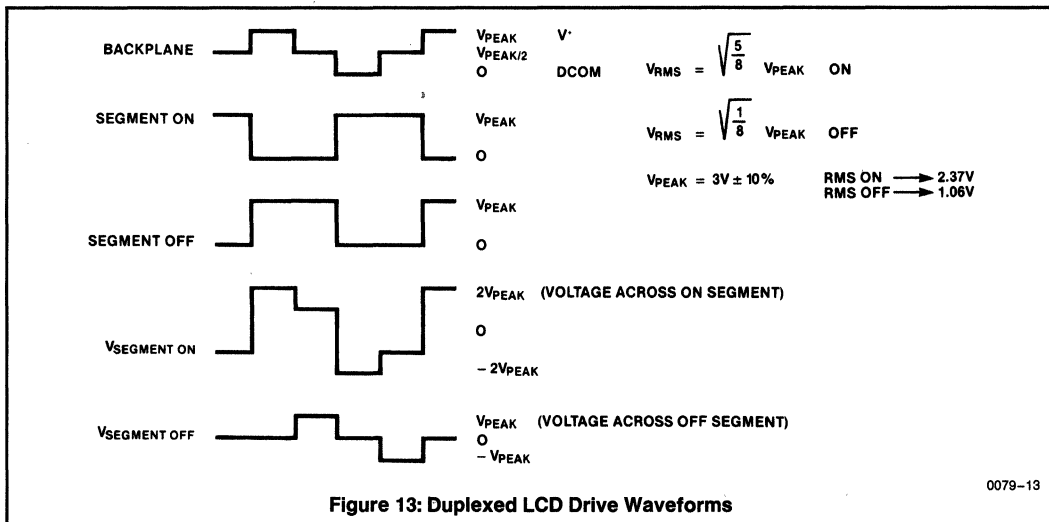
The conversion scheme used by the ICL7139 changes the common mode voltage on the integrator and the capacitors C_{AZ} and C_{INT} during a positive deintegrate cycle. Stray capacitance to ground is charged when this occurs, removing some of the charge on C_{INT} and causing rollover error. Rollover error increases about 1 count for each picofarad of capacitance between C_{AZ} or the Triple Point and ground, and is seen as a zero offset for positive voltages. Rollover error is not seen as gain error.

The rollover error causes the width of the +0 count to be larger than normal. The ICL7139 will thus read zero until several hundred microvolts are applied in the positive direction. The ICL7139 will read -1 when approximately -100 μ V is applied.

The rollover error can be minimized by guarding the Triple Point and C_{AZ} nodes with a trace connected to the C_{INT} pin, which is driven by the output of the integrator. Guarding these nodes with the output of the integrator reduces the stray capacitance to ground, which minimizes the charge error on C_{INT} and C_{AZ}. If possible, the guarding should be used on both sides of the PC board.

Stray Pickup

While the ICL7139 has excellent rejection of line frequency noise and pickup in the DC ranges, any stray coupling will effect the AC reading. Generally, the analog circuitry should be as close as possible to the ICL7139. The analog circuitry should be removed or shielded from any 120V AC power inputs, and any AC sources such as LCD drive waveforms. Keeping the analog circuit section close to the ICL7139 will also help keep the area free of any loops, thus reducing magnetically coupled interference coming from power transformers, or other sources.



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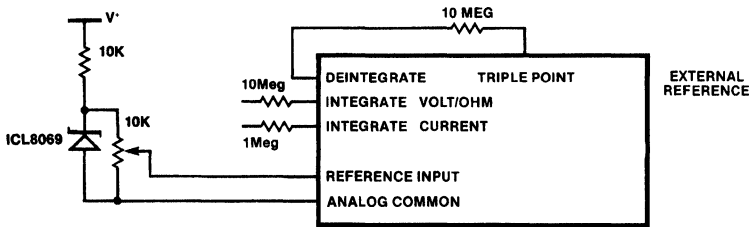


Figure 14: External Voltage Reference Connection to ICL7139

0079-14

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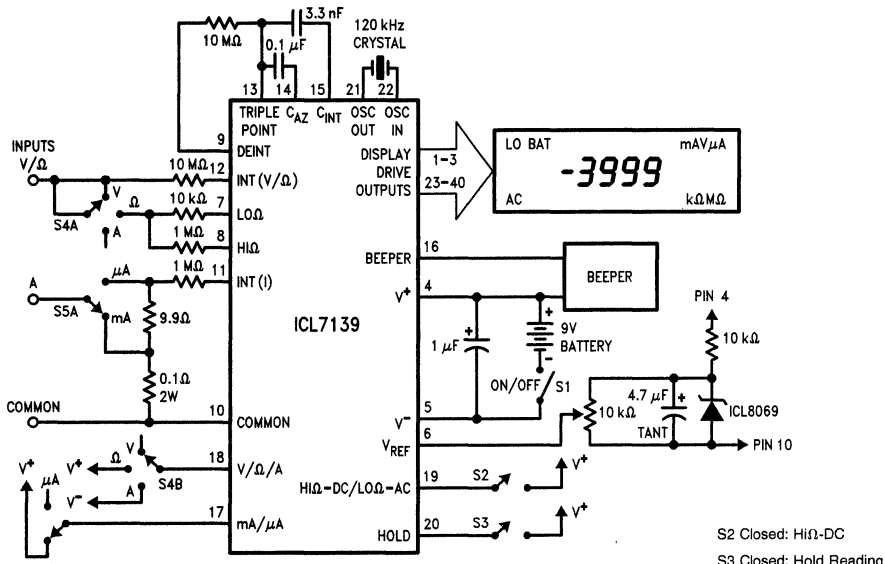


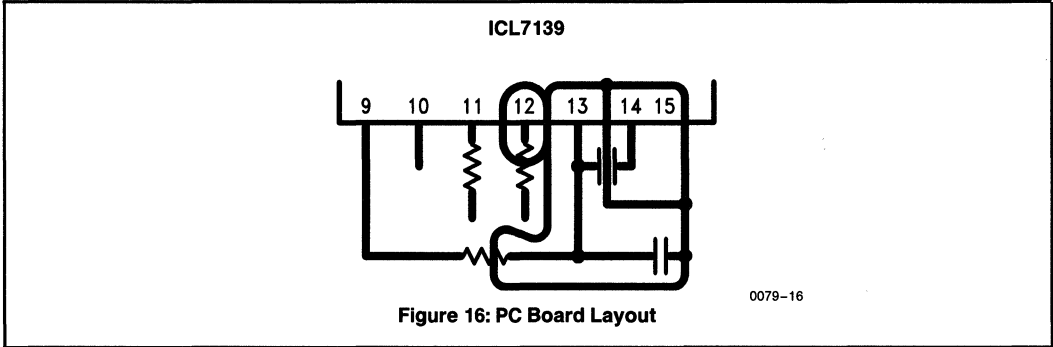
Figure 15: Basic Multimeter Application Circuit for ICL7139

S2 Closed: HIΩ-DC
S3 Closed: Hold Reading
0079-15

- NOTE 1: Crystal is a Statek or SaRonix CX-IV type.
 2: Multimeter protection components have not been shown.
 3: Display is from LX D, part number 38D3R02H.
 4: Beeper is from muRata, part number PKM24-4A0.

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ICL7149

Low Cost 3³/₄-Digit Autoranging Multimeter



ICL7149

GENERAL DESCRIPTION

The Intersil ICL7149 is a high performance, low power, autoranging digital multimeter IC. Unlike other autoranging multimeter ICs, the ICL7149 always displays the result of a conversion on the correct range. There is no "range hunting" noticeable in the display. The unit will autorange between the four different ranges in the DC voltage, DC current and resistance measurement modes. A manual switch is used to select the 2 high group ranges. DC current ranges are 4 mA and 40 mA in the low current group, 400 mA and 4A in the high current group. Resistance measurements are made on 4 ranges, which are divided into two groups. The low resistance ranges are 4/40 kilohms. High resistance ranges are 0.4/4 megohms. Resolution on the lowest range is 1 ohm.

PRELIMINARY
All Prices Subject To Change Without Notice

FEATURES

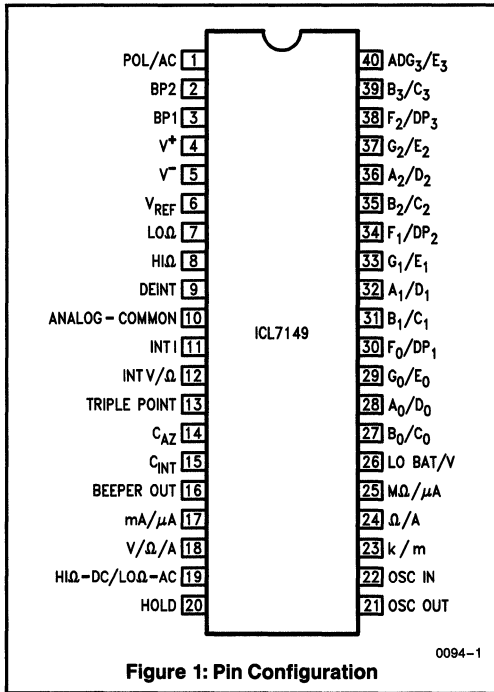
- **18 Ranges:**
 - 4 DC Voltage—400 mV, 4V, 40V, 400V
 - 2 AC Voltage—with Optional AC Circuit
 - 4 DC Current—4 mA, 40 mA, 400 mA, 4A
 - 4 AC Current with Optional AC Circuit
 - 4 Resistance—4 k Ω , 40 k Ω , 400 k Ω , 4 M Ω
- **Autoranging—First Reading is Always on Correct Range**
- **On-Chip Duplex LCD Display Drive Including Three Decimal Points and 11 Annunciators**
- **Low Power Dissipation—Less than 20 mW—1000 Hour Typical Battery Life**
- **Display Hold Input**
- **Continuity Output Drives Piezoelectric Beeper**
- **Low Battery Annunciator with On-Chip Detection**
- **Guaranteed Zero Reading for 0 Volts Input on All Ranges**

2

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7149CPL	0°C to +70°C	40 Pin Plastic DIP
*ICL7149CM44	0°C to +70°C	44 Pin Surface Mount

*Consult Factory for Details



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V⁺ to V⁻) 15V
 Reference Input Voltage (V_{REF} to COM) 3V
 Analog Input Current 100 μA
 (I_{N+} Current or I_{N+} Voltage)
 Clock Input Swing V⁺ to V⁺ - 3
 Power Dissipation (Plastic Package) 800 mW
 Operating Temperature Range 0°C to +70°C

Storage Temperature Range -65°C to +130°C
 Lead Temperature (Soldering, 10 sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V⁺ = +9.0V, T_A = +25°C, V_{REF} adjusted for -3.700 reading on DC volts, test circuit as shown in Figure 3. Crystal Frequency = 120 kHz.

Parameter	Test Conditions	Min	Typ	Max	Units
Zero Input Reading	V _{IN} or I _{IN} or R _{IN} = 0.00	-00.0		+00.0	V, I, Ohms
Rollover Error (Note 1)	V _{IN} or I _{IN} = ± Full Scale		4		Counts
Linearity (Best Straight Line) (Note 5)		-1		+1	Counts
Accuracy DC V, 400 Volt Range Only				±1	% of RDG + 1
Accuracy DC V, 400 Volt Range Excluded				±0.2	% of RDG + 1
Accuracy Ohms, 4K and 400K Range				±0.5	% of RDG + 8
Accuracy Ohms, 40K and 4Meg Range				±1	% of RDG + 9
Accuracy DC I, Unadjusted for FS				±0.5	% of RDG + 1
Accuracy DC I, Adjusted for FS				±0.2	% of RDG + 1
Open Circuit Voltage for Ohms Measurements	R _{UNKNOWN} = Infinity		V _{REF}		V
Noise (Note 2, 95% of Time)	V _{IN} = 0, DC Volts		0.1		LSB
Supply Current	V _{IN} = 0, DC Voltage Range		1.5	2.4	mA
Analog Common (with Respect to V ⁺)	I _{COMMON} < 10 μA	2.8	3.0	3.2	V
Temperature Coefficient of Analog Common	I _{COMMON} < 10 μA, Temp = 0°C-70°C		-100		ppm/°C
Output Impedance of Analog Common	I _{COMMON} < 100 μA		1	10	Ohms
Backplane/Segment Drive Voltage	Average DC < 50 mV	2.7	2.9	3.1	V
Backplane/Segment Display Frequency			75		Hz
Switch Input Current (Note 3)	V _{IN} = V ⁺ to V ⁻	-50		+50	μA
Switch Input Levels (High Trip Point)		V ⁺ - 0.5		V ⁺	V
Switch Input Levels (Mid Trip Point)		V ⁻ + 3		V ⁺ - 2.5	V
Switch Input Levels (Low Trip Point)		V ⁻		V ⁻ + 0.5	V
Beeper Output Drive (Rise or Fall Time)	C _{LOAD} = 10 nF		25	100	μs
Beeper Output Frequency			2		kHz
Continuity Detect	Range = Low Ohms, V _{REF} = 1.00V	500		2000	Counts
Power Supply Functional Operation	V ⁺ to V ⁻	7	9	11	V
Low Battery Detect (Note 4)	V ⁺ to V ⁻	6.5	7	7.5	V

NOTE 1: Rollover is defined as absolute value of negative reading minus absolute value of positive reading.

2: Noise is defined as the width of the uncertainty window (where the display will flicker) between two adjacent codes.

3: Applies to pins 17-20.

4: Analog Common falls out of regulation when the Low Battery Detect is asserted, however the ICL7149 will continue to operate correctly with a supply voltage above 7 volts and below 11 volts.

5: Guaranteed by design, not tested.

RDG = Reading

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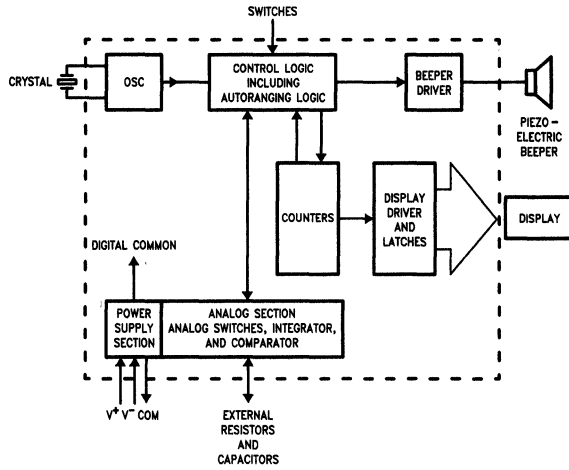


Figure 2: Functional Diagram

0094-2

3 1/4-Digit Autoranging DMM Using Intersil's ICL7149

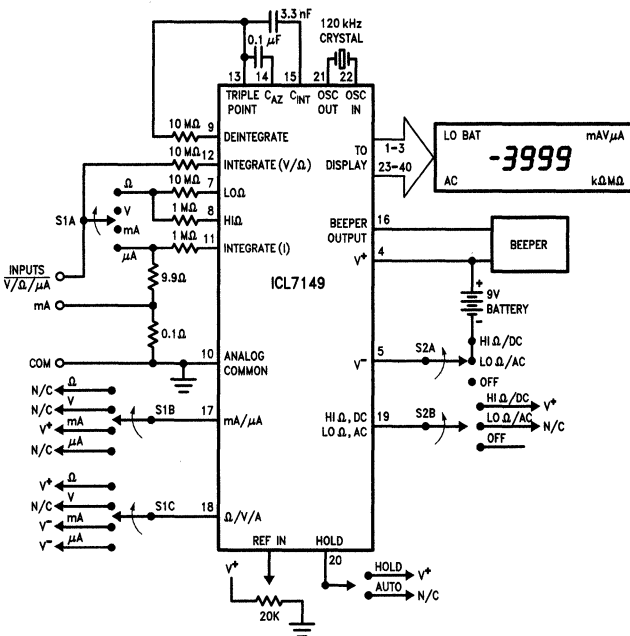


Figure 3: ICL7149 Test Circuit

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NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Numbers and Functions

I/O	Pin Number	Pin Function
O	1	Segment Driver, POL/AC
O	2	Backplane 2
O	3	Backplane 1
I	4	V+
I	5	V-
I	6	Reference Input
O	7	Lo Ohms
O	8	Hi Ohms
I/O	9	Deintegrate
I/O	10	Analog Common
I	11	Int I
I	12	Int V/Ohms
I	13	Triple Point
I	14	Auto Zero Capacitor (CAZ)
I	15	Integrate Capacitor (C _{INT})
O	16	Beeper Output
I	17	mA/μA
I	18	Ohms/V/A
I	19	Hi Ohms-DC/Lo Ohms-AC
I	20	Hold
O	21	Oscillator Out
I	22	Oscillator In
O	23	Segment Driver k/m
O	24	Segment Driver Ohms/A
O	25	Segment Driver M Ohms/μA
O	26	Segment Driver Lo Bat/V
O	27	Segment Driver B ₀ /C ₀
O	28	Segment Driver A ₀ /D ₀
O	29	Segment Driver G ₀ /E ₀
O	30	Segment Driver F ₀ /DP ₁
O	31	Segment Driver B ₁ /C ₁
O	32	Segment Driver A ₁ /D ₁
O	33	Segment Driver G ₁ /E ₁
O	34	Segment Driver F ₁ /DP ₁
O	35	Segment Driver B ₂ /C ₂
O	36	Segment Driver A ₂ /D ₂
O	37	Segment Driver G ₂ /E ₂
O	38	Segment Driver F ₂ /DP ₃
O	39	Segment Driver B ₃ /C ₃
O	40	Segment Driver ADG ₃ /E ₃

NOTE: For segment drivers, segments are listed as (segment for backplane 1)/(segment for backplane 2). Example: pin 27; segment B0 is on backplane 1, segment C0 is on backplane 2.

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DETAILED DESCRIPTION

General

Figure 2 is a simplified block diagram of the ICL7149. The digital section includes all control logic, counters, and display drivers. The digital section is powered by V⁺ and Digital Common, which is about 3V below V⁺. The oscillator is also in the digital section. Normally 120 kHz for rejection of 60 Hz AC interference and 100 kHz for rejection of 50 Hz AC, the oscillator output is divided by two to generate the internal master clock. The analog section contains the integrator, comparator, reference section, analog buffers, and several analog switches which are controlled by the digital logic. The analog section is powered from V⁺ and V⁻.

DC VOLTAGE MEASUREMENT

Autozero

Only those portions of the analog section which are used during DC voltage measurements are shown in Figure 5. As shown in the timing diagram (Figure 6), each measurement starts with an autozero (AZ) phase. During this phase, the integrator and comparator are configured as unity gain buffers and their non-inverting inputs are connected to Common. The output of the integrator, which is equal to its offset, is stored on CAZ, the autozero capacitor. Similarly, the offset of the comparator is stored in C_{INT}. The autozero cycle equals 1000 clock cycles, which is one 60 Hz line cycle with a 120 kHz crystal, or one 50 Hz line cycle with a 100 kHz crystal.

Range 1 Integrate

The ICL7149 performs a full autorange search for each reading, beginning with range 1. During the range 1 integrate period, internal switches connect the INT V/Ohm terminal to the Triple Point (Pin 13). The input signal is integrated for 10 clock cycles, which are gated out over a period of 1000 clock cycles to ensure good normal mode rejection of AC line interference.

Range 1 Deintegrate

At the beginning of the deintegrate cycle, the polarity of the voltage on the integrator capacitor (C_{INT}) is checked, and either the DEINT⁺ or DEINT⁻ is asserted. The integrator capacitor C_{INT} is then discharged with a current equal to V_{REF}/R_{DEINT}. The comparator monitors the voltage on C_{INT}. When the voltage on C_{INT} is reduced to zero (actually to the V_{OS} of the comparator), the comparator output switches, and the current count is latched. If the C_{INT} voltage zero-crossing does not occur before 4000 counts have elapsed, the overload flag is set. "OL" (overload) is then displayed on the LCD. If the latched result is between 360 and 3999, the count is transferred to the output latches and is displayed. When the count is less than 360, an under-range has occurred, and the ICL7149 then switches to range 2—the 40V scale.

Range 2

The range 2 measurement begins with an autozero cycle similar to the one that preceded range 1 integration. range 2 cycle length however, is one AC line cycle, minus 360 clock cycles. When performing the range 2 cycle, the signal is integrated for 100 clock cycles, distributed throughout one line cycle. This is done to maintain good normal mode rejection. Range 2 sensitivity is ten times greater than range 1 (100 vs 10 clock cycle integration) and the full scale voltage of range 2 is 40V. The range 2 deintegrate cycle is identical to the range 1 deintegrate cycle, with the result being displayed only for readings greater than 360 counts. If the reading is below 360 counts, the ICL7149 again asserts the internal underrange signal and proceeds to range 3.

Range 3

The range 3 or 4V full scale measurement is identical to the range 2 measurement, except that the input signal is integrated during the full 1000 clock cycles (one line frequency cycle). The result is displayed if the reading is greater than 360 counts. Underrange is asserted, and a range 4 measurement is performed if the result is below 360 counts.

Range 4

This measurement is similar to the range 1, 2 and 3 measurements, except that the integration period is 10,000 clock cycles (10 line cycles) long. The result of this measurement is transferred to the output latches and displayed even if the reading is less than 360.

Autozero

After finding the first range for which the reading is above 360 counts, the display is updated and an autozero cycle is entered. The length of the autozero cycle is variable which results in a fixed measurement period of 24,000 clock cycles (24 line cycles).

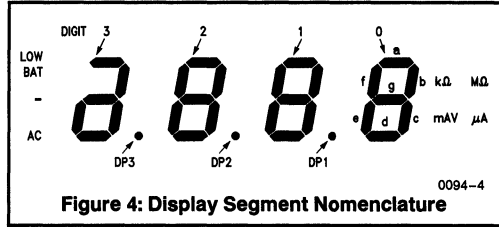


Figure 4: Display Segment Nomenclature

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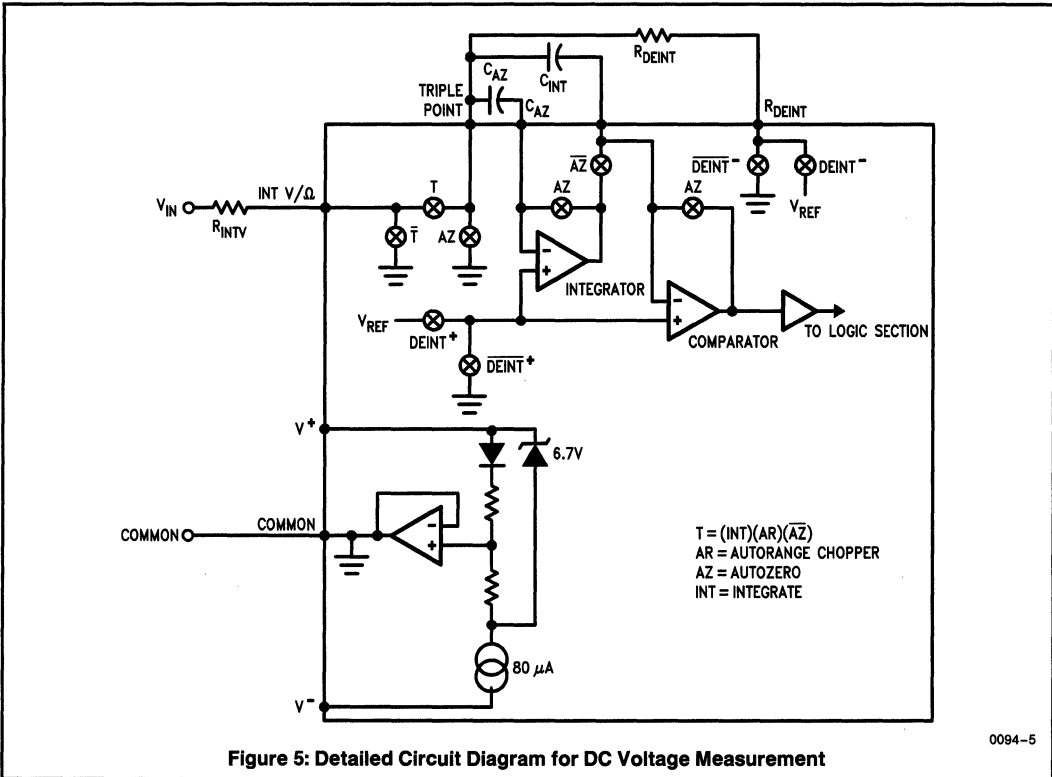
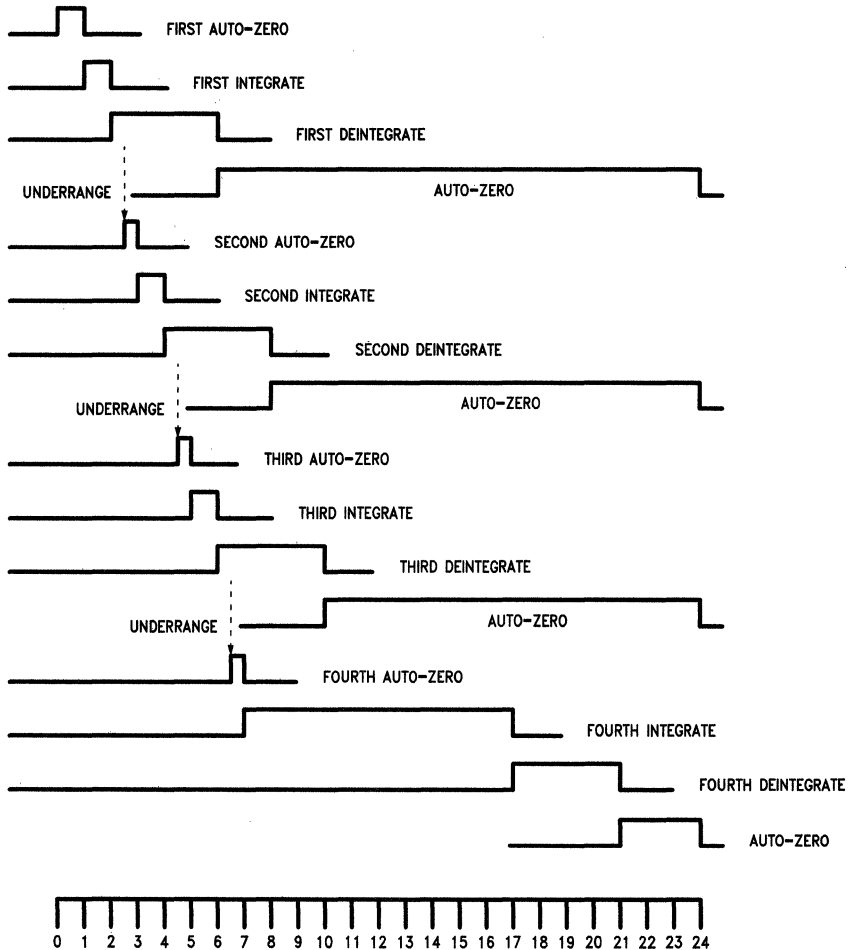


Figure 5: Detailed Circuit Diagram for DC Voltage Measurement

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Line Frequency Cycles
 (1 Cycle = 1000 Internal Clock Pulses = 2000 Oscillation Cycles)

0094-6

Figure 6: Timing Diagram for DC Voltage Measurement

DC CURRENT

Figure 7 shows a simplified block diagram of the analog section of the ICL7149 during DC current measurement. The DC current measurements are very similar to DC voltage measurements except: 1) The input voltage is developed by passing the input current through a 0.1 ohm (HI current ranges), or 9.9 ohm (LOW current ranges) current sensing resistor; 2) Only those ranges with 1000 and 10,000 clock cycles of integration are used; 3) The $R_{INT \downarrow}$ resistor is 1 megohm, rather than the 10 megohm value used for the $R_{INT \uparrow}$ resistor.

By using the lower value integration resistor, and only the 2 most sensitive ranges, the voltage drop across the current sensing resistor is 40 mV maximum on the 4 mA and 400 mA ranges; 400 mV maximum on the 40 mA and 4A scales. With some increase in noise, these "burden" voltages can be reduced by lowering the value of both the current sense resistors and the $R_{INT \downarrow}$ resistor proportionally. The DC current measurement timing diagram is similar to the DC voltage measurement timing diagram, except in the DC current timing diagram, the first and second integrate and deintegrate phases are skipped.

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AC VOLTAGE MEASUREMENT

The ICL7149 is designed to be used with an optional AC to DC voltage converter circuit. It will autorange through two voltage ranges (400V and 40V), and the AC annunciator is enabled as with the ICL7139. A typical averaging AC to DC converter is shown in Figure 8, while an RMS to DC converter is shown in Figure 9. AC current can also be measured with some simple modifications to either of the two circuits in Figures 8 and 9.

Ratiometric Ohms Measurement

The ratiometric ohms measurement is performed by first integrating the voltage across an unknown resistor, Rx, then effectively deintegrating the voltage across a known resistor (R_{KKNOWN1} or R_{KKNOWN2} of Figure 10). The shunting effect of R_{INTV} does not affect the reading because it cancels exactly between integration and deintegration. Like the current measurements, the ohm measurements are split into two sets of two ranges. LO ohms measurements use a 10 kilohm reference resistor, and the full scale ranges are 4 and 40 kilohms. HI ohms measurements use a 1 megohm reference resistor, and the full scale ranges are 0.4 and 4 megohms. The measurement phases and timing are the same as the measurement phases and timing for DC current except: 1) During the integrate phases the input voltage is the voltage across the unknown resistor Rx, and; 2) During the deintegrate phases, the input voltage is the voltage across the reference resistor R_{KKNOWN1} or R_{KKNOWN2}.

Continuity Indication

When the ICL7149 is in the LO ohms measurement mode, the continuity circuit of Figure 11 will be active. When the voltage across Rx is less than approximately 100 mV, the beeper output will be on. When R3 is 10 kilohms, the beeper output will be on when Rx is less than 1 kilohm.

Common Voltage

The analog and digital common voltages of the ICL7149 are generated by an on-chip resistor/zener/diode combination, shown in Figure 12. The resistor values are chosen so the coefficient of the diode voltage cancels the positive temperature coefficient of the zener voltage. This voltage is then buffered to provide the analog common and the digital common voltages. The nominal voltage between V⁺ and analog common is 3V. The analog common buffer can sink about 20 mA, or source 0.01 mA, with an output impedance of 10 ohms. A pullup resistor to V⁺ may be used if more sourcing capability is desired. Analog common may be used to generate the reference voltage, if desired.

Oscillator

The ICL7149 uses a parallel resonant-type crystal in a Pierce oscillator configuration, as shown in Figure 13, and requires no other external components. The crystal eliminates the need to trim the oscillator frequency. An external signal may be capacitively coupled to OSC IN, with a signal level between 0.5V and 3V pk-pk. Because the OSC OUT pin is not designed to drive large external loads, loading on this pin should not exceed a single CMOS input. The oscillator frequency is internally divided by two to generate the ICL7149 clock. The frequency should be 120 kHz to reject 60 Hz AC signals, and 100 kHz to reject 50 Hz signals.

Display Drivers

Figure 14 shows typical LCD Drive waveforms, RMS ON, and RMS OFF voltage calculations. Duplex multiplexing is used to minimize the number of connections between the ICL7149 and the LCD. The LCD has two separate backplanes. Each drive line can drive two individual segments, one referenced to each backplane. The ICL7149 drives 3¾ 7-segment digits, 3 decimal points, and 11 annunciators. Annunciators are used to indicate polarity, low battery condition, and the range in use. Peak drive voltage across the display is approximately 3V. An LCD with approximately 1.4V RMS threshold voltage should be used. The third voltage level needed for duplex drive waveforms is generated through an on-chip resistor string and the DC component of the drive waveforms is guaranteed to be less than 50 mV.

Ternary Input

The Ohms/Volts/Amps logic input is a ternary, or 3-level input. This input is internally tied to the common voltage through a high-value resistor, and will go to the middle, or "Volts" state, when not externally connected. When connected to V⁻, approximately 5 µA of current flows out of the input. In this case, the logic level is the "Amps", or low state. When connected to V⁺, about 5 µA of current flows into the input. Here, the logic level is the "Ohms", or high state. For other pins, see Table 2.

Table 2: Ternary Inputs Connections

Pin Number	V ⁺	OPEN or COM	V ⁻
17	mA	µA	Test
18	Ohms	Volts	Amps
19	HiΩ/DC	LoΩ/AC	Test
20	Hold	Auto	Test

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COMPONENT SELECTION

For optimum performance while maintaining the low-cost advantages of the ICL7149, care must be taken when selecting external components. This section reviews specifications and performance effects of various external components.

Integrator Capacitor, C_{INT}

As with all dual-slope integrating converters, the integration capacitor must have low dielectric absorption to reduce linearity errors. Polypropylene capacitors add undetectable errors at a reasonable cost, while polystyrene and polycarbonate may be used in less critical applications. The ICL7149 is designed to use a 3.3 nF (0.0033 μF) C_{INT} with

an oscillator frequency of 120 kHz and an R_{INTV} of 10 megohms. With a 100 kHz oscillator frequency (for 50 Hz line frequency rejection), both C_{INT} and R_{INTV} affect the voltage swing of the integrator. Voltage swing should be as high as possible without saturating the integrator, which occurs when the integrator output is within 1V of either V⁺ or V⁻. Integrator voltage swing should be about ±2V when using standard component values. For different R_{INTV} and oscillator frequencies the value of C_{INT} can be calculated from:

$$C_{INT} = \frac{(\text{Integrate Time}) \times (\text{Integrate Current})}{(\text{Desired Integrator Swing})}$$

$$= \frac{(10,000 \times 2 \times \text{Oscillator Period}) \times 0.4V/R_{INTV}}{(2V)}$$

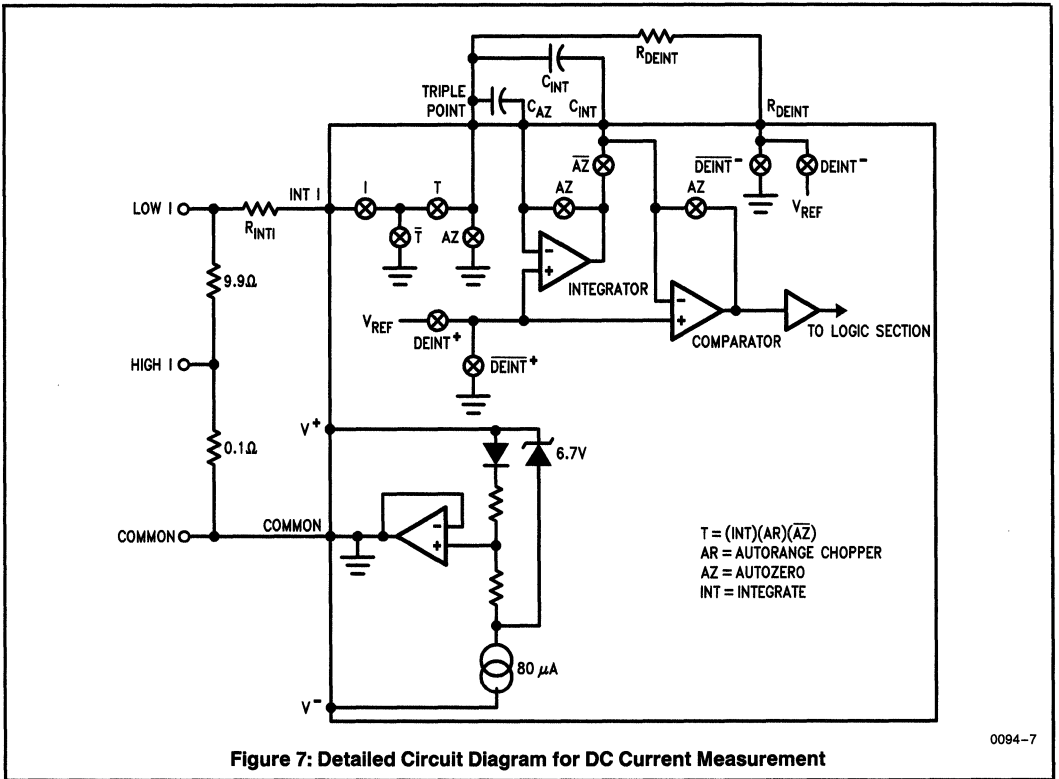
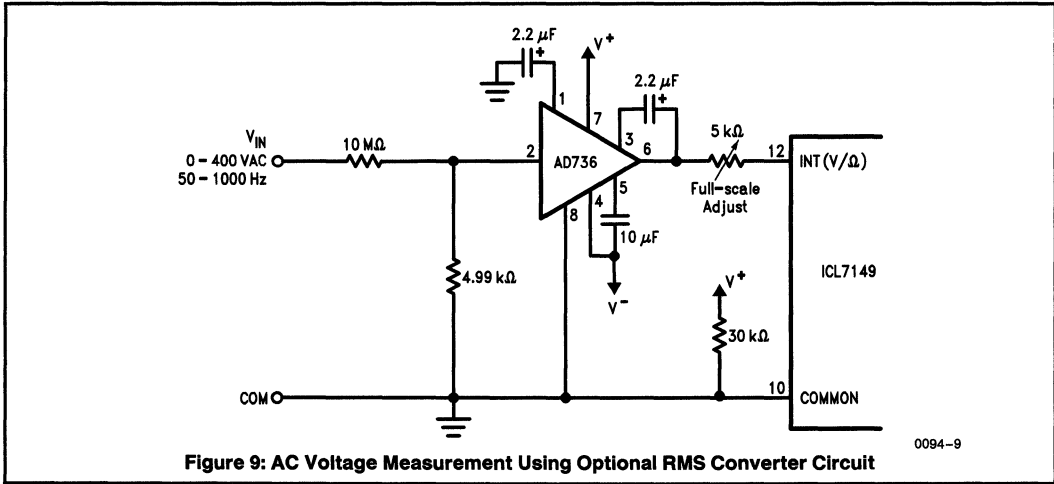
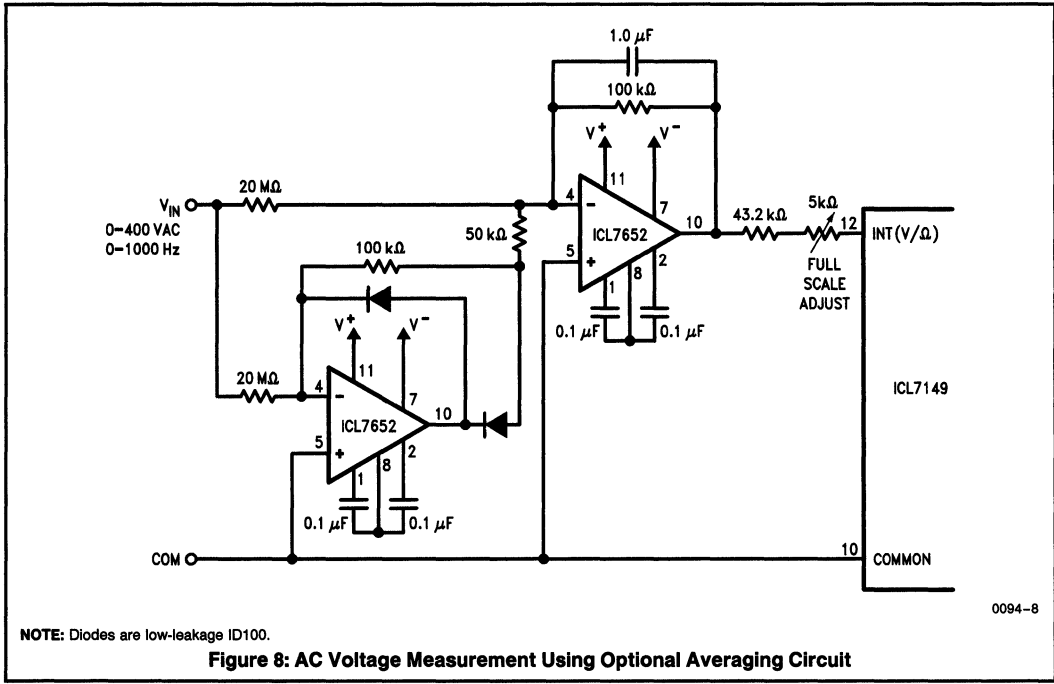


Figure 7: Detailed Circuit Diagram for DC Current Measurement

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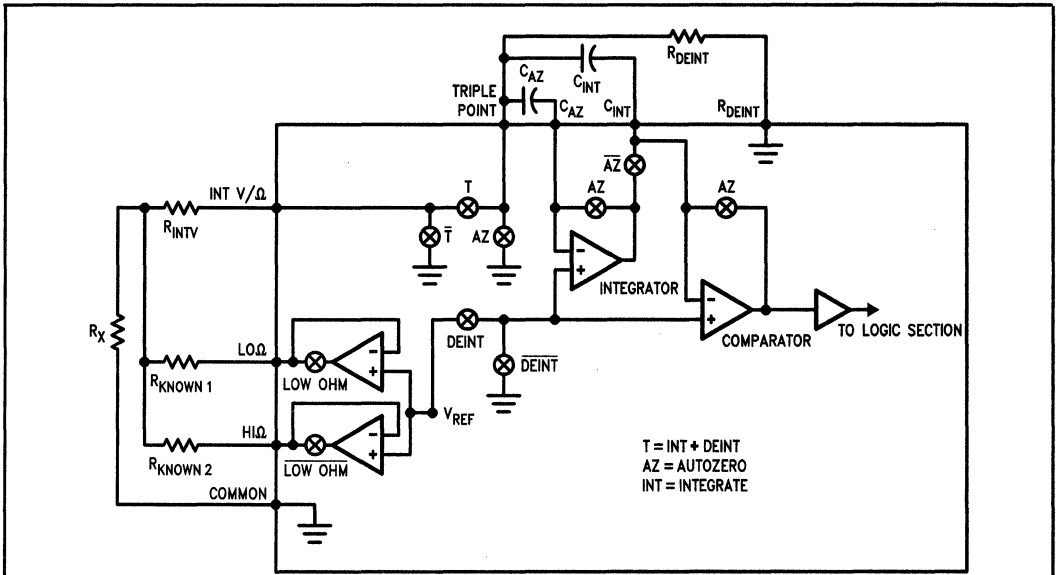


Figure 10: Detailed Circuit Diagram for Ratiometric Ohms Measurement

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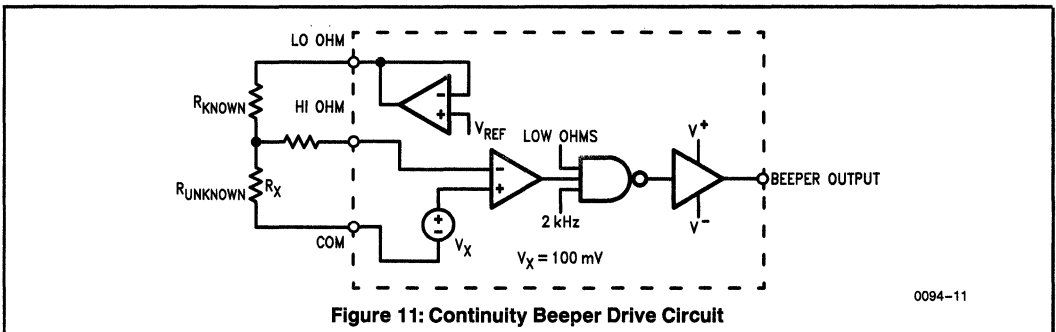


Figure 11: Continuity Beeper Drive Circuit

0094-11

NOTE: The ICL7139 contains a comparator that is enabled on the lowest ohms range. It trips at approximately 1/4 of the full scale value of that range and enables the beeper driver to oscillate (between V⁻ and V⁺) at 2 kHz. The beeper driver is capable of driving a piezo-electric transducer. The beeper output response is independent of the state of the conversion; therefore appears instantaneous to the user. Some applications may require a 150 pF capacitor between pin 4 and pin 8 to insure a sharp on/off continuity detection.

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Integrator Resistors

The normal values of the $R_{INT V}$ and $R_{INT I}$ resistors are 10 megohms and 1 megohm respectively. Though their absolute values are not critical, unless the value of the current sensing resistors are trimmed, their ratio should be 10:1, within 0.05%. Some carbon composition resistors have a large voltage coefficient which will cause linearity errors on the 400V scale. Also, some carbon composition resistors are very noisy. The class "A" output of the integrator begins to have nonlinearities if required to sink more than 70 μA (the sourcing limit is much higher). Because $R_{INT V}$ drives a virtual ground point, the input impedance of the meter is equal to $R_{INT V}$.

Deintegration Resistor, R_{DEINT}

Unlike most dual-slope A/D converters, the ICL7149 uses different resistors for integration and deintegration. R_{DEINT} should normally be the same value as $R_{INT V}$, and have the same temperature coefficient. Slight errors in matching may be corrected by trimming the reference voltage.

Autozero Capacitor, C_{AZ}

The C_{AZ} is charged to the integrator's offset voltage during the autozero phases, and subtracts that voltage from the input signal during the integrate phases. The integrator thus appears to have zero offset voltage. Minimum C_{AZ} value is determined by: 1) Circuit leakages; 2) C_{AZ} self-discharge; 3) Charge injection from the internal autozero switches. To avoid errors, the C_{AZ} voltage change should be less than $1/10$ of a count during the 10,000 count clock cycle integration period for the 400 mV range. These requirements set a lower limit of 0.047 μF for C_{AZ} but 0.1 μF is the preferred value. The upper limit on the value of C_{AZ} is set by the time constant of the autozero loop, and the line cycle time period allotted to autozero. C_{AZ} may be several 10s of microfarads before approaching this limit.

The ideal C_{AZ} is a low leakage polypropylene or Teflon capacitor. Other film capacitors such as polyester, polystyrene, and polycarbonate introduce negligible errors. If a few seconds of settling time upon power-up is acceptable, the C_{AZ} may be a ceramic capacitor, provided it does not have excessive leakage.

Ohms Measurement Resistors

Because the ICL7149 uses a ratiometric ohms measurement technique, the accuracy of ohms reading is primarily determined by the absolute accuracy of the R_{KNOWN1} and R_{KNOWN2} . These should normally be 10 kilohms and 1 megohm, with an absolute accuracy of at least 0.5%.

Current Sensing Resistors

The 0.1 ohm and 9.9 ohm current sensing resistors convert the measured current to a voltage, which is then measured using $R_{INT I}$. The two resistors must be closely matched, and the ratio between $R_{INT I}$ and these two resistors must be accurate—normally 0.5%. The 0.1 ohm resistor must be capable of handling the full scale current of 4 amps, which requires it to dissipate 1.6 watts.

Continuity Beeper

The Continuity Beeper output is designed to drive a piezoelectric transducer at 2 kHz (using a 120 kHz crystal), with a voltage output swing of V^+ to V^- . The beeper output off state is at the V^+ rail. When crystals with different frequencies are used, the frequency needed to drive the transducer can be calculated by dividing the crystal frequency by 60.

Display

The ICL7149 uses a custom, duplexed drive display with range, polarity, and low battery annunciators. With a 3 volt peak display voltage, the RMS ON voltage will be 2.37V minimum; RMS OFF voltage will be 1.06V maximum. Because the display voltage is not adjustable, the display should have a 10% ON threshold of about 1.4V. Most

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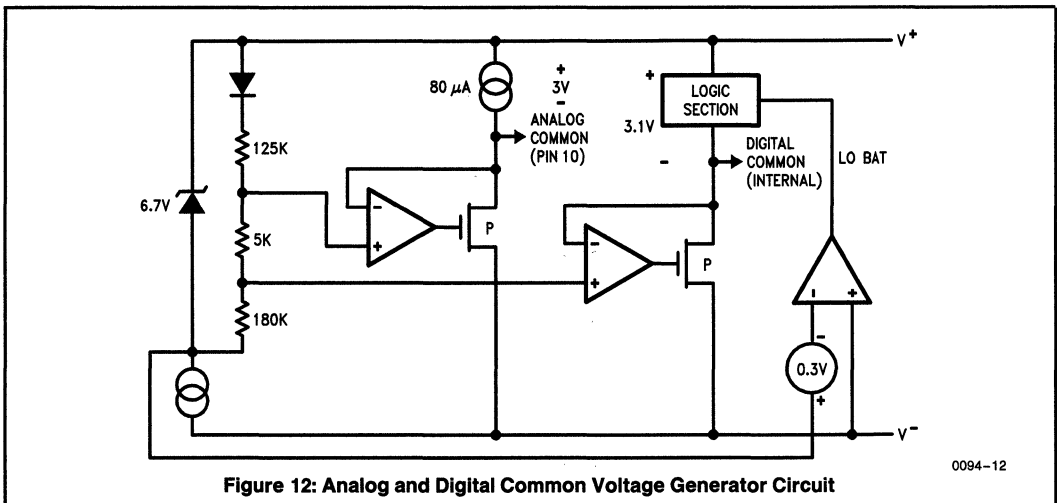


Figure 12: Analog and Digital Common Voltage Generator Circuit

0094-12

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display manufacturers supply a graph that shows contrast versus RMS drive voltage. This graph can be used to determine what the contrast ratio will be when driven by the ICL7149. Most display thresholds decrease with increasing temperature, and the threshold at the maximum operating temperature should be checked to ensure that the "off" segments will not be turned "on" at high temperatures.

Crystal

The ICL7149 is designed to use a parallel resonant 120 kHz or 100 kHz crystal with no additional external components. The R_S parameter should be less than 25 kilohms to ensure oscillation. Initial frequency tolerance of the crystal can be a relatively loose 0.05%

Switches

Because the logic input draws only about 5 μA , switches driving these inputs should be rated for low current, or "dry" operations. The switches on the external inputs must be able to reliably switch low currents, and be able to handle voltages in excess of 400V AC.

Reference Voltage Source

A voltage divider connected to V^+ and Common is the simplest source of reference voltage. While minimizing external component count, this approach will provide the same voltage tempco as the ICL7149 Common—about 100 PPM/ $^{\circ}C$. To improve the tempco, an ICL8069 bandgap reference may be used (see Figure 15). The reference voltage source output impedance must be $\leq R_{DEINT}/4000$.

Applications, Examples, and Hints

A complete autoranging 3 $\frac{3}{4}$ digit multimeter is shown in Figure 16. The following sections discuss the functions of specific components and various options.

Meter Protection

The ICL7149 and its external circuitry should be protected against accidental application of 110/220V AC line voltages on the ohms and current ranges. Without the necessary precautions, both the 7149 and its external components could be damaged under such fault conditions. For the current ranges, fast-blow fuses should be used between S5A in Figure 16 and the 0.1 ohm and 9.9 ohm shunt resistors. For the ohms ranges, no additional protection circuitry is required. However, the 10 kilohm resistor connected to pin 7 must be able to dissipate 1.2W or 4.8W for short periods of time during accidental application of 110V or 220V AC line voltages respectively.

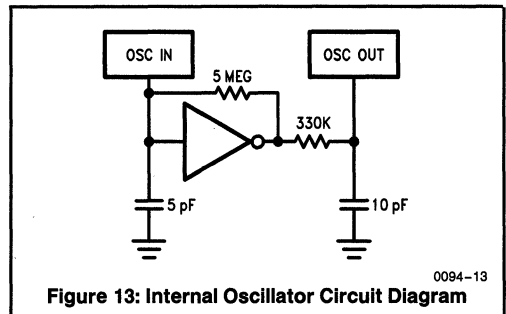
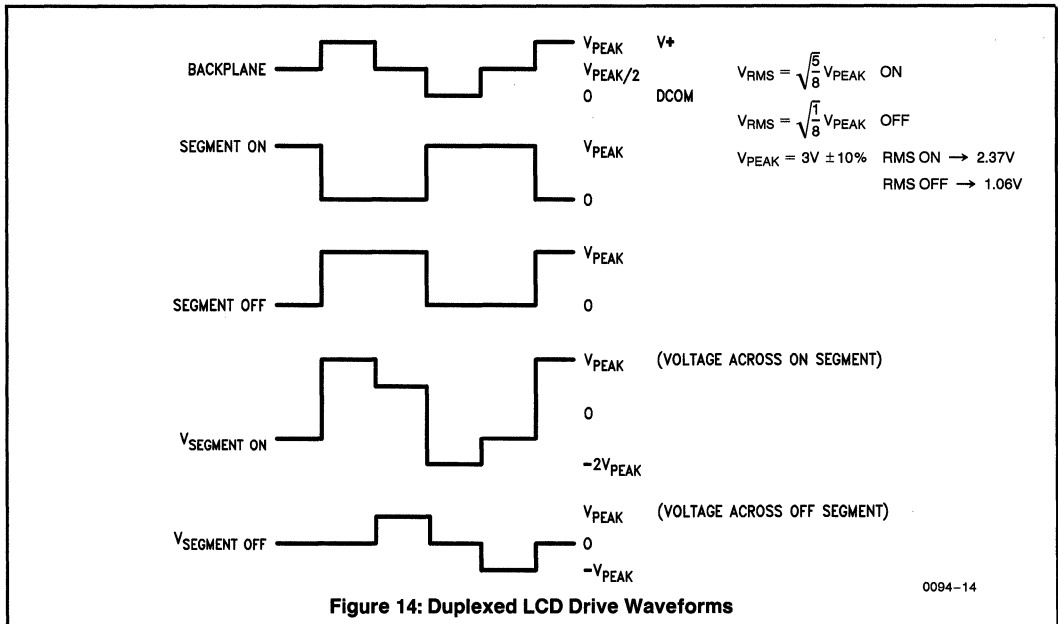


Figure 13: Internal Oscillator Circuit Diagram



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Printed Circuit Board Layout Considerations

Particular attention must be paid to rollover performance, leakages, and guarding when designing the PCB for a ICL7149-based multimeter.

Rollover Performance, Leakages, and Guarding

Because the ICL7139 system measures very low currents, it is essential that the PCB have low leakage. Boards should be properly cleaned after soldering. Areas of particular importance are: 1) The INT V/ Ω and INT I Pins; 2) The Triple Point; 3) The R_{DEINT} and the C_{AZ} pins.

The conversion scheme used by the ICL7139 changes the common mode voltage on the integrator and the capacitors C_{AZ} and C_{INT} during a positive deintegrate cycle. Stray capacitance to ground is charged when this occurs, removing some of the charge on C_{INT} and causing rollover error. Rollover error increases about 1 count for each picofarad of capacitance between C_{AZ} or the Triple Point and ground, and is seen as a zero offset for positive voltages. Rollover error is not seen as gain error.

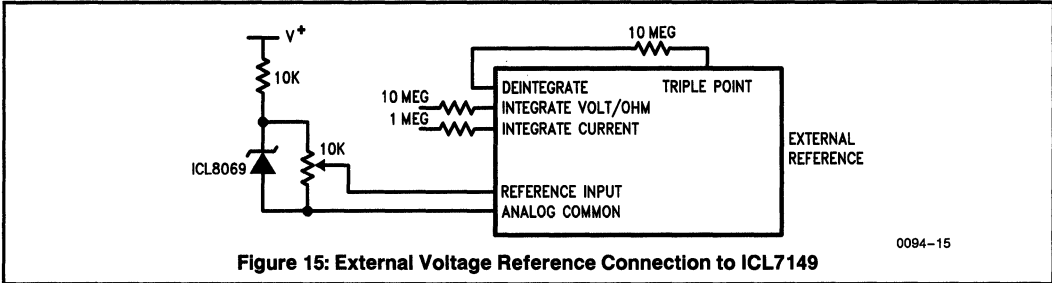
The rollover error causes the width of the +0 count to be larger than normal. The ICL7139 will thus read zero until several hundred microvolts are applied in the positive direction. The ICL7139 will read -1 when approximately -100 μ V are applied.

The rollover error can be minimized by guarding the Triple Point and C_{AZ} nodes with a trace connected to the C_{INT} pin, which is driven by the output of the integrator. Guarding these nodes with the output of the integrator reduces the stray capacitance to ground, which minimizes the charge error on C_{INT} and C_{AZ}. If possible, the guarding should be used on both sides of the PC board.

Stray Pickup

While the ICL7149 has excellent rejection of line frequency noise and pickup in the DC ranges, any stray coupling will affect the AC reading. Generally, the analog circuitry should be as close as possible to the ICL7149. The analog circuitry should be removed or shielded from any 120V AC power inputs, and any AC sources such as LCD drive waveforms. Keeping the analog circuit section close to the ICL7149 will also help keep the area free of any loops, thus reducing magnetically coupled interference coming from power transformers, or other sources.

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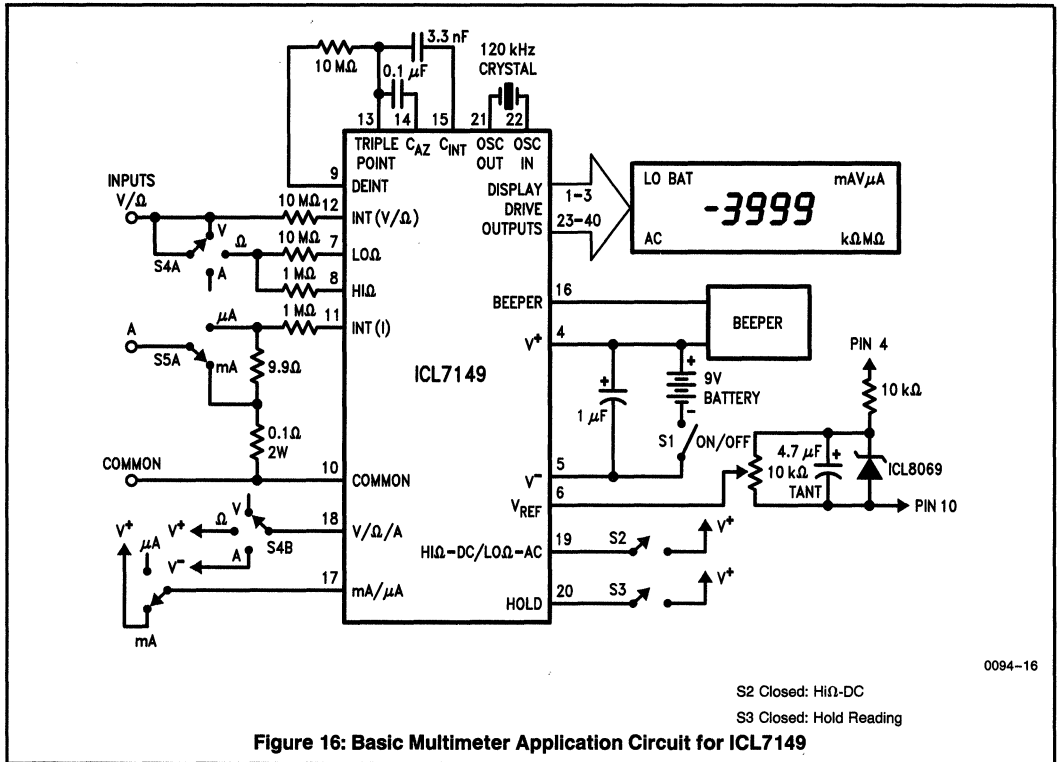


Figure 16: Basic Multimeter Application Circuit for ICL7149

- NOTE 1: Crystal is a Statek CX-1V type.
 2: Multimeter protection components have not been shown.
 3: Display is from LXD, part number 38D3R02H.
 4: Beeper is from muRata, part number PKM24-4A0.

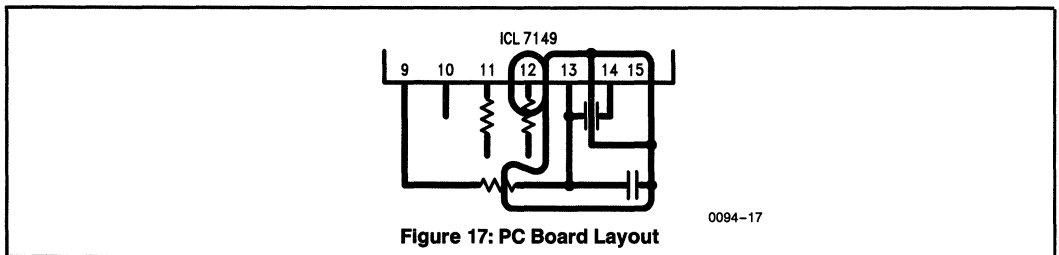


Figure 17: PC Board Layout

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ICL7182

101 Segment LCD Bargraph A/D Converter



ICL7182

GENERAL DESCRIPTION

The Intersil ICL7182 is a complete analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Included are a charge-balanced ADC, a 2.56V bandgap reference, display decode and driver, and a 50 kHz oscillator. Only a display and three passive components are required for a complete analog bargraph.

The fully differential analog and reference inputs may be operated anywhere between and including the supply rails. This allows sensing either ground-referenced signals or bridge configurations. Linearity and zero offset errors are guaranteed to be less than 0.5% for a 1V full-scale input. The full-scale differential input range is 200 mV to 1.1V.

The low drift 50 ppm/°C reference is trimmed to 1.5% accuracy and, when used with a simple resistor divider, can set the full-scale input voltage. The reference, when used with an Intersil ICL7660, extends the operating supply range from 3V to 40V and allows sensing input signals below ground.

The backplane and segment drivers supply the LCD with the proper waveforms to create a discrete series of segments forming a 101 segment bar which is proportional to the input voltage, with a plus or minus annunciator to indicate the polarity. In addition, three independent TTL controllable annunciators are provided for limit or unit indication. The bargraph multiplexing scheme provides duplex contrast ratio and allows the complete system to be placed in a standard 40 pin DIP. The LCD operating voltage is externally set to adjust contrast for a range of fluid types and temperature.

The internal oscillator requires no external components and establishes the conversion rate and backplane clock frequency. The nominal conversion rate of 25 per second can be easily changed between 15 to 40 conversions per second by adding a single capacitor or overdriving the oscillator.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7182CPL	0°C to +70°C	40 Pin Plastic
ICL7182IPL	-25°C to +85°C	40 Pin Plastic
*ICL7182CM44	0°C to +70°C	44 Pin Plastic

*Consult factory for details.

PRELIMINARY
Subject To Change Without Notice

FEATURES

- 1% Resolution . . . 100 Data Segments Plus Zero
- No Missing Segments Guaranteed
- Single 5V Supply Operation
- Only Three Passive Components Required
- True Differential Input and Reference
- Direct LCD Display Drive Provides Duplex Contrast Ratio
- Overrange and Polarity Indication
- Three User Defined Annunciators—Easily Expandable
- Precision On-Chip Reference . . . 50 ppm/°C
- Low Average Power Consumption . . . 1.8 mW
- 40 Pin DIP or 44 Pin Surface Mount Package
- Extended Temperature Range Operation

2

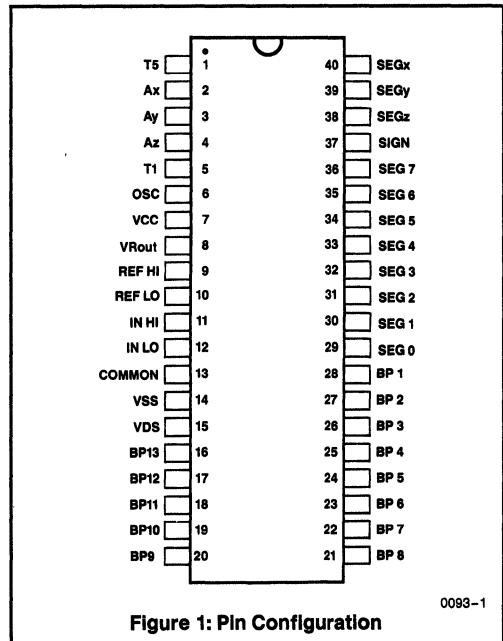


Figure 1: Pin Configuration

0093-1

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{SS}) 10V
 Supply Voltage (V_{CC} to V_{DS}) 11V
 Display Drive Pin Voltage ($V_{CC} + 0.3V$) to ($V_{DS} - 0.3V$)
 Analog or Reference Inputs ($V_{CC} + 0.3V$) to ($V_{SS} - 0.3V$)
 Com, Osc, Ax, Ay,
 Az, T1, T5 Pins ($V_{CC} + 0.3V$) to ($V_{SS} - 0.3V$)
 Reference Output Current 8 mA
 Lead Temperature (Soldering, 10 sec) 300°C
 Storage Temperature Range -65°C to +150°C

Operating Temperature Range -25°C to +85°C
 Continuous Total Power Dissipation ($T_A = 25^\circ\text{C}$)
 40 Pin DIP Plastic Package 500 mW
 44 Pin CM Plastic Package 375 mW

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $V_{CC} = 5.0V$, $V_{SS} = V_{DS} = \text{GND}$, $T_A = 25^\circ\text{C}$,

$V_{REF} = 1.000V$, $V_{INCM} = V_{REFCM} = 2.5V$, pin 6 open (Note 1)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
Zero Input Reading	$V_{IN} = 0.0V$	-0	± 0	+0	Segs
Unadjusted Gain Error	$V_{IN} = V_{REF}$	-1	± 0	+1	Segs
Linearity Error	(Note 2)	-0.63	± 0.2	+0.63	Segs
Rollover Error	$V_{IN} = -V_{REF}$ (Note 3)	-0.5	± 0.1	+0.5	Segs
Conversion Time			400		μs
Display Update Rate			25		Hz
Input Referred Noise	(Note 4)		500		μV
DC Power Supply Rejection	$V_{CC} = 4.5$ to $6.0V$		0.02	0.3	Segs/V
ANALOG INPUT					
Common Mode Rejection Ratio	$V_{INCM} = 0V$ to $5V$, $V_{IN} \approx 0V$		0.02	0.1	Segs/V
Differential Mode Input			1.0	1.1	V
Average Input Current	$V_{IN} = 1.0V$ (Note 5)		1.3		nA
REFERENCE INPUT					
Common Mode Rejection Ratio	$V_{REFCM} = 0.5V$ to $4.5V$		0.01	0.1	Segs/V
Average Input Current	(Note 6)		6		nA
REFERENCE OUTPUT					
Output Voltage	$V_{CC} - V_{Rout}$, $I_{out} = 0 \mu\text{A}$	2.520	2.560	2.590	V
Temperature Coefficient	-25°C < T_A < 85°C, $I_{out} = 0 \mu\text{A}$		50	200	ppm/°C
Output Impedance	$I_{out} = +10 \mu\text{A}$ to -2mA		1.3	5	Ω
Current Into VRout Pin		10	20		μA
Current Out of VRout			8	2	mA
Output Noise	0.1 Hz to 10 Hz (Note 4)		110		μV
POWER SUPPLY					
Supply Current Average	(Note 6)		350	500	μA
Supply Current Peak	(Note 6)		1.5	2.0	mA
Supply Voltage Range	Guaranteed by PSRR	4.5	5.0	6.0	V
OSCILLATOR					
Oscillator Frequency	Osc Pin Open	26	51	72	kHz
Backplane Frequency	Osc Pin Open	25	50	70	Hz
DISPLAY DRIVE					
Display Output Impedance	$V_{CC} - V_{DS} = 3V$ to $7V$		70	200	k Ω
DC Component of Display	$V_{CC} - V_{DS} = 3V$ to $7V$	-50	± 10	50	mV
V_{DS} Supply Current	$V_{CC} - V_{DS} = 3V$ to $7V$ (Note 7)		60	120	μA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise stated: $V_{CC} = 5.0V$, $V_{SS} = V_{DS} = GND$, $T_A = 25^\circ C$, $V_{REF} = 1.000V$, $V_{INCM} = V_{REFCM} = 2.5V$, pin 6 open (Note 1)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
ANNUNCIATOR INPUTS					
Input High Voltage	Operating Temp Range	2.4			V
Input Low Voltage	Operating Temp Range			0.8	V
Input Leakage	Operating Temp Range	-1	0.001	+1	μA

NOTE 1: The differential mode input voltages are defined as: $V_{IN} = (IN\ HI - IN\ LO)$ and $V_{REF} = (REF\ HI - REF\ LO)$. The common mode input voltage, V_{INCM} and V_{REFCM} , is defined as the average differential input voltage with respect to ground.

- 2: The linearity error is the deviation from a straight line which passes through negative full scale and positive full scale readings.
- 3: The rollover error is defined as the difference in reading for equal positive and negative inputs near full-scale.
- 4: Peak to peak value not exceeded 95% of the time (± 2 standard deviations).
- 5: Defined as the average current flowing into the input with a 1.0 μF capacitor across V_{IN} or V_{REF} inputs and the common mode voltage at $\frac{1}{2} V_{CC}$.
- 6: The average supply current is measured with a supply bypass capacitor and annunciator inputs tied to V_{SS} .
- 7: The supply current for V_{DS} flows from the V_{CC} pin.

PIN DESCRIPTION AND FUNCTION

Pin No.	Symbol	Description
1	T5	Test pin #5, buffered oscillator frequency divided by two that can typically source and sink 2 mA.
2	Ax	Annunciator Segx select, low turns on Segx, high turns off Segx.
3	Ay	Annunciator Segy select, low turns on Segy, high turns off Segy.
4	Az	Annunciator Segz select, low turns on Segz, high turns off Segz.
5	T1	Test pin #1, normally left open or tied to V_{SS} .
6	Osc	50 kHz free running oscillator control and clock input pin. The internal oscillator may be overdriven by a 30 to 80 kHz external clock driving pin 6, or the free running frequency can be reduced by adding an external capacitor between pin 6 and V_{CC} .
7	V_{CC}	Positive supply voltage.
8	VRout	Bandgap reference buffered output, down 2.56V from V_{CC} .
9	REF HI	Positive Reference Input.
10	REF LO	Negative Reference Input.
11	IN HI	Positive Analog Input.
12	IN LO	Negative Analog Input.
13	Common	Internally generated voltage which is typically within ± 50 mV of $\frac{1}{2} (V_{CC} - V_{SS})$ and has 1.4 k Ω output impedance. This pin is normally left open or bypassed with a 0.1 μF capacitor to signal ground.
14	V_{SS}	Negative supply voltage, normally ground.
15	V_{DS}	Display negative voltage, establishes the pk-pk display drive.
16-28	BP13-BP1	LCD backplane drivers.
29-36	Seg0-Seg7	LCD segment drivers.
37	Sign	Positive sign segment driver.
38	Segz	Annunciator driver selected by Az.
39	Segy	Annunciator driver selected by Ay.
40	Segx	Annunciator driver selected by Ax.

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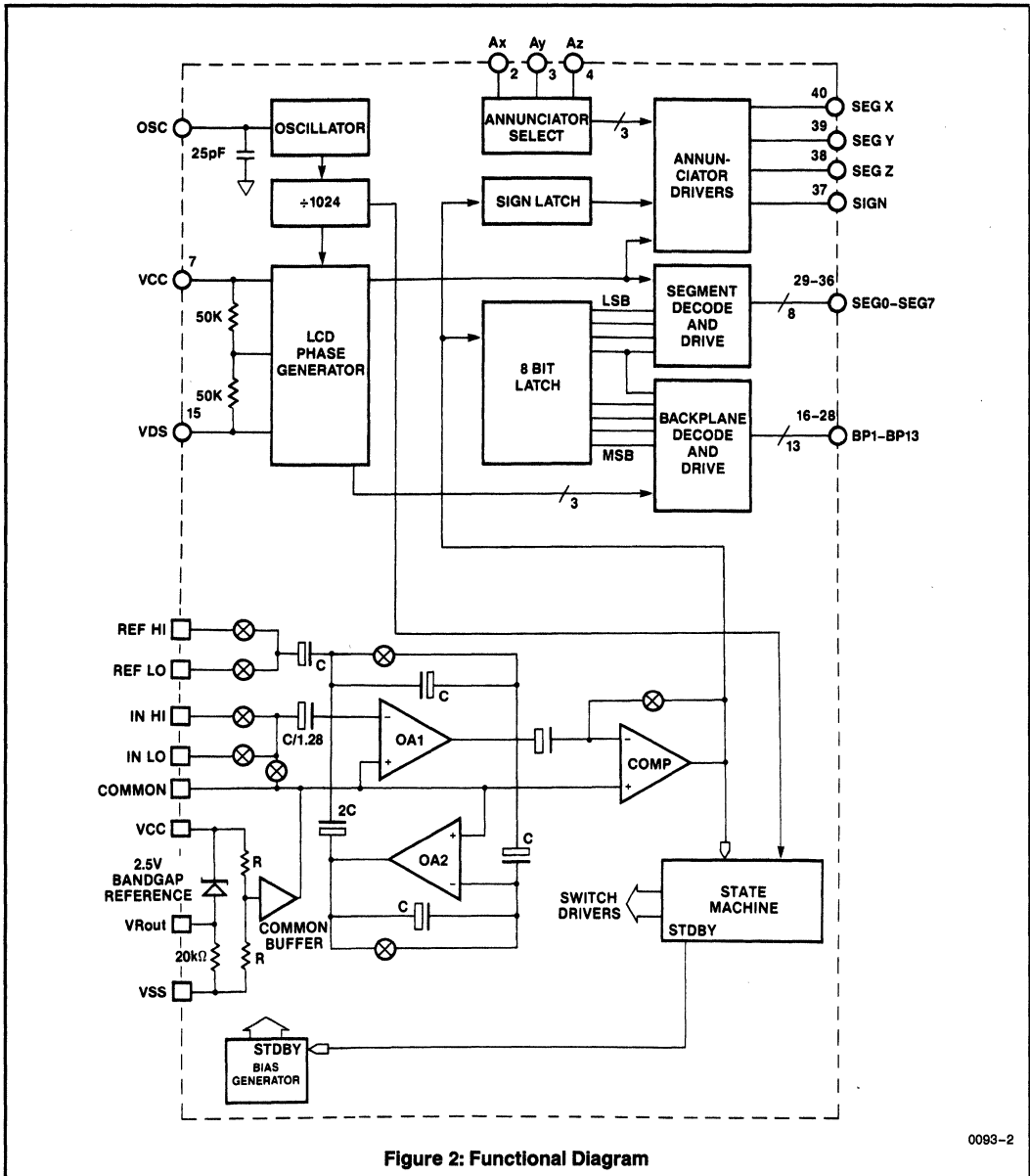


Figure 2: Functional Diagram

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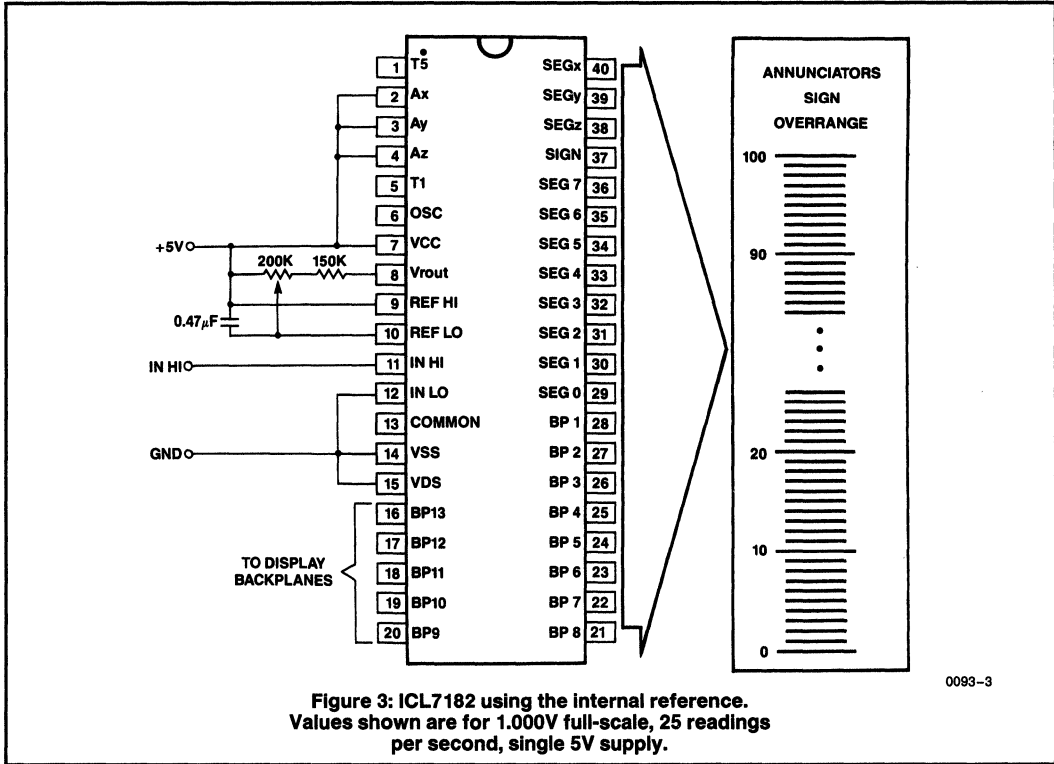
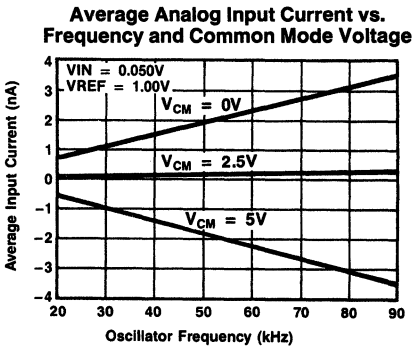


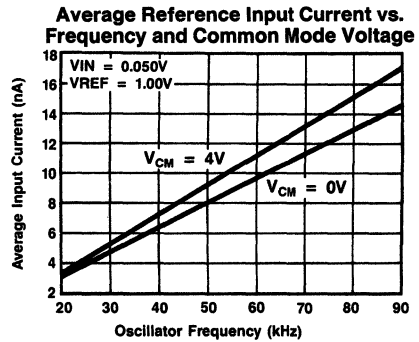
Figure 3: ICL7182 using the internal reference. Values shown are for 1.000V full-scale, 25 readings per second, single 5V supply.

0093-3

TYPICAL PERFORMANCE CHARACTERISTICS



0093-4

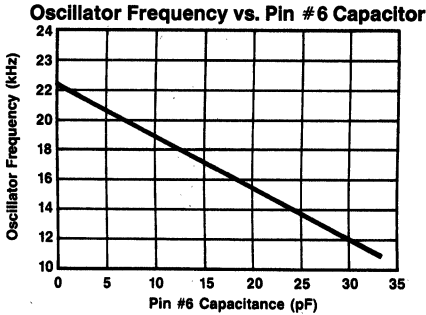


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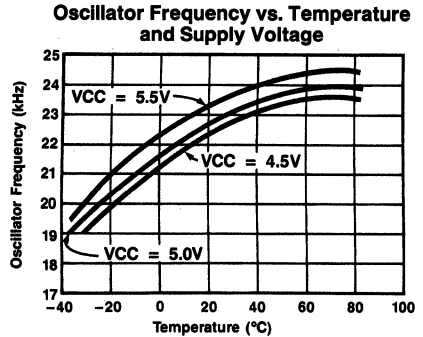
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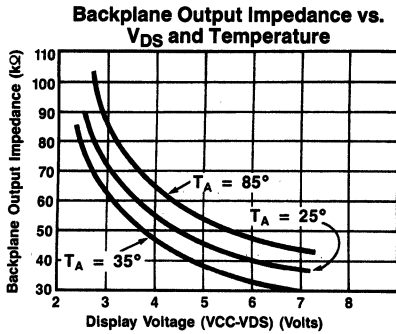
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



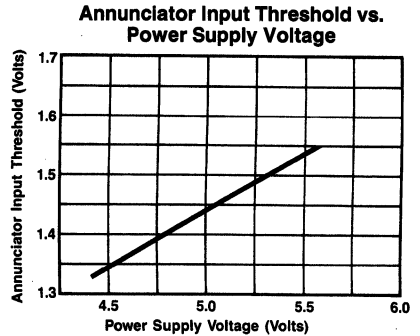
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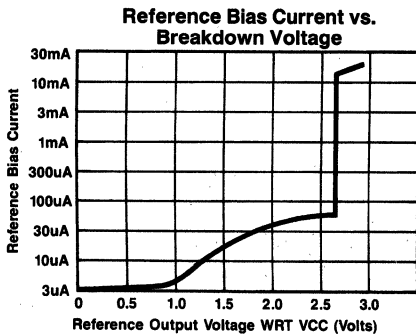
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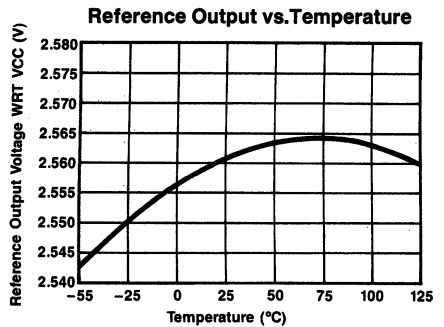
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0093-9



0093-10



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NOTE: All typical values have been characterized but are not tested.

FUNCTIONAL DESCRIPTION

A functional diagram of the ICL7182 A/D converter is shown in Figure 2. The device operates on the cyclic converter principle implemented with switched capacitor amplifiers. Analog switches are closed sequentially by state machine control logic to sample the input and perform a multi-by-two and delay function. The sampled input charge is recirculated and compared to the reference to determine the weight of each bit. The sign is determined first and after 18 cycles a 9-bit binary code is latched and the display is updated.

Under normal operation the conversion requires 32 clock cycles and the display updates once every 2048 clock cycles. Before and during the conversion the supply current for the analog section increases from typically 300 μ A to 1.3 mA and remains high for a total of 96 clock cycles. The operation proceeds as follows:

Clock Cycle	Operation
0-96	Supply current increases from 300 μ A to 1.3 mA
0-47	Converter autozero begins
48	IN LO is sampled
49	IN HI is sampled
50-70	REF LO and REF HI are sampled once per clock cycle
75-77	Converter output is latched and display is updated
96-2048	Supply current decreases from 1.3 mA to 300 μ A
2048	New conversion begins

The changing supply current may result in a noisy reading if the supply dynamic impedance is high. This can be resolved by using a supply bypass capacitor.

Analog Inputs

The analog and reference inputs are guaranteed to correctly operate within the supply voltage. Both inputs will continue to function 200 mV to 400 mV outside of the supplies but the converter specifications degrade as the input protection diodes become forward biased.

As the reference and analog inputs are sampled, transient currents flow from the inputs to charge small internal capacitors.

These transient currents occur at the leading edge of the internal clock and decay at a rate determined by the input capacitance of the converter and the source resistance. Source resistances larger than R_s given in the equation below will cause conversion errors.

$$R_s (\text{max}) = \frac{1}{6 (F_{osc}) (C_{in})}$$

Where: F_{osc} = Oscillator frequency

C_{in} = 40 pF, typical input capacitance

R_s = Source resistance

Input Bypass Capacitor

For source resistances larger than R_s above (typically 80 k Ω) bypass capacitors across the inputs will average these charging currents and cause a small DC current to flow through the output resistance of the analog and reference source signals. The average input current is a function of the common mode voltage and the oscillator frequency (see typical graphs). This current is typically 2 nA for the analog input and 6 nA for the reference input. The effects of the voltage drops across source resistances, due to the average value of input current, can be compensated by full-scale adjustment while the given source resistor and input bypass capacitor are in place.

Reference Output

The internal bandgap reference behaves like a 2.56V zener with the cathode tied to V_{CC} and the anode tied to V_{Rout} . The regulator circuitry maintains a low 1.3 Ω output impedance for bias currents through the zener between 90 μ A and 2 mA. At minimum supply voltage the internal 20 k Ω resistor will provide 10 μ A of current sink into V_{Rout} . The minimum sink current may be increased by adding an external resistor from V_{Rout} to V_{SS} .

The reference is internally trimmed to within 1.5% of 2.56V. The reference output can be externally divided (see Figure 3) to establish the full-scale input. Two fixed value resistors with 1% tolerance will relate to a system accuracy of 2% RMS.

With V_{Rout} pin tied to ground the reference becomes a shunt supply regulator for the ICL7182. Connections for this application are shown in the EV kit schematic, Figure 6.

2

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NOTE: All typical values have been characterized but are not tested.

Display Drive

The binary output of the A/D converter is encoded to drive 8 segments that serpentine across thirteen backplanes of an LCD display. The backplanes are driven with three level signals and the segment lines are driven with two level signals. The three levels of the backplane are set by the V_{CC} supply, the V_{DS} supply, and the output of a voltage divider which is connected between V_{CC} and V_{DS} . The two levels of the segment drive are set by the V_{CC} and V_{DS} supplies.

The bargraph takes advantage of the fact that above a particular segment all segments will be off and below that segment all segments will be on, also that only one backplane will have segments which are both on and off. The backplanes with all segments off are driven with an "off backplane" waveform, the backplanes with all segments on are driven with an "on backplane" waveform, and the one backplane with both on and off segments is driven with a "unique backplane" waveform. The off segments are driven with an off segment waveform and the on segments are driven with an on segment waveform with respect to the unique backplane. The sign segment and annunciator segment drives are designed for use with respect to BP1. The phasing between display waveforms is shown in Figure 4.

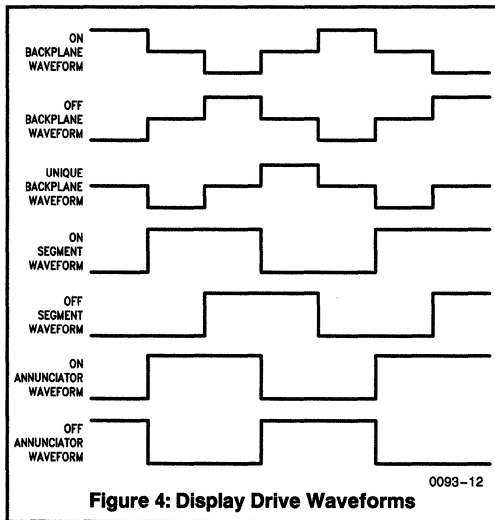


Figure 4: Display Drive Waveforms

The LCD segments appear ON when the RMS voltage between the backplane and segment drives is greater than the 90%-ON voltage of the LCD fluid, and they appear OFF when the RMS voltage is less than 10%-ON voltage of the LCD fluid. For the 1/2 multiplexed (duplex) waveforms used on the ICL7182 a 2.25:1 contrast ratio is achieved.

Display Set Voltage

The V_{DS} pin sets the peak-to-peak amplitude of the display drive waveforms. This voltage should be selected to give maximum contrast for a particular LCD fluid type and temperature. Good contrast ratio is obtained if V_{DS} is set within the range determined by the equation below.

$$(1.27)(V_{th90\%}) \leq (V_{CC} - V_{DS}) \leq (2.26)(V_{th10\%})$$

Where: $V_{th90\%}$ = 90% ON Visual Threshold

$V_{th10\%}$ = 10% ON Visual Threshold

For example the Hamlin Inc. type 02 LCD fluid has $V_{th90\%} = 3.05V$ and $V_{th10\%} = 2.2V$, therefore the best contrast is achieved when $V_{CC} - V_{DS}$ is set between 3.9V and 5V. For most applications where V_{CC} is tied to a +5V supply the V_{DS} pin can be tied to ground.

To accommodate a large range of temperatures and fluid types the V_{DS} pin can be driven above or below V_{SS} . The voltage difference between V_{CC} and V_{DS} can vary from from 3V to 7V. For $V_{CC} - V_{DS}$ less than 3V the output impedance of the backplane drivers increase substantially. The dependence of display drive output impedance on V_{DS} and temperature is shown in the typical performance curves.

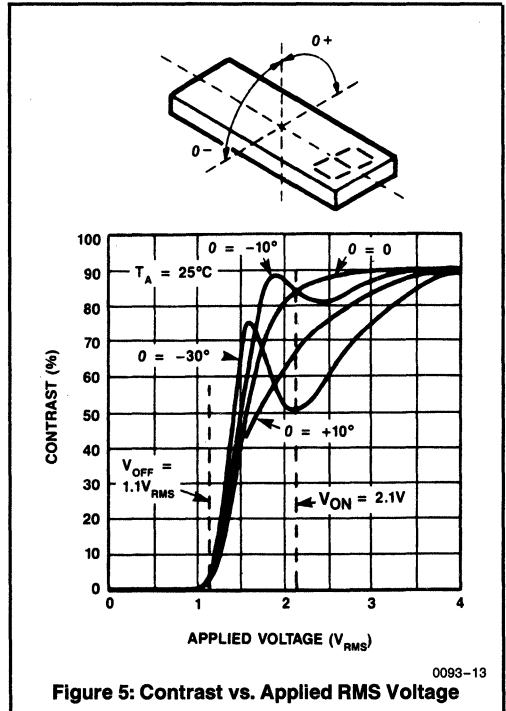


Figure 5: Contrast vs. Applied RMS Voltage

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Display Set Voltage (Continued)

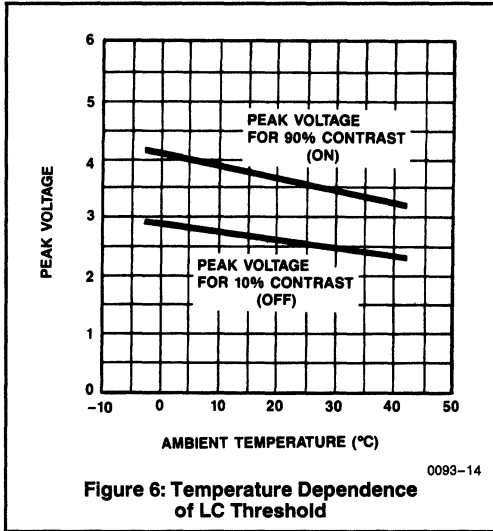


Figure 6: Temperature Dependence of LC Threshold

Temperature Effects and Temperature Compensation

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14 mV/ $^{\circ}\text{C}$. This means that as tem-

perature rises, the threshold voltage goes down. Assuming a fixed value for V_P , when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 6 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 5.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DJSP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

Display Voltage and Temperature Compensation

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 15. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 15 to V_{SS} as shown in Figure 7. A potentiometer with a maximum value of $100\text{ k}\Omega$ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than $\pm 5^{\circ}\text{C}$ ($\pm 9^{\circ}\text{F}$), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

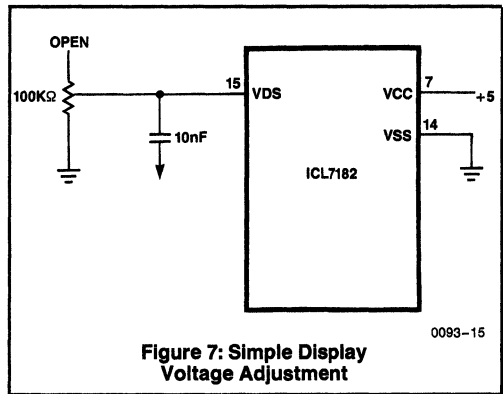


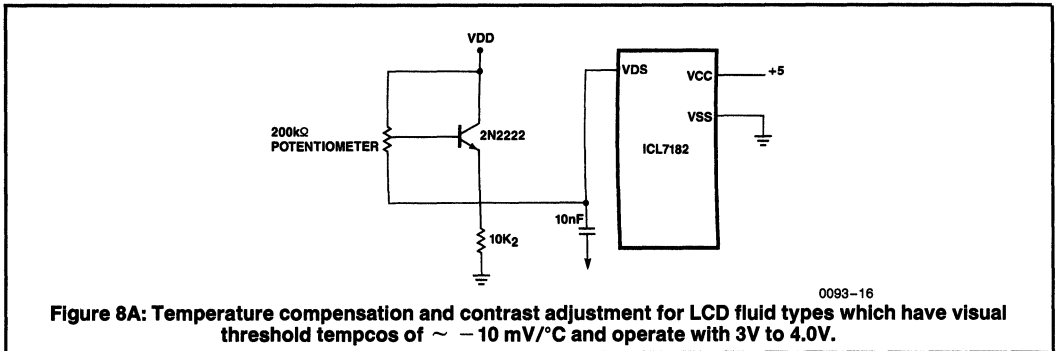
Figure 7: Simple Display Voltage Adjustment

2

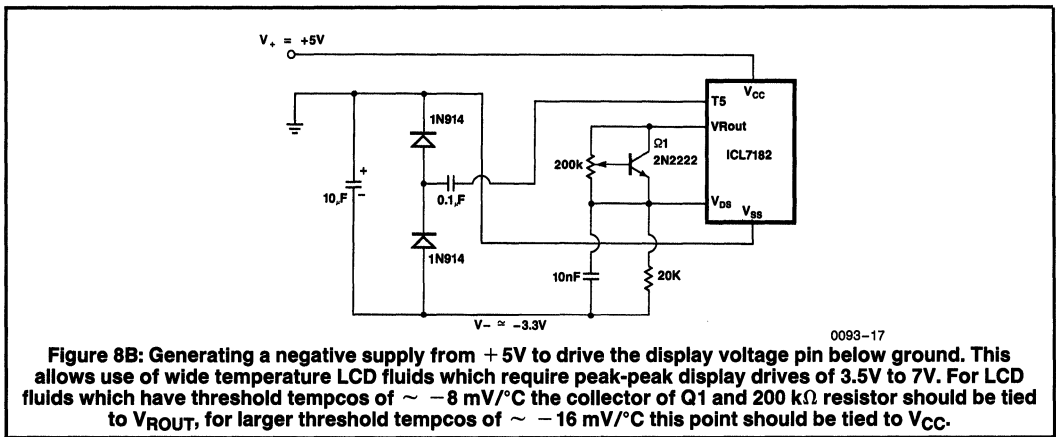
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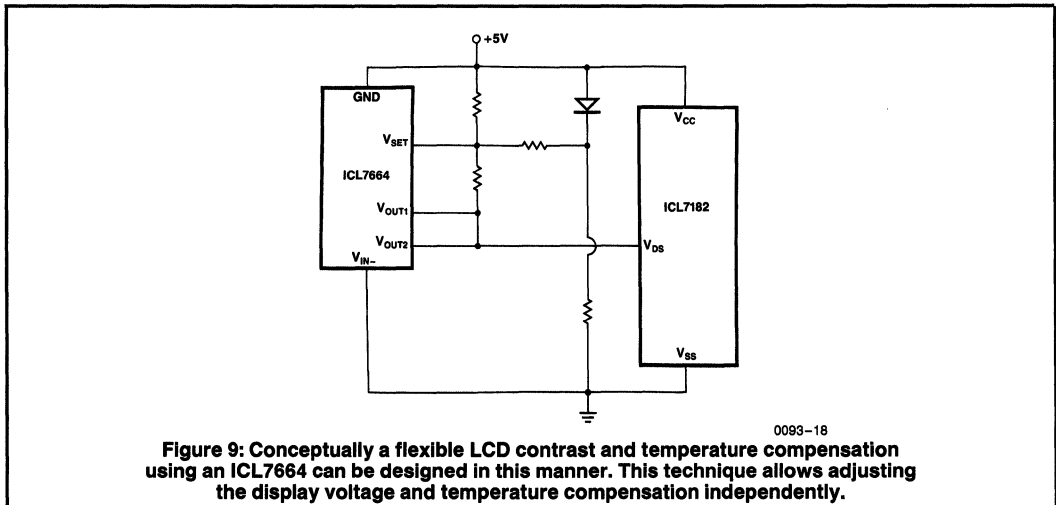
Display Set Voltage (Continued)



0093-16
Figure 8A: Temperature compensation and contrast adjustment for LCD fluid types which have visual threshold tempcos of ~ -10 mV/°C and operate with 3V to 4.0V.



0093-17
Figure 8B: Generating a negative supply from +5V to drive the display voltage pin below ground. This allows use of wide temperature LCD fluids which require peak-peak display drives of 3.5V to 7V. For LCD fluids which have threshold tempcos of ~ -8 mV/°C the collector of Q1 and 200 kΩ resistor should be tied to VROUT, for larger threshold tempcos of ~ -16 mV/°C this point should be tied to VCC.



0093-18
Figure 9: Conceptually a flexible LCD contrast and temperature compensation using an ICL7664 can be designed in this manner. This technique allows adjusting the display voltage and temperature compensation independently.

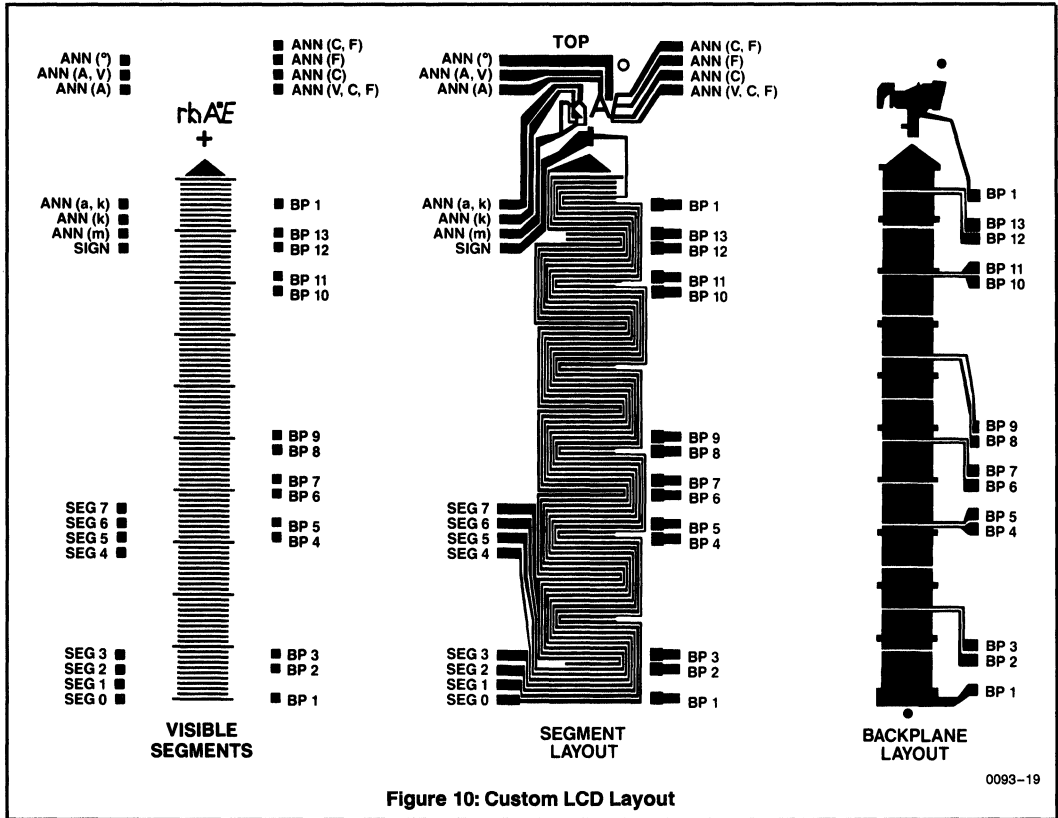
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NOTE: All typical values have been characterized but are not tested.

Display Layout

Custom displays developed for the ICL7182 need to be arranged such that the 8 segment lines serpentine across 13 backplanes. The annunciators and first eight data segments share a common backplane (BP1). An example layout is shown in Figure 10. This 1.3" by 4.5" display is available from Hamlin Inc. (part # 4464-363-921) for prototyping and evaluation.

Custom Display

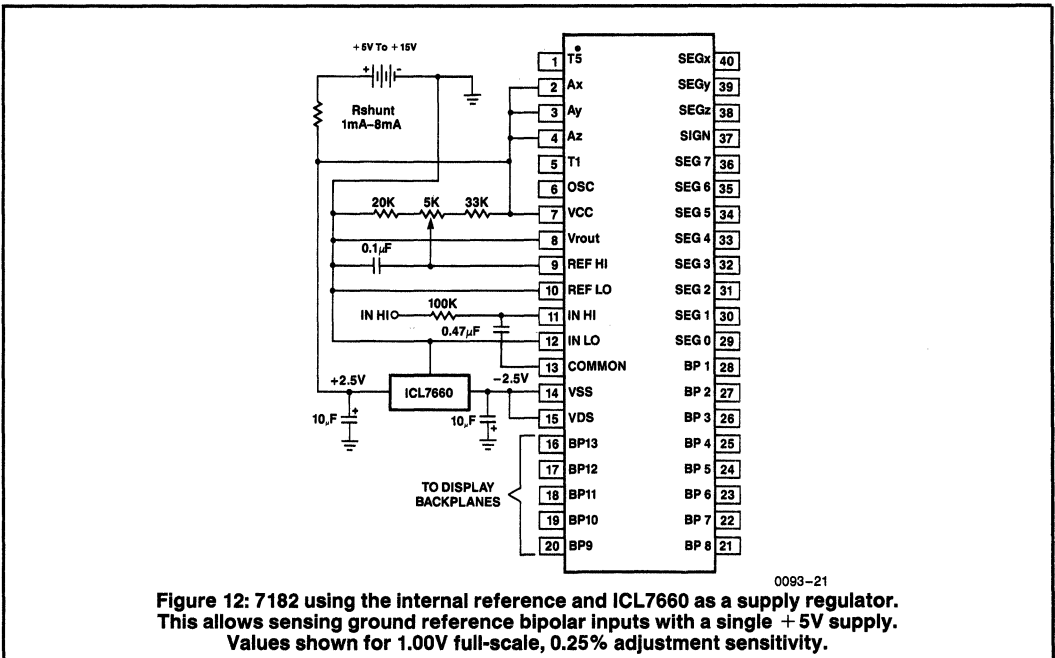
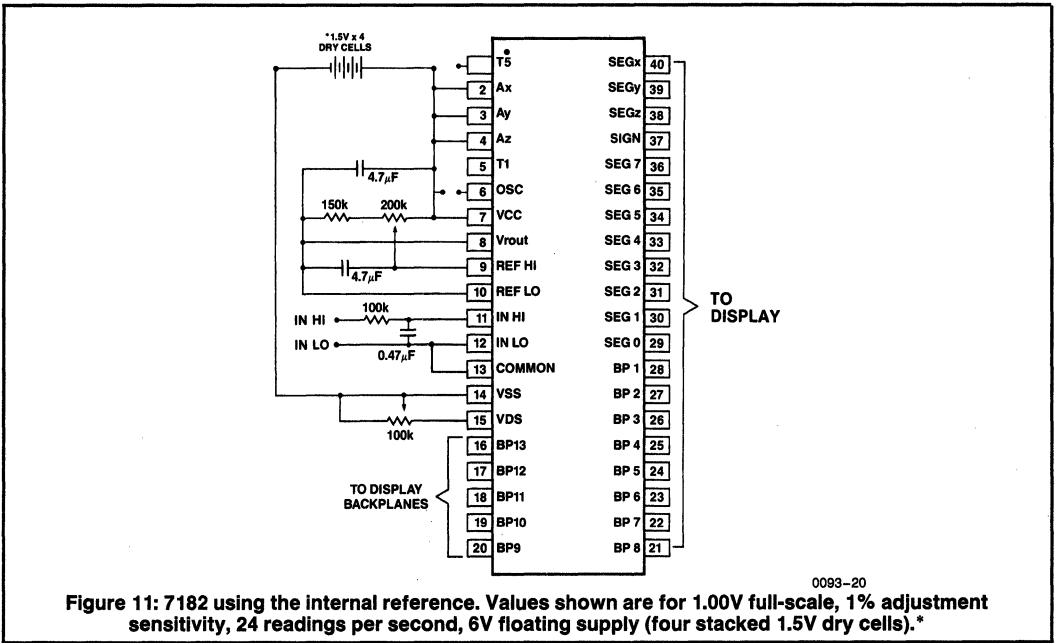


2

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS



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APPLICATIONS (Continued)

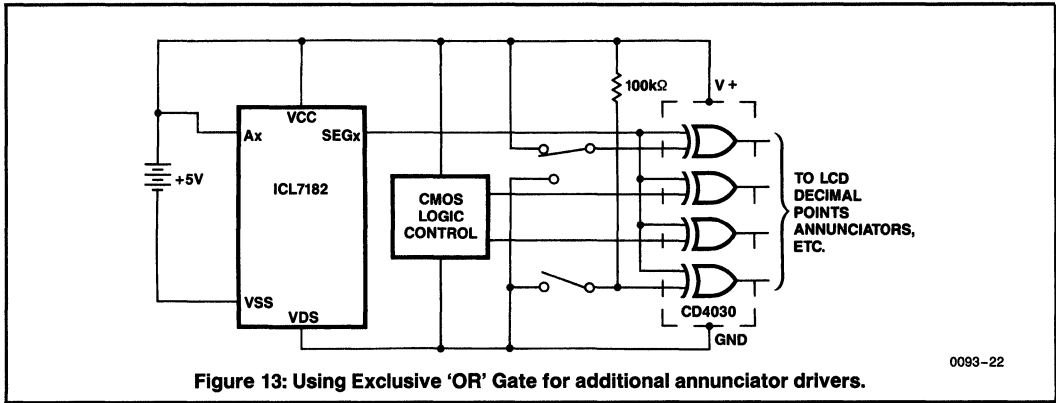


Figure 13: Using Exclusive 'OR' Gate for additional annunciator drivers.

0093-22

2

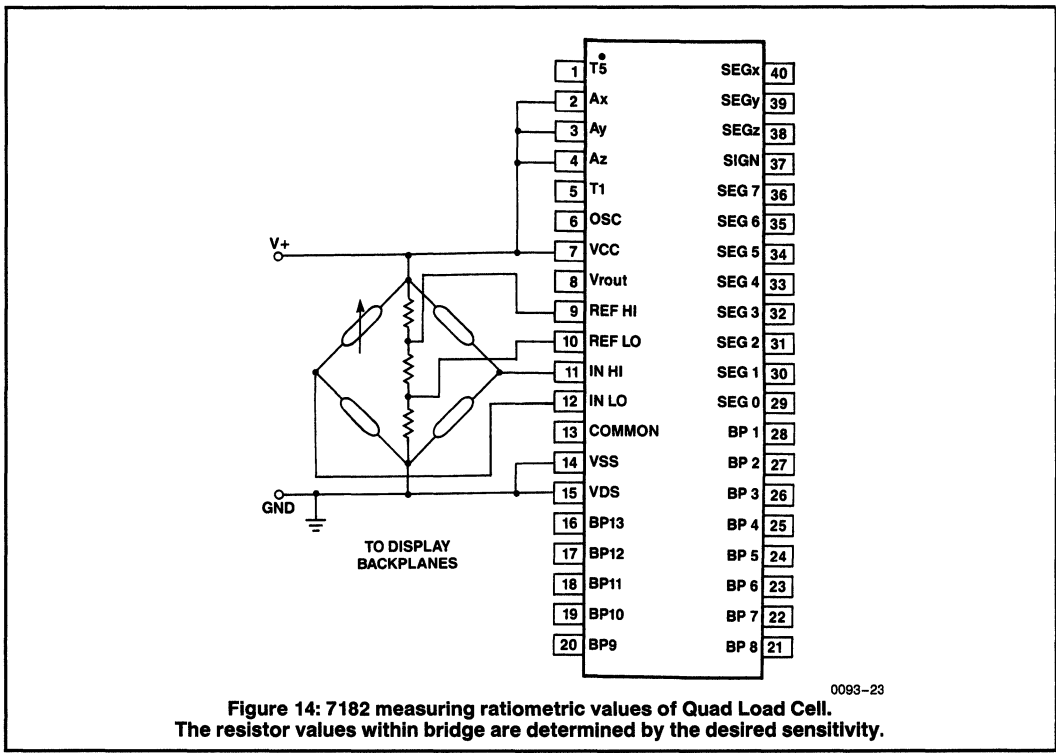


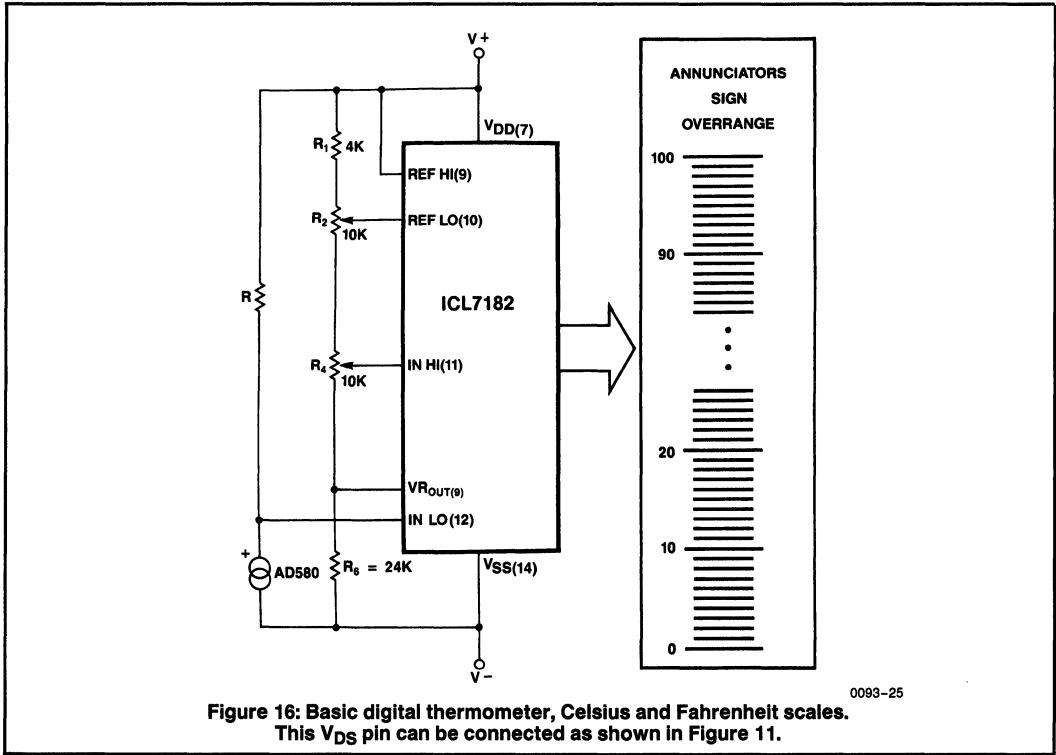
Figure 14: 7182 measuring ratiometric values of Quad Load Cell. The resistor values within bridge are determined by the desired sensitivity.

0093-23

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)



2

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NOTE: All typical values have been characterized but are not tested.

Section 3 — A/D Converters μ P Type

ADC0802	3-1
ADC0803	3-1
ADC0804	3-1
ICL7104/ICL8052	3-19
ICL7104/ICL8068	3-19
ICL7109	3-39
ICL7112	3-58
ICL7115	3-60
ICL7135	3-74

ADC0802 - ADC0804

8-Bit μ P-Compatible

A/D Converters



ADC0802-ADC0804

GENERAL DESCRIPTION

The ADC0802 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

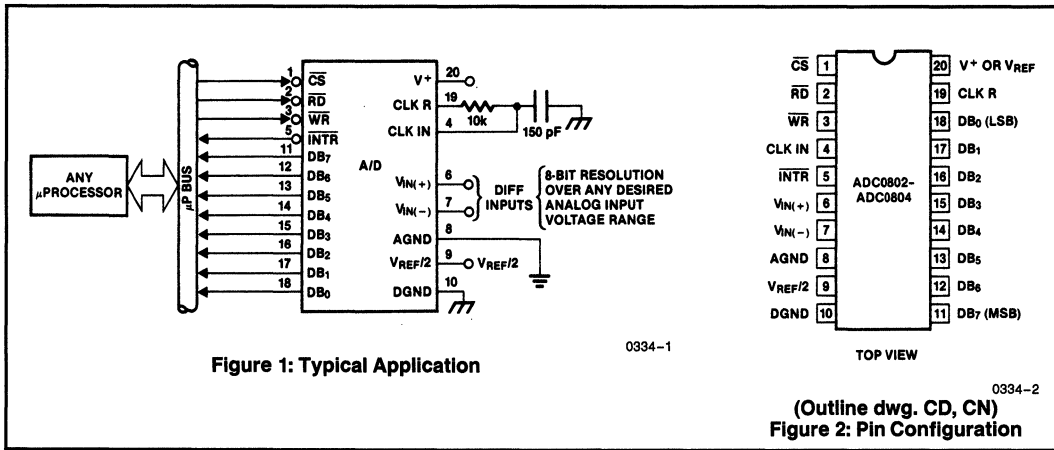
FEATURES

- 80C48 and 80C80/85 Bus Compatible — No Interfacing Logic Required
- Conversion Time < 100 μ s
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works With Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- 0V to 5V Analog Voltage Input Range (Single +5V Supply)
- No Zero-Adjust Required

ORDERING INFORMATION

Part Number	Error	Temperature Range	Package
ADC0802LCN ADC0802LCD ADC0802LD	$\pm 1/2$ bit no adjust $\pm 3/4$ bit no adjust ± 1 bit no adjust	0°C to +70°C -40°C to +85°C -55°C to +125°C	20 pin Plastic DIP 20 pin Cerdip 20 pin Cerdip
ADC0803LCN ADC0803LCD ADC0803LD	$\pm 1/2$ bit adjusted full-scale $\pm 3/4$ bit adjusted full-scale ± 1 bit adjusted full-scale	0°C to +70°C -40°C to +85°C -55°C to +125°C	20 pin Plastic DIP 20 pin Cerdip 20 pin Cerdip
ADC0804LCN ADC0804LCD	± 1 bit no adjust ± 1 bit no adjust	0°C to +70°C -40°C to +85°C	20 pin Plastic DIP 20 pin Cerdip

3



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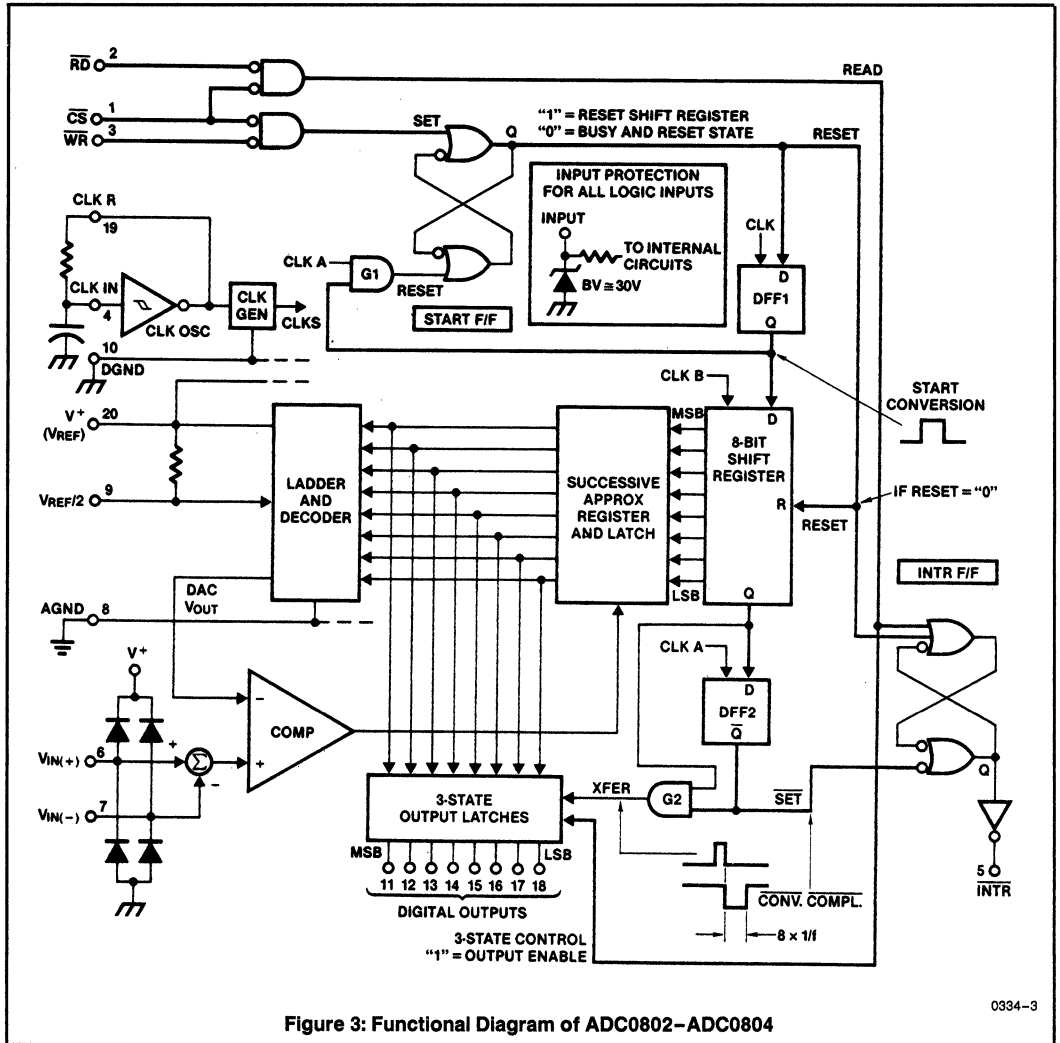


Figure 3: Functional Diagram of ADC0802-ADC0804

0334-3

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Voltage at Any Input	-0.3V to (V ⁺ + 0.3V)
Storage Temperature Range	-65°C to +150°C
Package Dissipation at T _A = +25°C	875mW
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Temperature Range	-55°C to +125°C
ADC0802/03LD	-55°C to +125°C
ADC0802/03/04LCD	-40°C to +85°C
ADC0802/03/04LCN	0°C to +70°C
Supply Voltage Range	4.5V to 6.3V

ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: V⁺ = 5V, V_{REF/2} = 2.500V, T_A = +25°C and f_{CLK} = 640kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			± 1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			± 1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			± 1	LSB
V _{REF/2} Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05		V ⁺ + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		± 1/16	± 1/8	LSB
Power Supply Sensitivity	V ⁺ = 5V ± 10% Over Allowed Input Voltage Range		± 1/16	± 1/8	LSB

3

Converter Specifications: V⁺ = 5V, V_{REF/2} = 2.500V, 0°C ≤ T_A ≤ +70°C and f_{CLK} = 640 kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			± 1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			± 1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			± 1	LSB
V _{REF/2} Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05		V ⁺ + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		± 1/16	± 1/8	LSB
Power Supply Sensitivity	V ⁺ = 5V ± 10% Over Allowed Input Voltage Range		± 1/16	± 1/4	LSB

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NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

Converter Specifications: $V^+ = 5V$, $V_{REF/2} = 2.500V$, $-25^\circ C \leq T_A \leq +85^\circ C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			$\pm 3/4$	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			$\pm 3/4$	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			± 1	LSB
$V_{REF/2}$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		k Ω
Analog Input Voltage Range	(Note 2)	GND-0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		$\pm 1/16$	$\pm 1/8$	LSB

Converter Specifications: $V^+ = 5V$, $V_{REF/2} = 2.500V$, $-55^\circ C \leq T_A \leq +125^\circ C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			± 1	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			± 1	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			$\pm 1 1/4$	LSB
$V_{REF/2}$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		k Ω
Analog Input Voltage Range	(Note 2)	GND-0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		$\pm 1/8$	$\pm 1/4$	LSB

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NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS

Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CONTROL INPUTS (Note 6)						
V_{INH}	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 5.25V$	2.0		V^+	V
V_{INL}	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 4.75V$			0.8	V
V^+_{CLK}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V
V^-_{CLK}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V
V_H	CLK IN (Pin 4) Hysteresis ($V_{CLK^+} - V_{CLK^-}$)		0.6	1.3	2.0	V
I_{INHI}	Logical "1" Input Current (All Inputs)	$V_{IN} = 5V$		0.005	1	μA
I_{INLO}	Logical "0" Input Current (All Inputs)	$V_{IN} = 0V$	-1	-0.005		μA
I^+	Supply Current (Includes Ladder Current)	$f_{CLK} = 640kHz$, $T_A = +25^\circ C$ and $\overline{CS} = HI$		1.3	2.5	mA

3

DC ELECTRICAL CHARACTERISTICS

Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted. (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DATA OUTPUTS AND INTR						
V_{OL}	Logical "0" Output Voltage	$I_o = 1.6mA$ $V^+ = 4.75V$			0.4	V
V_{OH}	Logical "1" Output Voltage	$I_o = -360\mu A$ $V^+ = 4.75V$	2.4			V
I_{LO}	3-State Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	-3		3	μA
I_{SOURCE}	Output Short Circuit Current	V_{OUT} Short to Gnd $T_A = +25^\circ C$	4.5	6		mA
I_{SINK}	Output Short Circuit Current	V_{OUT} Short to V^+ $T_A = +25^\circ C$	9.0	16		mA

NOTES: 1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

2. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.

3. With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.

4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

5. The \overline{CS} input is assumed to bracket the \overline{WR} strobe input so that timing is dependent on the \overline{WR} pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the \overline{WR} pulse (see **Timing Diagrams**).

6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.

7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See **Zero Error** on page 10 of this data sheet.

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NOTE: All typical values have been characterized but are not tested.

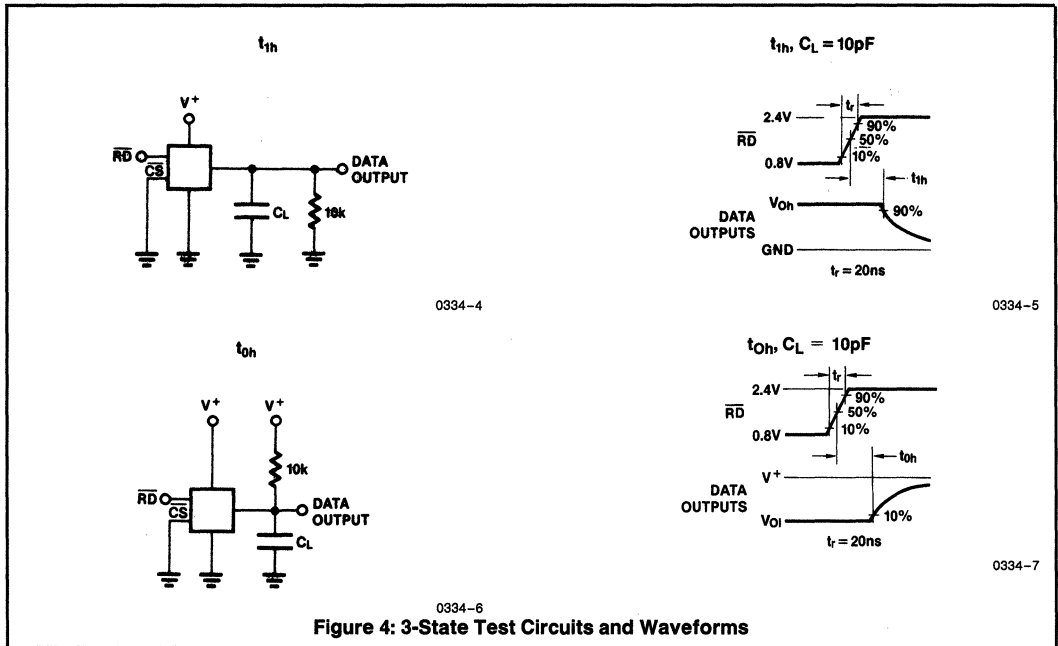
ADC0802-ADC0804



AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25^\circ C$ unless otherwise stated.

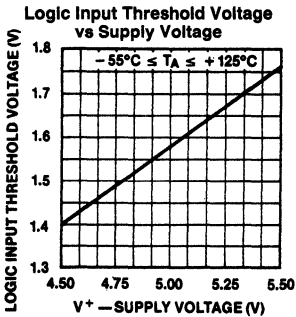
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{CLK}	Clock Frequency	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100	640	1280	kHz
t_{conv}	Clock Periods per Conversion (Note 4)		62		73	
CR	Conversion Rate In Free-Running Mode	\overline{INTR} tied to \overline{WR} with $\overline{CS} = 0V$, $f_{CLK} = 640kHz$			8888	conv/s
$t_{W(\overline{WR})}$	Width of \overline{WR} Input (Start Pulse Width)	$\overline{CS} = 0V$ (Note 5)	100			ns
t_{acc}	Access Time (Delay from Falling Edge of \overline{RD} to Output Data Valid)	$C_L = 100pF$ (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1h}, t_{0h}	3-State Control (Delay from Rising Edge of \overline{RD} to HI-Z State)	$C_L = 10pF$, $R_L = 10k$ (See 3-State Test Circuits)		125	250	ns
t_{Wl}, t_{Rl}	Delay from Falling Edge of \overline{WR} to Reset of \overline{INTR}			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5		pF
C_{OUT}	3-State Output Capacitance (Data Buffers)			5		pF



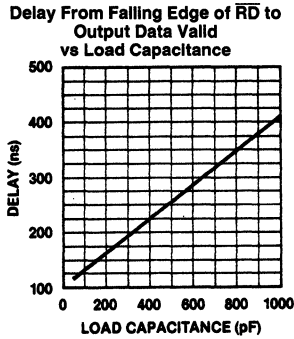
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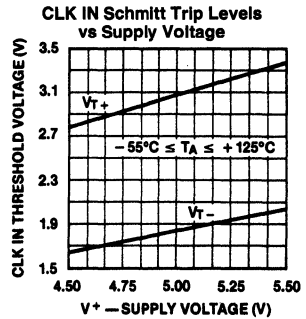
TYPICAL PERFORMANCE CHARACTERISTICS



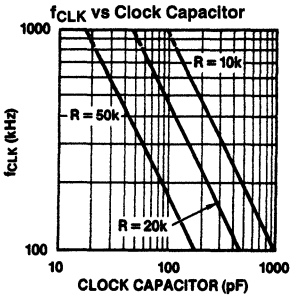
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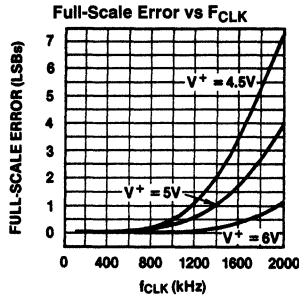
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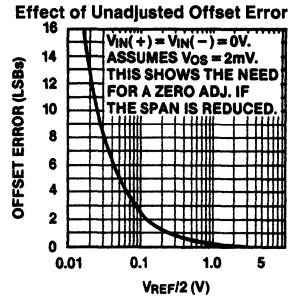
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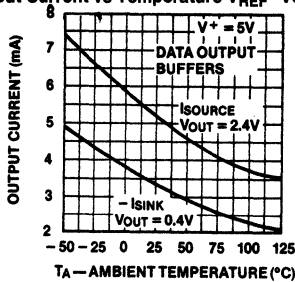


0334-12



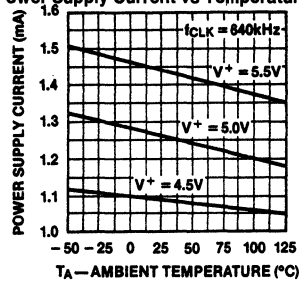
0334-13

Output Current vs Temperature V_{REF}^2 Voltage



0334-14

Power Supply Current vs Temperature

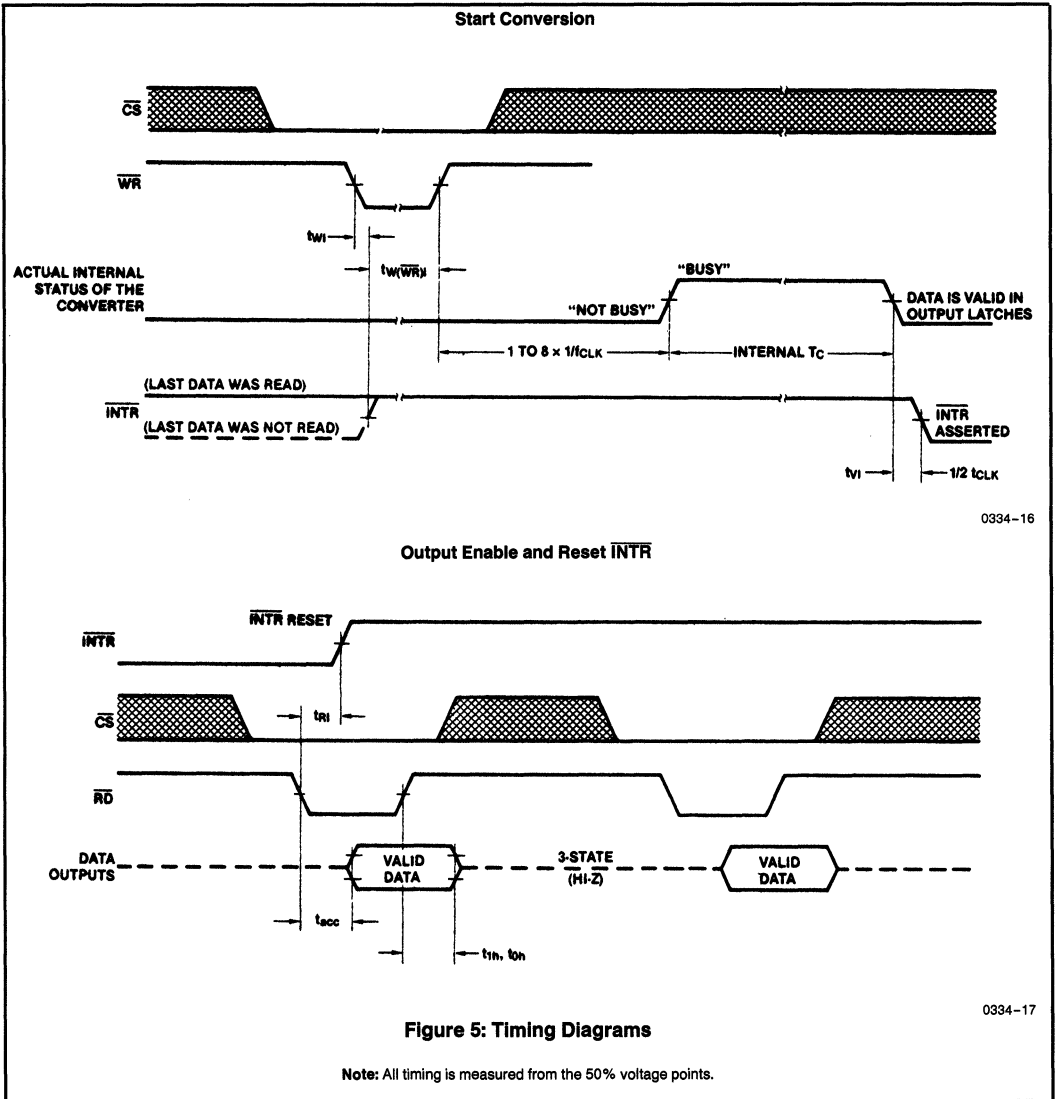


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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



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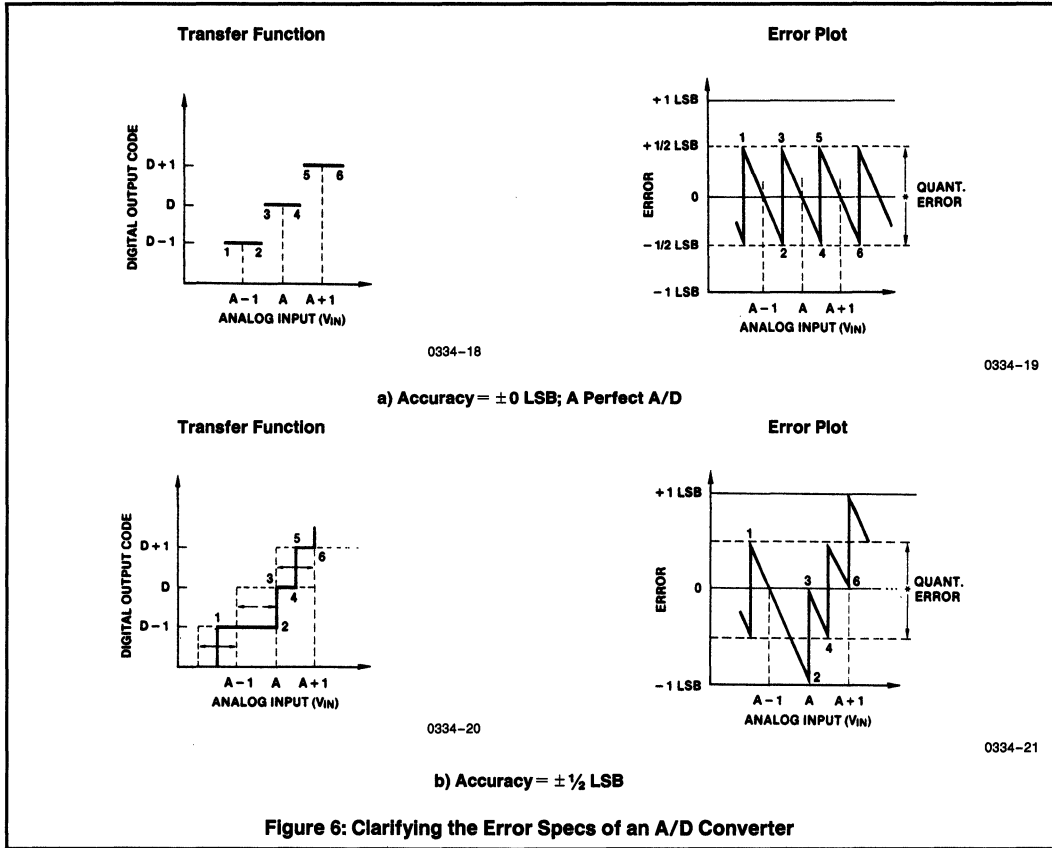


Figure 6: Clarifying the Error Specs of an A/D Converter

UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 6a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D - 1, D, and D + 1. For the perfect A/D, not only will center-value (A - 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located $\pm \frac{1}{2}$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend $\pm \frac{1}{2}$ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1LSB wide.

The error curve of Figure 6b shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 6a is $+\frac{1}{2}$ LSB because the digital code appeared $\frac{1}{2}$ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1LSB in magnitude, unless the device has missing codes.

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NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804



FUNCTIONAL DESCRIPTION

A functional diagram of the ADC0802 series of A/D converters is shown in Figure 3. All of the package pinouts are shown and the major logic control paths are drawn in heavier-weight lines. The device operates on the successive approximation principle (see APPLICATION NOTE A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the \overline{WR} input, the internal SAR latches and the shift-register stages are reset, and the \overline{INTR} output will be set high. As long as the \overline{CS} input and \overline{WR} input remain low, the A/D will remain in a reset state. **Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.** After the requisite number of clock pulses to complete the conversion, the \overline{INTR} pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A \overline{RD} operation (with \overline{CS} low) will clear the \overline{INTR} line high again. The device may be operated in the free-running mode by connecting \overline{INTR} to the \overline{WR} input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external \overline{WR} pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Details

The converter is started by having \overline{CS} and \overline{WR} simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (\overline{INTR}) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either \overline{WR} or \overline{CS} is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide \overline{CS} and \overline{WR} signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the \overline{Q} output makes a high-to-low transition which causes the \overline{INTR} F/F to set. An inverting buffer then supplies the \overline{INTR} output signal.

When data is to be read, the combination of both \overline{CS} and \overline{RD} being low will cause the \overline{INTR} F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs (\overline{CS} , \overline{RD} , and \overline{WR}) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the \overline{CS} input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the \overline{WR} input (pin 3). The Output Enable function is achieved by an active low pulse at the \overline{RD} input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by $\frac{1}{2}$ LSB (see Figure 6a).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA - 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is $4\frac{1}{2}$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(\text{MAX}) = (V_p)(2\pi f_{cm}) \left[\frac{4.5}{f_{CLK}} \right]$$

where:

ΔV_e is the error voltage due to sampling delay

V_p is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{cm} , and a 640kHz A/D clock, f_{CLK} , keeping this error to $\frac{1}{4}$ LSB ($\sim 5\text{mV}$) would allow a common-mode voltage, V_p , given by:

$$V_p = \frac{[\Delta V_e(\text{MAX})(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_p = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)} \approx 1.9\text{V}$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see **Reference Voltage Span Adjust**).

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NOTE: All typical values have been characterized but are not tested.

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and **do not inherently cause errors** as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately $5\mu A$. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin** for high resistance sources ($> 1k\Omega$). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

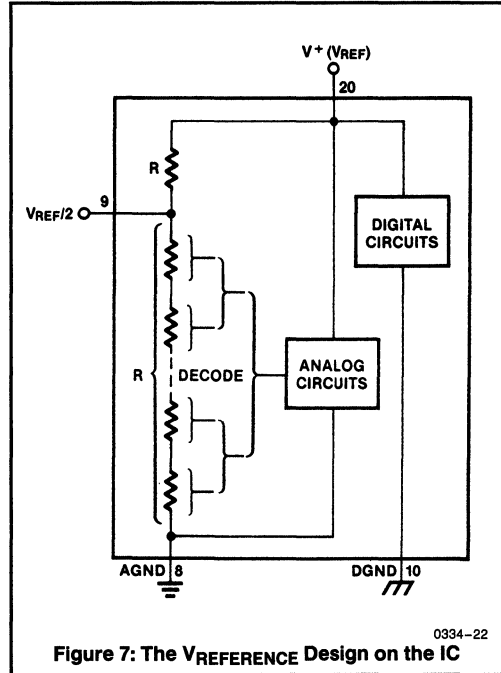
Large values of source resistance where an input bypass capacitor is not used, **will not cause errors** since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor ($\leq 1k\Omega$) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, ($\leq 1k\Omega$), a $0.1\mu F$ bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below $5k\Omega$. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see **Analog Input Current**). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see **Full-Scale Adjustment**) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 7.



0334-22
Figure 7: The $V_{REFERENCE}$ Design on the IC

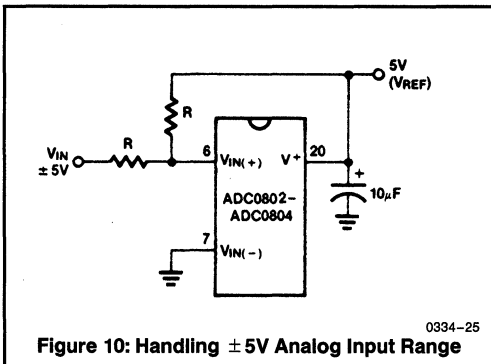
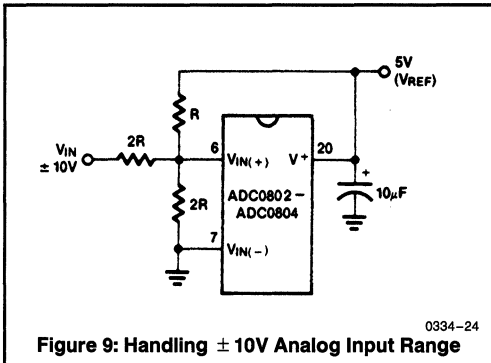
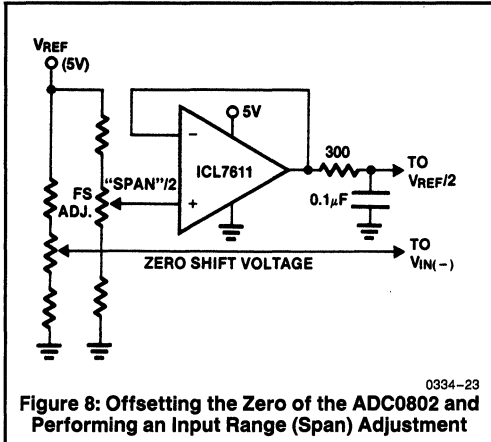
Notice that the reference voltage for the IC is either $1/2$ of the voltage which is applied to the V^+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V^+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $1/2$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 8. For expanded scale inputs, the circuits of Figures 9 and 10 can be used.

3

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NOTE: All typical values have been characterized but are not tested.



Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final

digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of $\pm 10\text{mV}$ will cause conversion errors of $\pm 1\text{LSB}$ due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $1/2$ LSB value ($1/2$ LSB = 9.8mV for $V_{REF}/2 = 2.500\text{V}$).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is $1\frac{1}{2}$ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}\text{fsadj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

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NOTE: All typical values have been characterized but are not tested.

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 11.

Heavy capacitive or DC loading of the CLoCK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted (\overline{CS} and \overline{WR} go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the \overline{CS} input is grounded and the \overline{WR} input is tied to the INTR output. This \overline{WR} and INTR node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 12 for details.

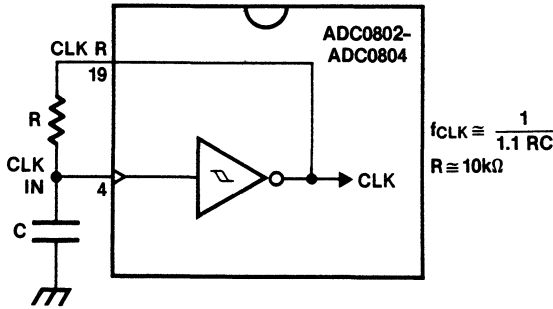


Figure 11: Self-Clocking the A/D

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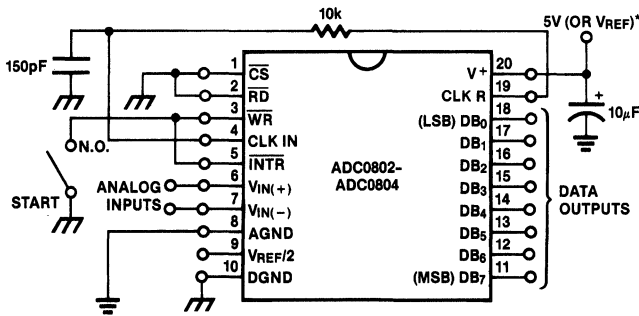


Figure 12: Free-Running Connection

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NOTE: All typical values have been characterized but are not tested.

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see **Typical Performance Characteristics**).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V^+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V^+ pin, and values of $1\mu\text{F}$ or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V^+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF/2}$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $1/4$ LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in A018.

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 13.

For ease of testing, the $V_{REF/2}$ (pin 9) should be supplied with 2.560V and a V^+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V ($5.120 - 1/2$ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF/2}$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF/2}$ should then be used for all the tests.

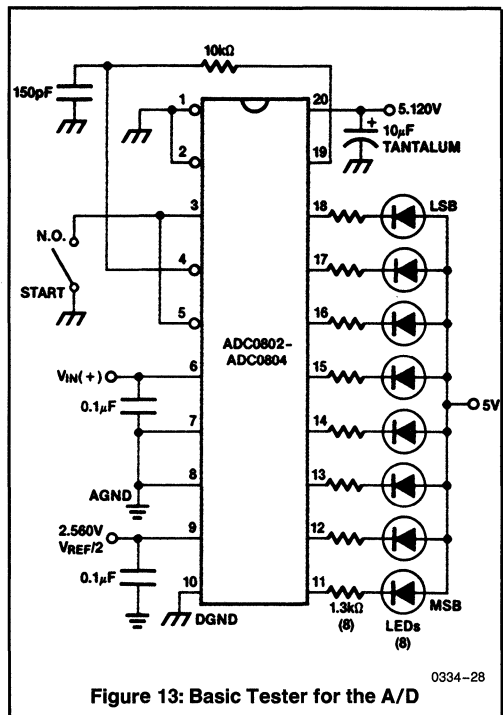


Figure 13: Basic Tester for the A/D

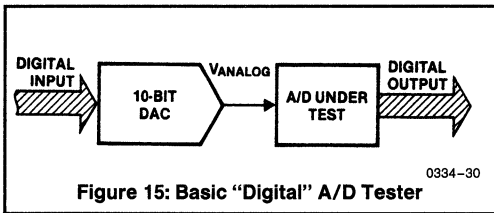
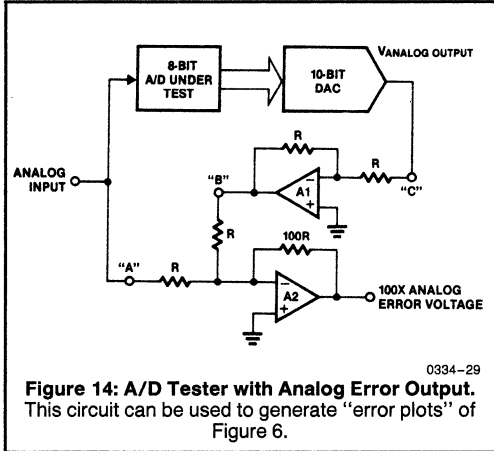
The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256} \right) (5.12)V.$$

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256} \right) (5.12) = 3.64V.$$

Figures 14 and 15 show more sophisticated test circuits.



APPLICATIONS

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate \overline{CS} for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for \overline{CS} and the \overline{MEMR} and \overline{MEMW} strobes) or it can be controlled as an I/O device by using the $\overline{I/O R}$ and $\overline{I/O W}$ strobes and decoding the address bits $A_0 \rightarrow A_7$ (or address bits $A_8 \rightarrow A_{15}$, since they will contain the same 8-bit address information) to obtain the \overline{CS} input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 16.

The standard control-bus signals of the 8080 (\overline{CS} , \overline{RD} and \overline{WR}) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A_0 to A_7) can be directly used as \overline{CS} inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General \overline{RD} and \overline{WR} strobes are provided and separate memory request, \overline{MREQ} , and I/O request, \overline{IORQ} , signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the \overline{RD} and \overline{WR} strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 17. By using \overline{MREQ} in place of \overline{IORQ} , a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A_8 to A_{15}) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized \overline{RD} and \overline{WR} strobe, with an $\overline{IO/M}$ line to distinguish I/O and memory requests. The circuit of Figure 17 can again be used, with $\overline{IO/M}$ in place of \overline{IORQ} for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO/M}$ for an I/O-mapped connection.

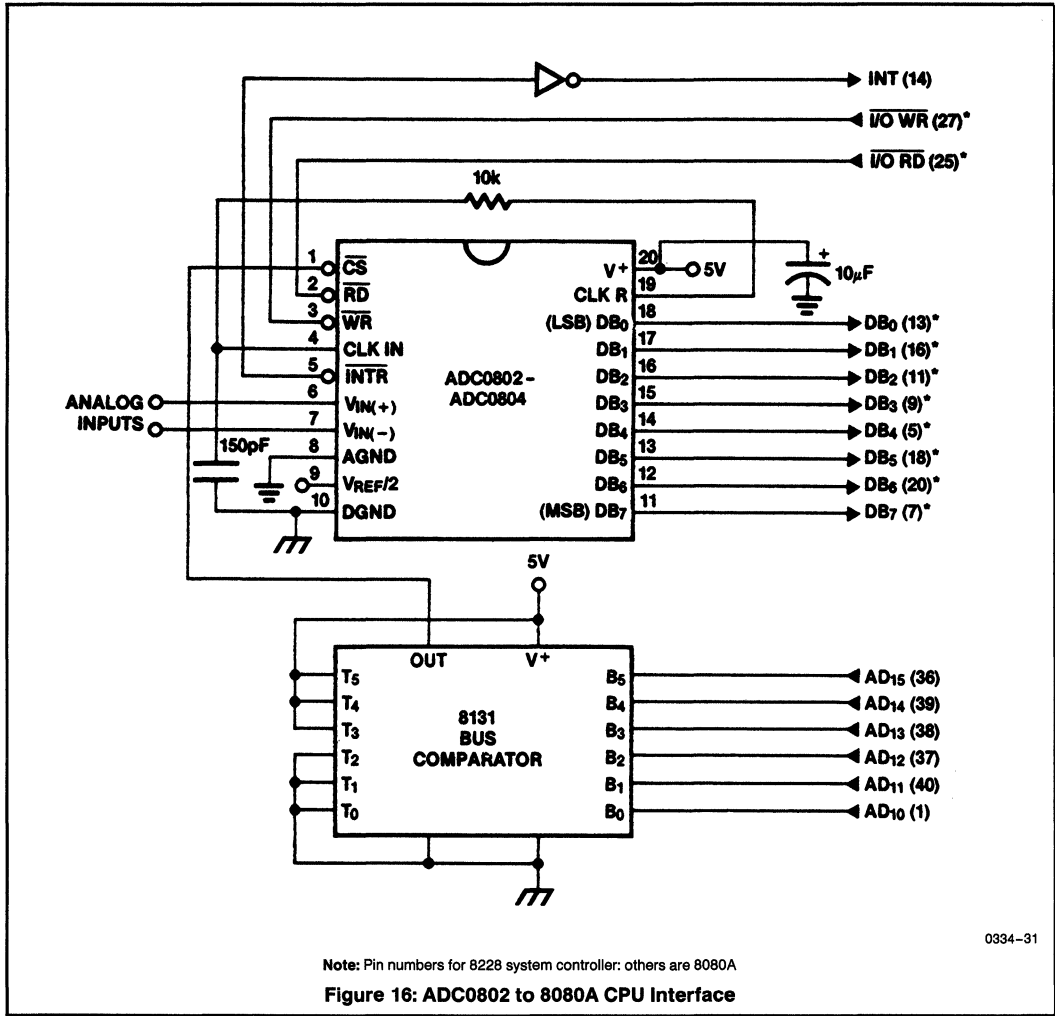
Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the \overline{RD} and \overline{WR} strobe signals. Instead it employs a single $\overline{R/W}$ line and additional timing, if needed, can be derived from the ϕ_2 clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 16 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the \overline{CS} decoding is shown using $\frac{1}{2}$ DM8092. Note that in many 6800 systems, an already decoded $\frac{1}{2}$ line is brought out to the common bus at pin 21. This can be tied directly to the \overline{CS} pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 19 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the \overline{CS} pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no \overline{CS} decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D \overline{RD} pin can be grounded.

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NOTE: All typical values have been characterized but are not tested.



Note: Pin numbers for 8228 system controller; others are 8080A

Figure 16: ADC0802 to 8080A CPU Interface

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ADC0802-ADC0804

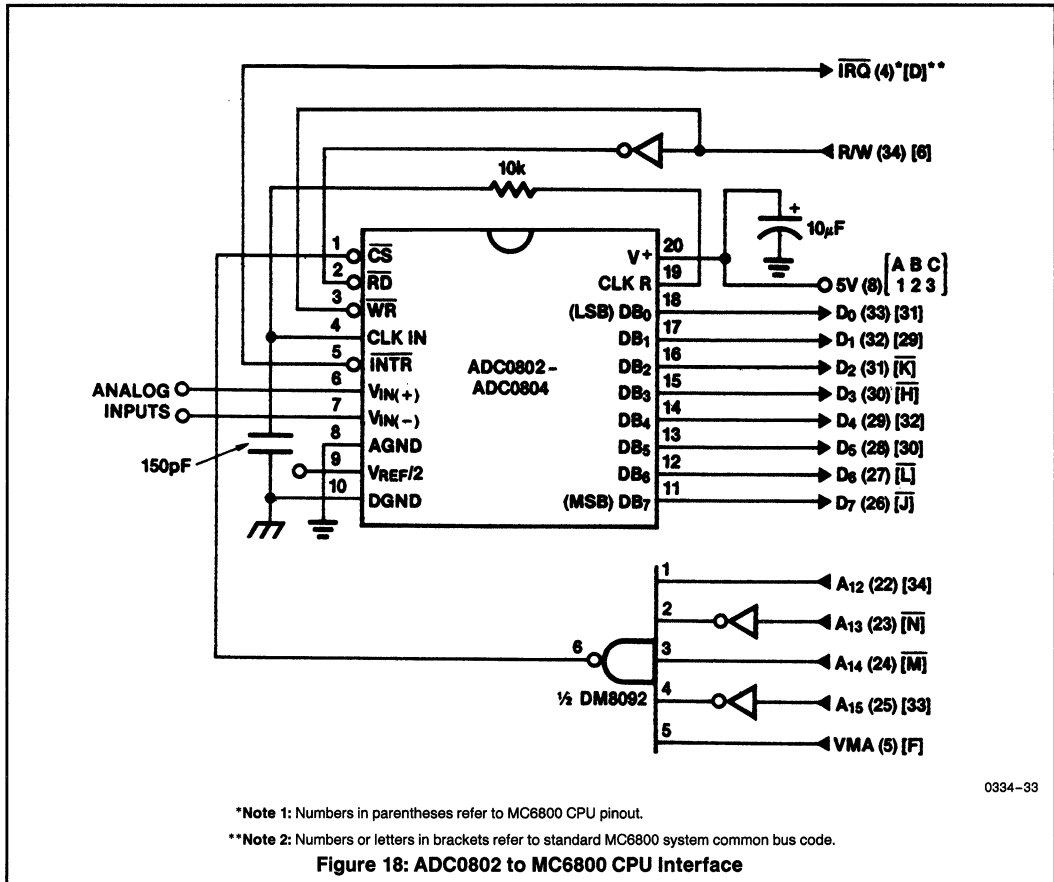
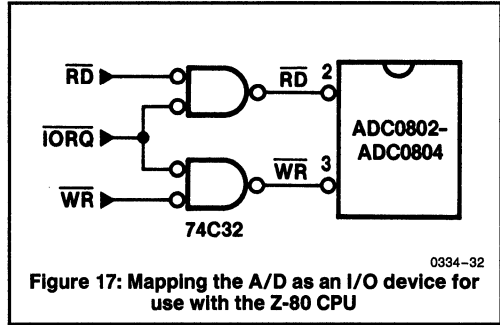


ADC0802-ADC0804

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

- A016** "Selecting A/D Converters," by Dave Fullagar.
- A018** "Do's and Don't's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A020** "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.
- A030** "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.
- R005** "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.



3

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NOTE: All typical values have been characterized but are not tested.

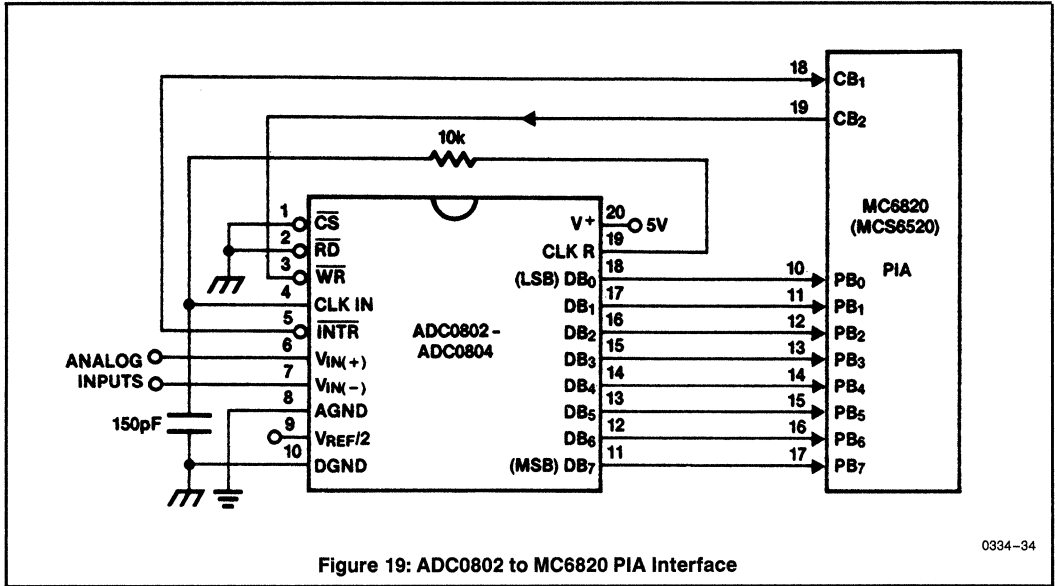


Figure 19: ADC0802 to MC6820 PIA Interface

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NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104 14/16-Bit μ P-Compatible 2-Chip A/D Converter



ICL8052/ICL7104 and ICL8068/ICL7104

3

GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for easy interfacing. The ICL7014-14 is a 14-bit version. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ± 0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

FEATURES

- 16/14 Bit Binary Three-State Latched Outputs Plus Polarity and Overrange
- Ideally Suited for Interface to UARTs and Microprocessors
- Conversion On Demand or Continuously
- Guaranteed Zero Reading for Zero Volts Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage for True Ratiometric Operation
- Onboard Clock and Reference
- Auto-Zero; Auto-Polarity
- Accuracy Guaranteed to 1 Count
- All Outputs TTL Compatible
- $\pm 4V$ Analog Input Range
- Status Signal Available for External Sync, A/Z in Preamp, etc

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL8052CPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052ACPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068CJD	0°C to +70°C	14-Pin CERDIP
ICL8068ACJD	0°C to +70°C	14-Pin CERDIP

Part Number	Temp. Range	Package
ICL7104-14CJL	0°C to -70°C	40-Pin CERDIP
ICL7104-14CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-14CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7104-16CJL	0°C to +70°C	40-Pin CERDIP
ICL7104-16CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-16CDL	0°C to +70°C	40-Pin Ceramic DIP

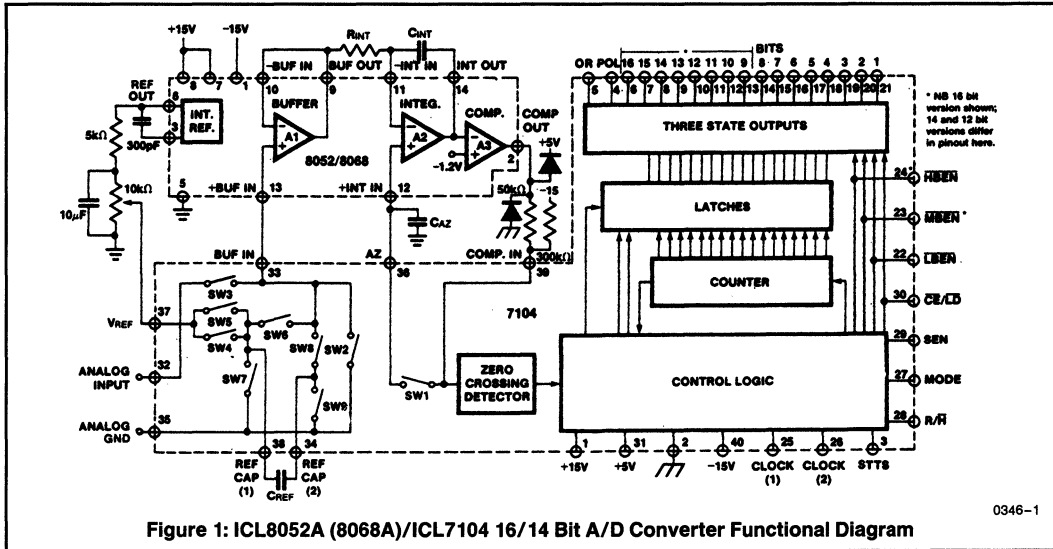


Figure 1: ICL8052A (8068A)/ICL7104 16/14 Bit A/D Converter Functional Diagram

0346-1

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NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1) All Devices 500mW
 Storage Temperature -65°C to +150°C
 Operating Temperature 0°C to +70°C
 Lead Temperature (Soldering, 10sec) 300°C
ICL8052, 8068

Supply Voltage ±15V
 Differential Input Voltage (8068) ±30V
 (8052) ±6V
 Input Voltage (2) ±15V
 Output Short Circuit Duration,
 All Outputs (3) Indefinite

NOTE 1 Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

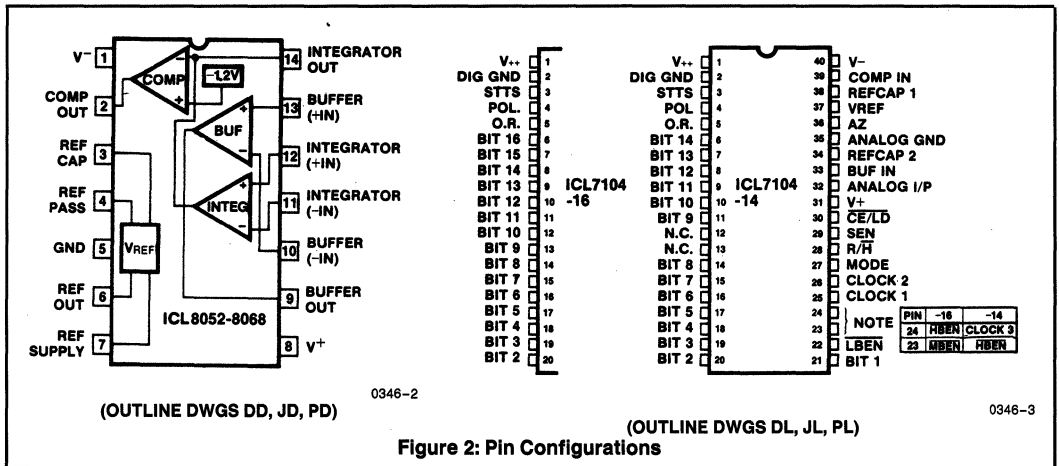
4 Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.

5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7104

V+ Supply (GND to V+) 12V
 V++ to V- 32V
 Positive Supply Voltage (GND to V++) 17V
 Negative Supply Voltage (GND to V-) 17V
 Analog Input Voltage (Pins 32 - 39) (4) V++ to V-
 Digital Input Voltage
 (Pins 2 - 30) (5) (GND - 0.3V) to (V+ + 0.3V)



ICL7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V- = -15V, TA = 25°C)

Symbol	Characteristics		Test Conditions	Min	Typ	Max	Unit
I _{IN}	Clock Input	CLOCK 1	V _{in} = +5V to 0V	±2	±7	±30	µA
I _{IN}	Comparator I/P	COMP IN (Note 1)	V _{in} = 0V to +5V	-10	±0.001	+10	µA
I _{IH}	Inputs with Pulldown	MODE	V _{in} = +5V	+1	+5	+30	µA
I _{IL}			V _{in} = 0V	-10	±0.01	+10	µA
I _{IH}	Inputs with Pullups	SEN, R/H LBEN, MBEN, HBEN, CE/LD } (Note 2)	V _{in} = +5V	-10	±0.01	+10	µA
I _{IL}			V _{in} = 0V	-30	-5	-1	µA

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NOTE: All typical values have been characterized but are not tested.

ICL7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V- = -15V, TA = 25°C)

(Continued)

Symbol	Characteristics		Test Conditions	Min	Typ	Max	Unit
V _{IH}	Input High Voltage	All Digital Inputs		2.5	2.0	—	V
V _{IL}	Input Low Voltage	All Digital Inputs			1.5	1.0	V
V _{OL}	Digital	} (Note 3) LBEN MBEN (16-only) HBEN CE/LD BIT n, POL, OR	I _{OL} = 1.6mA	—	0.27	.4	V
V _{OH}	Outputs		I _{OH} = -10μA		4.5	—	V
V _{OH}	Three-States On		I _{OH} = -240μA	2.4	3.5	—	V
I _{OL}	Digital Outputs Three-States Off	BIT n, POL, OR	0 ≤ V _{out} ≤ V+	-10	±.001	+10	μA
V _{OL}	Non-Three State	STTS	I _{OL} = 3.2mA	—	0.3	.4	V
V _{OH}	Digital		I _{OH} = -400μA	2.4	3.3	—	V
V _{OL}	Output	CLOCK 2	I _{OL} = 320μA		0.5		V
V _{OH}			I _{OH} = -320μA		4.5		V
V _{OL}		CLOCK 3 (-14 ONLY)	I _{OL} = 1.6mA		0.27	.4	V
V _{OH}			I _{OH} = -320μA	2.4	3.5		V
R _{DS(on)}	Switch	Switch 1		—	25k		Ω
R _{DS(on)}		Switches 2,3		—	4k	20k	Ω
R _{DS(on)}		Switches 4,5,6,7,8,9		—	2k	10k	Ω
I _{D(off)}		Switch Leakage		—	15		pA
	Clock	Clock Freq. (Note 4)		DC	200	400	kHz
I+	Supply Currents	+5V Supply Current All outputs high impedance	Freq. = 200kHz		200	600	μA
I++		+15V Supply Current	Freq. = 200kHz		.3	1.0	mA
I-		-15V Supply Current	Freq. = 200kHz		25	200	μA
V+	Supply Voltage	Logic Supply	Note 5	4.0		+11.0	V
V++	Range	Positive Supply		+10.0		+16.0	V
V-		Negative Supply		-16.0		-10.0	V

NOTES: 1. This spec applies when not in Auto-Zero phase.

2. Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.

3. Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.

4. Clock circuit shown in Figs. 15 and 16.

5. V+ must not be more positive than V++.

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NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104



ICL8068 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

Symbol	Characteristics	Test Conditions	8068			8068A			Unit
			Min	Typ	Max	Min	Typ	Max	
EACH OPERATIONAL AMPLIFIER									
V _{OS}	Input Offset Voltage	V _{CM} = 0V		20	65		20	65	mV
I _{IN}	Input Current (either input) (Note 1)	V _{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V _{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V _{CM} = ±2V		110			110		dB
A _V	Large Signal Voltage Gain	R _L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I _{SC}	Output Short-Circuit Current			5			5		mA
COMPARATOR AMPLIFIER									
A _{VOL}	Small-signal Voltage Gain	R _L = 30kΩ		4000					V/V
+V _O	Positive Output Voltage Swing		+12	+13		+12	+13		V
-V _O	Negative Output Voltage Swing		-2.0	-2.6		-2.0	-2.6		V
VOLTAGE REFERENCE									
V _O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R _O	Output Resistance			5			5		Ω
TC	Temperature Coefficient			50			40		ppm/°C
V _{SUPPLY}	Supply Voltage Range		±10		±16	±10		±16	V
I _{SUPPLY}	Supply Current Total				14		8	14	mA

ICL8052 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

Symbol	Characteristics	Test Conditions	8052			8052A			Unit
			Min	Typ	Max	Min	Typ	Max	
EACH OPERATIONAL AMPLIFIER									
V _{OS}	Input Offset Voltage	V _{CM} = 0V		20	75		20	75	mV
I _{IN}	Input Current (either input) (Note 1)	V _{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V _{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V _{CM} = ±2V		110			110		dB
A _V	Large Signal Voltage Gain	R _L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I _{SC}	Output Short-Circuit Current			20			20		mA
COMPARATOR AMPLIFIER									
A _{VOL}	Small-signal Voltage Gain	R _L = 30kΩ		4000					V/V
+V _O	Positive Output Voltage Swing		+12	+13		+12	+13		V
-V _O	Negative Output Voltage Swing		-2.0	-2.6		-2.0	-2.6		V

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NOTE: All typical values have been characterized but are not tested.

ICL8052 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified) (Continued)

Symbol	Characteristics	Test Conditions	8052			8052A			Unit
			Min	Typ	Max	Min	Typ	Max	
VOLTAGE REFERENCE									
V _O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R _O	Output Resistance			5			5		Ω
TC	Temperature Coefficient			50			40		ppm/°C
V _{SUPPLY}	Supply Voltage Range		±10		±16	±10		±16	V
I _{SUPPLY}	Supply Current Total			6	12		6	12	mA

NOTES: 1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. T_J = T_A + R_{θJA}P_d where R_{θJA} is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

2. This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: ICL8068/7104 (V₊ = +15V, V₊ = +5V,

V₋ = -15V, Clock Frequency = 200kHz)

Characteristics	Test Conditions	8068A/7104-14			8068A/7104-16			Unit
		Min	Typ	Max	Min	Typ	Max	
Zero Input Reading (4)	V _{in} = 0.0V Full Scale = 4.000V	-0.0000	±0.0000	+0.0000	-0.0000	-0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1) (4)	V _{in} = V _{Ref} . Full Scale = 4.000V	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line) (4)	-4V ≤ V _{in} ≤ +4V		0.5	1		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	-4V ≤ V _{in} ≤ +4V		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale) (4)	-V _{in} = +V _{in} ≈ 4V		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V _{in} = 0V Full scale = 4.000V		2			2		μV
Leakage Current at Input (2) (4)	V _{in} = 0V		100	165		100	165	pA
Zero Reading Drift (A)	V _{in} = 0V 0°C ≤ T _A ≤ 70°C		0.5			0.5		μV/°C
Scale Factor Temperature (3) (4) Coefficient	V _{in} = +4V 0 ≤ T _A ≤ 50°C ext. ref. 0ppm/°C		2	5		2	5	ppm/°C

3

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NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104



SYSTEM ELECTRICAL CHARACTERISTICS: ICL8052/7104 ($V^{++} = +15V$, $V^+ = +5V$,
 $V^- = -15V$, Clock Frequency = 200kHz)

Characteristics	Test Conditions	8052A/7104-14			8052A/7104-16			Unit
		Min	Typ	Max	Min	Typ	Max	
Zero Input Reading	$V_{in} = 0.0V$ Full Scale = 4.000V	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3) (4)	$V_{in} = V_{Ref}$. Full Scale = 4.000V	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line) (4)	$-4V \leq V_{in} \leq +4V$		0.5	1		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	$-4V \leq V_{in} \leq +4V$.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} = +V_{in} \approx 4V$		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	$V_{in} = 0V$ Full scale = 4.000V		30			30		μV
Leakage Current at Input (2) (4)	$V_{in} = 0V$		20	30		20	30	pA
Zero Reading Drift (4)	$V_{in} = 0V$ $0 \leq T_A \leq 70^\circ C$		0.5			0.5		μV/°C
Scale Factor Temperature Coefficient (4)	$V_{in} = +4V$ $0 \leq T_A \leq 70^\circ C$ (ext. ref. 0ppm/°C)		2			2		ppm/°C

NOTES: 1. Tested with low dielectric absorption integrating capacitor.

2. the input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d . $T_J = T_A + R_{\theta JA} P_d$ where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.
3. The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.
4. Parameter has been characterized but is not production tested.

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NOTE: All typical values have been characterized but are not tested.

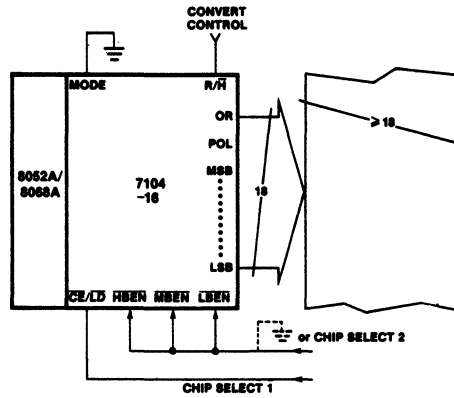


Figure 3: Full 18 Bit Three State Output

0346-4

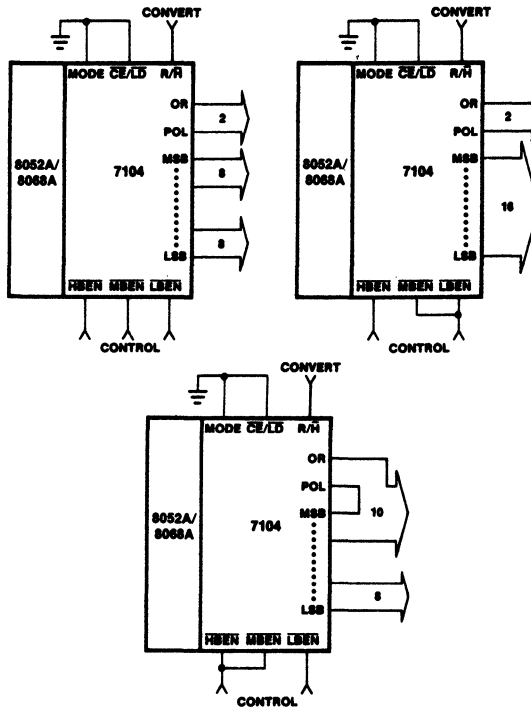


Figure 4: Various Combinations of Byte Disables

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NOTE: All typical values have been characterized but are not tested.

AC CHARACTERISTICS (V₊₊ = +15V, V₊ = +5V, V₋₋ = -15V)

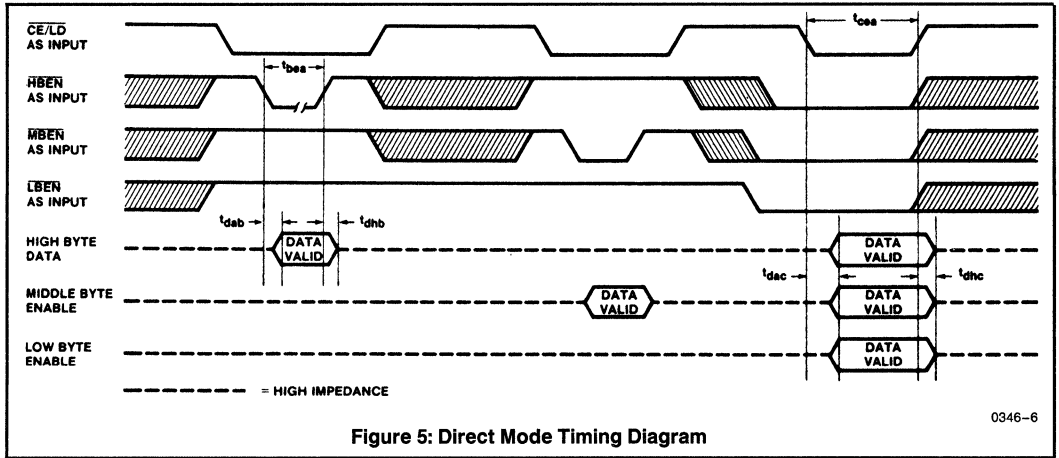


Figure 5: Direct Mode Timing Diagram

Table 1: Direct Mode Timing Requirements (Note: Not tested in production)

Symbol	Description	Min	Typ	Max	Unit
t _{bea}	\overline{XBEN} Min. Pulse Width		300		ns
t _{dab}	Data Access Time from \overline{XBEN}		300		
t _{dhb}	Data Hold Time from \overline{XBEN}		200		
t _{cea}	$\overline{CE/LD}$ Min. Pulse Width		350		
t _{dac}	Data Access Time from $\overline{CE/LD}$		350		
t _{dhc}	Data Hold Time from $\overline{CE/LD}$		280		
t _{cwh}	CLOCK 1 High Time		1000		

Table 2: Handshake Timing Requirements (Note: Not tested in production.)

Name	Description	Min	Typ	Max	Unit
t _{mw}	MODE Pulse (minimum)		20		ns
t _{sm}	MODE pin set-up time		-150		
t _{me}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t _{mb}	MODE pin high to \overline{XBEN} low Z (high) delay		200		
t _{cel}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t _{ceh}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t _{cbl}	CLOCK 1 high to \overline{XBEN} low delay		900		
t _{cbh}	CLOCK 1 high to \overline{XBEN} high delay		700		
t _{cdh}	CLOCK 1 high to data enabled delay		1100		
t _{cdl}	CLOCK 1 low to data disabled delay		1100		
t _{ss}	Send ENable set-up time		-350		
t _{cbz}	CLOCK 1 high to \overline{XBEN} disabled delay		2000		
t _{cez}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		
t _{cwh}	CLOCK 1 High Time	1250	1000		

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NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104



Table 3: Pin Descriptions

Pin	Symbol	Option	Description
1	V(+ +)		Positive Supply Voltage Nominally + 15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output. HI during Integrate and Deintegrate until data is latched. LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14	-16 -14	(Most significant bit)
7	BIT 15 BIT 13	-16 -14	Data Bits, Three-state outputs. See Table 4 for format of ENables and bytes. HIGH = true
8	BIT 14 BIT 12	-16 -14	
9	BIT 13 BIT 11	-16 -14	
10	BIT 12 BIT 10	-16 -14	
11	BIT 11 BIT 9	-16 -14	
12	BIT 10 nc	-16 -14	
13	BIT 9 nc	-16 -14	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit.
22	LBEN		Low Byte ENable. If not in handshake mode (see pin 27) when LO (with CE/LD, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 12, 13, 14.
23	MBEN	-16	Mid Byte ENable. Activates BITS 9-16, see LBEN (pin 22)
	HBEN	-14	High Byte ENable. Activates BITS 9-14, POL, OR, see LBEN (pin 22)

Pin	Symbol	Option	Description
24	HBEN	-16	High Byte ENable. Activates POL, OR, see LBEN (pin 22). RC oscillator pin. Can be used as clock output.
	CLOCK3	-14	
Pin	Symbol	Description	
25	CLOCK1	Clock input. External clock or oscillator.	
26	CLOCK2	Clock output. Crystal or RC oscillator.	
27	MODE	Input LO; Direct output mode where CE/LD, HBEN, MBEN and LBEN act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 14). If HI, enables CE/LD, HBEN, MBEN, and LBEN as outputs. Handshake mode will be entered and data output as in Figures 12 & 13 at conversion completion.	
28	R/H	Run/Hold: Input HI-conversions continuously performed every 2 ¹⁷ (-16) or 2 ¹⁵ (-14) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.	
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.	
30	CE/LD	Chip-ENable/LoaD. With MODE (pin 27) LO, CE/LD serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a LoaD strobe (-ve going) used in handshake mode. See Figures 12 & 13.	
31	V(+)	Positive Logic Supply Voltage. Nominally + 5V.	
32	AN,IN	ANalog INput. High side.	
33	BUF IN	BUFFer INput to analog chip (ICL8052 or ICL8068)	
34	REFCAP2	REFerence CAPAcitor (negative side)	
35	AN.GND.	ANalog GrouND. Input low side and reference low side.	
36	A-Z	Auto-Zero node.	
37	VREF	Voltage REFerence input (positive side).	
38	REFCAP1	REFerence CAPAcitor (positive side).	
39	COMP-IN	COMParator INput from 8052/8068	
40	V(-)	Negative Supply Voltage. Nominally - 15V.	

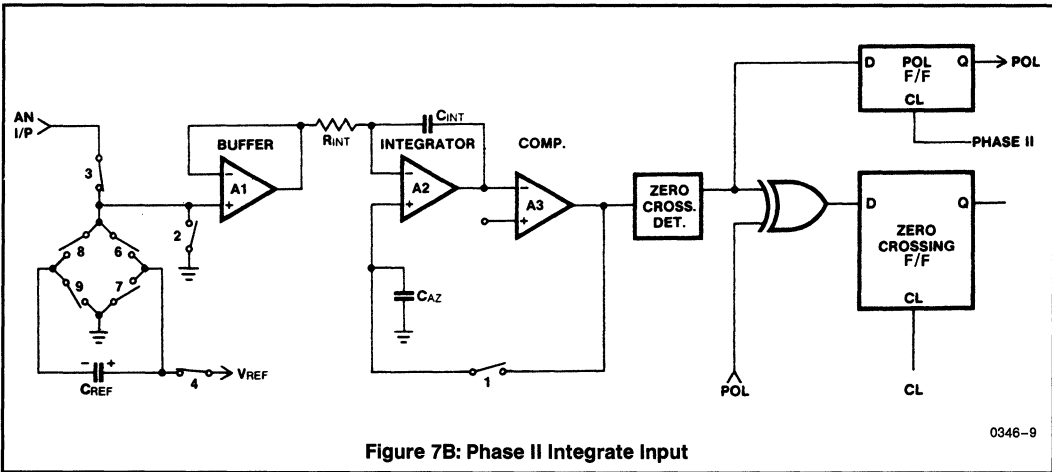
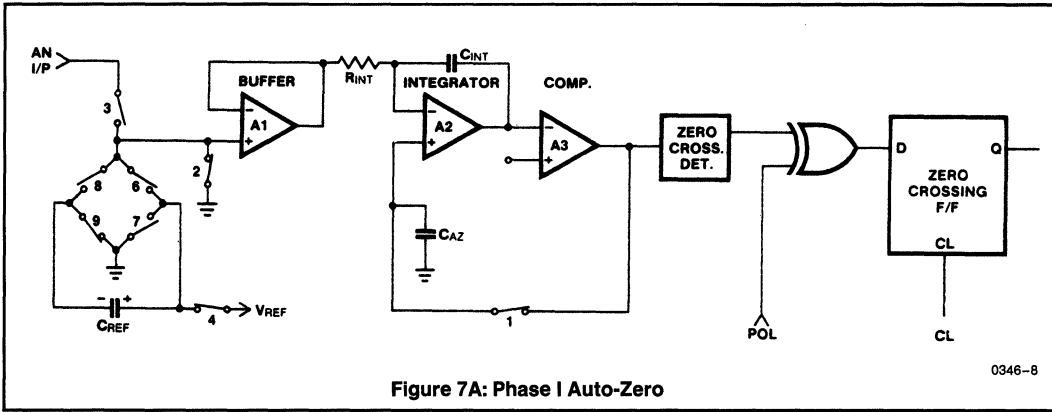
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NOTE: All typical values have been characterized but are not tested.

Table 4: Three-State Byte Formats and \overline{E} Enable Pins

		CE/LD															
		HBEN		MBEN								LBEN					
7104-16	POL O/R	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
		HBEN								LBEN							
7104-14	POL O/R	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1		

Figure 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to Figure 7 below.



3

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NOTE: All typical values have been characterized but are not tested.

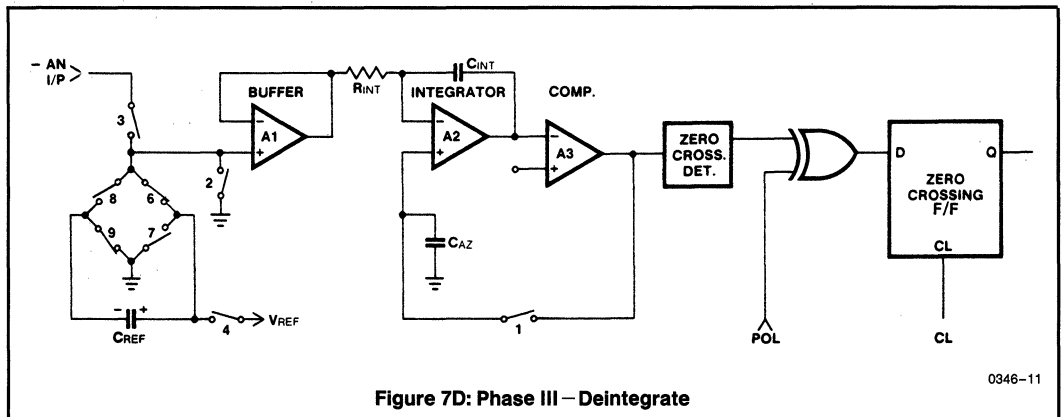
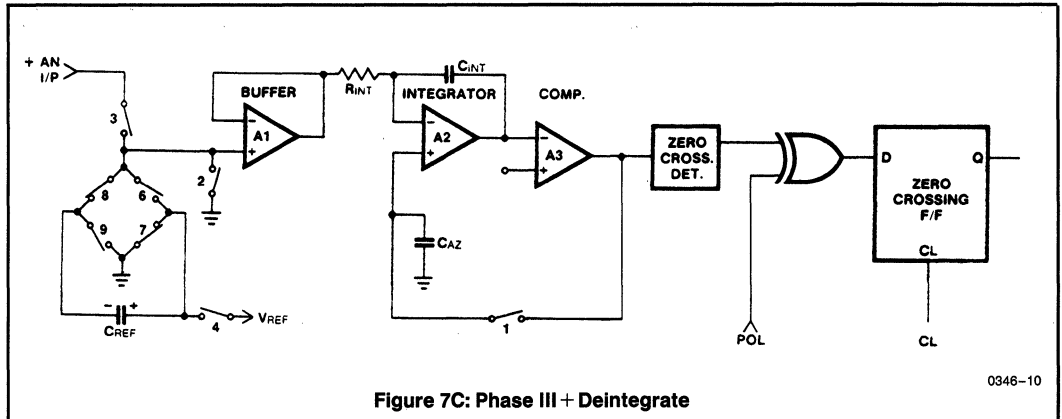
DETAILED DESCRIPTION

Analog Section

Figure 7 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/Hold pin is left open or tied to $V+$, the system will perform conversions at a rate determined by the clock frequency: 131,072 for — 16 and 32,368 for — 14 clock periods per cycle (see Figure 9 conversion timing).

Auto-Zero Phase I Figure 7A

During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to V_{REF} .



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NOTE: All typical values have been characterized but are not tested.

Input Integrate Phase II Figure 7B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN} . At the end of this phase, the sign of the ramp is latched into the polarity F/F.

Deintegrate Phase III Figure 7C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (-) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate

phase, the input voltage required to give a full scale reading = $2V_{REF}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/Hold is manipulated, see Run/Hold Input in detailed description, digital section).

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 8. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1 to 2 μV , allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

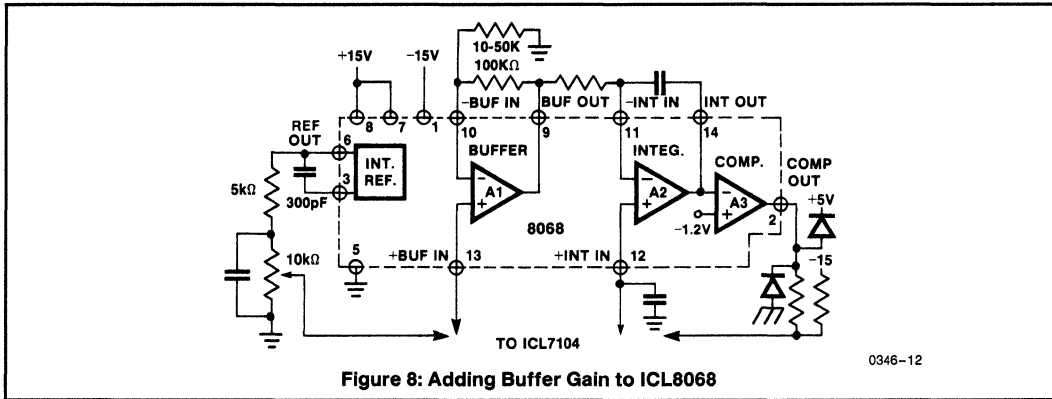


Figure 8: Adding Buffer Gain to ICL8068

Table 5: Typical Component Values ($V_{++} = +15V$, $V_{+} = 5V$, $V^{-} = -15V$, Clock Freq = 200kHz)

ICL8052/8068 with	ICL7104-16	ICL7104-14	Unit			
Full scale V_{IN}	200	800	4000	100	4000	mV
Buffer Gain	10	1	1	10	1	V/V
R_{INT}	100	43	200	47	180	k Ω
C_{INT}	.33	.33	.33	0.1	0.1	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	μF
C_{ref}	10	1.0	1.0	10	1.0	μF
V_{REF}	100	400	2000	50	2000	mV
Resolution	3.1	12	61	6.1	244	μV

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NOTE: All typical values have been characterized but are not tested.

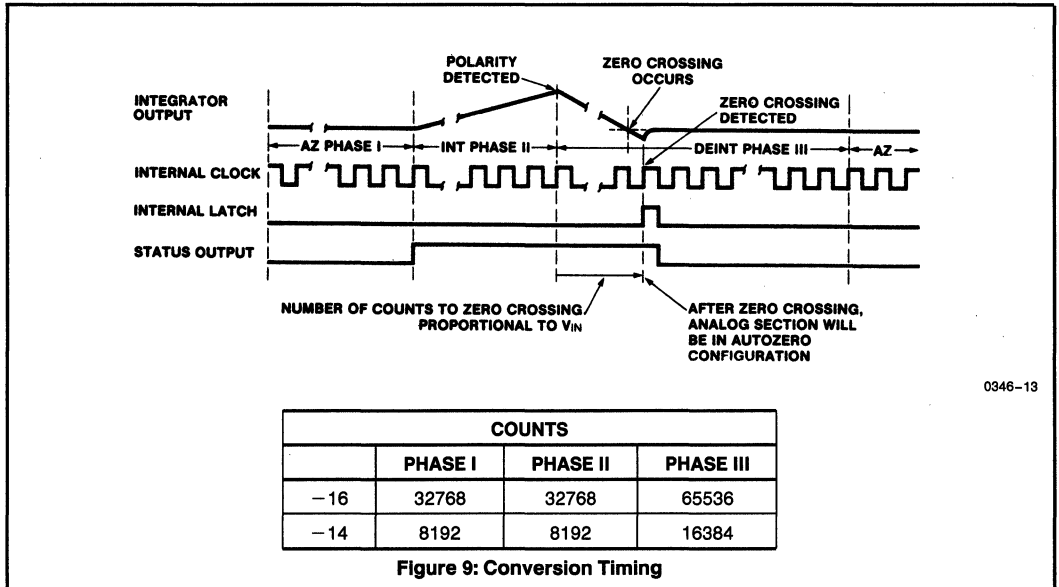


Figure 9: Conversion Timing

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ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40µA give good results with a nominal of 20µA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then —

$$R_{INT} = \frac{(\text{Buffer gain}) (\text{full scale voltage})}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14

volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\left[\begin{matrix} (32768 \text{ for } -16) \\ (8192 \text{ for } -14) \end{matrix} \right] \times 20\mu A \times \text{clock period}}{\text{Integrator Output Voltage Swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale (100 . . . 000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

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NOTE: All typical values have been characterized but are not tested.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2 V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16 or 14 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 10 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power

consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pull-down resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 9 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

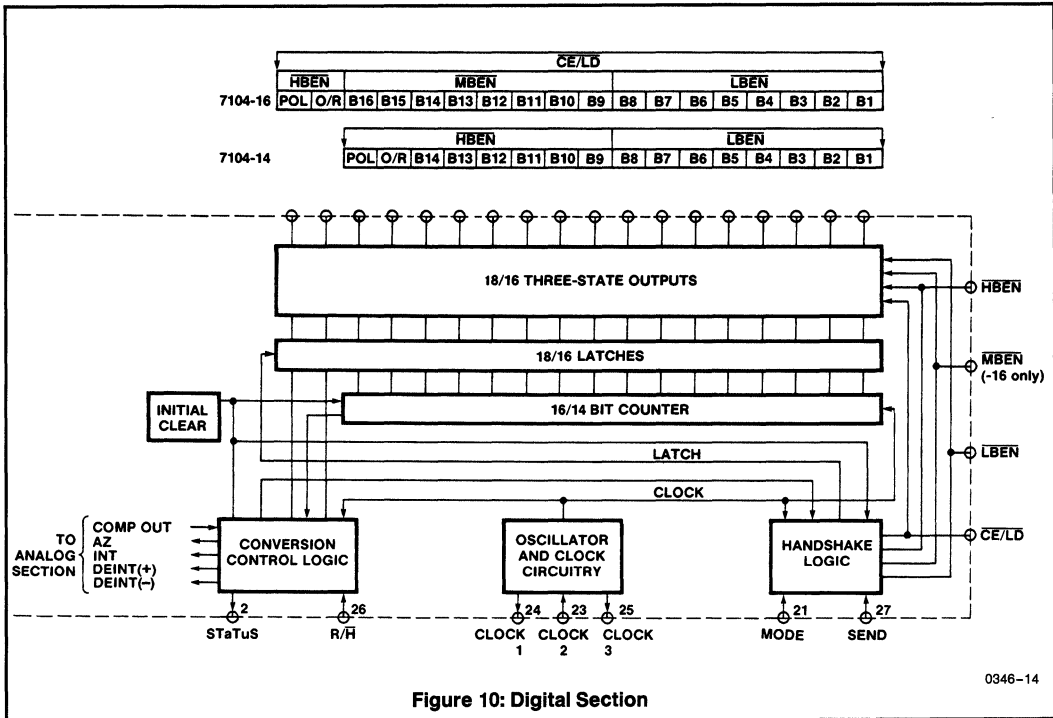
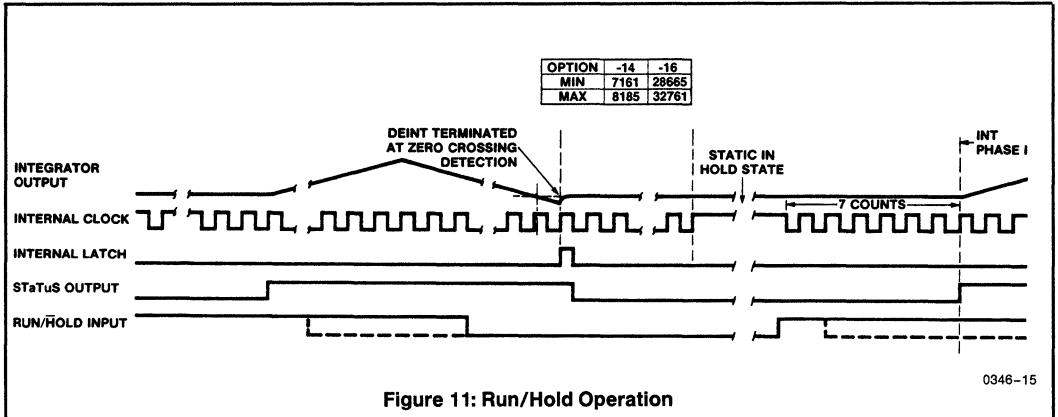


Figure 10: Digital Section

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Run/Hold Input

When the Run/Hold input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 9). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16 and 32768 for 7104-14 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 11 for details.

Using the Run/Hold input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/Hold low. When Run/Hold goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred) to the UART — see Handshake Mode). Run/Hold may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/Hold can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/Hold input can be provided by connecting it to the CLOCK3 (-14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Inte-

grate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs [bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes] are accessible under control of the byte and chip ENable terminals as inputs. These ENable inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip ENable input is low, taking a byte ENable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

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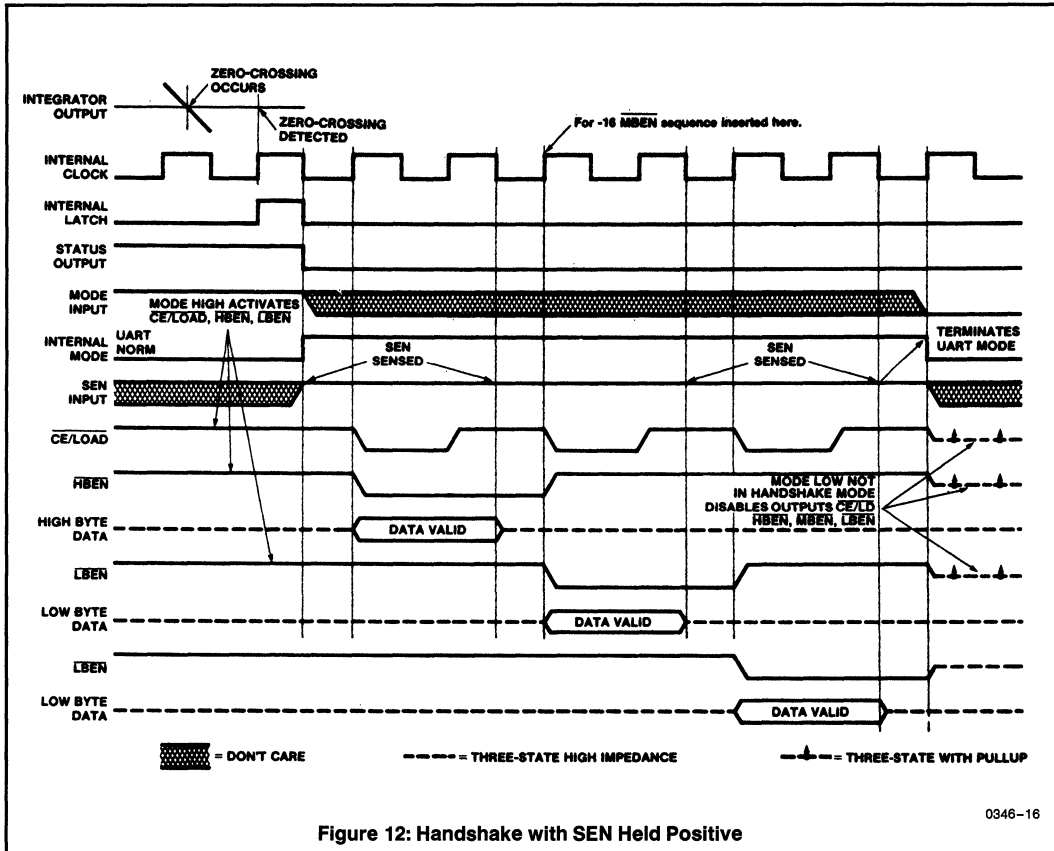
NOTE: All typical values have been characterized but are not tested.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte $\overline{\text{ENable}}$ terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send $\overline{\text{ENable}}$ pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed

once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte $\overline{\text{ENable}}$ line goes low, and the Chip $\overline{\text{ENable/Load}}$ pin (pin 30) ($\overline{\text{CE/LD}}$) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte $\overline{\text{ENable}}$ pin will be cleared high, and (unless finished) the $\overline{\text{CE/LD}}$ and the next byte $\overline{\text{ENable}}$ pin will go low. This will continue until all three (2 in the case of the 14 bit device) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte $\overline{\text{ENable}}$ pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip $\overline{\text{ENable}}$ will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 12, 13, and 14, and Table 2.



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ICL8052/ICL7104 and ICL8068/ICL7104



Figure 12 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the \overline{CE}/LD , \overline{LBEN} , \overline{MBEN} and \overline{HBEN} terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next to high internal clock edge, the \overline{CE}/LD and the \overline{HBEN} outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bits 9 – 14) outputs are enabled. The \overline{CE}/LD output remains low for one full internal clock period only, the data outputs remain active for $1\frac{1}{2}$ internal clock periods, and the high byte \overline{ENable} remains low for two clock periods. Thus the \overline{CE}/LD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte \overline{ENable} as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using \overline{CE}/LD , \overline{MBEN} and \overline{LBEN} while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14).

Figure 13 shows an output sequence where the SEN input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the \overline{CE}/LD terminal of the ICL7104

drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The \overline{CE}/LD and \overline{HBEN} terminals will go low after SEN is sensed, and the high order byte outputs become active. When \overline{CE}/LD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the \overline{HBEN} output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the \overline{HBEN} output returns high. At the same time, the \overline{CE}/LD and \overline{MBEN} (-16) or \overline{LBEN} outputs go low, and the corresponding byte outputs become active. Similarly, when the \overline{CE}/LD returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for \overline{LBEN} . One-half internal clock later, the handshake mode will be cleared, and the chip and byte \overline{ENable} terminals return high and stay active (as long as MODE stays high).

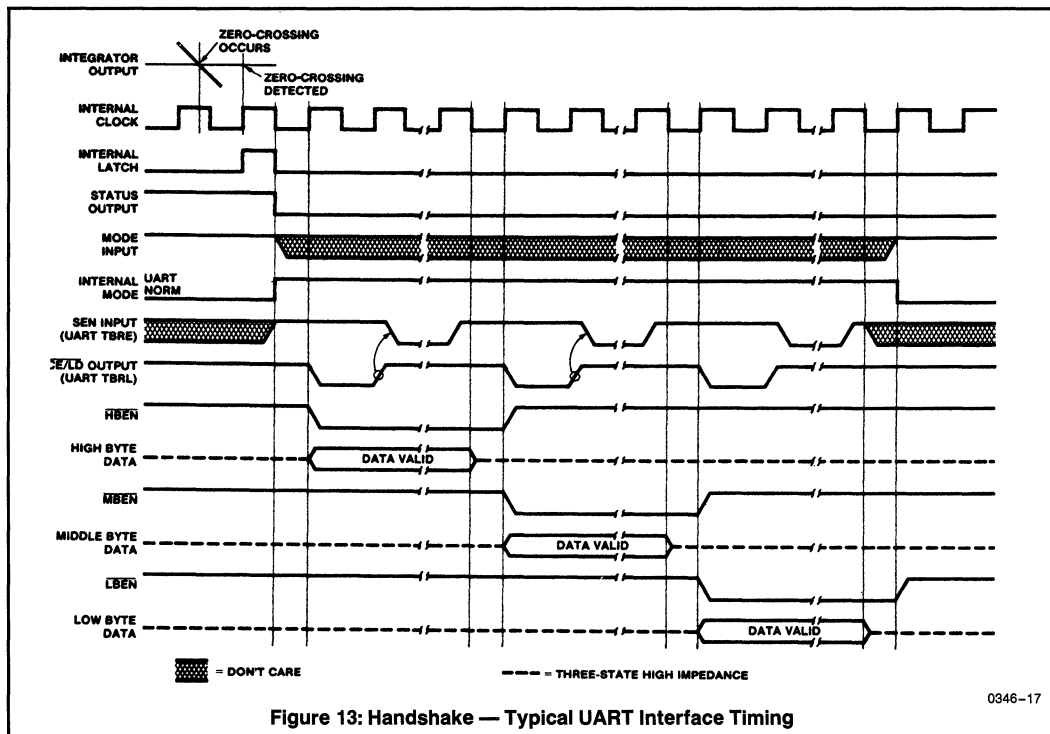
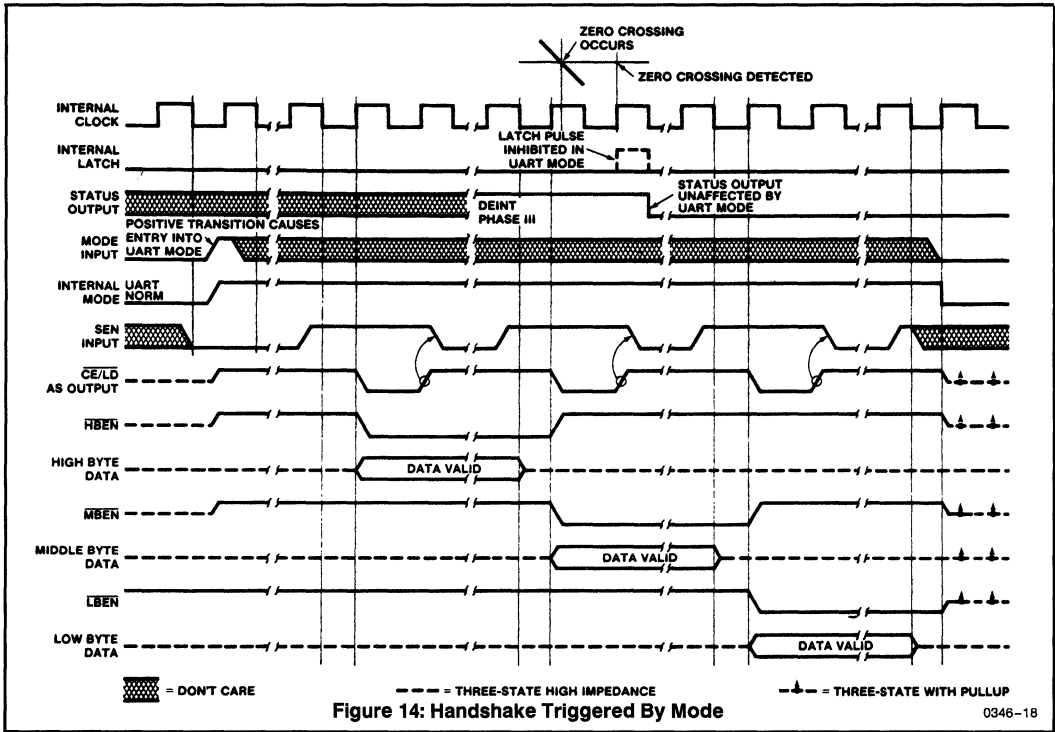


Figure 13: Handshake — Typical UART Interface Timing

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With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 14 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/Hold input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V₊ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" F/F cleared (i.e. in "direct" mode). This, however, will also clear these regis-

ters if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" F/F should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to bus conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE F/F will be cleared as fast as possible (see Figure 12 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 15 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by $f = .45/RC$. A 50 - 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14) clock periods is close to an integral multiple of the 60Hz period.

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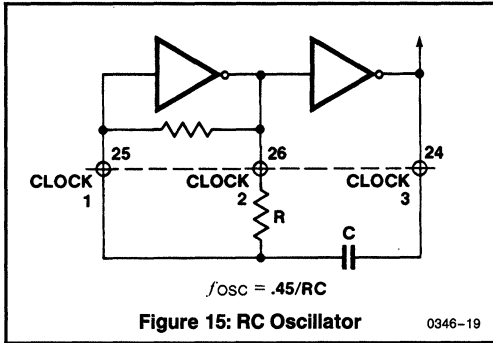


Figure 15: RC Oscillator

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Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 16 shows a crystal oscillator circuit, which can be used with both 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

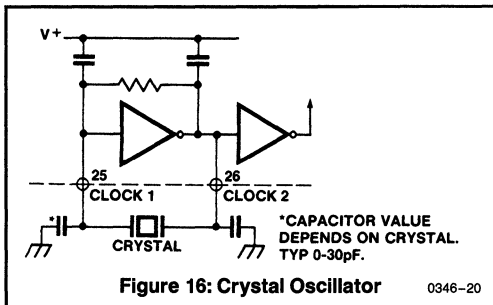


Figure 16: Crystal Oscillator

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POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occurring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V+ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL8068 or ICL8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 17.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

- A016** "Selecting A/D Converters", by Dave Fullagar
- A017** "The Integrating A/D Converter", by Lee Evans
- A018** "Do's and Don't's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
- A025** "Building a Remote Data Logging Station", by Peter Bradshaw
- A030** "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
- R005** "Interfacing Data Converter & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

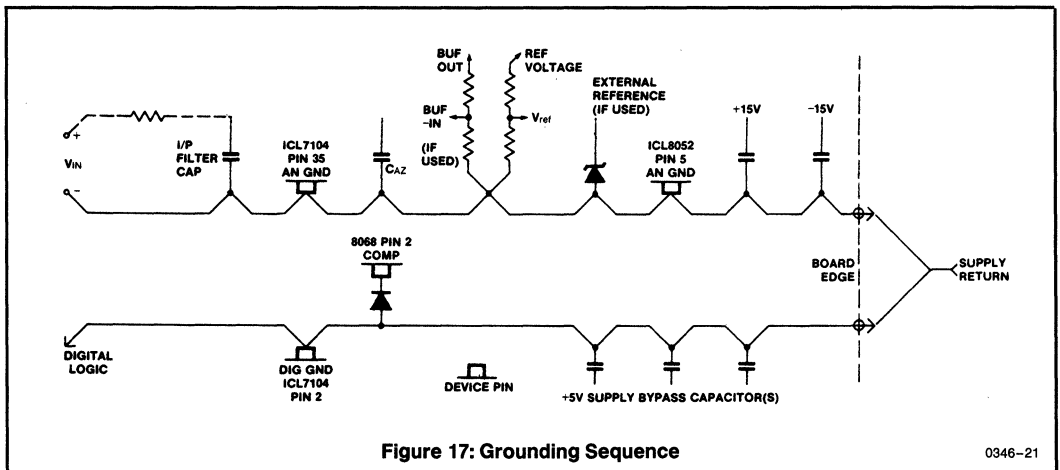


Figure 17: Grounding Sequence

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V⁺) +6.2V
 Negative Supply Voltage (GND to V⁻) -9V
 Analog Input Voltage (Lo or Hi) (Note 1) V⁺ to V⁻
 Reference Input Voltage (Lo or Hi) (Note 1) V⁺ to V⁻
 Digital Input Voltage V⁺ + 0.3V
 (Pins 2-27) (Note 2) GND - 0.3V

Power Dissipation (Note 3)
 Ceramic Package 1W @ +85°C
 Plastic Package 500mW @ +70°C
 Operating Temperature
 Ceramic Package (MDL) -55°C to +125°C
 Ceramic Package (IDL) -25°C to +85°C
 Plastic Package (CPL) 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Lead Temperature (Soldering, 10sec) +300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V⁺ = +5V, V⁻ = -5V, GND = 0V, T_A = 25°C, f_{CLK} = 3.58 MHz, unless otherwise indicated.) Test circuit as shown on first page of this data sheet.

ANALOG SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Zero Input Reading	V _{IN} = 0.0V Full Scale = 409.6mV	-0000 ₈	±0000 ₈	+0000 ₈	Octal Reading
	Ratiometric Reading	V _{IN} = V _{REF} V _{REF} = 204.8mV	3777 ₈	3777 ₈ 4000 ₈	4000 ₈	Octal Reading
	Non-Linearity (Max deviation from best straight line fit)	Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 4), (Note 6)	-1	±.2	+1	Counts
	Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)	Full Scale = 409.6mV to 2.048V (Note 5), (Note 6)	-1	±.2	+1	Counts
CMRR	Common Mode Rejection Ratio	V _{CM} ± 1V V _{IN} = 0V Full Scale = 409.6mV		50		μV/V
VCMR	Input Common Mode Range	Input Hi, Input Lo, Common (Note 4)	V ⁻ + 1.5		V ⁺ - 1.0	V
e _n	Noise (p-p value not exceeded 95% of time)	V _{IN} = 0V Full Scale = 409.6mV		15		μV
I _{ILK}	Leakage current at Input	V _{IN} = 0 All devices at 25°C ICL7109CPL 0°C ≤ T _A ≤ +70°C (Note 4) ICL7109IDL -25°C ≤ T _A ≤ +85°C (Note 4) ICL7109MDL -55°C ≤ T _A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
	Zero Reading Drift	V _{IN} = 0V R ₁ = 0Ω (Note 4)		0.2	1	μV/°C
	Scale Factor Temperature Coefficient	V _{IN} = 408.9mV = >7770 ₈ reading Ext. Ref. 0 ppm/°C (Note 4)		1	5	ppm/°C
I ₊	Supply Current V ⁺ to GND	V _{IN} = 0, Crystal Osc 3.58MHz test circuit		700	1500	μA
I _{SUPP}	Supply Current V ⁺ to V ⁻	Pins 2-21, 25, 26, 27, 29; open		700	1500	μA
V _{REF}	Ref Out Voltage	Referred to V ⁺ , 25kΩ between V ⁺ and REF OUT	-2.4	-2.8	-3.2	V
	Ref Out Temp. Coefficient	25kΩ between V ⁺ and REF OUT		80		ppm/°C

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V^+ = +5V$, $V^- = -5V$, $GND = 0V$, $T_A = 25^\circ C$, unless otherwise indicated.) Test circuit as shown on first page of this data sheet. (Continued)

DIGITAL SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	$I_{OUT} = 100\mu A$ Pins 2-16, 18, 19, 20	3.5	4.3		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1.6mA$		0.2	0.4	V
	Output Leakage Current	Pins 3-16 high impedance		$\pm .01$	± 1	μA
	Control I/O Pullup Current	Pins 18, 19, 20 $V_{OUT} = V^+ - 3V$ MODE input at GND		5		μA
	Control I/O Loading	\overline{HBEN} Pin 19 \overline{LBEN} Pin 18 (Note 4)			50	pF
V_{IH}	Input High Voltage	Pins 18-21, 26, 27 referred to GND	2.5			V
V_{IL}	Input Low Voltage	Pins 18-21, 26, 27 referred to GND			1	V
	Input Pull-up Current	Pins 26, 27 $V_{OUT} = V^+ - 3V$		5		μA
	Input Pull-up Current	Pins 17, 24 $V_{OUT} = V^+ - 3V$		25		μA
	Input Pull-down Current	Pin 21 $V_{OUT} = GND + 3V$		5		μA
O_{OH}	Oscillator Output Current	High	$V_{OUT} = 2.5V$		1	mA
O_{OL}		Low	$V_{OUT} = 2.5V$		1.5	mA
BO_{OH}	Buffered Oscillator Output Current	High	$V_{OUT} = 2.5V$		2	mA
BO_{OL}		Low	$V_{OUT} = 2.5V$		5	mA
t_W	MODE Input Pulse Width	(Note 4)	50			ns

- NOTES:**
1. Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100\mu A$
 2. Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.
 3. This limit refers to that of the package and will not be obtained during normal operation.
 4. This parameter is not production tested, but is guaranteed by design.
 5. Roll-over error for $T_A = -55^\circ C$ to $+125^\circ C$ is ± 3 counts maximum.
 6. A full scale voltage of 2.048V is used because a full scale voltage of 4.096V exceeds the devices Common Mode Voltage Range.

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NOTE: All typical values have been characterized but are not tested.

TABLE 1: Pin Assignment and Function Description

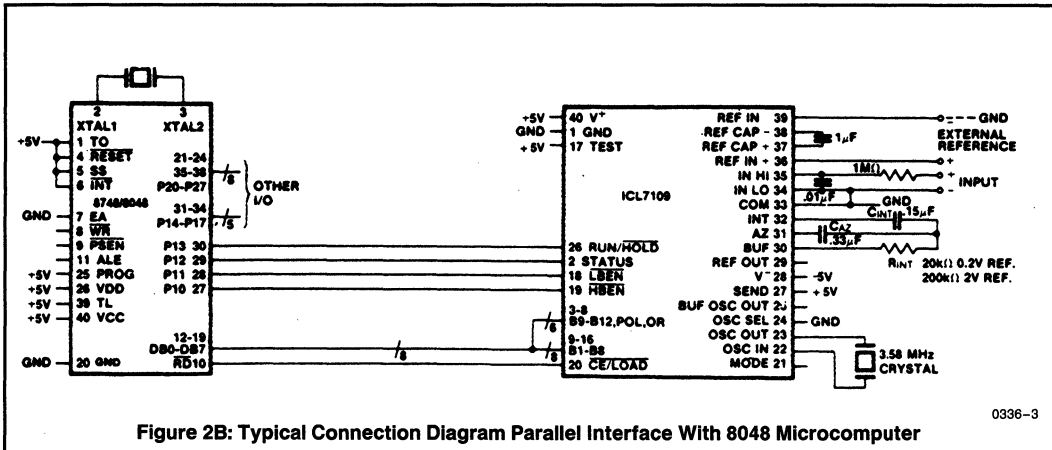
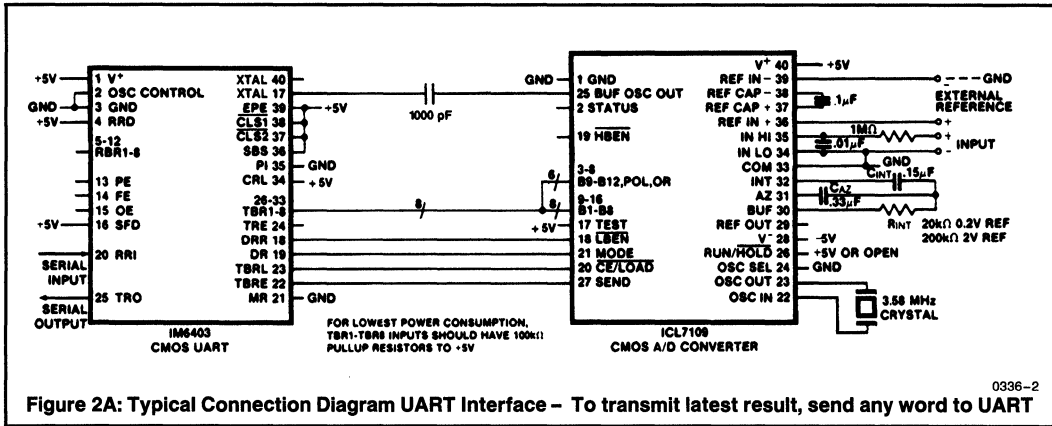
Pin	Symbol	Description	
1	GND	Digital Ground, 0V. Ground return for all digital logic.	
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.	
3	POL	Polarity — HI for Positive input.	
4	OR	Overrange — HI if Overranged.	
5	B12	Bit 12	All three state output data bits
6	B11	Bit 11	
7	B10	Bit 10	
8	B9	Bit 9	
9	B8	Bit 8	
10	B7	Bit 7	
11	B6	Bit 6	
12	B5	Bit 5	
13	B4	Bit 4	
14	B3	Bit 3	
15	B2	Bit 2	
16	B1	Bit 1	(Least Significant Bit)
17	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.	
18	LBEN	Low Byte Enable — With Mode (Pin 21) low, and CE/LOAD (Pin 20) low, taking this pin low activates low order byte outputs B1 — B8. — With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 8, 9, 10.	
19	HBEN	High Byte Enable — With Mode (Pin 21) low, and CE/LOAD (Pin 20) low, taking this pin low activates high order byte outputs B9 — B12, POL, OR. — With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 8, 9, 10.	
20	CE/LOAD	Chip Enable Load — With Mode (Pin 21) low. CE/LOAD serves as a master output enable. When high, B1 — B12, POL, OR outputs are disabled. — With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 8, 9, 10.	

Pin	Symbol	Description
21	MODE	Input Low — Direct output mode where CE/LOAD (Pin 20), HBEN (Pin 19) and LBEN (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 10. Input High — Enables CE/LOAD (Pin 20), HBEN (Pin 19), and LBEN (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 8 and 9 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. — Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/HOLD	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to +5V if not used.
28	V-	Analog Negative Supply — Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V* (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node — Inside foil of CAZ
32	INTEGRATOR	Integrator Output — Outside foil of CINT
33	COMMON	Analog Common — System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP -	Reference Capacitor Negative
39	REF IN -	Differential Reference Input Negative
40	V+	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

Note: All digital levels are positive true.

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NOTE: All typical values have been characterized but are not tested.



3

DETAILED DESCRIPTION

Analog Section

Figure 3 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/HOLD input is left open or connected to V+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 4. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

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NOTE: All typical values have been characterized but are not tested.

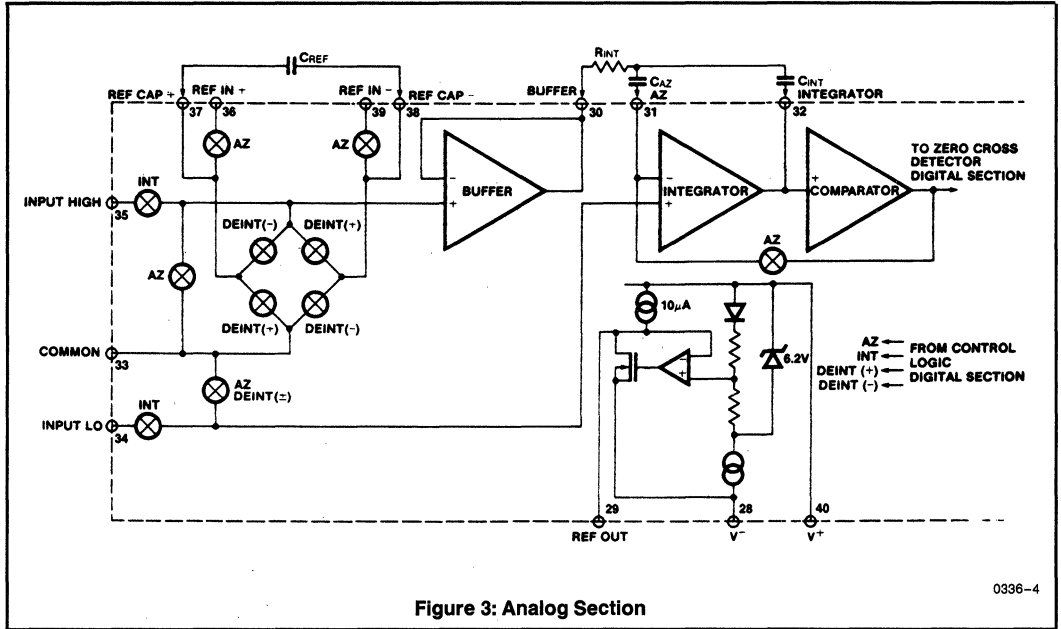


Figure 3: Analog Section

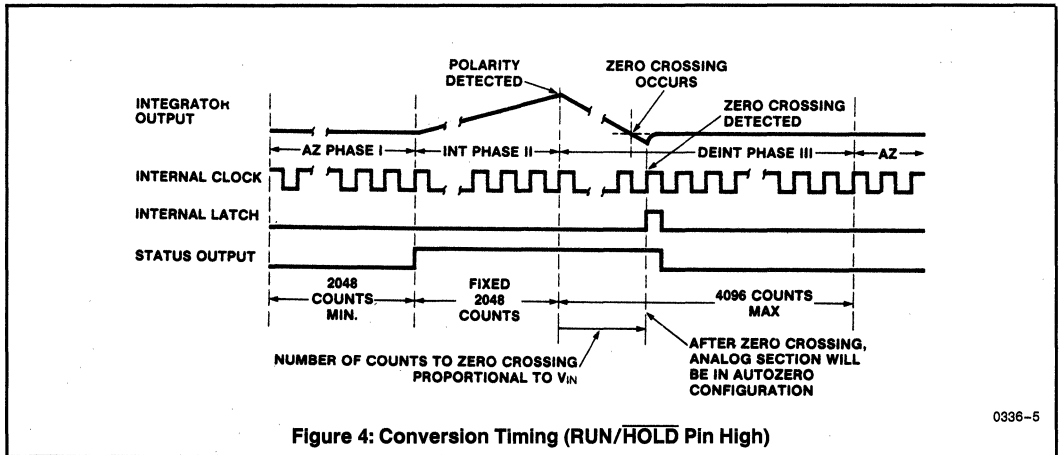


Figure 4: Conversion Timing (RUN/HOLD Pin High)

Signal Integrate Phase

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

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Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and -5V, this allows a 4V full scale integrator swing positive or negative thus maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be

reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They supply 20µA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72kHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15µF and 0.33µF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{(2048 \times \text{clock period})(20\mu A)}{\text{integrator output voltage swing}}$$

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system: the smaller the capacitor the lower the overall system noise. However, C_{AZ} cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mV full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

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NOTE: All typical values have been characterized but are not tested.

Reference Capacitor

A 1 μF capacitor gives good results in most applications. However, where a large reference common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10 μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

Reference Voltage

The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 33k Ω and 0.15 μF . This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

Reference Sources

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFERENCE OUTPUT (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10 μA . The output voltage is nominally 2.8V below V^+ , and has a temperature coefficient of $\pm 80\text{ppm}/^\circ\text{C}$ typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF- (pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+ . The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25k Ω precision potentiometer between REF OUT and V^+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1k Ω resistor in series with pin 39.

DETAILED DESCRIPTION

Digital Selection

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in Figure 5.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in the Electrical Characteristics Table. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5k Ω pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 4 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/HOLD Input

When the RUN/HOLD input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 4). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/HOLD goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/HOLD stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/HOLD input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/HOLD. See Figure 6 for details.

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NOTE: All typical values have been characterized but are not tested.

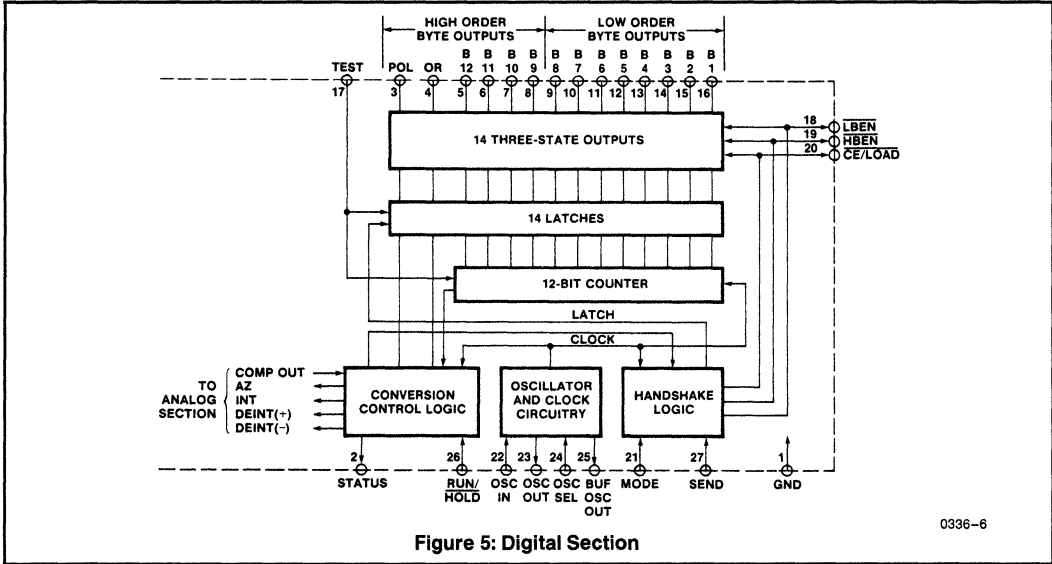


Figure 5: Digital Section

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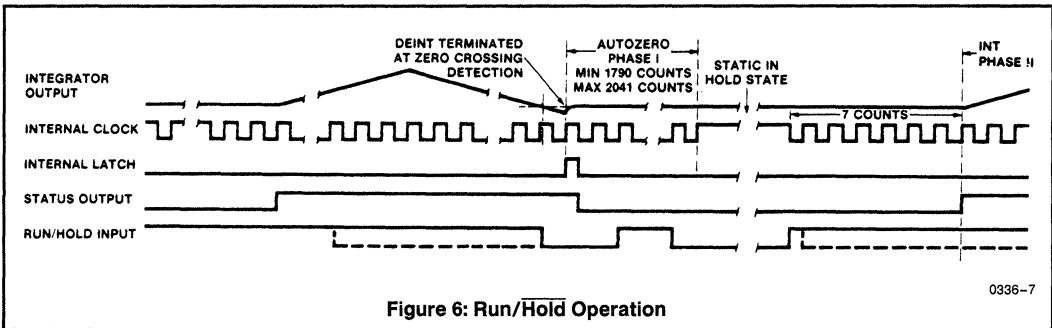


Figure 6: Run/Hold Operation

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Using the RUN/HOLD input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/HOLD low. When RUN/HOLD goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART — see Handshake Mode). RUN/HOLD may now be taken low which terminates deintegrate and ensures a minimum Auto-Zero time before the next conversion.

Alternately, RUN/HOLD can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/HOLD input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/HOLD to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 7 and Table 2.

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NOTE: All typical values have been characterized but are not tested.

Table 2 — Direct Mode Timing Requirements
(See Note 4 of Electrical Characteristics)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t _{BEA}	Byte Enable Width	350	220		ns
t _{DAB}	Data Access Time from Byte Enable		210	350	ns
t _{DHB}	Data Hold Time from Byte Enable		150	300	ns
t _{CEA}	Chip Enable Width	400	260		ns
t _{DAC}	Data Access Time from Chip Enable		260	400	ns
t _{DHC}	Data Hold Time from Chip Enable		240	400	ns

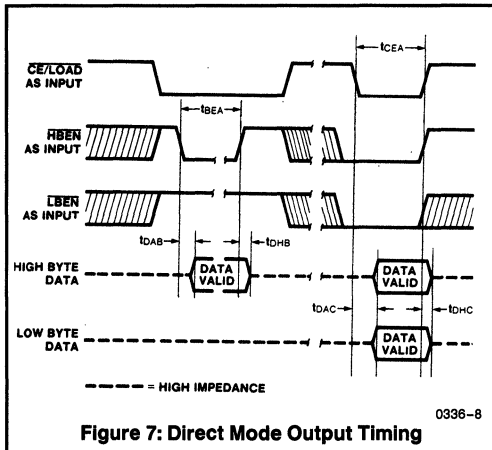


Figure 7: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the latches while they are being updated, which could lead to erroneous data. Synchronizing the access of the latches with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil IM6402/3) with no external logic required. When triggered into the handshake mode, the

ICL7109 provides all the control and flag signals necessary to sequentially transfer two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of a conversion (See Figures 8 and 9). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 10) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 8, 9, and 10).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 8 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse, and since MODE remains high the CE/LOAD, LBEN and HBEN terminals are active as outputs. The high level at the SEND input is sensed on the same high to low internal clock edge that terminates the data latch pulse. On the next low to high internal clock edge the CE/LOAD and the HBEN outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The CE/LOAD output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the CE/LOAD output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using CE/LOAD and LBEN while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 9 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM640 2/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the CE/LOAD terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

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NOTE: All typical values have been characterized but are not tested.

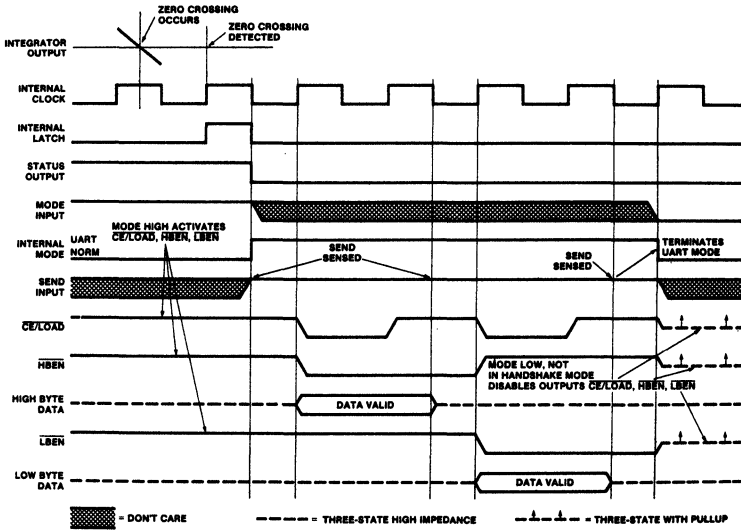


Figure 8: Handshake With Send Held Positive

0336-9

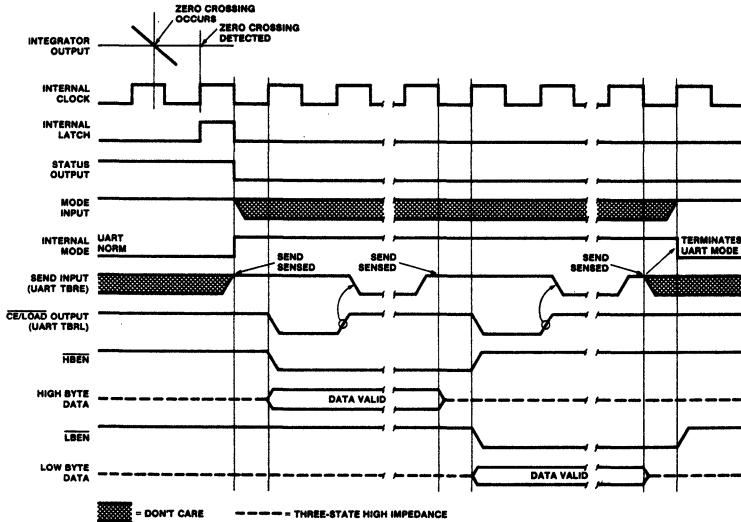


Figure 9: Handshake — Typical UART Interface Timing

0336-10

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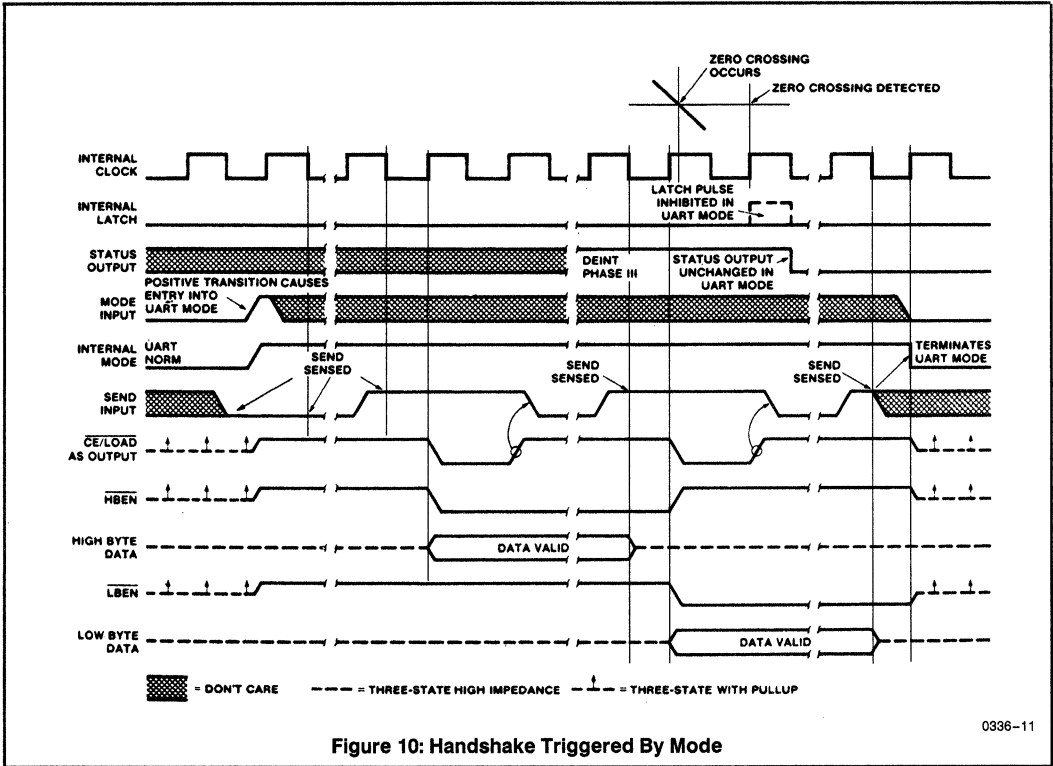


Figure 10: Handshake Triggered By Mode

0336-11

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The CE/LOAD and HBEN terminals will go low after SEND is sensed, and the high order byte outputs become active. When CE/LOAD goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the HBEN output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the HBEN output returns high. At the same time, the CE/LOAD and LBEN outputs go low, and the low order byte outputs become active. Similarly, when the CE/LOAD returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the CE/LOAD, HBEN, and LBEN terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/HOLD input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated with an RC network or crystal. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

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NOTE: All typical values have been characterized but are not tested.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 11. The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but should not be less than 50pF).

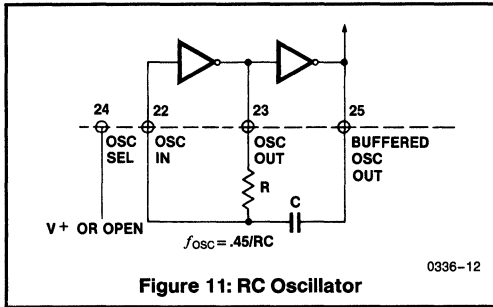


Figure 11: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 12, the oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock.

$$T = (2048 \text{ clock periods}) \times \left[\frac{58}{3.58\text{MHz}} \right] = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

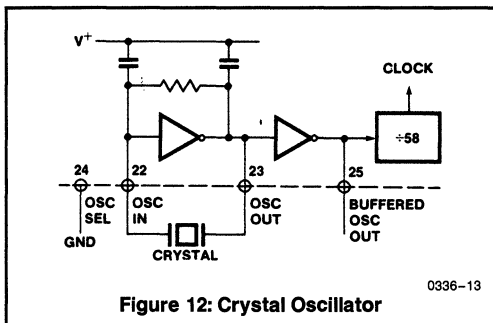


Figure 12: Crystal Oscillator

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive capability, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V+ - GND) voltage (or to V+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

3

INTERFACING

Direct Mode

Figure 13 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The CE/LOAD input may be tied low, allowing either byte to be controlled by its own enable as in Figure 13A. Figure 13B shows a configuration where the two byte enables are connected together. In this configuration, the CE/LOAD serves as a chip enable, and the HBEN and LBEN may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 13C shows the HBEN and LBEN as flag inputs, and CE/LOAD as a master enable, which could be the READ strobe available from most microprocessors.

Figure 14 shows an approach to interfacing several ICL7109s to a bus, ganging the HBEN and LBEN signals to several converters together, and using the CE/LOAD inputs (perhaps decoded from an address) to select the desired converter.

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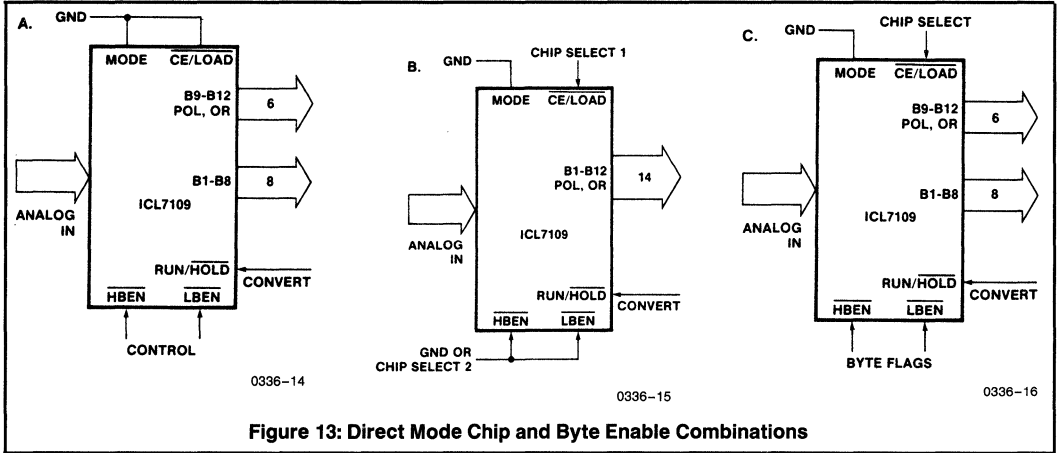


Figure 13: Direct Mode Chip and Byte Enable Combinations

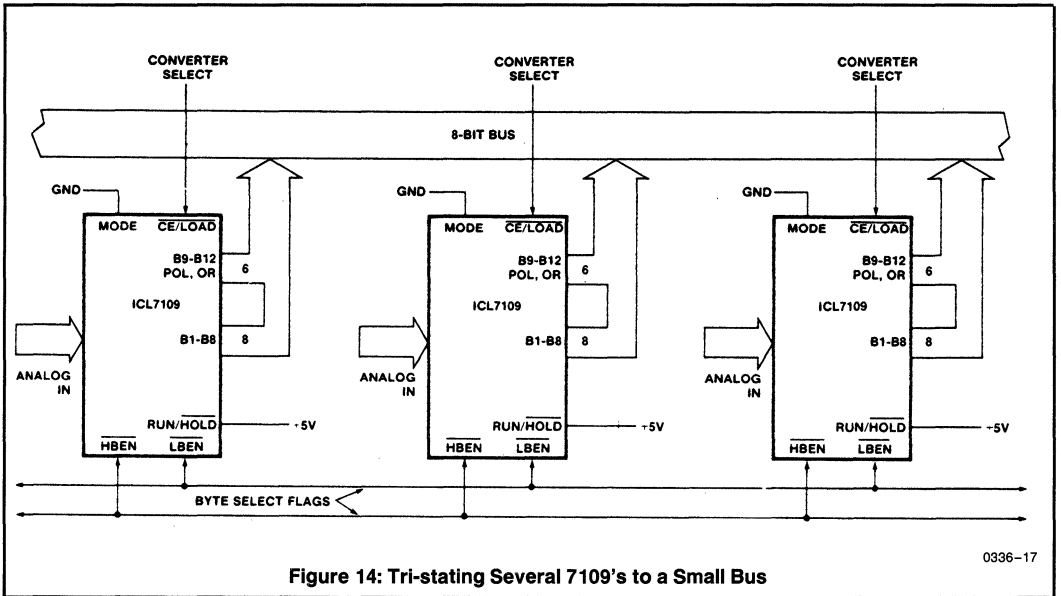


Figure 14: Tri-stating Several 7109's to a Small Bus

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 15 through 20. Figure 15 shows a straightforward application to the Intel 8048/80/85 microprocessors via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2

converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 16. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data latches. This application also shows the RUN/HOLD input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or Rockwell R650X systems is shown in Figure 17. The high to low transition of the STATUS output generates an interrupt via the

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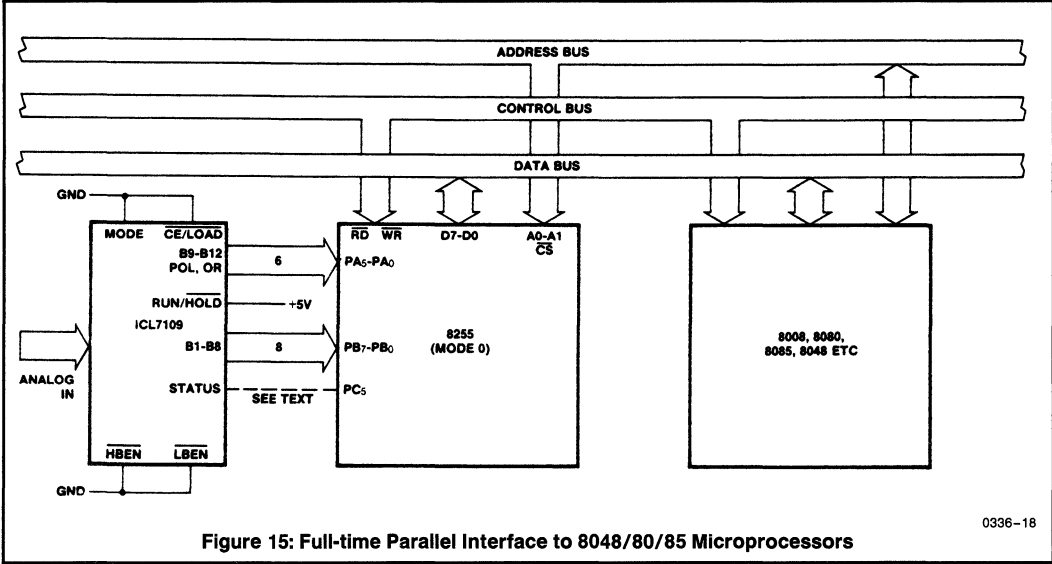


Figure 15: Full-time Parallel Interface to 8048/80/85 Microprocessors

0336-18

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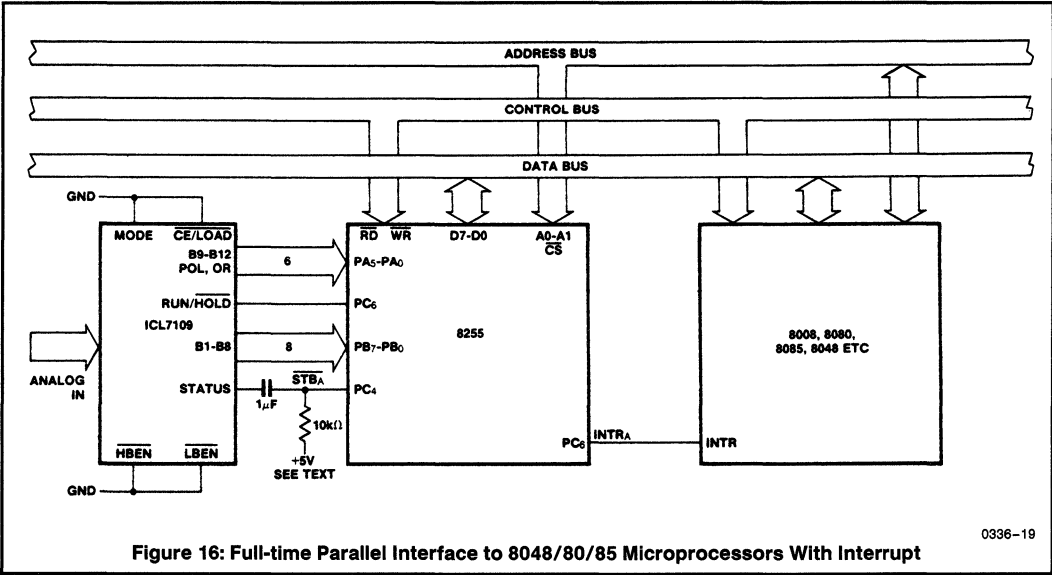


Figure 16: Full-time Parallel Interface to 8048/80/85 Microprocessors With Interrupt

0336-19

Control Register B CB1 line. Note that CB2 controls the RUN/HOLD pin through Control Register B, allowing software-controlled initiation of conversions in this system as well.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 18 and 19. It is necessary to carefully consider the system timing in this type of interface,

to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long buses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

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NOTE: All typical values have been characterized but are not tested.

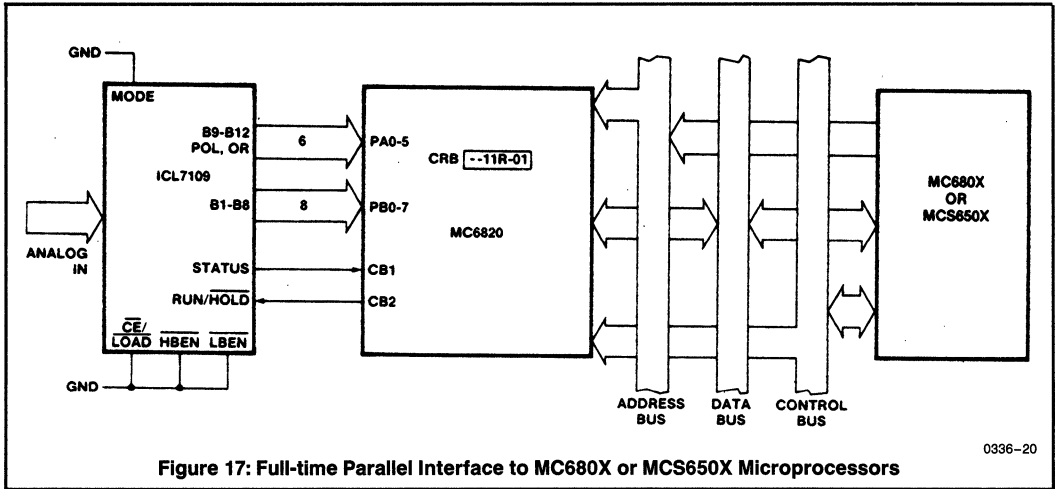


Figure 17: Full-time Parallel Interface to MC680X or MCS650X Microprocessors

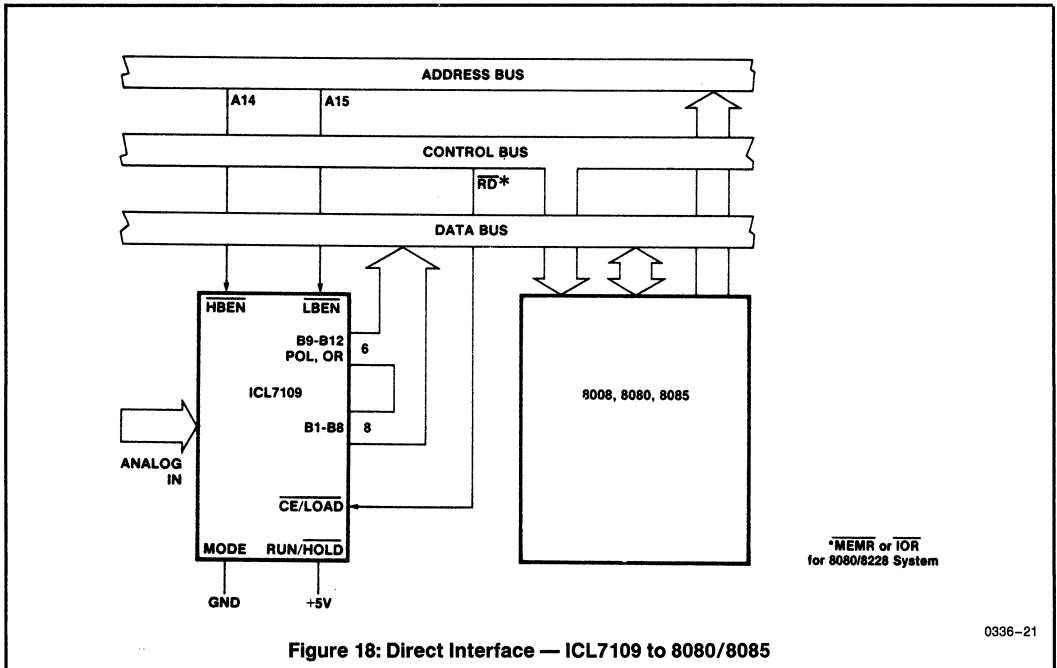


Figure 18: Direct Interface — ICL7109 to 8080/8085

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NOTE: All typical values have been characterized but are not tested.

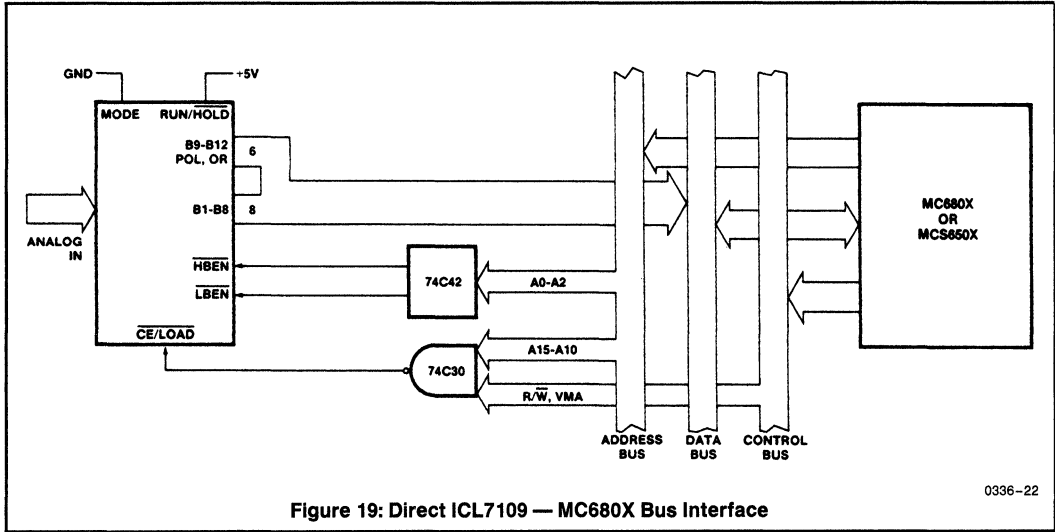


Figure 19: Direct ICL7109 — MC680X Bus Interface

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3

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/HOLD input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command

under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

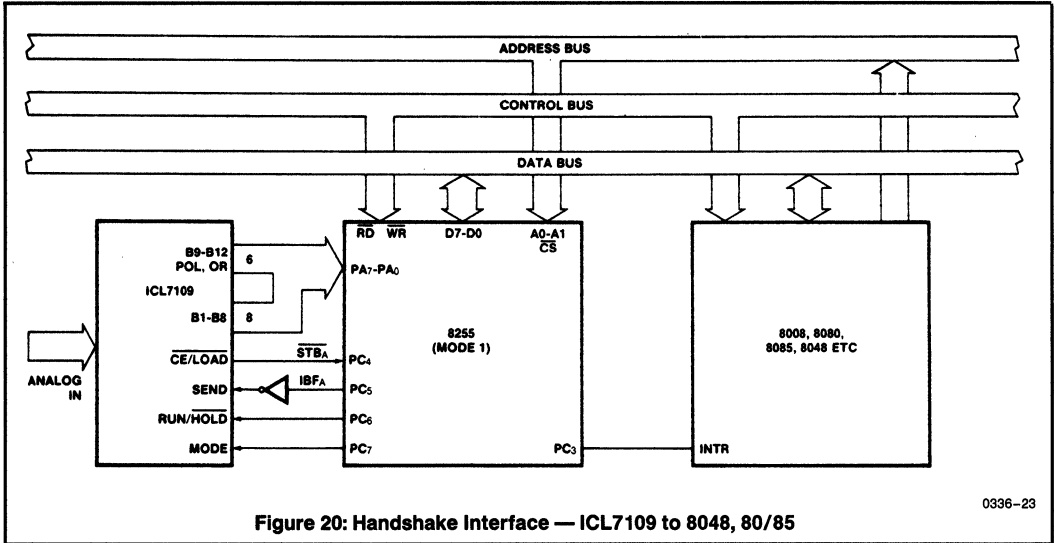
Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/HOLD are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown in Figure 2A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, \overline{LBEN} will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

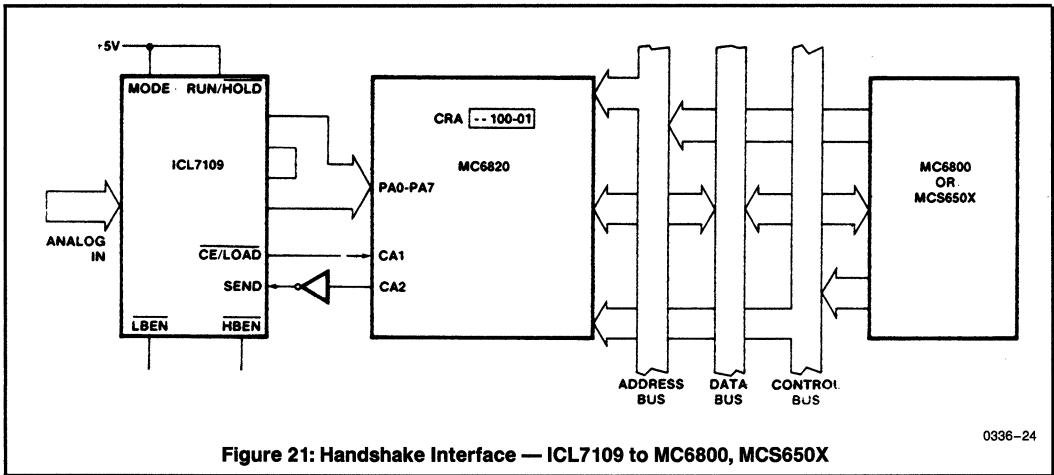
Figure 22 shows an extension of the one converter — one UART scheme to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

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NOTE: All typical values have been characterized but are not tested.



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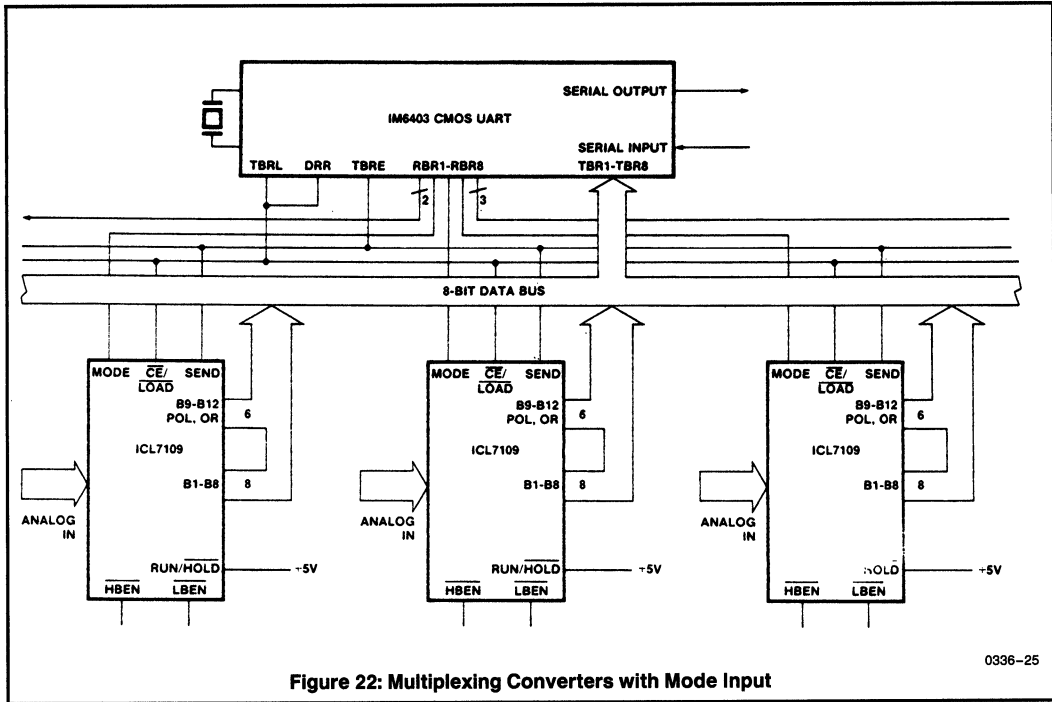


Figure 22: Multiplexing Converters with Mode Input

0396-25

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/HOLD, and MODE signals may be mixed.

APPLICATION NOTES

- A016 "Selecting A/D Converters," by David Fullagar
- A017 "The Integrating A/D Converters," by Lee Evans
- A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw
- A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw
- R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

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NOTE: All typical values have been characterized but are not tested.

ICL7112

12-Bit High-Speed CMOS μ P-Compatible A/D Converter

ADVANCE
INFORMATION



GENERAL DESCRIPTION

The ICL7112 is a monolithic 12-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 12-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is eased by the use of standard memory Write and Read cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8- and 16-bit systems.

The ICL7112 provides separate Analog and Digital grounds for increased system accuracy. Operating with $\pm 5V$ supplies, the ICL7112 accepts 0V to +10V input with a -10V reference or 0V to -10V input with a +10V reference.

FEATURES

- 12-Bit Resolution and Accuracy
- No Missing Codes
- Microprocessor Compatible Byte-Organized Buffered Outputs
- Auto-Zeroed Comparator for Low Offset Voltage
- Low Linearity and Gain Temperature Coefficients
- Low Power Consumption (60 mW)
- No Gain or Offset Adjustment Necessary
- Provides 3% Useable Overrange
- Fast Conversion (30 μ sec.)

ORDERING INFORMATION

Part Number	Resolution with No Missing Codes	Temperature Range	Package
ICL7112JC DL	11 Bits	0°C to +70°C	40 Pin Ceramic
ICL7112KC DL	12 Bits	0°C to +70°C	40 Pin Ceramic
ICL7112JIDL	11 Bits	-25°C to +85°C	40 Pin Ceramic
ICL7112KIDL	12 Bits	-25°C to +85°C	40 Pin Ceramic
ICL7112JMDL	11 Bits	-55°C to +125°C	40 Pin Ceramic
ICL7112KMDL	12 Bits	-55°C to +125°C	40 Pin Ceramic

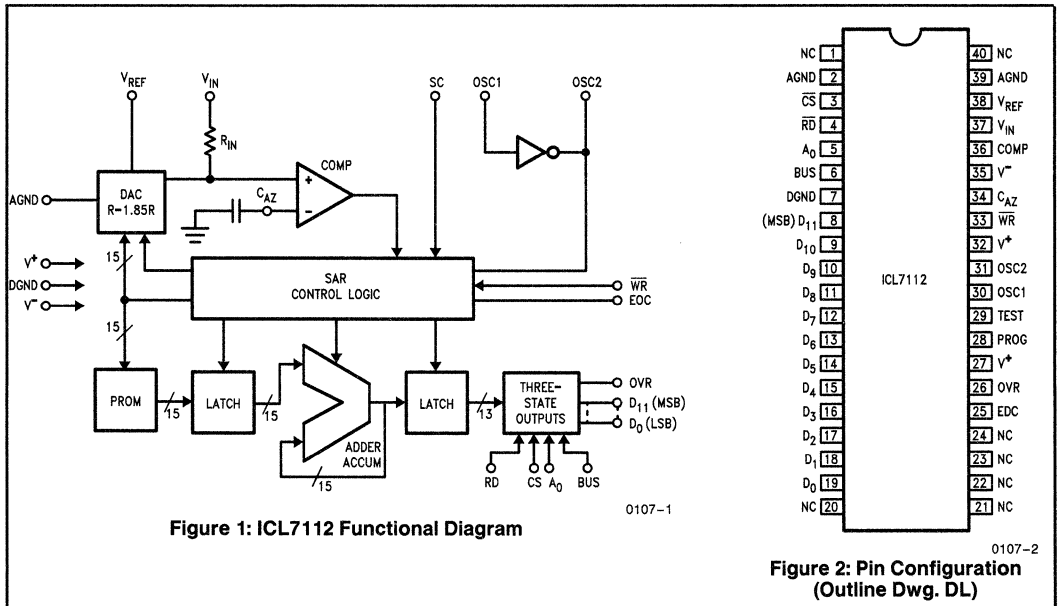


Figure 1: ICL7112 Functional Diagram

Figure 2: Pin Configuration (Outline Dwg. DL)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V^+ to DGND -0.3V to +6.5V
Supply Voltage V^- to DGND +0.3V to -6.5V
V_{REF} , V_{IN} to DGND $\pm 25V$
AGND to DGND +1V to -1V
V_{REF} , V_{IN} , AGND Current 25 mA
Digital I/O Pin Voltages -0.3V to ($V^+ + 0.3V$)
PROG to DGND Voltage V^- to ($V^+ + 0.3$)

Note 1: All voltages with respect to DGND, unless otherwise noted.

2: Assumes all leads soldered or welded to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Temperature

ICL7112XCXX 0°C to +70°C
ICL7112XIXX -25°C to +70°C
ICL7112MXX -55°C to +125°C
Storage Temperature -65°C to +150°C
Power Dissipation (Note 2) 500 mW
derate above 70°C @10 mW/°C	
Lead Temperature (soldering, 10 sec.) 300°C

D.C. ELECTRICAL CHARACTERISTICS

$V^+ = +5V$, $V^- = -5V$, $V_{REF} = -10.0V$, $T_A = +25^\circ C$, $f_{clk} = 500$ kHz unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	Resolution		12			Bits
I_{LE}	Integral Linearity Error	Note 1	J		± 0.024	%FSR
			K		± 0.012	%FSR
$T_{C(I_{LE})}$	Temperature Coefficient of I_{LE}	$T_A =$ Operating Range		1	1.5	ppm/°C
$RES_{(NMC)}$	Resolution with No Missing Codes		J	11		Bits
			K	12		
FSE	Full Scale Calibration Error	Adjustable to Zero			± 0.1	%FSR
ZE	Zero Error	Notes 1, 2			± 1	LSB
PSRR	Power Supply Rejection Ratio				± 1	LSB
V_{IN}	Analog Input Range (V_{IN} , V_{REF})		0		10	V
R_{IN}	Input Resistance (V_{IN} , V_{REF})		4		9	k Ω
I_{SUPPLY}	Supply Current I^+ , I^-			2	4	mA
V_{SUPPLY}	Supply Voltage Range	Functional Operation Only	± 4.5		± 6.0	V
V_{IL}	Low State Input Voltage				0.8	V
V_{IH}	High State Input Voltage		2.4			V
I_{LIH}	Logic Input Current	$0 < V_{IN} < V^+$		1	10	μA
V_{OL}	Low State Output Voltage	$I_{OUT} = 1.6$ mA			0.4	V
V_{OH}	High State Output Voltage	$I_{OUT} = 200$ μA	2.8			V
I_{OX}	Three-State Output Current	$0 < V_{OUT} < V^+$		1		μA
CR	Conversion Rate			30		μs

Note 1: Full Scale Range (FSR) is 10 V (reference adjusted).

2: Assume all leads soldered or welded to printed circuit board.

ADVANCE INFORMATION

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NOTE: All typical values have been characterized but are not tested.

ICL7115

14-Bit High-Speed CMOS μ P-Compatible A/D Converter



GENERAL DESCRIPTION

The ICL7115 is the first monolithic 14-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 13-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard **WRite** and **ReaD** cycle timing and control signals, combined with **Chip Select** and **Address** pins. The digital output pins are byte-organized and three-state gated for bus interface to 8 and 16-bit systems.

The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with $\pm 5V$ supplies, the ICL7115 accepts 0V to +5V input with a -5V reference or 0V to -5V input with a +5V reference.

ORDERING INFORMATION

Part Number	Resolution with No Missing Codes	Temp. Range	Package
ICL7115JCDL	12 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115KCDL	13 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115JIDL	12 Bits	-25°C to +85°C	40 Pin Ceramic
ICL7115KIDL	13 Bits	-25°C to +85°C	40 Pin Ceramic
ICL7115JMDL	12 Bits	-55°C to +125°C	40 Pin Ceramic
ICL7115KMDL	13 Bits	-55°C to +125°C	40 Pin Ceramic
ICL7115JMLL	12 Bits	-55°C to +125°C	40 Pin LCC
ICL7115KMLL	13 Bits	-55°C to +125°C	40 Pin LCC

FEATURES

- 14-Bit Resolution (LSB = 305 μ V)
- No Missing Codes
- Microprocessor Compatible Byte-Organized Buffered Outputs
- Fast Conversion (40 μ s)
- Auto-Zeroed Comparator for Low Offset Voltage
- Low Linearity and Gain Tempco (1.5ppm/°C, 5ppm/°C)
- Low Power Consumption (60mW)
- No Gain or Offset Adjustment Necessary
- Provides 3% Useable Overrange
- FORCE/SENSE and Separate Digital and Analog Ground Pins for Increased System Accuracy

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ABSOLUTE MAXIMUM RATINGS (Note 1)

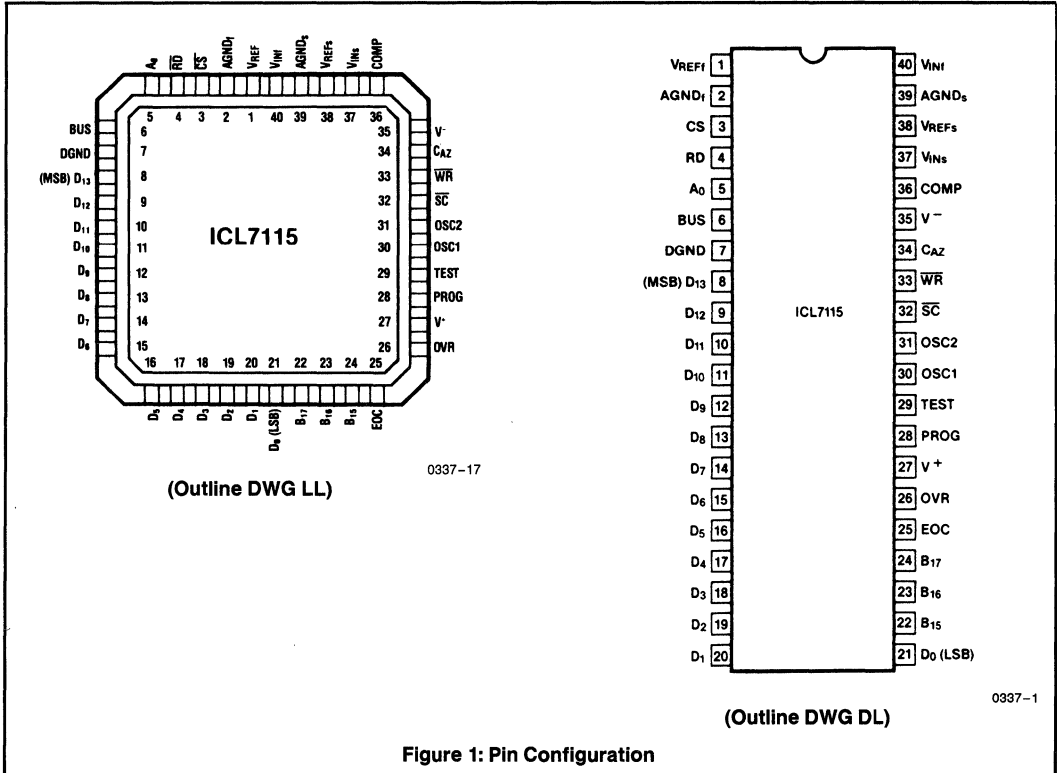
Supply Voltage V ⁺ to DGND -0.3V to +6.5V
Supply Voltage V ⁻ to DGND +0.3V to -6.5V
V _{REFs} , V _{REFf} , V _{INs} , V _{INf} to DGND +25V to -25V
AGND _s , AGND _f to DGND +1V to -1V
Current in FORCE and SENSE Lines 25mA
Digital I/O Pin Voltages -0.3V to V ⁺ +0.3V
PROG to DGND Voltage V ⁻ to V ⁺ +0.3V

Operating Temperature Range

ICL7115XCXX 0°C to +70°C
ICL7115IXXX -25°C to +85°C
ICL7115XMXX -55°C to +125°C
Storage Temperature Range -65°C to +150°C
Power Dissipation 500mW
derate above 70°C @ 100mW/°C	
Lead Temperature (Soldering, 10sec) 300°C

NOTE 1: All voltages with respect to DGND, unless otherwise noted.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS $V^+ = +5.0V$, $V^- = -5.0V$, $V_{REFS} = -5.0V$, $T_A = +25^\circ C$, $f_{CLK} = 500kHz$, $\overline{SC} = V_{IH}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Resolution	$\overline{SC} = V_{IH}$	14			Bits
		$\overline{SC} = V_{IL}$	12			
I_{LE}	Integral Linearity Error	Note 1	J		± 0.018	%FSR
			K		± 0.012	
$T_{C(I_{LE})}$	Temperature Coefficient of I_{LE}	$T_A =$ Operating Range		1	1.5	ppm/ $^\circ C$
$RES_{(NMC)}$	Min Resolution with No Missing Codes	$T_A = 25^\circ C$	J	12		Bits
			K	13		
		$T_A =$ Operating Range (Note 2)	J	11		
			K	12		
FSE	Full Scale Calibration Error (Adjustable to Zero)	J			± 0.1	%FSR
		K			± 0.08	
$T_{C(FSE)}$	Temperature Coefficient of FSE	$T_A =$ Operating Range		2	5	ppm/ $^\circ C$
ZE	Zero Error	Notes 1,2			± 1	LSB
$T_{C(ZE)}$	Temperature Coefficient of ZE	$T_A =$ Operating Range			1	ppm/ $^\circ C$
PSRR	Power Supply Rejection Ratio	$T_A = 25^\circ C$		$\pm 1/2$	± 1	LSB
		$T_A =$ Operating Range			± 2	
V_{IN}	Analog Input Range (V_{INs} , V_{REFs})		0 to +5			V
R_{IN}	Input Resistance (V_{INs} , V_{REFs})	Note 3	4		9	k Ω
$T_{C(R_{IN})}$		$T_A =$ Operating Range		-300		ppm/ $^\circ C$
I_{SUPPLY}	Supply Current, I^+ , I^-	$T_A = 25^\circ C$		2	4	mA
		$T_A =$ Operating Range			6	
V_{SUPPLY}	Supply Voltage Range	Functional Operation Only	± 4.5		± 6.0	V
V_{IL}	Low State Input Voltage	Operating Temperature Range			0.8	V
V_{IH}	High State Input Voltage	Operating Temperature Range	2.4			V
I_{LIH}	Logic Input Current	$0 < V_{IN} > V^+$		1	10	μA
V_{OL}	Low State Output Voltage	$I_{OUT} = 1.6mA$ Operating Temperature Range			0.4	V
V_{OH}	High State Output Voltage	$I_{OUT} = -200\mu A$ Operating Temperature Range	2.8			V
I_{OX}	Three-State Output Current	$0 < V_{OUT} > V^+$		1		μA
C_{IN}	Logic Input Capacitance			15		pF
C_{OUT}	Logic Output Capacitance	Three-State		15		

- NOTES:** 1. Full-scale range (FSR) is 5V (reference adjusted).
 2. Assume all leads soldered or welded to printed circuit board.
 3. Assume all leads soldered or welded to printed circuit board.

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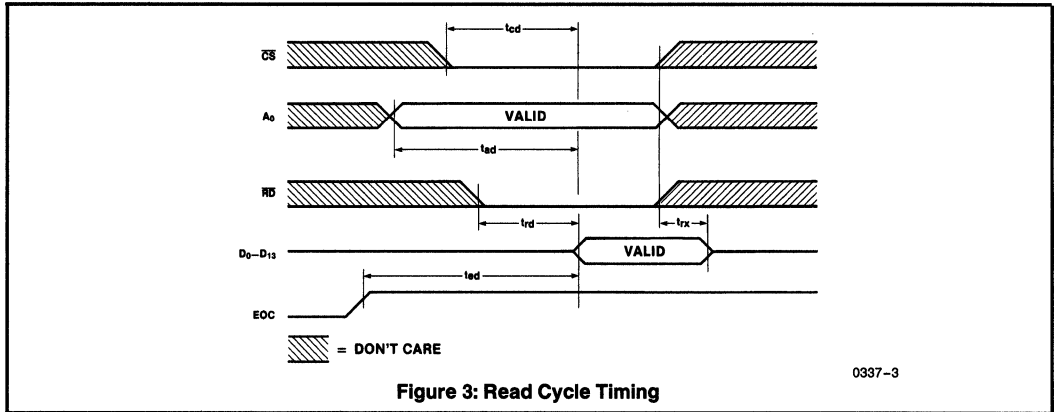


Figure 3: Read Cycle Timing

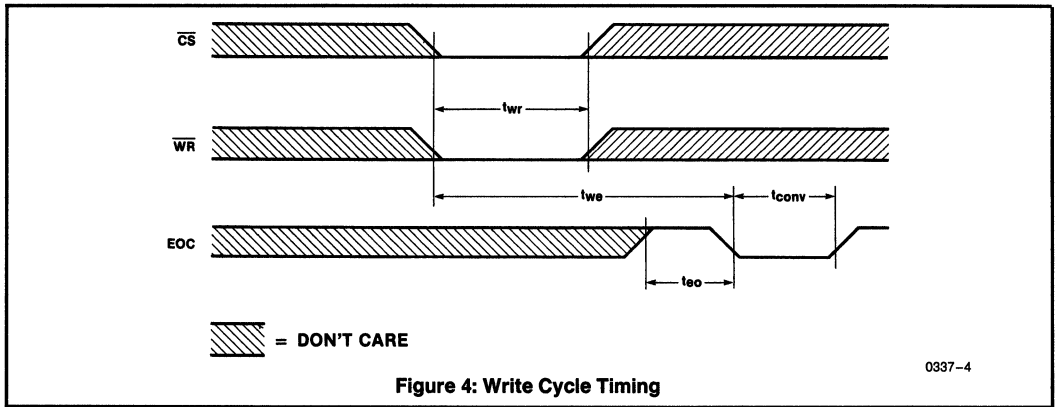


Figure 4: Write Cycle Timing

AC ELECTRICAL CHARACTERISTICS $V^+ = +5.0V$, $V^- = -5.0V$, $T_A = +25^\circ C$, $f_{clk} = 500kHz$ unless otherwise noted. Data derived from extensive characterization testing. Parameters are not 100% production tested.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
READ CYCLE TIMING						
t_{cd}	Prop. Delay \overline{CS} to Data	\overline{RD} Low, A_0 Valid			200	ns
t_{ad}	Prop. Delay A_0 to Data	\overline{CS} Low, \overline{RD} Low			200	
t_{rd}	Prop. Delay \overline{RD} to Data	\overline{CS} Low, A_0 Valid			200	
t_{rx}	Prop. Delay Data to Three State				100	
t_{ed}	Prop. Delay EOC High to Data				200	
WRITE CYCLE TIMING						
t_{wr}	\overline{WR} Low Time		100			ns
t_{we}	Prop. Delay \overline{WR} Low to EOC Low	Wait Mode	1		2	1/fclk
t_{eo}	EOC High Time	Free-Run Mode	0.5		1.5	
t_{conv}	Conversion Time	$\overline{SC} = V_{IH}$			20	
		$\overline{SC} = V_{IL}$			18	

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TABLE 1: PIN DESCRIPTIONS

PIN	NAME	FUNCTION		
1	V _{REFf}	FORCE line for reference input.		
2	AGND _f	FORCE input for analog ground		
3	\overline{CS}	Chip Select enables reading and writing (active low)		
4	\overline{RD}	\overline{Read} (active low)		
5	A ₀	Byte select (low = D ₀ - D ₇ , high = D ₈ - D ₁₃ , OVR)		
6	BUS	Bus select (low = outputs enabled by A ₀ , high = all outputs enabled together)		
7	DGND	Digital GrouND return		
8	D ₁₃	Bit 13 (most significant)	High Byte	
9	D ₁₂	Bit 12		
10	D ₁₁	Bit 11		
11	D ₁₀	Bit 10		
12	D ₉	Bit 9		Output
13	D ₈	Bit 8		Data
14	D ₇	Bit 7		Bits
15	D ₆	Bit 6		(High = True)
16	D ₅	Bit 5	Low Byte	
17	D ₄	Bit 4		
18	D ₃	Bit 3		
19	D ₂	Bit 2		
20	D ₁	Bit 1		
21	D ₀	Bit 0 (least significant)		
22	B ₁₅	Used for programming only (leave open)		
23	B ₁₆			
24	B ₁₇			
25	EOC	End Of Conversion flag (low = busy, high = conversion complete)		
26	OVR	OverRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)		
27	V ⁺	Positive power supply input		
28	PROG	Used for programming only. Tie to V ⁺ for normal operation		
29	TEST	Used for programming only. Tie to V ⁺ for normal operation		

PIN	NAME	FUNCTION
30	OSC1	Oscillator inverter input
31	OSC2	Oscillator inverter output
32	\overline{SC}	Short cycle input (high = 14-bit, low = 12-bit operation)
33	\overline{WR}	\overline{WR} ite pulse input (low starts new conversion)
34	C _{AZ}	Auto-zero capacitor connection
35	V ⁻	Negative power supply input
36	COMP	Used in test, tie to V ⁻
37	V _{INs}	SENSE line for input voltage
38	V _{REFs}	SENSE line for reference input
39	AGND _s	SENSE line for analog ground
40	V _{INf}	FORCE line for input voltage

TABLE 2: I/O CONTROL

CS	WR	RD	A ₀	BUS	FUNCTION
0	0	x	x	x	Initiates a Conversion
1	x	x	x	x	Disables all Chip Commands
0	x	0	0	0	Low Byte is Enabled
0	x	0	1	0	High Byte is Enabled
0	x	0	x	1	Low and High Bytes Enabled Together
x	x	1	x	x	Disables Outputs (High-Impedance)

TABLE 3: TRANSFER FUNCTION

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
	V _{REF} = -5.0V	OVR	MSB	LSB
0	0	0	000000000000	0
+0.0003	0	0	000000000000	1
+0.150	0	0	000011110101	1
+2.4997	0	0	111111111111	1
+2.500	0	1	000000000000	0
+4.9994	0	1	111111111111	0
+4.9997	0	1	111111111111	1
+5.000	1	0	000000000000	0
+5.0003	1	0	000000000000	1
+5.150	1	0	000011110101	1

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DETAILED DESCRIPTION

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 2 shows the functional diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the 40 μ s range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (B₁₆) and the MSB-4 bit (B₁₂). The sequence continues for each bit pair, B_x and B_{x-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion. When the Short Cycle (SC) input is low, 18 clock cycles are required to complete a 12-bit conversion.

The overflow output of the 17-bit full-adder is also the OverRange (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

OPTIMIZING SYSTEM PERFORMANCE

The FORCE and SENSE inputs for V_{IN} and V_{REF} are also shown driven by external op-amps. This technique elimi-

nates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than 300m Ω of total series resistance, the result can be a voltage error equivalent to 1LSB. If no op-amps are used for V_{IN} and V_{REF}, connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the V_{IN} and V_{REF} pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

When using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115 as shown in Figures 5 and 6. In Figure 5 the FORCE line is the only point that is connected to system analog ground. In Figure 6, the op-amp A₃ forces the voltage at AGND to be equal to analog system ground. The addition of this op-amp overcomes the main deficiency of the arrangement in Figure 5: the V_{IN} and V_{REF} sources are not referenced to true analog system ground.

The clamp diodes in Figure 6 are required because spurious op-amp output on AGNDf during power-on can exceed the absolute max rating of ± 1.0 V between AGDf and DGND. The two inverse-parallel diodes clamp the voltage between AGNDs and DGND to ± 0.7 V.

INPUT WARNING

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7115 until the ± 5 V power supplies have stabilized.

INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers, CS, RD, WR, and bus select inputs (A₀ and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A₀ lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a WR pulse (pin 33) when CS (pin 3) is low. Data is enabled on the bus when the chip is selected and RD (pin 4) is low.

Figure 7 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the WR input to the ICL7115 after the I/O or memory-mapped address decoder has brought the CS input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A₀ enables the LSBs and a high level enables the MSBs.

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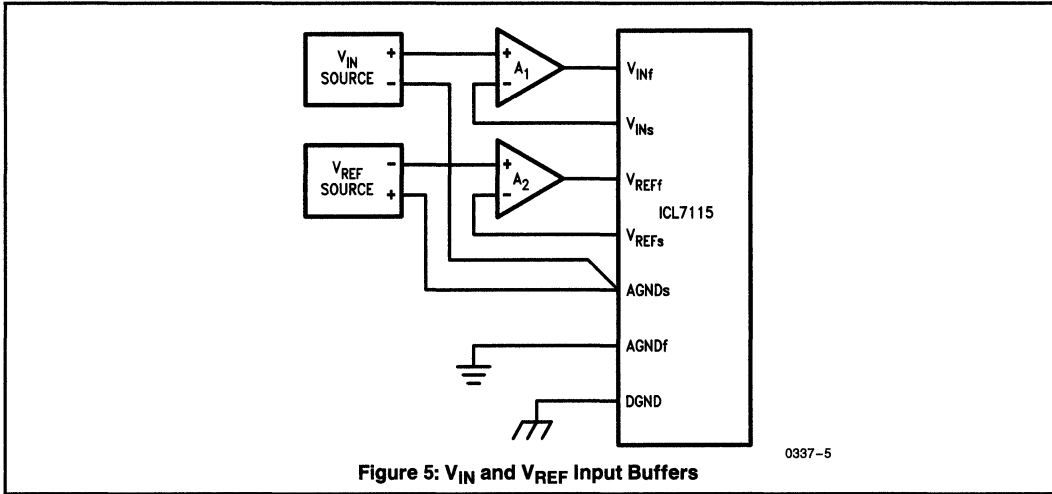


Figure 5: V_{IN} and V_{REF} Input Buffers

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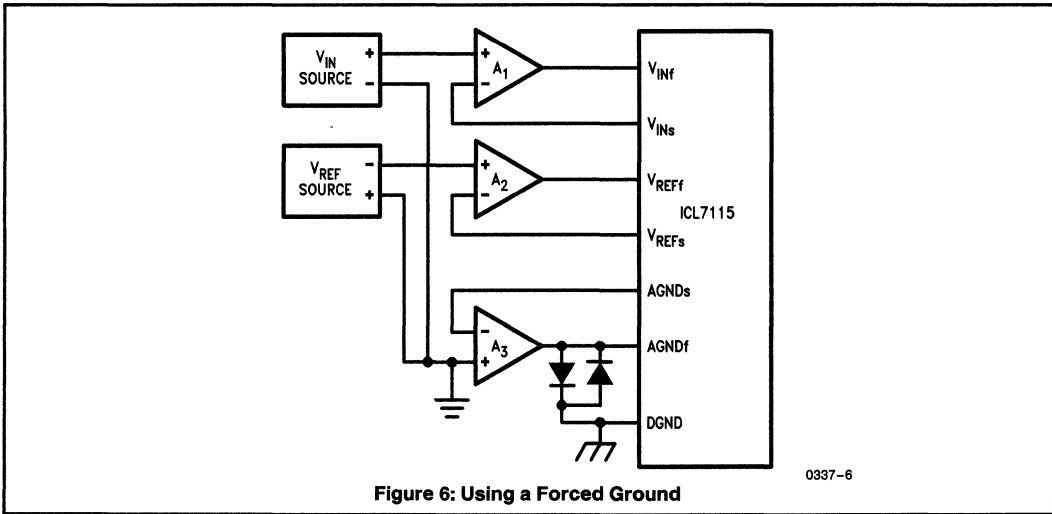
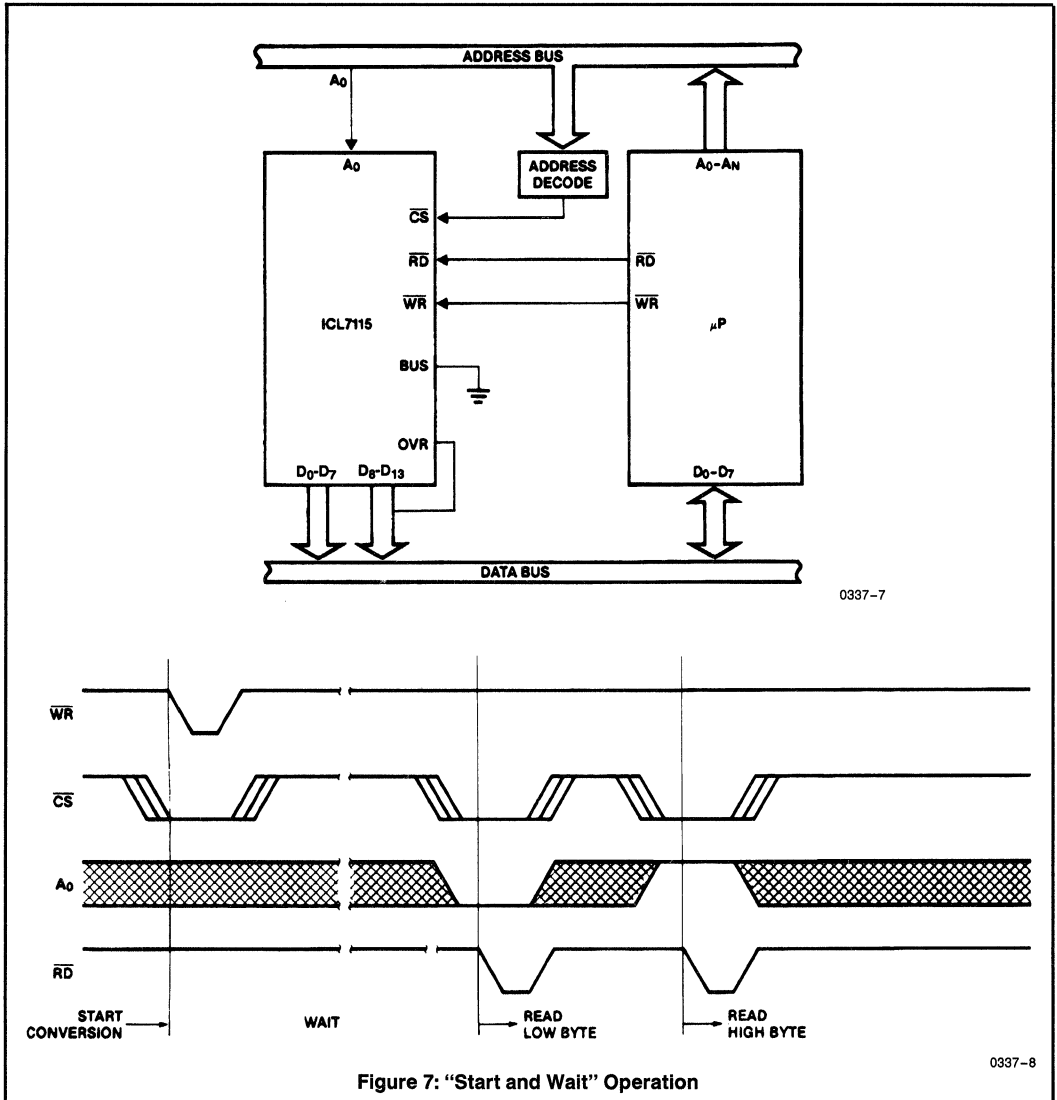


Figure 6: Using a Forced Ground

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By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 8). In this mode, the A_0 and \overline{CS} lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the \overline{WR} line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 9. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 9.

APPLICATIONS

Figure 11 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of +5V to -5V is the result of using the current through R_2 to force a $1/2$ scale offset on the input amplifier (A_2). The output of A_2 swings from 0V to -5V. The overall gain of the A/D is varied by adjusting the 100k Ω trim resistor, R_5 . Since the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/ $^{\circ}$ C and stable external resistors are used.

In Figure 11, note that the 0.22 μ F auto-zero capacitor is connected directly between the C_{AZ} pin and analog ground SENSE. A_3 forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground. It is important to note that since the 7115's DAC current flows in A_1 , A_2 and A_3 these amplifiers should be wideband (GBW > 20MHz) types to minimize errors.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for

a conversion time of 40 μ s. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 12 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 11, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1 . A flip-flop in IC_3 sets IC_2 's Track/Hold input after the microprocessor has initiated a \overline{WR} command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from IC_1 , IC_2 , and A_1 . Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

The ICL7115 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}} \text{ for 14-bit operation}$$

and

$$f_{CLK} = \frac{18}{t_{conv}} \text{ for 12-bit operation}$$

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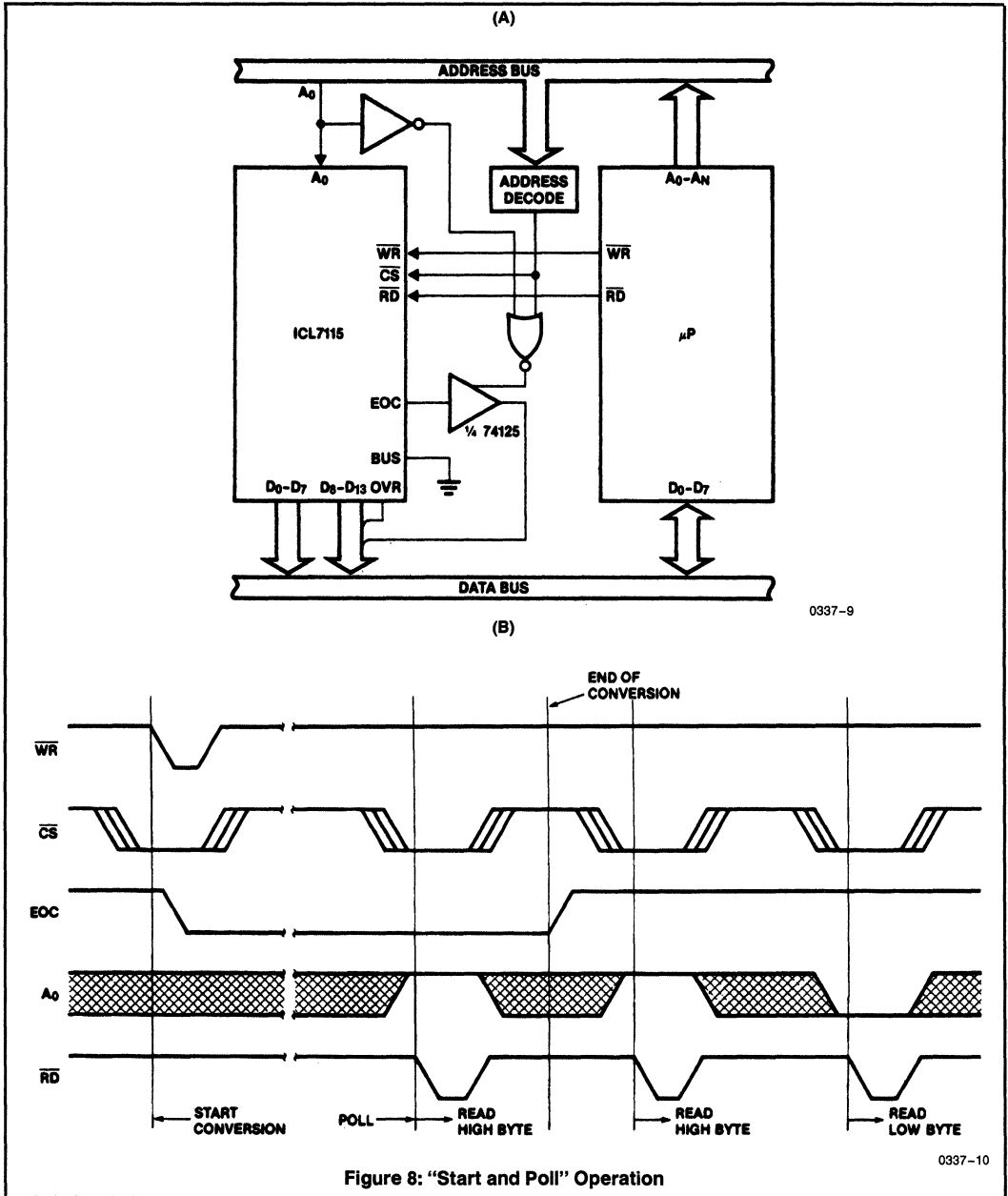
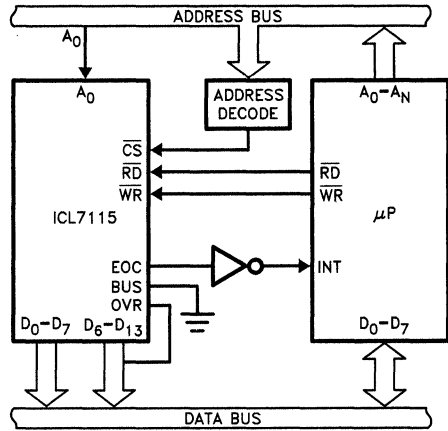


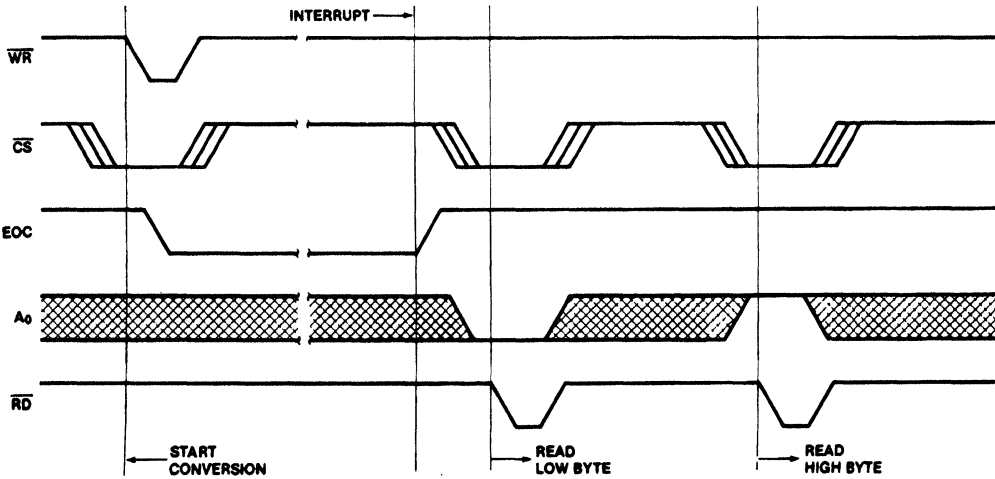
Figure 8: "Start and Poll" Operation

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0337-11



0337-12

Figure 9: Using EOC as an Interrupt

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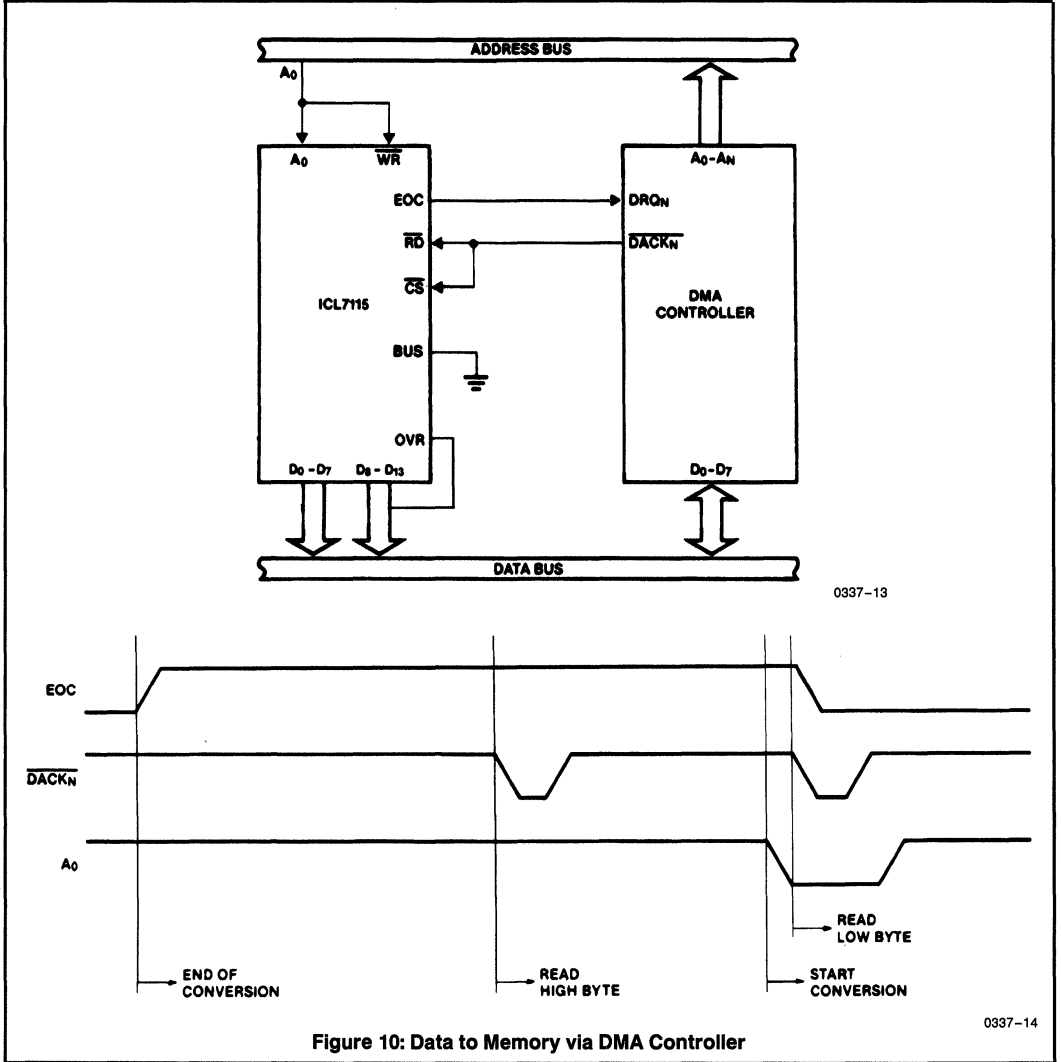


Figure 10: Data to Memory via DMA Controller

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NOTE: All typical values have been characterized but are not tested.

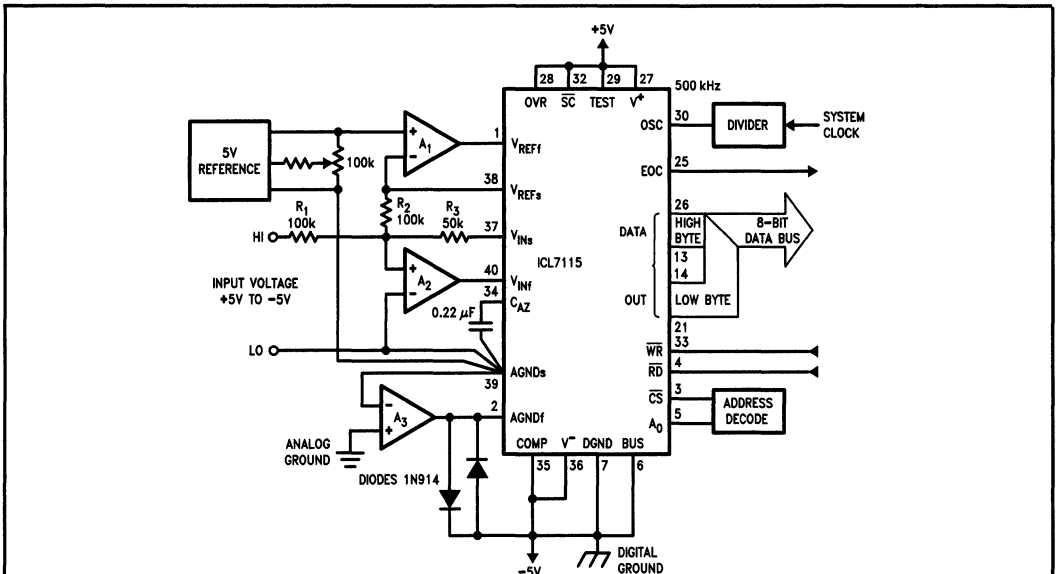


Figure 11: Typical Application with Bipolar Input Range, Forced Ground, and 5 Volt Ultra-Stable Reference

0337-15

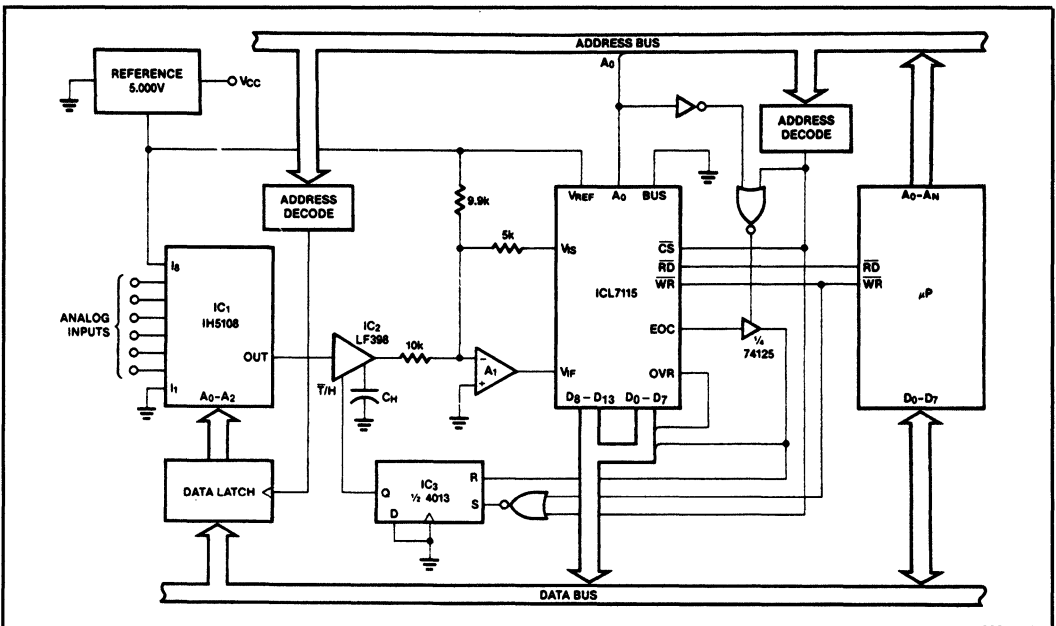


Figure 12: Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

0337-16

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NOTE: All typical values have been characterized but are not tested.

ICL7135

4¹/₂-Digit BCD Output A/D Converter



GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ± 1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than $10\mu\text{V}$, zero drift of less than $1\mu\text{V}/^\circ\text{C}$, input bias current of 10 pA max. , and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDER-RANGE, RUN/HOLD and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

FEATURES

- Accuracy Guaranteed to ± 1 Count Over Entire $\pm 20,000$ Counts (2.0000 Volts Full Scale)
- Guaranteed Zero Reading for 0 Volts Input
- 1pA Typical Input Current
- True Differential Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Over-Range and Under-Range Signals Available for Auto-Range Capability
- All Outputs TTL Compatible
- Blinking Outputs Gives Visual Indication of Over-range
- Six Auxiliary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other Circuitry
- Multiplexed BCD Outputs

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7135CJI	0°C to +70°C	28-Pin CERDIP
ICL7135CPI	0°C to +70°C	28-Pin Plastic DIP
ICL7135EV/KIT	Evaluation Kit (PC Board, active, passive components)	

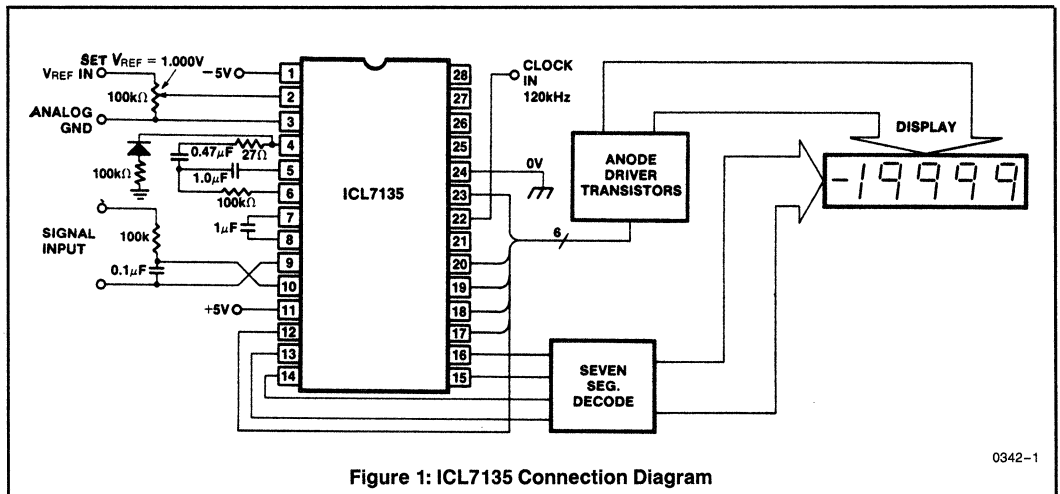


Figure 1: ICL7135 Connection Diagram

0342-1

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ABSOLUTE MAXIMUM RATINGS

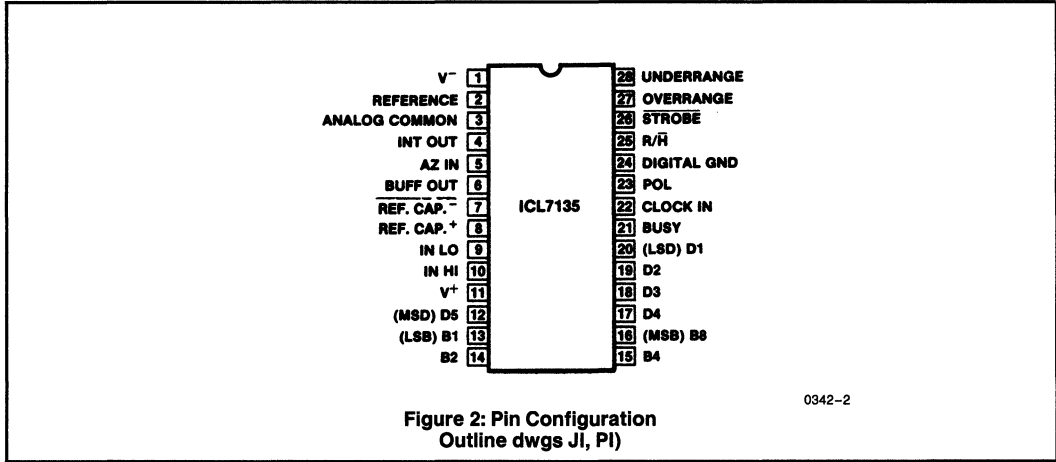
Supply Voltage V^+	+6V
V^-	-9V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Gnd to V^+

Power Dissipation (Note 2)	
Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100 μ A.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



3

ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25^\circ C$, Clock Frequency Set for 3 Reading/Sec)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
ANALOG (Note 1) (Note 2)						
	Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 2.000V	-0.0000	± 0.0000	+0.0000	Digital Reading
	Ratiometric Reading (2)	$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
	Linearity over \pm Full Scale (error of reading from best straight line)	$-2V \leq V_{IN} \leq +2V$		0.5	1	Digital Count Error
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \leq V_{IN} \leq +2V$.01		LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25^\circ C$, Clock Frequency Set for 3 Reading/Sec) (Continued)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit	
e_n	Noise (P-P value not exceeded 95% of time)	$V_{IN} = 0V$ Full scale = 2.000V		15		μV	
I_{ILK}	Leakage Current at Input	$V_{IN} = 0V$		1	10	pA	
	Zero Reading Drift	$V_{IN} = 0V$ $0^\circ \leq T_A \leq 70^\circ C$		0.5	2	$\mu V/^\circ C$	
TC	Scale Factor Temperature Coefficient (3)	$V_{IN} = +2V$ $0 \leq T_A \leq 70^\circ C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C	
DIGITAL							
INPUTS							
V_{INH} V_{INL} I_{INL} I_{INH}	Clock in, Run/Hold, See Figure 4	$V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2		V	
				1.6	0.8		
				0.02	0.1		mA
				0.1	10		μA
OUTPUTS							
V_{OL} V_{OH} V_{OH}	All Outputs B ₁ , B ₂ , B ₄ , B ₈ D ₁ , D ₂ , D ₃ , D ₄ , D ₅ BUSY, STROBE, OVER-RANGE, UNDER-RANGE POLARITY	$I_{OL} = 1.6mA$ $I_{OH} = -1mA$	2.4	0.25 4.2	0.40	V V	
		$I_{OH} = -10\mu A$	4.9	4.99		V	
SUPPLY							
V^+	+5V Supply Range		+4	+5	+6	V	
V^-	-5V Supply Range		-3	-5	-8	V	
I^+	+5V Supply Current	$f_c = 0$		1.1	3.0	mA	
I^-	-5V Supply Current	$f_c = 0$		0.8	3.0		
C_{PD}	Power Dissipation Capacitance	vs. Clock Freq		40		pF	
CLOCK							
	Clock Freq. (Note 4)		DC	2000	1200	kHz	

- NOTES:**
1. Tested in 4-½ digit (20,000 count) circuit shown in Figure 3, clock frequency 120kHz.
 2. Tested with a low dielectric absorption integrating capacitor and $R_{INT} = 0$. See Component Selection Section.
 3. The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
 4. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" section for limitations on the clock frequency range in a system.

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NOTE: All typical values have been characterized but are not tested.

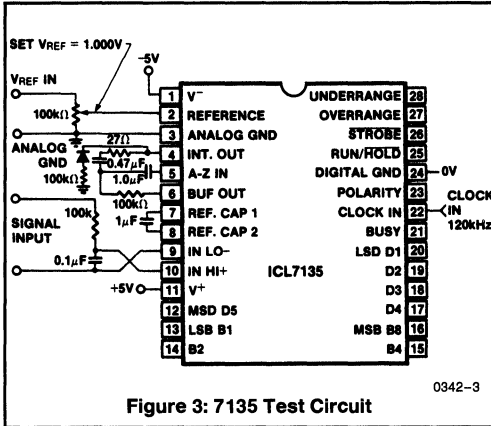


Figure 3: 7135 Test Circuit

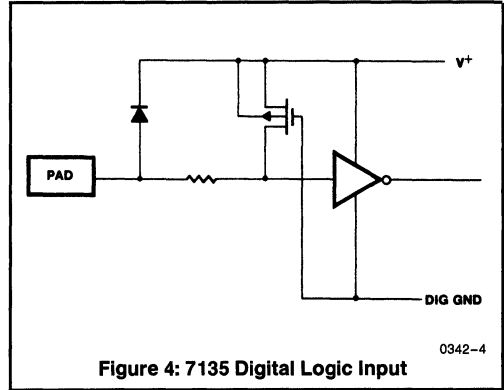


Figure 4: 7135 Digital Logic Input

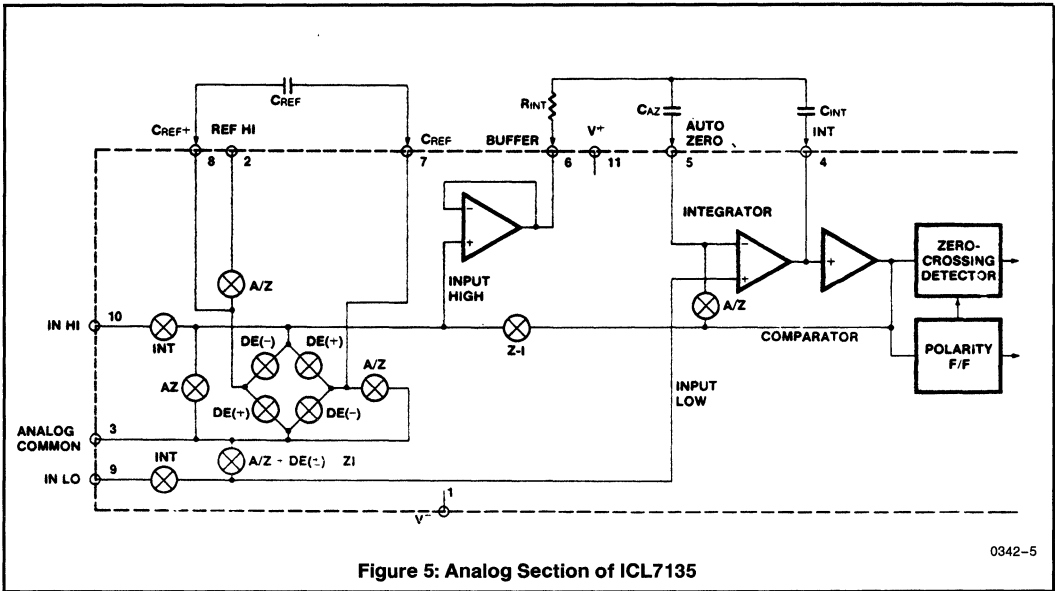


Figure 5: Analog Section of ICL7135

3

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Analog Section

Figure 5 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal-integrate (INT), (3) deintegrate (DE) and (4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than $10\mu V$.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

DE-INTEGRATE PHASE

The Third phase is de-integrate, or reference integrate. Input LOW is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $10,000 \left(\frac{V_{IN}}{V_{REF}} \right)$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

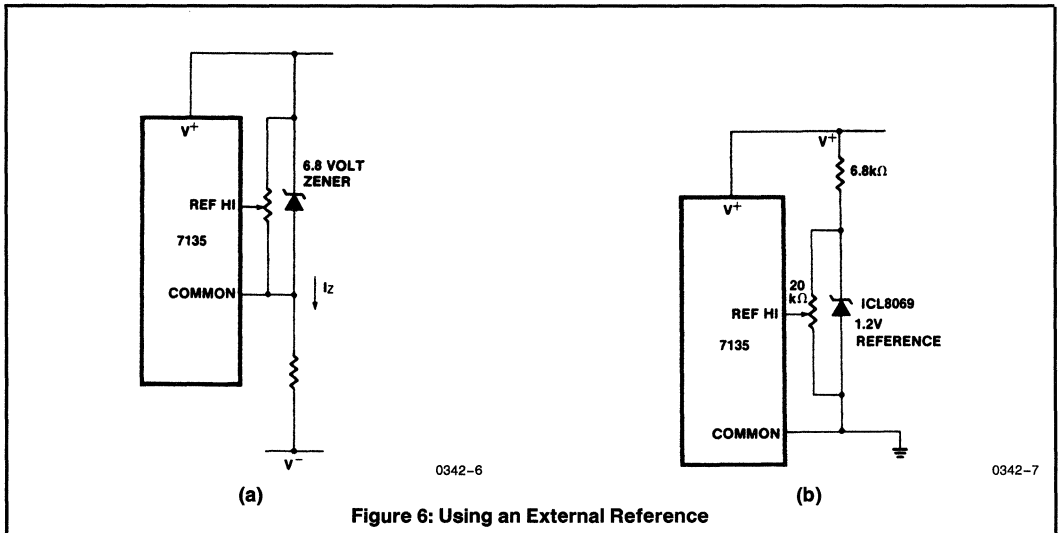


Figure 6: Using an External Reference

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NOTE: All typical values have been characterized but are not tested.

Analog Common

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 6.

DETAILED DESCRIPTION

Digital Section

Figure 7 shows the Digital Section of the 7135. The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

Run/HOLD (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. It taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/H is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/HOLD is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

STROBE (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going STROBE pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first STROBE pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the STROBE goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last STROBE pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional STROBE pulses will be sent until a new measurement is available.

BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to

auto-zero when not BUSY, so it may also be considered a $(Z1+AZ)$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

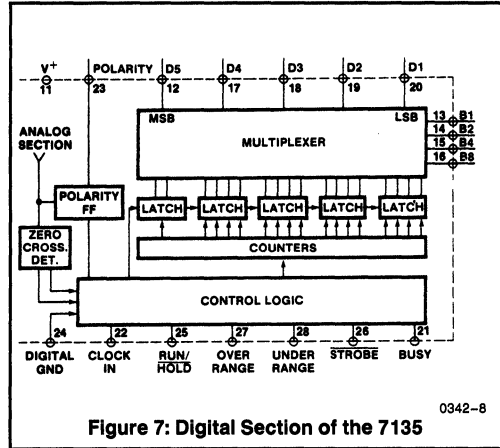


Figure 7: Digital Section of the 7135

OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F/F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F/F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (-) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D₅ (MSD), D₄, D₃, D₂ and D₁ (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D₅ will start the scan again. This can give a blinking display as a visual indication of over-range.

BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B₈, B₄, B₂ and B₁ are positive logic signals that go on simultaneously with the digit driver signal.

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NOTE: All typical values have been characterized but are not tested.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 20µA of drive current with negligible non-linearity. Values of 5 to 40µA give good results, with a nominal of 20µA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance built-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.47µF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{[10,000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}}$$

$$= \frac{(10,000) (\text{clock period}) (20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

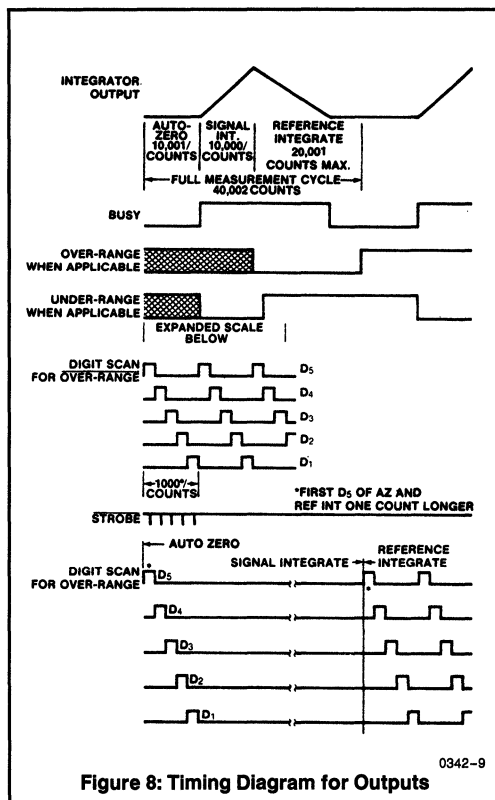


Figure 8: Timing Diagram for Outputs

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

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NOTE: All typical values have been characterized but are not tested.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2 V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INtegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified, adjustment may be needed. The diode can be any silicon diode, such as 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a $3\mu s$ delay, and at a clock frequency of 160kHz ($6\mu s$ period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a $50\mu V$ input, 1 to 2 with $150\mu V$, 2 to 3 at $250\mu V$, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~ 1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

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NOTE: All typical values have been characterized but are not tested.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, $33\frac{1}{3}$ kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, $166\frac{2}{3}$ kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

3

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray} .
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray} .

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately $15\mu V$ (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately $30\mu V$. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

The 7135 is designed to work from $\pm 5V$ supplies. However, in selected applications no negative supply is required. The conditions to use a single $+5V$ supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ± 1.5 volts.

See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 9 shows the complete circuit for a 4-1/2 digit ($\pm 2,000V$) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to $50\mu A$. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

A suitable circuit for driving a plasma-type display is shown in Figure 10. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The $2.5k\Omega$ & $3k\Omega$ resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 11. A standard CMOS 4030 QUAD XOR gate is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit ($\pm 2,000V$) A/D.

Figure 12 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the STROBE signal and 'Overrange' is indicated by blanking the 4 full digits.

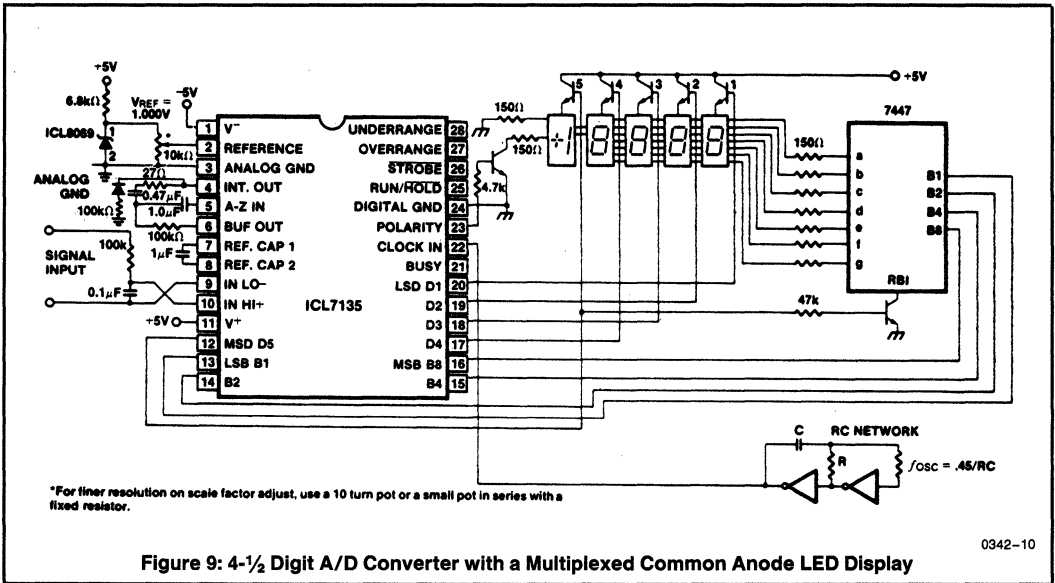


Figure 9: 4-1/2 Digit A/D Converter with a Multiplexed Common Anode LED Display

0342-10

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NOTE: All typical values have been characterized but are not tested.

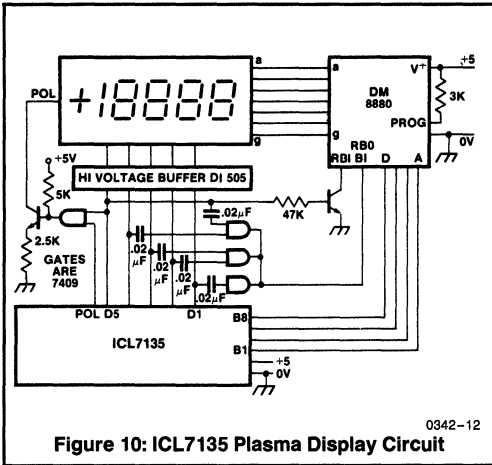


Figure 10: ICL7135 Plasma Display Circuit

0342-12

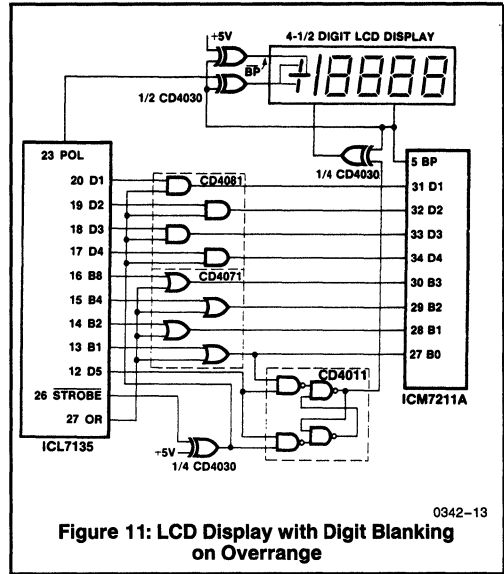


Figure 11: LCD Display with Digit Blanking on Overrange

0342-13

3

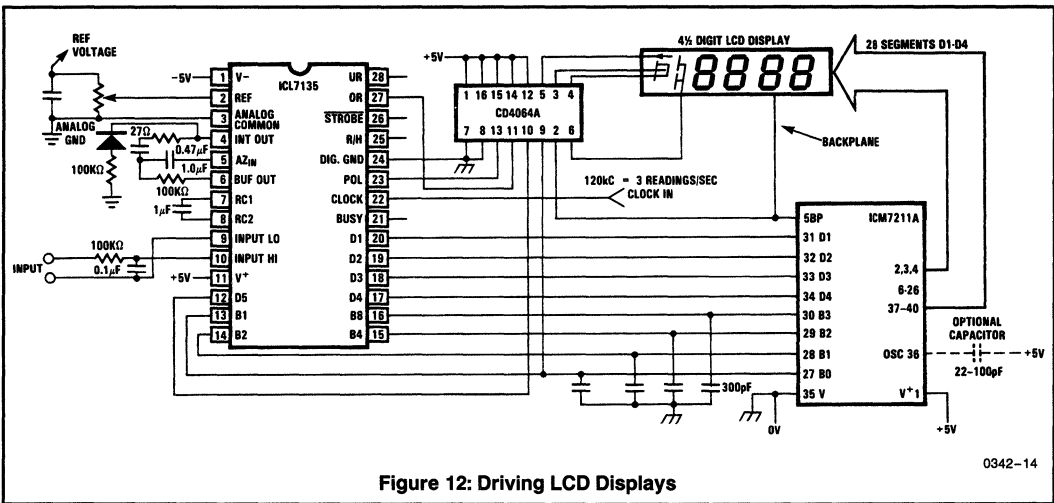


Figure 12: Driving LCD Displays

0342-14

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NOTE: All typical values have been characterized but are not tested.

A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using an LM311 voltage comparator with positive feedback (Figure 13) could minimize any clock frequency shift problem.

The 7135 is designed to work from ± 5 volt supplies. However, if a negative supply is not available, it can be generated with an ICL7660 and two capacitors (Figure 14).

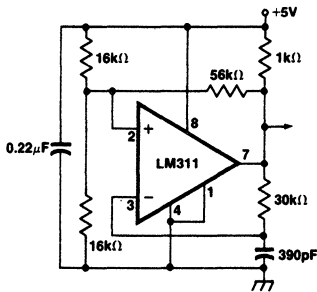


Figure 13: LM311 Clock Source

0342-15

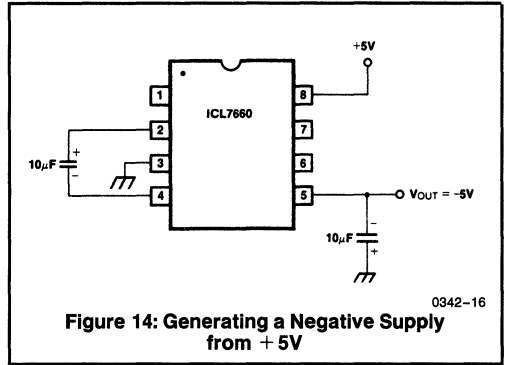


Figure 14: Generating a Negative Supply from +5V

0342-16

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 15 shows a very simple interface between a free-running ICL7135 and a UART. The five STROBE pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 16. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again STROBE starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D₅ word since in this instance it is known that B₂ = B₄ = B₈ = 0.

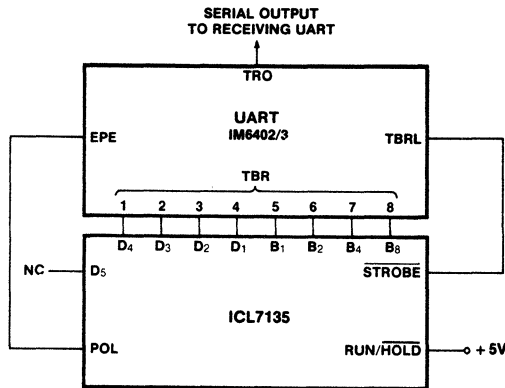


Figure 15: ICL7135 to UART Interface

0342-17

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NOTE: All typical values have been characterized but are not tested.

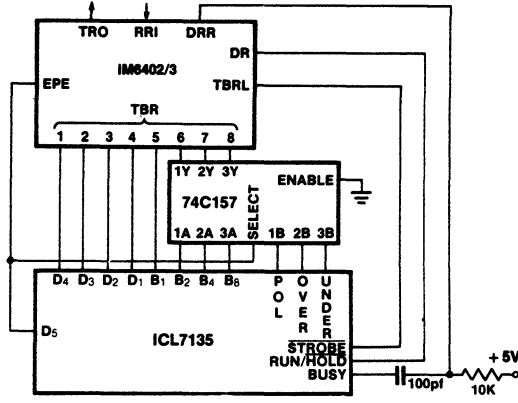


Figure 16: Complex ICL7135 to UART Interface

0342-18

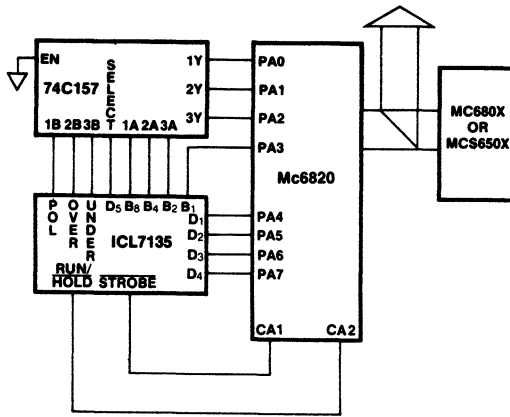
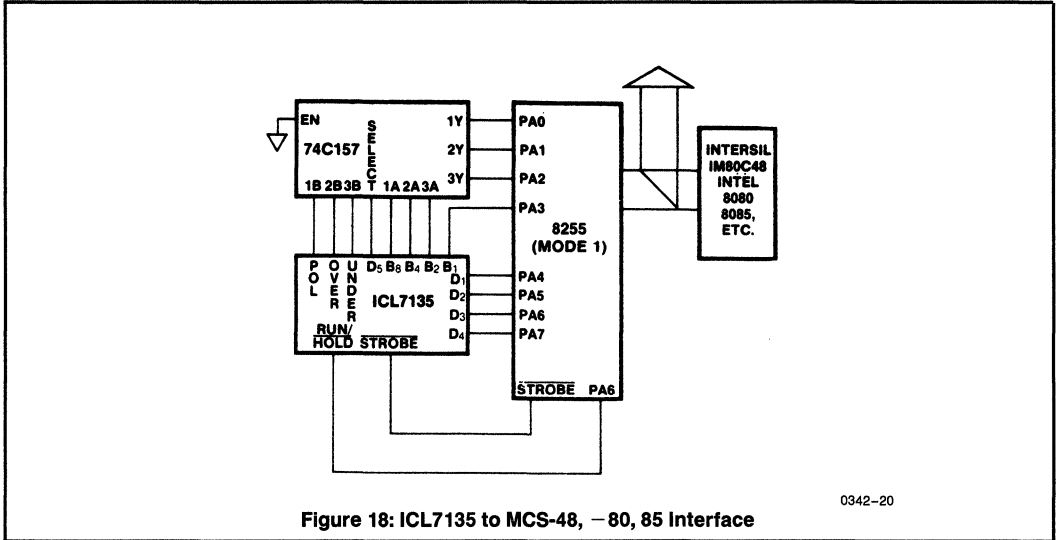


Figure 17: ICL7135 to MC6800, MCS650X Interface

0342-19

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NOTE: All typical values have been characterized but are not tested.



0342-20

Figure 18: ICL7135 to MCS-48, -80, 85 Interface

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 17 and 18. The 8080/8048 and the MC6800 groups with 8 bit buses need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

- A016** "Selecting A/D Converters," by David Fullagar
- A017** "The Integrating A/D Converters," by Lee Evans

- A018** "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A019** "4-1/2 Digit Plan Meter Demonstrator/Instrumentation Boards," by Michael Dufort
- A023** "Low Cost Digital Panel Meter Designs," by David Fullager and Michael Dufort
- A028** "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff
- A030** "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
- A032** "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw
- R005** "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

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NOTE: All typical values have been characterized but are not tested.

Section 4 — D/A Converters

AD7520	4-1
AD7521	4-1
AD7530	4-1
AD7531	4-1
AD7523	4-8
AD7533	4-13
AD7541	4-18
ICL7121	4-25
ICL7134	4-32
IM2110	4-46

AD7520/AD7530 AD7521/AD7531 10/12-Bit Multiplying D/A Converters



AD7520/AD7530 AD7521/AD7531

GENERAL DESCRIPTION

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Intersil's thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

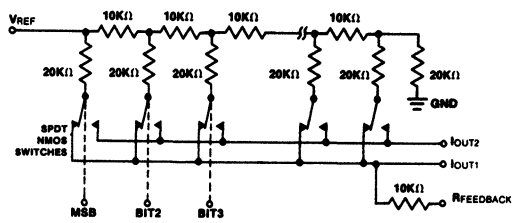
FEATURES

- AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity
- AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity
- Low Power Dissipation: 20mW (Max)
- Low Nonlinearity Tempco: 2 ppm of FSR/°C
- Current Settling Time: 500ns to 0.05% of FSR
- Supply Voltage Range: +5V to +15V
- TTL/CMOS Compatible
- Full Input Static Protection
- /883B Processed Versions Available

ORDERING INFORMATION

Nonlinearity	Part Number/Package		
	Plastic DIP	CERDIP	CERDIP
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD
TEMPERATURE RANGE	0°C to +70°C	-25°C to +85°C	-55°C to +125°C

4



(Switches shown for Digital Inputs "High")
(Resistor values are nominal)
Figure 1: Functional Diagram

0330-1

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NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530 AD7521/AD7531



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Supply Voltage (V ⁺)	+17V
V _{REF}	±25V
Digital Input Voltage Range	V ⁺ to GND
Output Voltage Compliance	-100mV to V ⁺
Power Dissipation (package)	
up to +75°C	450mW
derate above +75°C @	6mW/°C

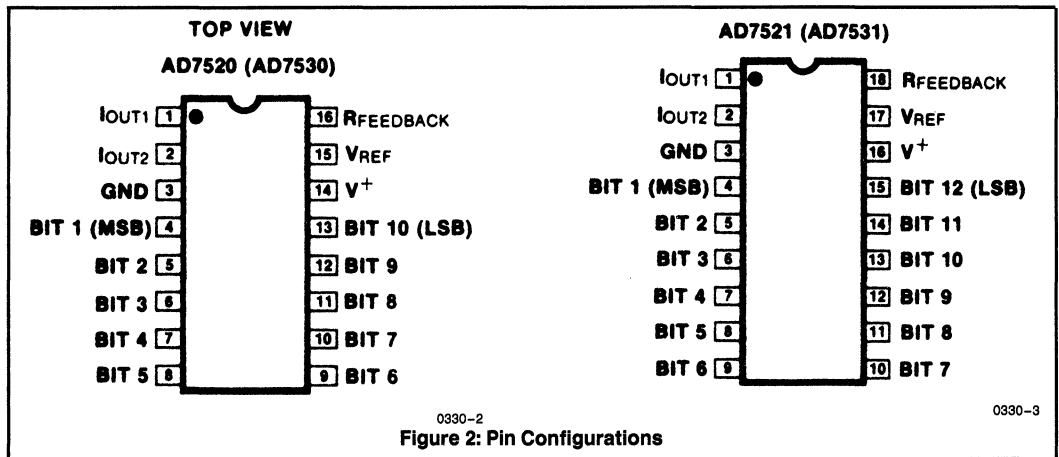
Operating Temperature	
JN, KN, LN Versions	0°C to +70°C
JD, KD, LD Versions	-25°C to 85°C
SD, TD, UD Versions	-55°C to +125°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	300°C

CAUTION:

1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FEEDBACK}.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0330-2
Figure 2: Pin Configurations

0330-3

ELECTRICAL CHARACTERISTICS (V⁺ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

Parameter	Test Conditions	AD7520 (AD7530)	AD7521 (AD7531)	Unit	Limit
DC ACCURACY (Note 1)					
Resolution		10	12	Bits	
Nonlinearity (Note 2)	J S, T, U: over -55°C to +125°C K T L U: -10V ≤ V _{REF} ≤ +10V	Fig. 3	0.2 (8-Bit)	% of FSR	Max
		Fig. 3	0.1 (9-Bit)	% of FSR	Max
		Fig. 3	0.05 (10-Bit)	% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)	-10V ≤ V _{REF} ≤ +10V		2	ppm of FSR/°C	Max
Gain Error (Note 2)			0.3	% of FSR	Typ
Gain Error Tempco (Notes 2 and 3)			10	ppm of FSR/°C	Max

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NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530 AD7521/AD7531



AD7520/AD7530 AD7521/AD7531

ELECTRICAL CHARACTERISTICS (V⁺ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

(Continued)

Parameter	Test Conditions		AD7520 (AD7530)	AD7521 (AD7531)	Unit	Limit
Output Leakage Current (either output)	Over the specified temperature range		200 (300)		nA	Max
Power Supply Rejection (Note 2)		Fig. 4	± 0.005		% of FSR/%	Typ
AC ACCURACY (Note 3)						
Output Current Settling Time	To 0.05% of FSR (All digital inputs low to high and high to low)	Fig. 8	500		ns	Typ
Feedthrough Error	V _{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	Fig. 7	10		mV pp	Max
REFERENCE INPUT						
Input Resistance	All digital inputs high I _{OUT1} at ground.		5k 10k 20k		Ω	Min Typ Max
ANALOG OUTPUT						
Voltage Compliance (both outputs)	(Note 3)		See absolute max. ratings			
Output Capacitance (Note 3)	I _{OUT1} I _{OUT2}	All digital inputs high	Fig. 6	120 37	pF pF	Typ Typ
	I _{OUT1} I _{OUT2}	All digital inputs low	Fig. 6	37 120	pF pF	Typ Typ
Output Noise (both outputs) (Note 3)		Fig. 5	Equivalent to 10kΩ Johnson noise			Typ
DIGITAL INPUTS						
Low State Threshold	Over the specified temp range		0.8		V	Max
High State Threshold			2.4		V	Min
Input Current (low to high state)			1		μA	Typ
Input Coding	See Tables 1 & 2		Binary/Offset Binary			
POWER REQUIREMENTS						
Power Supply Voltage Range			+ 5 to + 15		V	
I ⁺	All digital inputs at 0V or V ⁺		1		μA	Typ
	All digital inputs high or low		2		mA	Max
Total Power Dissipation (Including the ladder network)			20		mW	Typ

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.

2. Using internal feedback resistor, R_{FEEDBACK}.

3. Guaranteed by design, not subject to test.

4. Accuracy not guaranteed unless outputs at GND potential.

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NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530 AD7521/AD7531



TEST CIRCUITS NOTE: The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.

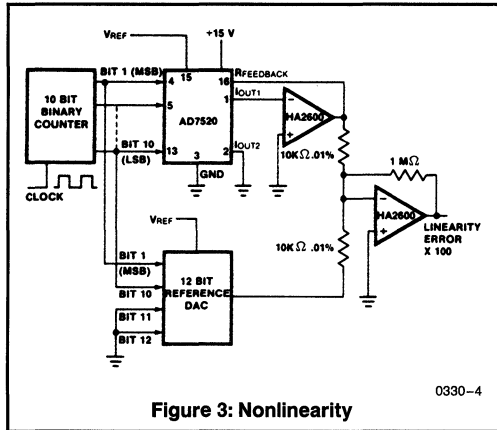


Figure 3: Nonlinearity

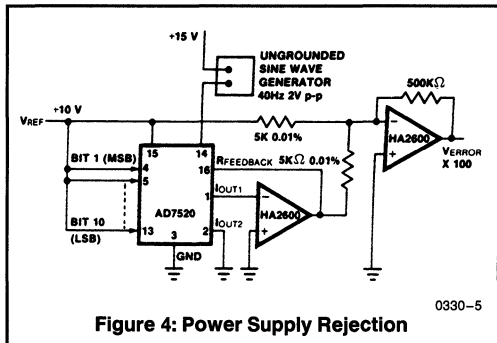


Figure 4: Power Supply Rejection

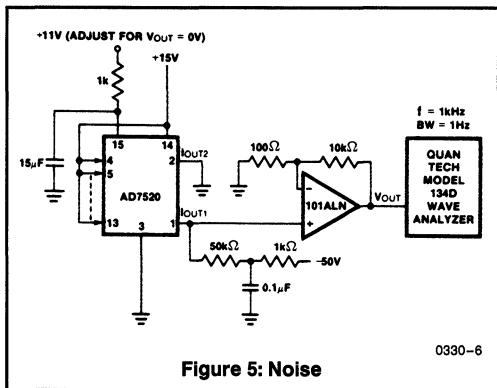


Figure 5: Noise

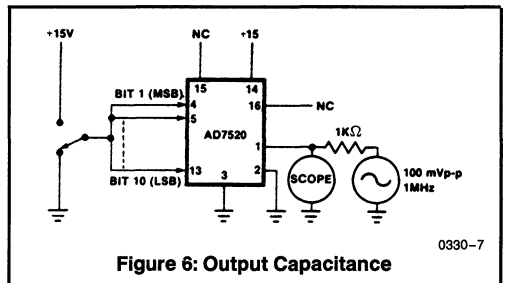


Figure 6: Output Capacitance

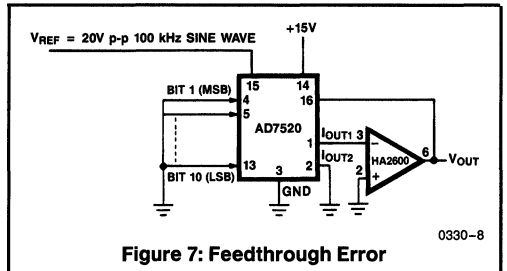


Figure 7: Feedthrough Error

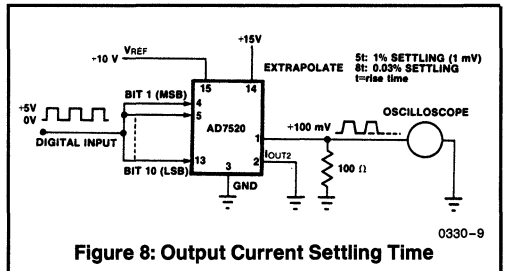


Figure 8: Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n}) (V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}] (V_{REF})$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within $1/2$ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

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NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530 AD7521/AD7531



AD7520/AD7530 AD7521/AD7531

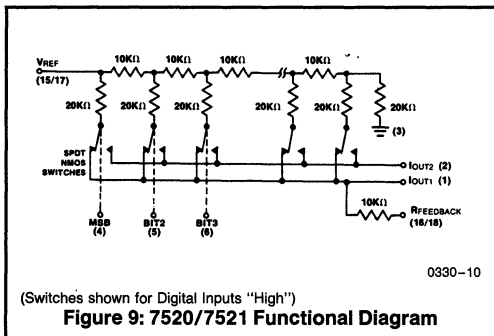
OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DETAILED DESCRIPTION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 10). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

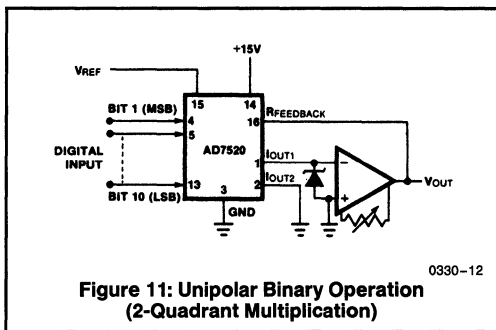
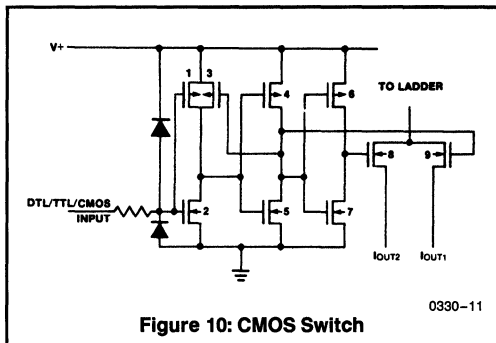


TABLE 1
CODE TABLE — UNIPOLAR BINARY OPERATION

Digital Input	Analog Output
1111111111	$-V_{REF} (1 - 2^{-n})$
1000000001	$-V_{REF} (\frac{1}{2} + 2^{-n})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF} (\frac{1}{2} - 2^{-n})$
0000000001	$-V_{REF} (2^{-n})$
0000000000	0

NOTE: 1. $LSB = 2^{-n} V_{REF}$
2. $n = 10$ for 7520, 7530
 $n = 12$ for 7521, 7531

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 11. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

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NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530 AD7521/AD7531



ZERO OFFSET ADJUSTMENT

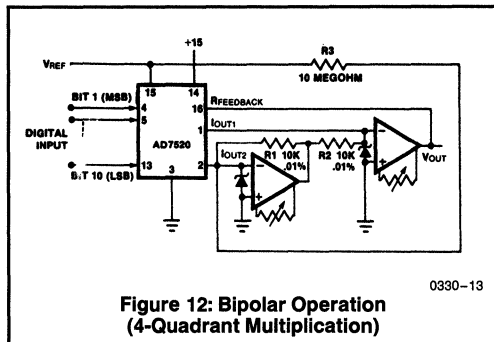
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for $0V \pm 1\text{ mV}$ at V_{OUT} .

GAIN ADJUSTMENT

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to V^+ .
2. Monitor V_{OUT} for a $-V_{REF}$ ($1-2^{-n}$) reading. ($n=10$ for AD7520 (AD7530) and $n=12$ for AD7521 (AD7531)).
3. To decrease V_{OUT} , connect a series resistor (0 to 500Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT} , connect a series resistor (0 to 500Ω) in the I_{OUT1} amplifier feedback loop.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.



**Figure 12: Bipolar Operation
(4-Quadrant Multiplication)**

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY)
OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF} (1 - 2^{-(n-1)})$
1000000001	$-V_{REF} (2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF} (2^{-(n-1)})$
0000000001	$V_{REF} (1 - 2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. $LSB = 2^{-(n-1)} V_{REF}$
2. $n=10$ for 7520 and 7521
= 12 for 7530 and 7531

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2} .

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately $+10V$.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for $0V \pm 1\text{ mV}$ at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for $0V \pm 1\text{ mV}$ at V_{OUT} .

GAIN ADJUSTMENT

1. Connect all digital inputs to V^+ .
2. Monitor V_{OUT} for a $-V_{REF}$ ($1-2^{-(n-1)}$) volts reading. ($n=10$ for AD7520 and AD7530, and $n=12$ for AD7521 and AD7531).
3. To increase V_{OUT} , connect a series resistor of up to 500Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT} , connect a series resistor of up to 500Ω between the reference voltage and the V_{REF} terminal.

POWER DAC DESIGN USING AD7520

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 13. An INTERSIL ICH8510 power operational amplifier (1 Amp continuous output at up to $\pm 25V$) is driven by the AD7520.

A summing amplifier between the AD7520 and the ICH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7520 can be directly connected to the ICH8510, by using a 25V reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Note that the output of the 101A is fed into an inverting amplifier with a gain of -3 , which can be easily changed to a non-inverting configuration. (For more information see: INTERSIL Application Bulletin A021: Power D/A Converters Using The IH8510 by Dick Wilenken.)

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NOTE: All typical values have been characterized but are not tested.

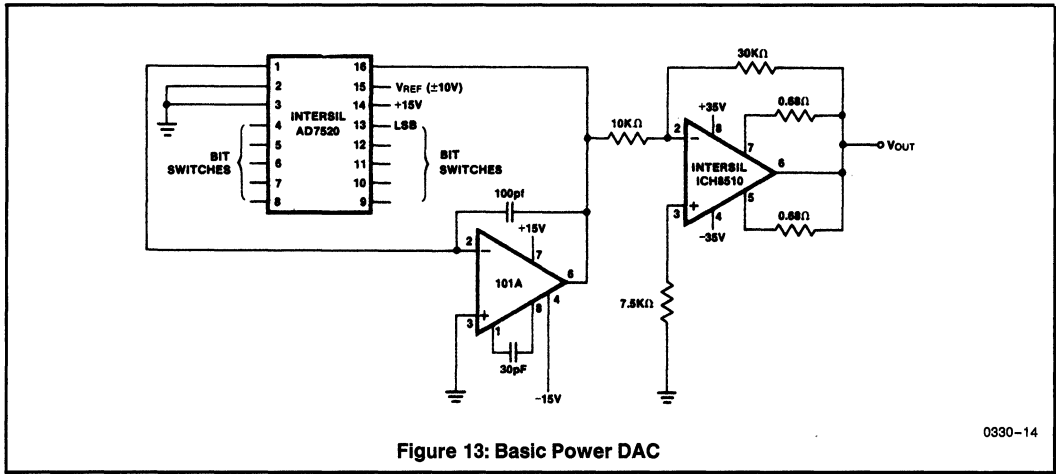


Figure 13: Basic Power DAC

0330-14

Analog/Digital Division

With the AD7520 connected in its normal multiplying configuration as shown in Figure 13, the transfer function is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_n}{2^n} \right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 14, the transfer function becomes:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_n}{2^n}} \right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (± 1 LSB).

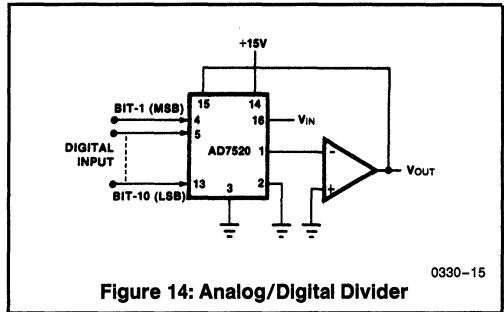


Figure 14: Analog/Digital Divider

0330-15

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For further information on the use of this device, see the following Application Bulletins:

- A016** "Selecting A/D Converters," by David Fullagar
- A018** "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A020** "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
- A021** "Power D/A Converters Using the IH8510," by Dick Wilenken

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NOTE: All typical values have been characterized but are not tested.

AD7523

8-Bit Multiplying D/A Converter



GENERAL DESCRIPTION

The AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.

Low noise audio gain controls, motor speed controls, digitally controlled gain and attenuators are a few of the wide range of applications of the 7523.

FEATURES

- 8, 9 and 10 Bit Linearity
- Low Gain and Linearity Temperature Coefficients
- Full Temperature Range Operation
- Static Discharge Input Protection
- DTL/TTL/CMOS Compatible
- +5 to +15 Volts Supply Range
- Fast Settling Time: 150ns Max at 25°C
- Four Quadrant Multiplication

ORDERING INFORMATION

Nonlinearity	Part Number/Package		
	Plastic DIP	CERDIP	CERDIP
0.2% (8 Bit)	AD7523JN	AD7523AD	AD7523SD
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD
TEMPERATURE RANGE	0°C to +70°C	-25°C to +85°C	-55°C to +125°C

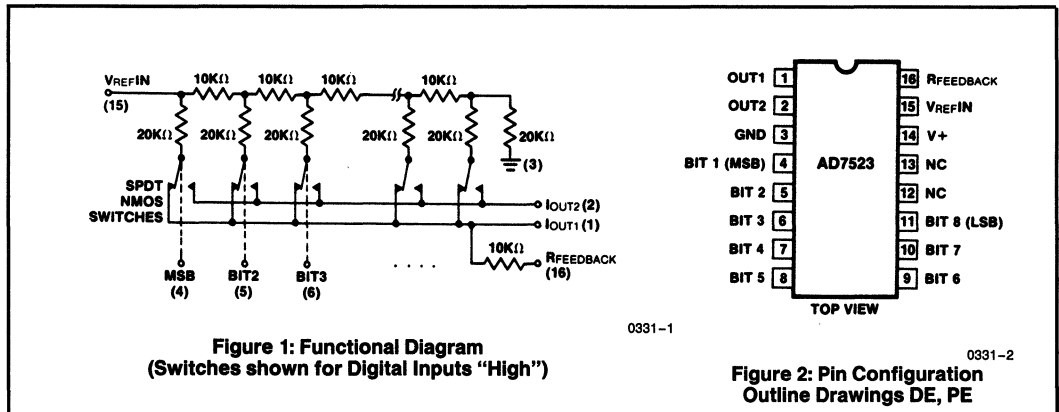


Figure 1: Functional Diagram
(Switches shown for Digital Inputs "High")

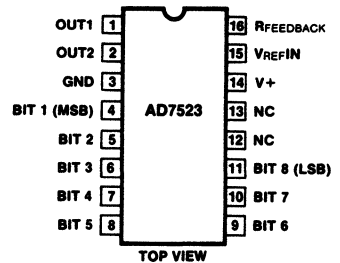


Figure 2: Pin Configuration
Outline Drawings DE, PE

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Supply Voltage (V ⁺)	+17V
V _{REF}	±25V
Digital Input Voltage Range	V ⁺ to GND
Output Voltage Compliance	-100mV to V ⁺
Power Dissipation:	
Plastic Package —	
up to +70°C	670mW
derate above +70°C by	8.3mW/°C

Ceramic Package —	
up to 75°C	450mW
derate above 75°C by	6mW/°C
Operating Temperatures	
JN, KN, LN Versions	0°C to +70°C
AD, BD, CD Versions	-25°C to +85°C
SD, TD, UD Versions	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

CAUTION:

- The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- Do not apply voltages higher than VDD and lower than GND to any terminal except V_{REF} + R_{FEEDBACK}.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V⁺ = +15V, V_{REF} = +10V unless otherwise specified)

Parameter		Test Conditions	T _A +25°C	T _A Min-Max	Unit	Limit
DC ACCURACY (Note 1)						
Resolution			8	8	Bits	Min
Nonlinearity (Note 2)	(± ½ LSB)	-10V ≤ V _{REF} ≤ +10V V _{OUT1} = V _{OUT2} = 0V	± 0.2	± 0.2	% of FSR	Max
	(± ¼ LSB)		± 0.1	± 0.1	% of FSR	Max
	(± ⅙ LSB)		± 0.05	± 0.05	% of FSR	Max
Monotonicity			Guaranteed			
Gain Error (Note 2)		Digital Inputs high.	± 1.5	± 1.8	% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)		-10V V _{REF} + 10V	2		ppm of FSR/°C	Max
Gain Error Tempco (Notes 2 and 3)			10		ppm of FSR/°C	Max
Output Leakage Current (either output)		V _{OUT1} = V _{OUT2} = 0	± 50	± 200	nA	Max
AC ACCURACY						
Power Supply Rejection (Note 2)		V ⁺ = 14.0 to 15.0V	0.02	0.03	% of FSR	Max
Output Current Settling Time (Note 3)		To 0.2% of FSR, R _L = 100Ω	150	200	ns	Max
Feedthrough Error (Note 3)		V _{REF} = 20V pp, 200kHz sine wave. All digital inputs low.	± ½	± 1	LSB	Max
REFERENCE INPUT						
Input Resistance (Pin 15)		All digital inputs high. I _{OUT1} at ground.	5K		Ω	Min
			20K			Max
Temperature Coefficient (Note 3)			-500		ppm/°C	Max
ANALOG OUTPUT						
Output Capacitance (Note 3)	C _{OUT1}	All digital inputs high (VINH)	100		pF	Max
	C _{OUT2}		30		pF	Max
	C _{OUT1}	All digital inputs low (VINL)	30		pF	Max
	C _{OUT2}		100		pF	Max

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (V⁺ = +15V, V_{REF} = +10V unless otherwise specified) (Continued)

Parameter	Test Conditions	T _A +25°C	T _A Min-Max	Unit	Limit
DIGITAL INPUTS					
Low State Threshold (V _{INL})		0.8		V	Max
High State Threshold (V _{INH})		2.4		V	Min
Input Current (Low or high)	V _{IN} = 0V or +15V	±1		μA	Max
Input Coding	See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)		4		pF	Max
POWER REQUIREMENTS					
Power Supply Voltage Range	Accuracy is tested and guaranteed at V ⁺ = +15V, only.	+5 to +16		V	
I ⁺	All digital inputs low or high.	2	2.5	mA	Max

- NOTES:**
1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
 2. Using internal feedback resistor, R_{FEEDBACK}.
 3. Guaranteed by design; not subject to test.
 4. Accuracy not guaranteed unless outputs at ground potential.

APPLICATIONS

UNIPOLAR OPERATION

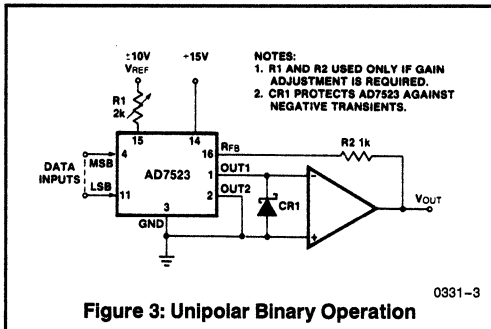


Figure 3: Unipolar Binary Operation

Table 1. Unipolar Binary Code Table

Digital Input MSB LSB	Analog Output
11111111	$-V_{REF} \left(\frac{255}{256} \right)$
10000001	$-V_{REF} \left(\frac{129}{256} \right)$
10000000	$-V_{REF} \left(\frac{128}{256} \right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF} \left(\frac{127}{256} \right)$
00000001	$-V_{REF} \left(\frac{1}{256} \right)$
00000000	$-V_{REF} \left(\frac{0}{256} \right) = 0$

NOTE: 1 LSB = $(2^{-8}) (V_{REF}) = \left(\frac{1}{256} \right) (V_{REF})$

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BIPOLAR OPERATION

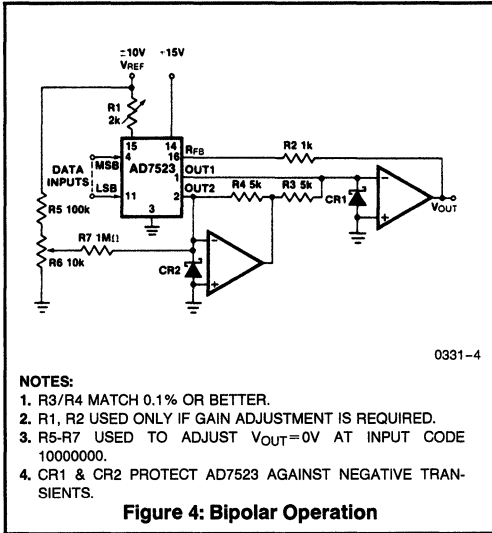


Table 2. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Analog Output
11111111	$-V_{REF} \left(\frac{127}{128} \right)$
10000001	$-V_{REF} \left(\frac{1}{128} \right)$
10000000	0
01111111	$+V_{REF} \left(\frac{1}{128} \right)$
00000001	$+V_{REF} \left(\frac{127}{128} \right)$
00000000	$+V_{REF} \left(\frac{128}{128} \right)$

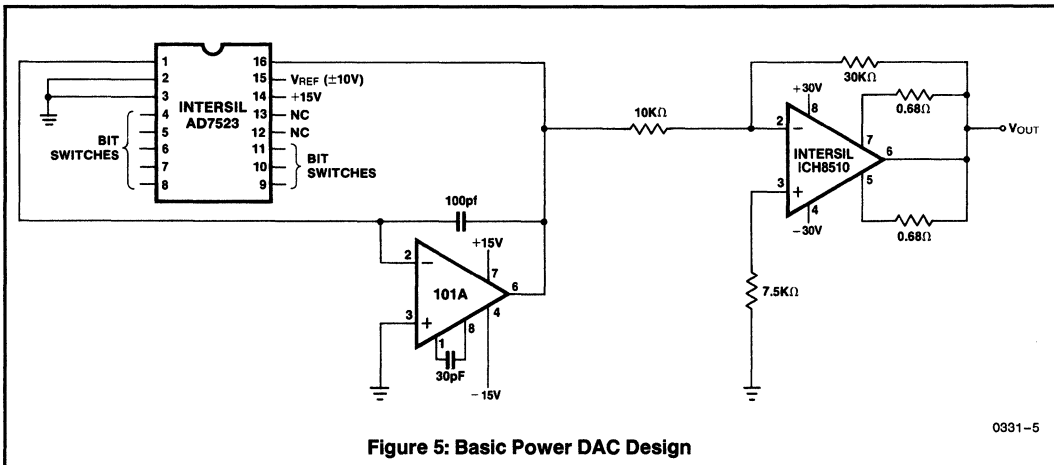
NOTE: $1 \text{ LSB} = (2^{-7}) (V_{REF}) = \left(\frac{1}{128} \right) (V_{REF})$

4

A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 5. The Intersil ICH8510 power operational amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the ICH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage, whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the ICH8510, by using a 25 volt reference for the DAC.

POWER DAC DESIGN USING AD7523



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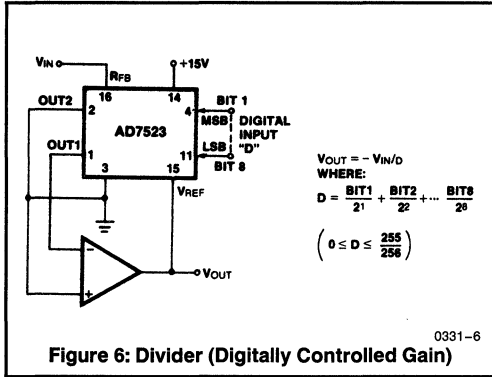


Figure 6: Divider (Digitally Controlled Gain)

$$V_{OUT} = -V_{IN}/D$$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \dots + \frac{BIT8}{2^8}$$

$$(0 \leq D \leq \frac{255}{256})$$

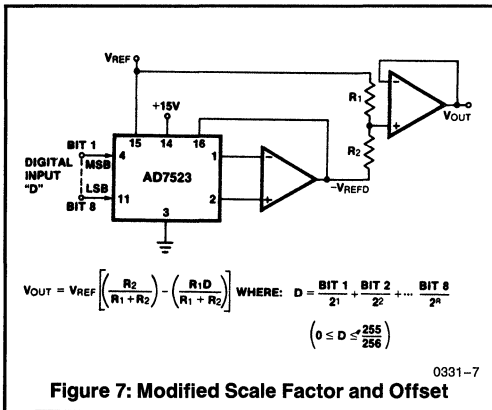


Figure 7: Modified Scale Factor and Offset

$$V_{OUT} = V_{REF} \left[\left(\frac{R_2}{R_1 + R_2} \right) - \left(\frac{R_1 D}{R_1 + R_2} \right) \right]$$

WHERE: $D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \dots + \frac{BIT8}{2^8}$

$$(0 \leq D \leq \frac{255}{256})$$

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire VREF range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2⁻ⁿ) (VREF). A bipolar converter of n bits has a resolution of [2⁻⁽ⁿ⁻¹⁾] [VREF]. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from VREF to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from IOUT1 and IOUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on IOUT1 terminal with all digital inputs LOW or on IOUT2 terminal when all inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

- A016 "Selecting A/D Converters," by David Fullagar
- A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
- A020 "A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger
- A021 "Power D/A Converters Using the IH8510," by Dick Wilenken

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NOTE: All typical values have been characterized but are not tested.

AD7533

10-Bit Multiplying D/A Converter



AD7533

GENERAL DESCRIPTION

The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC). Intersil's thin-film resistor on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V supply voltage range, full input protection from damage due to static discharge by clamps to V⁺ and ground and very low power dissipation.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Applications for the AD7533 include programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

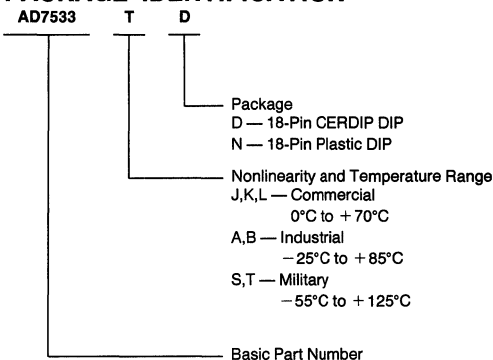
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

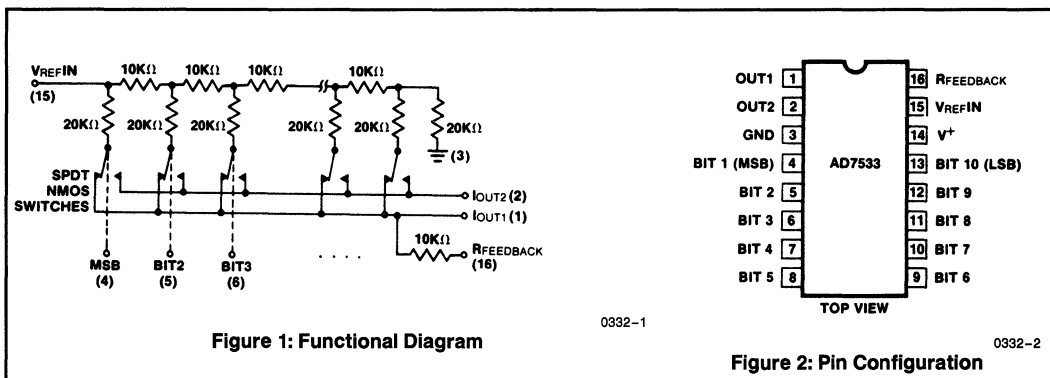
FEATURES

- Lowest Cost 10-Bit DAC
- 8, 9 and 10 Bit Linearity
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- TTL/CMOS Direct Interface
- +5 to +15 Volts Supply Range
- Low Power Dissipation
- Fast Settling Time
- Four Quadrant Multiplication
- Direct AD7520 Equivalent
- 883B Processed Versions Available

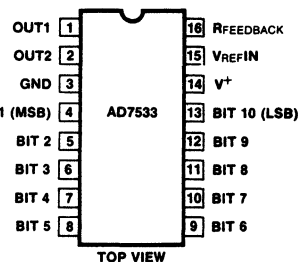
PACKAGE IDENTIFICATION



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0332-1



0332-2

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V^+	+17V	Plastic Package:	
V_{REF}	$\pm 25\text{V}$	up to 70°C	670mW
Digital Input Voltage Range	V^+ to GND	derates above 70°C by	8.3mW/ $^\circ\text{C}$
Output Voltage Compliance	-0.1V to V^+	Operating Temperature Range:	
Power Dissipation		JN, KN, LN Versions	0°C to $+70^\circ\text{C}$
Ceramic Package:		AD, BD, CD Versions	-25°C to 85°C
up to $+75^\circ\text{C}$	450mW	SD, TD, UD Versions	-55°C to $+125^\circ\text{C}$
derates above $+75^\circ\text{C}$ by	6mW/ $^\circ\text{C}$	Storage Temperature Range	-65°C to 150°C
		Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB} .

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V^+ = +15\text{V}$, $V_{REF} = +10\text{V}$, $V_{OUT1} = V_{OUT2} = 0$ unless otherwise specified.)

Parameter	Test Conditions	T_A $+25^\circ\text{C}$	T_A Min-Max	Limit	Unit
DC ACCURACY (Note 1)					
Resolution		10	10	Min	Bits
Nonlinearity (Note 2)	$-10\text{V} \leq V_{REF} \leq +10\text{V}$ $V_{OUT1} = V_{OUT2} = 0\text{V}$	± 0.2	± 0.2	Max	% of FSR
		± 0.1	± 0.1	Max	% of FSR
		± 0.05	± 0.05	Max	% of FSR
Gain Error (Note 2 and 5)	Digital Inputs = V_{INH}	± 1.4	± 1.5	Max	% of FS
Output Leakage Current (either output)	$V_{REF} = \pm 10\text{V}$	± 50	± 200	Max	nA
AC ACCURACY					
Power Supply Rejection (Note 2)	$V^+ = 14.0$ to 17.0V	0.005	0.008	Max	% of FSR/%
Output Current Settling Time (Note 3)	To 0.05% of FSR, $R_L = 100\Omega$	600	800	Max	ns
Feedthrough Error (Note 3)	$V_{REF} = \pm 10\text{V}$, 100kHz sine wave. Digital inputs low.	± 0.05	± 0.1	Max	% FSR
REFERENCE INPUT					
Input Resistance (Pin 15)	All digital inputs high.	5k		Min	Ω
		20k		Max	
Temperature Coefficient		-300		Typ	ppm/ $^\circ\text{C}$
ANALOG OUTPUT					
Voltage Compliance (Note 3)	Both outputs. See maximum ratings	-100mV to V^+			
Output Capacitance (Note 3)	C_{OUT1}	All digital inputs high (V_{INH})	100	Max	pF
	C_{OUT2}		35	Max	pF
	C_{OUT1}	All digital inputs low (V_{INL})	35	Max	pF
	C_{OUT2}		100	Max	pF

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

(V⁺ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0 unless otherwise specified.) (Continued)

Parameter	Test Conditions	T _A + 25°C	T _A Min-Max	Limit	Unit
DIGITAL INPUTS					
Low State Threshold (VINL)		0.8		Max	V
High State Threshold (VINH)		2.4		Min	V
Input Current (I _{IN})	V _{IN} = 0V and V ⁺	± 1		Max	μA
Input Coding	See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)		5		Max	pF
POWER REQUIREMENTS					
V _{DD}	Rated Accuracy	+ 15 ± 10%			V
Power Supply Voltage Range		+ 5 to + 16			V
I ⁺	Digital Inputs = V _{INL} to V _{INH}	2/2.5		Max	mA
	Digital Inputs = 0V or V ⁺	100	150	Max	μA

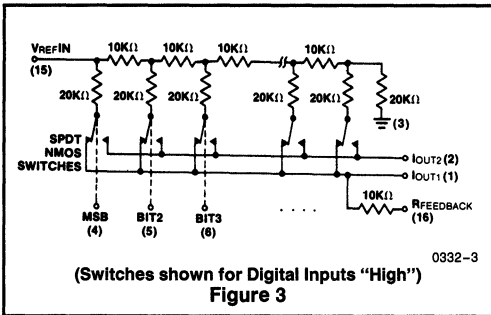
- NOTES: 1. Full scale range (FSR) is 10V for unipolar and ± 10V for bipolar modes.
 2. Using internal feedback resistor, R_{FEEDBACK}.
 3. Guaranteed by design; not subject to test.
 4. Accuracy not guaranteed unless outputs at ground potential.
 5. Full scale (FS) = -(V_{REF}) • (1023/1024)

Specifications subject to change without notice.

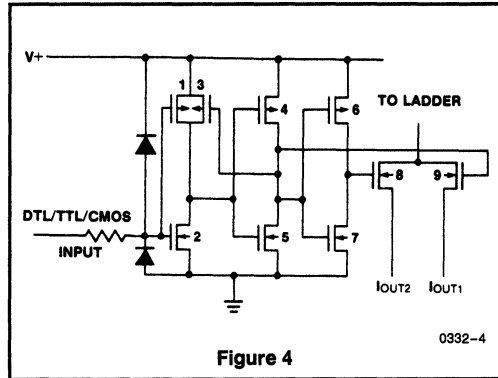
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DETAILED DESCRIPTION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.



A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS SPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



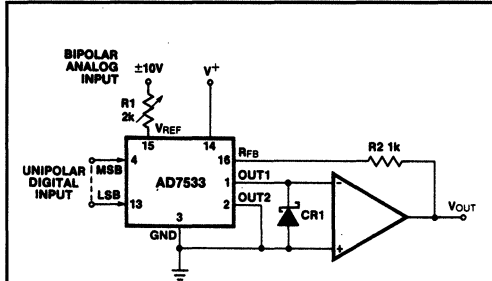
The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 4). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

UNIPOLAR OPERATION
(2-QUADRANT MULTIPLICATION)

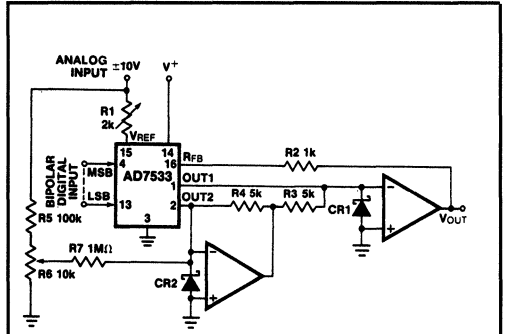


0332-5

- NOTES: 1. R1 and R2 used only if gain adjustment is required.
 2. Schottky diode CR1 (HP5082-2811 or equiv) protects OUT1 terminal against negative transients.

Figure 5: Unipolar Binary Operation
(2-Quadrant Multiplication)

BIPOLAR OPERATION
(4-QUADRANT MULTIPLICATION)



0332-6

- NOTES: 1. R3/R4 match 0.05% or better.
 2. R1 and R2 used only if gain adjustment is required.
 3. Schottky diodes CR1 and CR2 (HP5082-2811 or equiv) protect OUT1 and OUT2 terminals against negative transients.

Figure 6: Bipolar Operation
(4-Quadrant Multiplication)

Table 1. Unipolar Binary Code

Digital Input MSB LSB	Nominal Analog Output (V _{OUT} as shown in Figure 3)
111111111	$-V_{REF} \left(\frac{1023}{1024} \right)$
100000001	$-V_{REF} \left(\frac{513}{1024} \right)$
100000000	$-V_{REF} \left(\frac{512}{1024} \right) = -\frac{V_{REF}}{2}$
011111111	$-V_{REF} \left(\frac{511}{1024} \right)$
000000001	$-V_{REF} \left(\frac{1}{1024} \right)$
000000000	$-V_{REF} \left(\frac{0}{1024} \right) = 0$

NOTES: 1. Nominal Full Scale for the circuit of Figure 3 is given by

$$FS = -V_{REF} \left(\frac{1023}{1024} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF} \left(\frac{1}{1024} \right)$$

Table 2. Bipolar (Offset Binary)
Code Table

Digital Input MSB LSB	Nominal Analog Output (V _{OUT} as shown in Figure 4)
111111111	$-V_{REF} \left(\frac{511}{512} \right)$
100000001	$-V_{REF} \left(\frac{1}{512} \right)$
100000000	0
011111111	$+V_{REF} \left(\frac{1}{512} \right)$
000000001	$+V_{REF} \left(\frac{511}{512} \right)$
000000000	$+V_{REF} \left(\frac{512}{512} \right)$

NOTES: 1. Nominal Full Scale for the circuit of Figure 4 is given by

$$FSR = V_{REF} \left(\frac{1023}{512} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF} \left(\frac{1}{512} \right)$$

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NOTE: All typical values have been characterized but are not tested.

POWER DAC DESIGN USING AD7533

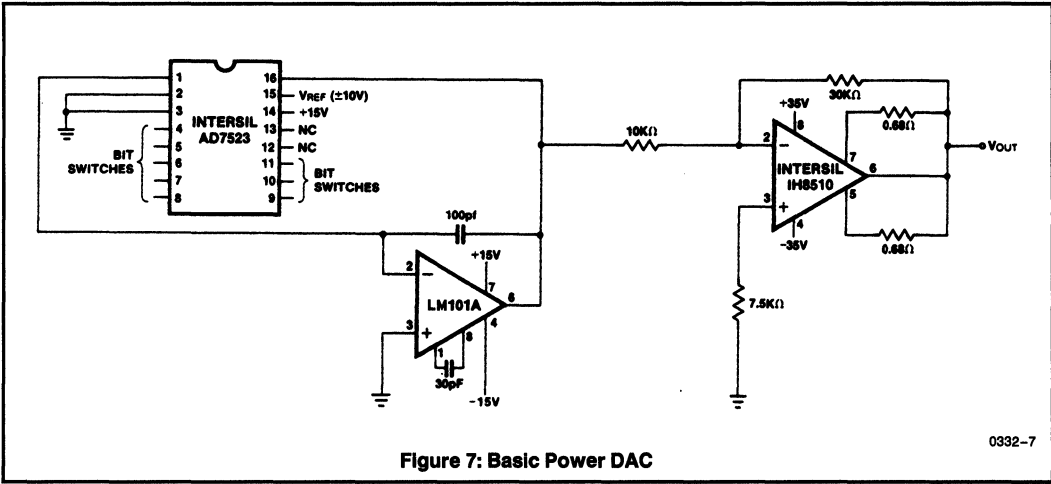


Figure 7: Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 7. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to ±25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise the AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the LM101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

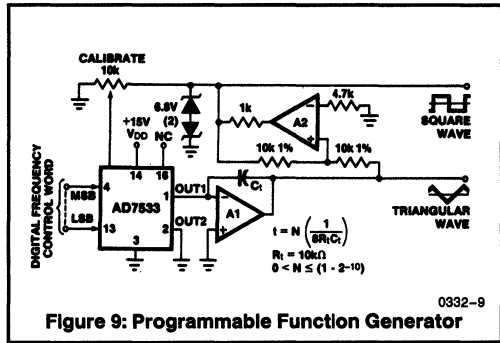


Figure 9: Programmable Function Generator

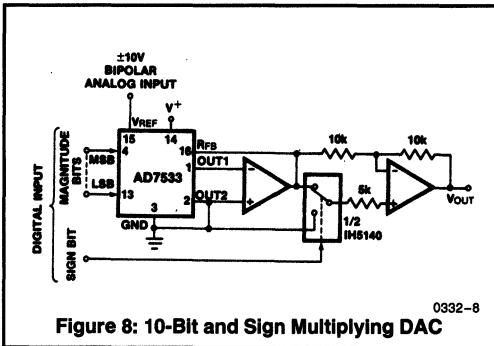


Figure 8: 10-Bit and Sign Multiplying DAC

4

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NOTE: All typical values have been characterized but are not tested.

AD7541 12-Bit Multiplying D/A Converter



GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FEATURES

- 12 Bit Linearity (0.01%)
- Pretrimmed Gain
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- DTL/TTL/CMOS Compatible
- + 5 to + 15 Volts Supply Range
- Low Power Dissipation (20mW)
- Current Settling Time: 1μs to 0.01% of FSR
- Four Quadrant Multiplication
- 883B Processed Versions Available

ORDERING INFORMATION

Nonlinearity	Part Number/Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	-	-

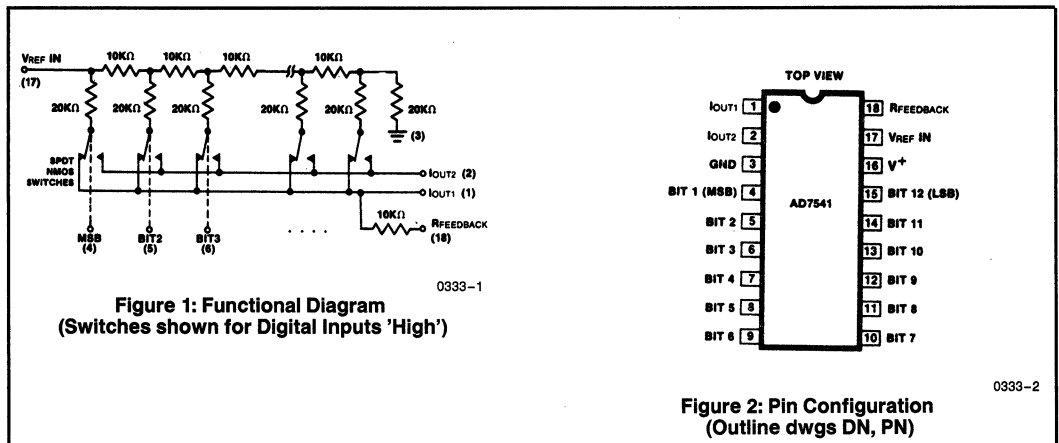


Figure 1: Functional Diagram
(Switches shown for Digital Inputs 'High')

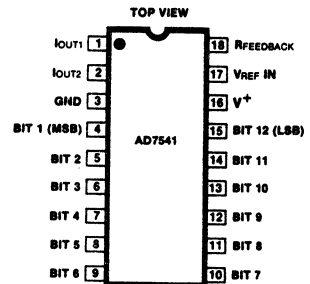


Figure 2: Pin Configuration
(Outline dwgs DN, PN)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

V ⁺	+17V
V _{REF}	±25V
Digital Input Voltage Range	GND to V ⁺
Output Voltage Compliance	-100mV to V ⁺
Power Dissipation (package):	
up to +75°C	450mW
derate above +75°C by	6mW/°C

Operating Temperature Range:	
JN, KN, LN Versions	0°C to +70°C
AD, BD Versions	-25°C to +85°C
SD, TD Versions	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

CAUTION

- The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{IB}.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V⁺ = +15V, V_{REF} = +10V, T_A = 25°C unless otherwise specified)

Parameter		Test Conditions	T _A +25°C	T _A Min-Max	Limit	Fig.	Unit
DC ACCURACY (Note 1)							
Resolution			12	12	Min		Bits
Nonlinearity (Note 2)	S	-10V ≤ V _{REF} ≤ +10V V _{OUT1} = V _{OUT2} = 0V	±0.024	±0.024	Max	3	% of FSR
	T						% of FSR
	L						% of FSR
			Guaranteed Monotonic				
Gain Error (Note 2)		-10V ≤ V _{REF} ≤ +10V	±0.3	±0.4	Max		% of FSR
Output Leakage Current (either output)		V _{OUT1} = V _{OUT2} = 0	±50	±200	Max		nA
AC ACCURACY (Note 3)							
Power Supply Rejection (Note 2)		V ⁺ = 14.5 to 15.5V	±0.005	±0.01	Max	4	% of FSR/%
Output Current Settling Time		To 0.01% of FSR	1		Max	8	μs
Feedthrough Error		V _{REF} = 20V pp, 10kHz. All digital inputs low.	1		Max	7	mV pp
REFERENCE INPUT							
Input Resistance	All digital inputs high. I _{OUT1} at ground.		5K		Min		Ω
			10K		Typ		
			20K		Max		
ANALOG OUTPUT							
Voltage Compliance (Note 4)		Both outputs. See maximum ratings.	-100mV to V ⁺				
Output Capacitance (Note 3)	C _{OUT1}	All digital inputs high (V _{INH})	200		Max	6	pF
	C _{OUT2}		60				
	C _{OUT1}	All digital inputs low (V _{INL})	60		Max	6	pF
	C _{OUT2}		200				
Output Noise (both outputs)			Equivalent to 10KΩ Johnson noise		Typ	5	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V_{REF} = +10V$, $T_A = 25^\circ C$ unless otherwise specified)

(Continued)

Parameter	Test Conditions	TA + 25°C	TA Min-Max	Limit	Fig.	Unit
DIGITAL INPUTS						
Low State Threshold (V_{INL})		0.8		Max		V
High State Threshold (V_{INH})		2.4		Min		V
Input Current	$V_{IN} = 0$ or V^+	± 1		Max		μA
Input Coding	See Tables 1 & 2	Binary/Offset Binary				
Input Capacitance (Note 3)		8		Max		pF
POWER REQUIREMENTS						
Power Supply Voltage Range	Accuracy is not guaranteed over this range	+ 5 to + 16				V
I^+	All digital inputs high or low	2.0	2.5	Max		mA
Total Power Dissipation (Including the ladder)		20		Typ		mW

- NOTES: 1. Full scale range (FSR) is 10V for unipolar and $\pm 10V$ for bipolar modes.
 2. Using internal feedback resistor, $R_{FEEDBACK}$.
 3. Guaranteed by design; not subject to test.
 4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

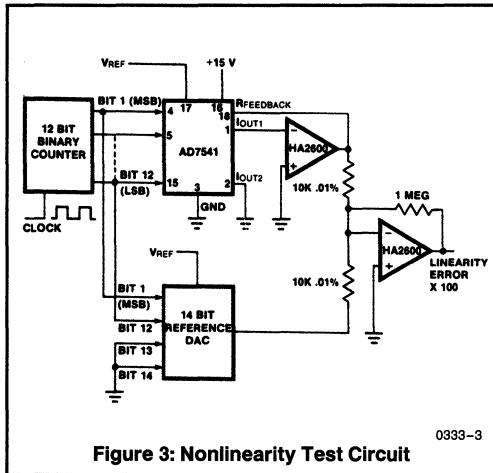


Figure 3: Nonlinearity Test Circuit

0333-3

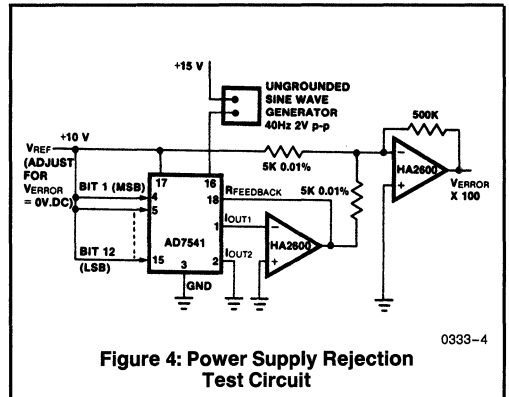


Figure 4: Power Supply Rejection Test Circuit

0333-4

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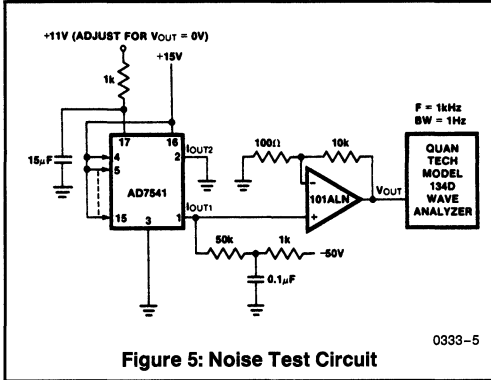


Figure 5: Noise Test Circuit

0333-5

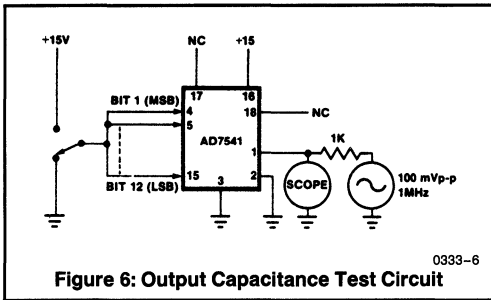


Figure 6: Output Capacitance Test Circuit

0333-6

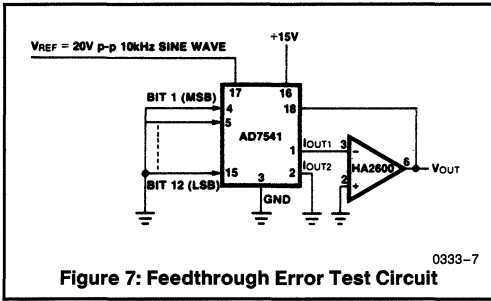


Figure 7: Feedthrough Error Test Circuit

0333-7

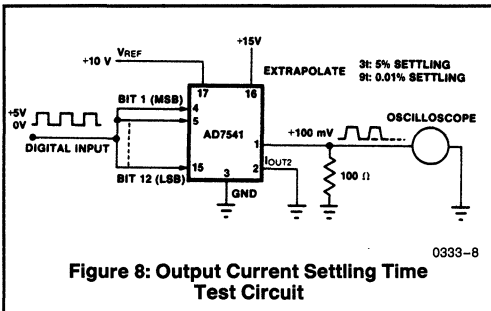


Figure 8: Output Current Settling Time Test Circuit

0333-8

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n}) (V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}] [V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within $1/2$ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

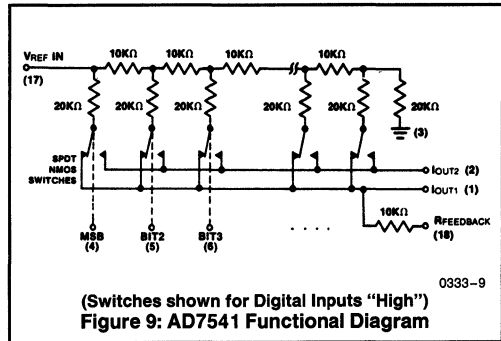
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DETAILED DESCRIPTION

The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.



(Switches shown for Digital Inputs "High")
Figure 9: AD7541 Functional Diagram

0333-9

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NOTE: All typical values have been characterized but are not tested.

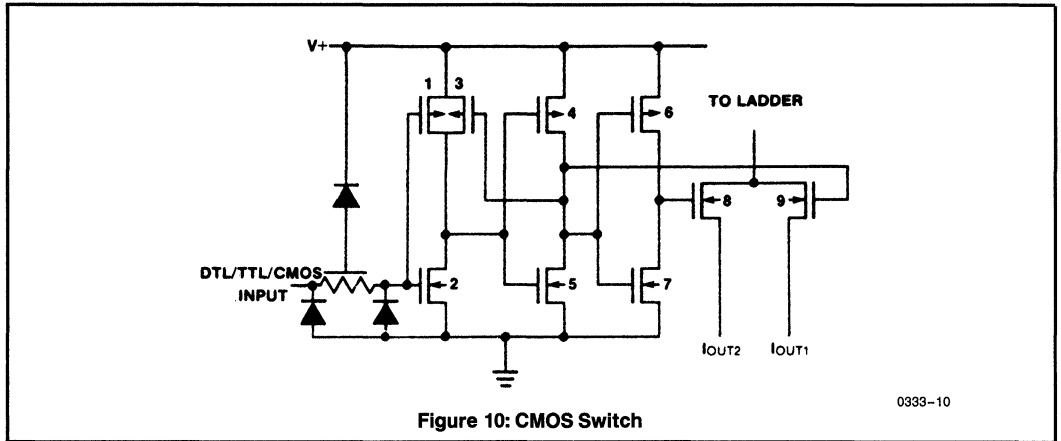


Figure 10: CMOS Switch

0333-10

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 10). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on IOUT1 and IOUT2 (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu\text{V}$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or VDD for proper operation.

A high value resistor ($\sim 1\text{M}\Omega$) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 11. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents IOUT1 from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

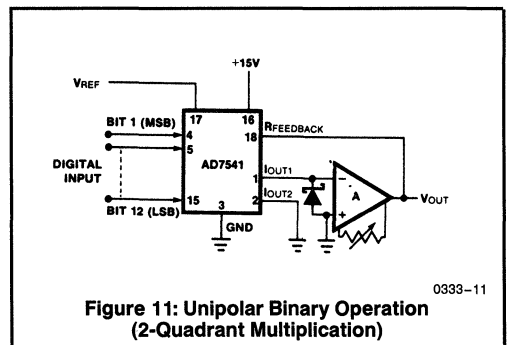


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

0333-11

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NOTE: All typical values have been characterized but are not tested.

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for $0V \pm 0.5mV$ (max) at V_{OUT} .

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor V_{OUT} for a $-V_{REF}$ ($1 - 1/2^{12}$) reading.
3. To increase V_{OUT} , connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease V_{OUT} , connect a series resistor, (0 to 500 ohms), between the reference voltage and the V_{REF} terminal.

Table 1: Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF} (1 - 1/2^{12})$
100000000001	$-V_{REF} (1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF} (1/2 - 1/2^{12})$
000000000001	$-V_{REF} (1/2^{12})$
000000000000	0

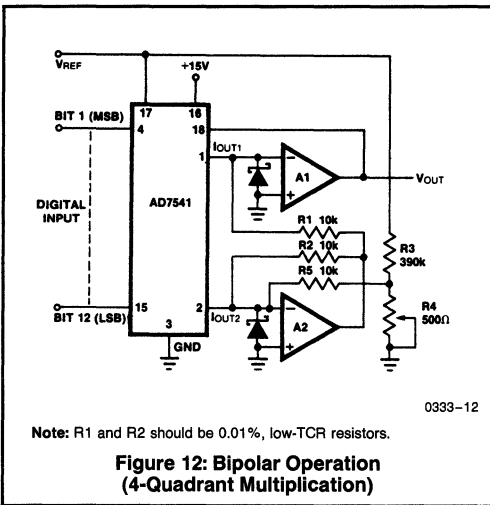


Figure 12: Bipolar Operation (4-Quadrant Multiplication)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB="Logic 1", All other bits="Logic 0"), is corrected by using an external resistive divider, from V_{REF} to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust IOUT2 amplifier offset zero adjust trimpot for $0V \pm 0.1mV$ at IOUT2 amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust IOUT2 amplifier offset zero adjust trimpot for $0V \pm 0.1mV$ at IOUT1 amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for $0V \pm 0.2mV$ at V_{OUT} .

Gain Adjustment

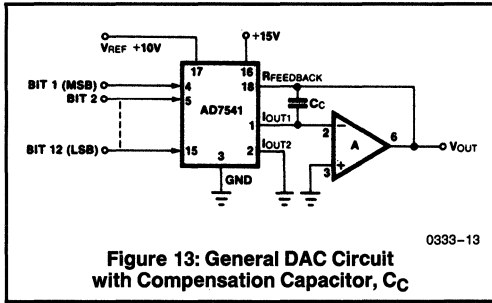
1. Connect all digital inputs to VDD.
2. Monitor V_{OUT} for a $-V_{REF}$ ($1 - 1/2^{11}$) volts reading.
3. To increase V_{OUT} , connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease V_{OUT} , connect a series resistor, (0 to 500 ohms), between the reference voltage and the V_{REF} terminal.

Table 2: Code Table Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF} (1 - 1/2^{11})$
100000000001	$-V_{REF} (1/2^{11})$
100000000000	0
011111111111	$V_{REF} (1/2^{11})$
000000000001	$V_{REF} (1 - 1/2^{11})$
000000000000	V_{REF}

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NOTE: All typical values have been characterized but are not tested.



DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, openloop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between $10k\Omega$ ($R_{FEEDBACK}$ alone) and $5K\Omega$ ($R_{FEEDBACK}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor (as shown in Figure 13) provides the necessary phase compensation to critically damp the output.

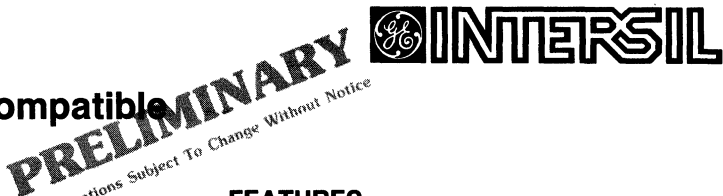
A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

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NOTE: All typical values have been characterized but are not tested.

ICL7121

16-Bit Multiplying Microprocessor-Compatible D/A Converter



GENERAL DESCRIPTION

The ICL7121 achieves 0.003% linearity without laser trimming by combining a four quadrant multiplying DAC using thin film resistors with an on-chip PROM-controlled correction circuit. Silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. The input buffer register is loaded with the 16-bit input and directly controls the output switches. The register is transparent if WR and CS are held low.

The ICL7121 is designed and programmed for bipolar operation. There is an offset resistor to the output with a reference input which should be connected to $-V_{REF}$, giving the DAC a true 2's complement input transfer function. Two extra resistors are included on the chip to facilitate the reference inversion, so that only an external op amp is needed.

FEATURES

- 16-Bit Resolution
- Low Integral Linearity Error—0.003% FSR
- Monotonic to 16 Bits Over Full Military Temperature Range (LM Grade)
- Microprocessor Compatible with Buffered Inputs
- Bipolar Application Requires No External Resistors
- Output Current Settling Time 3 μ s Max (1 μ s Typ)
- Low Linearity and Gain Temperature Coefficients
- Low Power Dissipation (25 mW)
- Full Four-Quadrant Multiplication
- Low Differential Nonlinearity Error at Bipolar Zero

ORDERING INFORMATION

Part Number	Temperature Range	Package	Monotonicity
ICL7121JCJ ICL7121JMJI	0°C to +70°C -55°C to +125°C	28-Pin CERDIP 28-Pin CERDIP	14 Bits
ICL7121KCJ ICL7121KMJI	0°C to +70°C -55°C to +125°C	28-Pin CERDIP 28-Pin CERDIP	15 Bits
ICL7121LCJ ICL7121LMJI	0°C to +70°C -55°C to +125°C	28-Pin CERDIP 28-Pin CERDIP	16 Bits

4

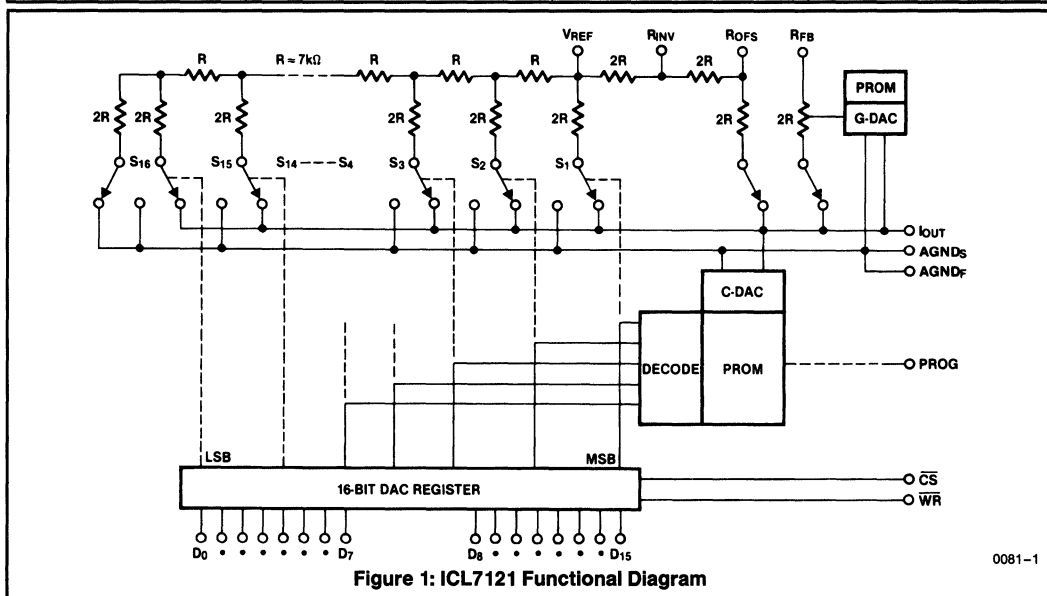


Figure 1: ICL7121 Functional Diagram

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NOTE: All typical values have been characterized but are not tested.

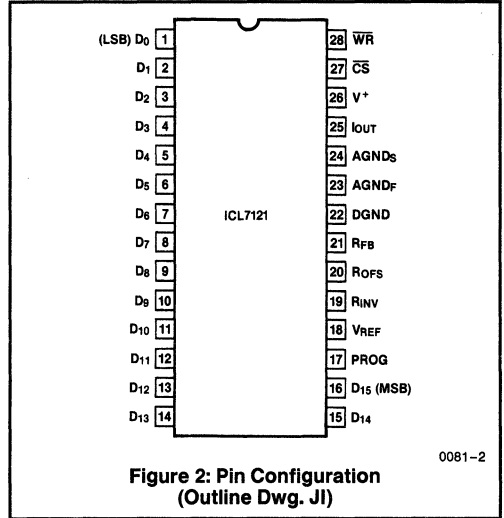
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND -0.3V to 7.5V
 V_{REF} , R_{OFS} , R_{INV} , R_{FB} to DGND $\pm 25V$
 Current in $AGND_F$, $AGND_S$ 25 mA
 D_N , \overline{WR} , \overline{CS} , $PROG$, I_{OUT} ,
 $AGND_F$, $AGND_S$ -0.3V to ($V^+ + 0.3V$)

Operating Temperature
 ICL7121C 0°C to +70°C
 ICL7121M -55°C to +125°C
 Storage Temperature -65°C to +150°C
 Power Dissipation (Note 2) 500 mW
 derate above 70°C @ 10 mW/°C
 Lead Temperature (soldering, 10 sec) 300°C

NOTE 1: All voltages with respect to DGND.
2: Assumes all leads soldered or welded to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0081-2

DC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $V_{REF} = +5V$, $T_A = +25^\circ C$ unless otherwise specified

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
	Resolution	All Grades	16			Bits	
	Monotonicity	(Note 3)	J K L	14 15 16		Bits	
	Differential Linearity Error at Bipolar Zero	$T_A = +25^\circ C$	J K L		1 1 1/2	LSB	
		Operating Temperature Range	J K L		1 1/2 1 1/2 1	LSB	
DLE	Differential Linearity Error	$T_A = +25^\circ C$	J K L	-0.006 -0.003 -0.0015	+0.006 +0.003 +0.003	%FSR	
			Operating Temperature Range	J	-0.006	+0.006	%FSR
				KC LC	-0.006 -0.003	+0.006 +0.0045	
			KM LM	-0.003 -0.0015	+0.0045 +0.0045		
ILE	Integral Linearity Error	$T_A = +25^\circ C$	J K L	-0.006 -0.003 -0.003	± 0.003 ± 0.0015 ± 0.0015	+0.006 +0.003 +0.003	%FSR
			Operating Temperature Range	J K LC LM	-0.009 -0.006 -0.003 -0.006	± 0.006 ± 0.003 ± 0.0015 ± 0.003	+0.009 +0.006 +0.003 +0.006

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NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS

V⁺ = +5V, V_{REF} = +5V, T_A = +25°C unless otherwise specified (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
T _{C(ILE)}	Integral Linearity Error Temperature Coefficient	J K, L		0.3 0.2	1.2 0.9	ppm/°C
GE	Unadjusted Gain Error	T _A = +25°C	J K L	-0.012 ±0.004 ±0.003 ±0.002	+0.012 ±0.009 ±0.006	%FSR
		Operating Temperature Range	J K L	-0.04 ±0.02 ±0.01 ±0.02	+0.04 ±0.02 ±0.01 ±0.02	%FSR
T _{C(GE)}	Unadjusted Gain Error Temperature Coefficient	J K, L		1.0 0.5	5.2 2.0	ppm/°C
V _{oz}	Unadjusted Output Offset	D _N = All 0's (Note 6)		4	±15	mV
ΔV _{oz} /ΔT	Output Offset Drift	D _N = All 0's (Note 6)			5	μV/°C
PSRR	Power Supply Rejection Ratio	V ⁺ = 5V ± 10%, T _A = +25°C		30	100	ppm/V
		Operating Temperature Range		50	150	
t _s	Output Current Settling Time	(Note 4)		1.8	3	μs
Z _{REF}	Reference Input Resistance		3	4.2	6	kΩ
C _{OUT}	Output Capacitance	D _N = All 0's		150		pF
		D _N = All 1's		300		
V _{IL}	Low Level Input Voltage	Operating Temperature Range			0.8	V
V _{IH}	High Level Input Voltage	Operating Temperature Range	2.4			V
I _{IN}	Logic Input Current	0V ≤ V _{IN} ≤ V ⁺	-1.0	0.001	+1.0	μA
C _{IN}	Logic Input Capacitance			15		pF
V ⁺	Supply Voltage Range	Functional Operation (Note 5)	4.5	5.0	5.5	V
I ⁺	Supply Current, excluding Ladder Current	V _{IL} = 0.8V, V _{IH} = 2.4V, T _A = 25°C		0.6	1.5	mA
		Operating Temperature Range		1.0	2.5	

4

NOTES 3: Military temperature range parts are also tested to stated limits at -55°C and +125°C.

4: Guaranteed by characterization but not tested on a production basis.

5: Guaranteed by PSRR test.

6: Refer to Figure 4. Measured at output of amplifier A1 (A1 having zero offset). V_{REF} = +5V. Adjustable to zero with external potentiometer.

AC ELECTRICAL CHARACTERISTICS V⁺ = +5V, T_A = +25°C; see Timing Diagram, Figure 3 (Note 4)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
t _{CWs}	Chip Select-Write Set-Up Time		0			ns
t _{CWh}	Chip Select-Write Hold Time		0			
t _{WR}	Write Pulse Width Low		200			
t _{DWs}	Data-Write Set-Up Time		200			
t _{DWh}	Data-Write Hold Time		0			

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NOTE: All typical values have been characterized but are not tested.

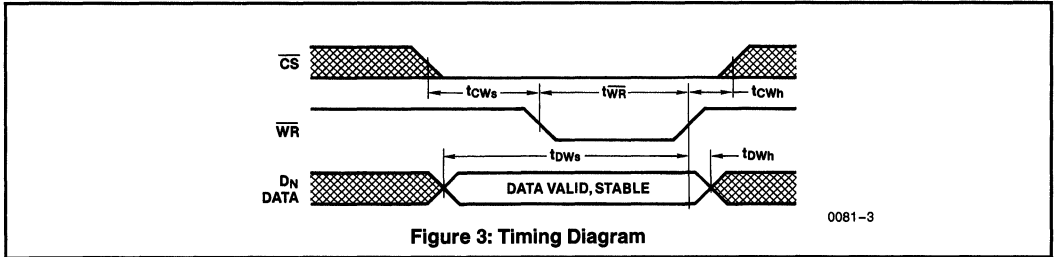


Figure 3: Timing Diagram

Table 1. Pin Assignment and Function Description

Pin	Name	Description	
1	D ₀	Least Significant Bit	
2	D ₁		
3	D ₂		
4	D ₃		
5	D ₄		Input
6	D ₅		
7	D ₆		Data
8	D ₇		
9	D ₈		Bits
10	D ₉		
11	D ₁₀		(HIGH = True)
12	D ₁₁		
13	D ₁₂		
14	D ₁₃		
15	D ₁₄		
16	D ₁₅	Most Significant Bit	
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V _{REF}	V _{REF} input to ladder.	
19	R _{INV}	Summing node for inverting amplifier.	
20	R _{OFFS}	Bipolar offset resistor, to V _{REF} .	
21	R _{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	AGND _F	Analog GrouND Force Line. Used to carry current from internal Analog GrouND connections.	
24	AGND _S	Analog GrouND Sense line. Reference point for external circuitry. Pin should carry minimal current.	
25	I _{OUT}	Current output pin.	
26	V ⁺	Positive supply voltage.	
27	\overline{CS}	Chip Select. Active low. Enables writing to register.	
28	\overline{WR}	Write input. Active low. Writes into register. Equivalent to \overline{CS} .	

DEFINITION OF TERMS

NON-LINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full-scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2⁻ⁿ) (V_{REF}). A bipolar converter of n bits has a resolution of (2⁻⁽ⁿ⁻¹⁾) (V_{REF}). Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

DETAILED DESCRIPTION

The ICL7121 consists of a 16-bit primary DAC, PROM controlled correction DACs, input buffer registers, and microprocessor interface logic. The 16-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances and all other resistors in the ladder results in excellent temperature stability.

The low linearity error is achieved by programming a floating polysilicon gate PROM array which controls a 12-bit correction DAC (C-DAC). The most significant bits of the primary DAC register address this PROM array. Thus for every combination of the primary DAC's most significant bits a different C-DAC code is selected, allowing correction of superposition errors. These errors are caused by bit interaction on the primary ladder's current bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method that corrects individual bits only, such as laser trimming.

The onboard PROM also controls the 6-bit gain DAC. The G-DAC reduces gain error to less than 0.006% FSR by diverting to analog ground up to 2% of the current flowing in R_{FB}.

Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging, unlike wafer-level trimming methods. Also, since the thin film resistors do not suffer laser trimming stresses, no degradation of time-stability results.

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

Bipolar Operation

The circuit diagram for the normal configuration of the ICL7121 is shown in Figure 4. The 2's complement input and positive and negative reference voltage values allow full four-quadrant multiplication. Amplifier A_3 , together with the internal resistors R_{INV1} and R_{INV2} , forms a simple voltage inverter circuit to generate $-V_{REF}$ for the R_{OFS} offset input pin. This will give the nominal "digital input code/analog output value" relationship of Table 2.

Table 2. Code Table—Bipolar Operation

Digital Input	Analog Output
0111111111111111	$-V_{REF} (1 - 1/2^{15})$
0000000000000001	$-V_{REF} (1/2^{15})$
0000000000000000	0
1111111111111111	$V_{REF} (1/2^{15})$
1000000000000001	$V_{REF} (1 - 1/2^{15})$
1000000000000000	V_{REF}

Amplifier A_1 is the output amplifier. An additional amplifier A_2 may be used to force $AGND_F$ if the ground reference point is established elsewhere than at the DAC, as in Figure 5.

4

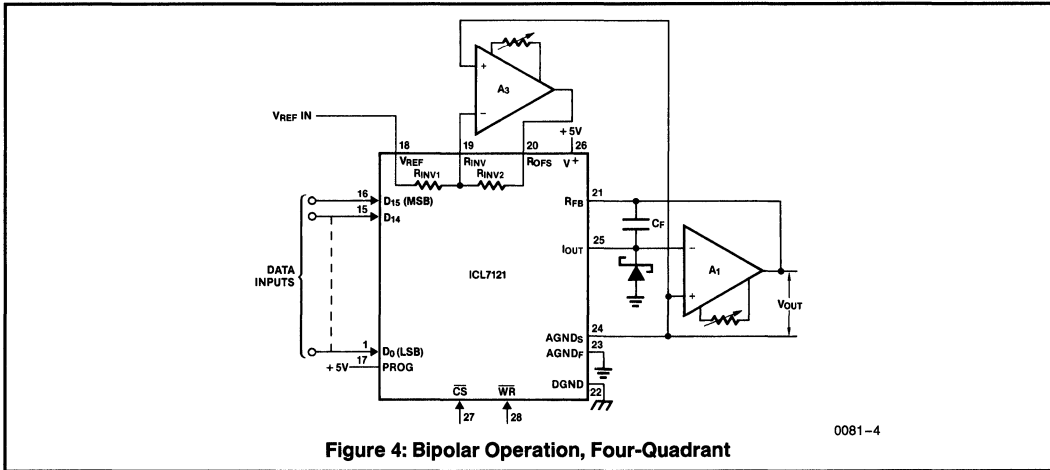


Figure 4: Bipolar Operation, Four-Quadrant

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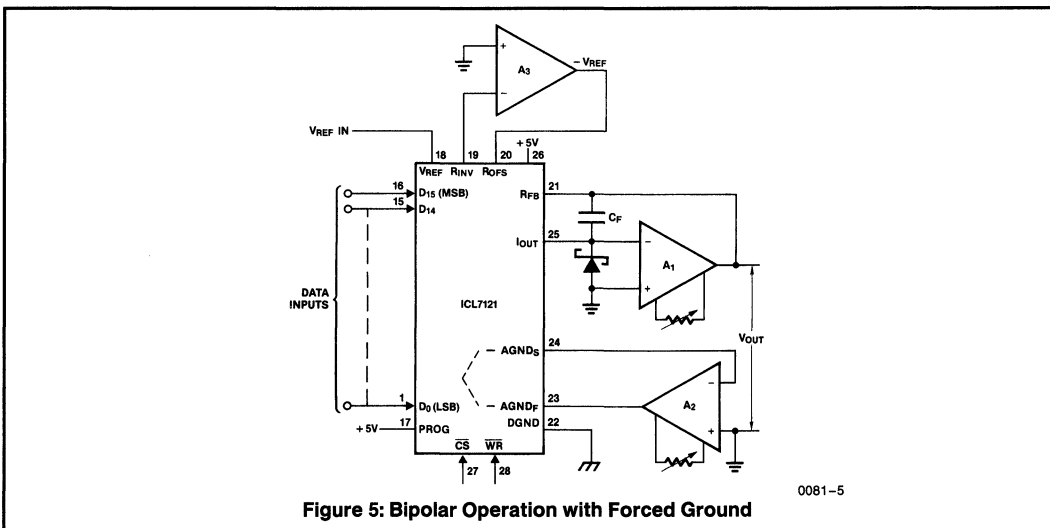


Figure 5: Bipolar Operation with Forced Ground

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NOTE: All typical values have been characterized but are not tested.

A feedback compensation capacitor, C_F , improves the settling time by reducing ringing. This capacitor is normally in the 10 pF–40 pF range, depending on layout and the output amplifier selected. If C_F is too small, ringing or oscillation can occur when using an op amp with a high gain-bandwidth. If C_F is too large, the response of the output amplifier will be overdamped and will settle slowly.

The input circuits of some high speed op amps will sink large currents to their negative supply during power up and power down. The Schottky diode at I_{OUT} limits any negative-going transitions to less than $-0.4V$, avoiding the SCR latchup which could result if significant current was injected into the parasitic diode between I_{OUT} and V^- of the ICL7121. This diode is not needed when using the ICL7650 ultra low V_{OS} op amp.

Offset Adjustment

1. Connect all data inputs and \overline{WR} and \overline{CS} to DGND.
2. Adjust the offset zero-adjust of the operational amplifier A_2 , if used, for $< \pm 50 \mu V$ at $AGND_S$.
3. Set data to 0000 . . . 000 (all low). Adjust the offset zero-adjust of output operational amplifier A_1 for $< \pm 50 \mu V$ at I_{OUT} . V_{OUT} will be offset from 0V by the bipolar zero error.

The bipolar zero error can be as large as 15 mV, but has a typical temperature coefficient of only $3 \mu V/^{\circ}C$. This error may be trimmed out by adjusting the offset of A_3 .

Gain Adjustment

In many systems, gain adjustment will not be needed since the gain of the ICL7121 is accurate to within 0.006% FSR. When system gain must be adjusted, the low gain error limits the required adjustment range to only slightly more than the initial accuracy error of the reference. This is desirable since external gain trims degrade the gain temperature coefficient of a monolithic DAC. This degradation of the gain temperature coefficient occurs because, although the internal resistors track each other closely, they have a temperature coefficient of resistance of approximately $-250 \text{ ppm}/^{\circ}C$.

To increase V_{OUT} , connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21). To decrease V_{OUT} , connect a series resistor of 100Ω or less between the reference voltage and the V_{REF} terminal

(pin 18). These resistor values result in a minimum of 1% FSR gain trim and add about $3 \text{ ppm}/^{\circ}C$ gain temperature coefficient. If only a small gain trim range is needed, the resistor values should be reduced in order to preserve the excellent $0.5 \text{ ppm}/^{\circ}C$ gain temperature coefficient.

Digital Interface

The ICL7121 has a 16-bit latch onboard and can interface directly to a 16-bit data bus. As shown in Figure 6, external latches or peripheral ICs can be used to interface to an 8-bit data bus. To ensure that the data is written into the onboard latch, the data must be valid 200 ns before the rising edge of \overline{WR} . If \overline{WR} and \overline{CS} are both low, the onboard latch is transparent and the input data is directly applied to the internal R-2R ladder switches. While this simplifies interfacing in non-microprocessor systems, having \overline{WR} low before data is valid may cause additional glitches in some microprocessor systems. To avoid these glitches, data must be valid at the time \overline{WR} goes low.

All digital interfaces can suffer from capacitive coupling between the digital lines and the analog section. There are two general precautions that will reduce this capacitive coupling problem: 1) reduce stray capacitance between digital lines and analog lines; and 2) reduce the number of transitions on the digital inputs. Careful board layout and shielding can minimize the capacitive coupling (see Figure 8). The activity on the digital input lines can be reduced by using external latches or peripheral interface ICs between the microprocessor bus and the ICL7121. This will reduce the number of transitions on the digital data and control lines of the ICL7121, thereby reducing the amount of digital noise coupled into sensitive analog sections.

OPERATIONAL AMPLIFIER SECTION

The input offset voltage, input current, gain, and bandwidth of the op amps used affect the circuit performance. Since the output impedance of I_{OUT} varies with the digital input code, the input current of amplifier A_1 will cause a code-dependent error at V_{OUT} , degrading the linearity. The input bias current should be significantly less than 1 LSB current, which is about 10 nA. In a similar manner, any offset voltage in A_1 will also cause linearity errors. The offset voltage of the output amplifier should be significantly less than 1 LSB ($153 \mu V$ at $V_{REF} = 5V$).

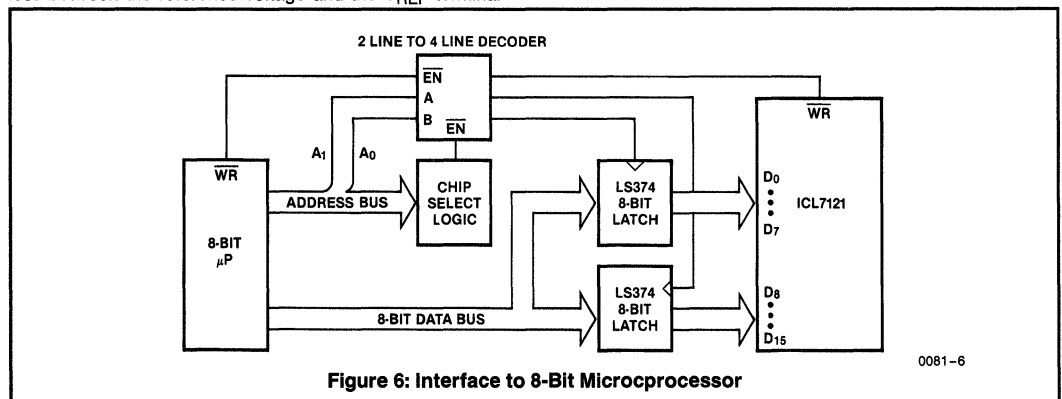


Figure 6: Interface to 8-Bit Microprocessor

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NOTE: All typical values have been characterized but are not tested.

The voltage output settling time is highly dependent on the slow rate and gain-bandwidth of A_1 , so for high speed operation a high speed op amp such as the HA2600 is recommended. For applications where high speed is not required, the ICL7650 or ICL7652 can be used for A_1 . Since the ICL7650/52 offset voltage is less than $5 \mu\text{V}$, no offset trimming is needed. To get a full 5V output swing from these op amps, $\pm 7.5\text{V}$ supplies should be used for the ICL7650/52.

Amplifier A_3 , which is used to generate the inverted reference, needs only to have a stable offset and to be able to drive a $3 \text{ k}\Omega$ load. Since this is strictly a DC amplifier, the low noise ICL7652 is an ideal choice. Any variation in the offset voltage of A_3 will result in a drift in the bipolar zero, but will not affect the linearity of the ICL7121.

Amplifier A_2 , used to generate a high quality ground, also needs a low offset and the ability to sink up to 2 mA.

MULTIPLYING MODE PERFORMANCE

While the ICL7121 can perform full four-quadrant multiplication, full 0.003% linearity is guaranteed only at $V_{\text{REF}} = +5\text{V}$. This is because the voltage coefficient of resistance of the R-2R ladder and the feedback resistor are significant at the 14- or 16-bit level. This effect is most significant at higher voltages, and adds errors on the order of 0.01% for a $\pm 10\text{V}$ full-scale. While the ICL7121 is tested and specified for $V_{\text{REF}} = +5\text{V}$, the R-2R ladder has the same voltage across it when $V_{\text{REF}} = -5\text{V}$. Therefore, voltage coefficients do not add any error with a -5V reference voltage.

GROUND LOOPS

Careful consideration must be given to ground loops in any high accuracy system. The current into the analog

ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC: AGND_S and AGND_F . The varying current should be absorbed through the AGND_F pin, and the AGND_S pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 7. Output signals should ideally be referenced to the sense pin AGND_S , as shown in the application circuits.

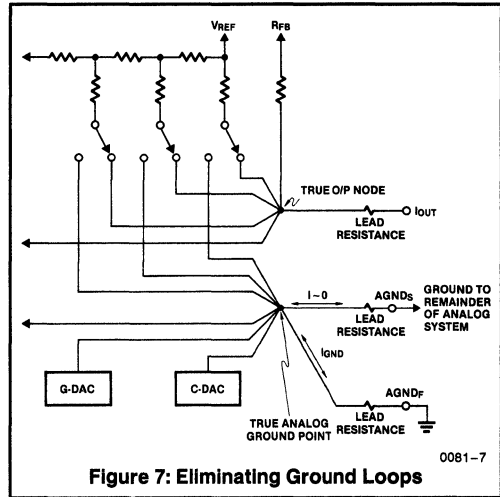
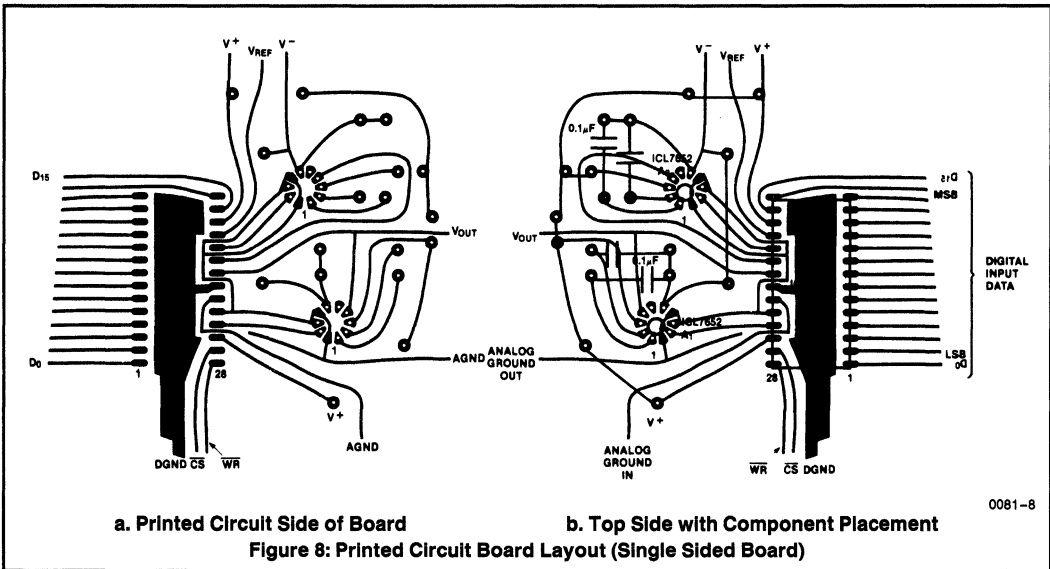


Figure 7: Eliminating Ground Loops

4



a. Printed Circuit Side of Board

b. Top Side with Component Placement

Figure 8: Printed Circuit Board Layout (Single Sided Board)

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NOTE: All typical values have been characterized but are not tested.

ICL7134

14-Bit Multiplying μ P-Compatible D/A Converter



GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistor and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent.

The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

FEATURES

- 14-Bit Linearity (0.003% FSR)
- No Gain Adjustment Necessary
- Microprocessor-Compatible With Double Buffered Inputs
- Bipolar Application Requires No Extra Adjustments or External Resistors
- Low Linearity and Gain Temperature Coefficients
- Low Power Dissipation
- Full Four-Quadrant Multiplication

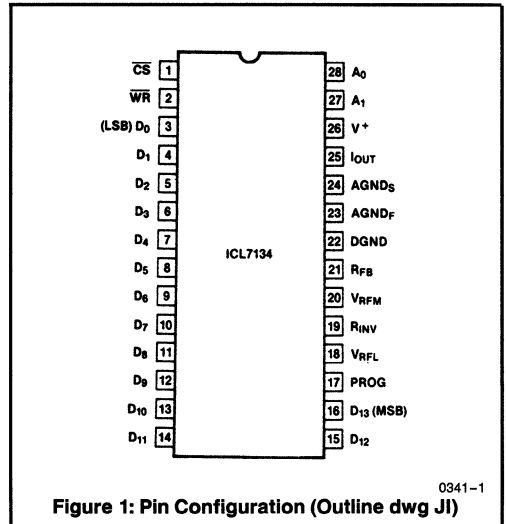


Figure 1: Pin Configuration (Outline dwg JI)

ORDERING INFORMATION

Non-Linearity at 25°C	Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
Bipolar Versions			
0.01% (12-bit)	ICL7134BJCJI	ICL7134BJIJI	ICL7134BJMJI
0.006% (13-bit)	ICL7134BKCJI	ICL7134BKJIJI	ICL7134BKMIJI
0.003% (14-bit)	ICL7134BLCJI	ICL7134BLIJI	ICL7134BLMIJI
Unipolar Versions			
0.01% (12-bit)	ICL7134UJCJI	ICL7134UJIJI	ICL7134UJMJI
0.006% (13-bit)	ICL7134UKCJI	ICL7134UKIJI	ICL7134UKMIJI
0.003% (14-bit)	ICL7134ULCJI	ICL7134ULIJI	ICL7134ULMIJI

PACKAGE: 28-pin CERDIP only

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to DGND) -0.3V to 7.5V
 V_{RFL} , V_{RFM} , R_{INV} , R_{FB} to DGND $\pm 15V$
 I_{OUT} , $AGND_S$, $AGND_F$ -0.1V to V^+
 Current in $AGND_S$, $AGND_F$ 25mA
 A_n , D_n , WR , CS , $PROG$ -0.3V to $V^+ + 0.3V$

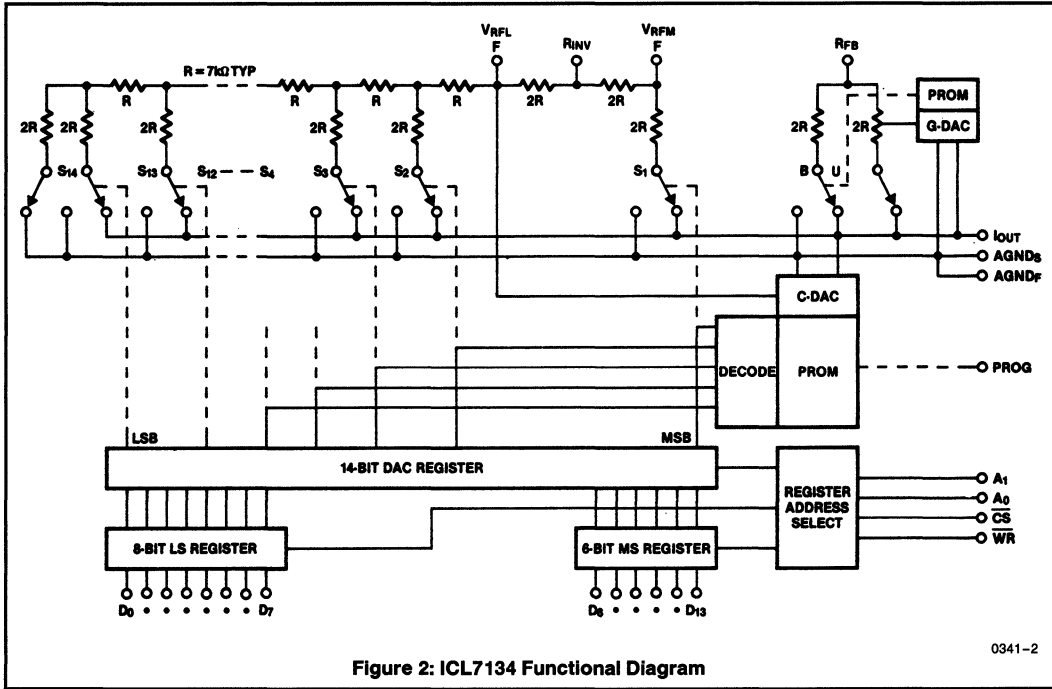
Operating Temperature Range

ICL7134XXC 0°C to +70°C
 ICL7134XXI -25°C to +85°C
 ICL7134XXM -55°C to +125°C
 Storage Temperature Range -65°C to +150°C
 Power Dissipation (Note 2) 500mW
 Derate Linearly Above 70°C @ 10mW/°C
 Lead Temperature (Soldering, 10sec) 300°C

Note 1: All voltages with respect to DGND.

Note 2: Assumes all leads soldered or welded to printed circuit board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



4

Figure 2: ICL7134 Functional Diagram

ELECTRICAL CHARACTERISTICS ($V^+ = 5V$, $V_{REF} = 10V$, $T_A = 25^\circ C$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
	Resolution		14			Bits
	Non-Linearity	Test Figure 4 (Notes 1 and 2)			0.012	% FSR
					0.006	% FSR
					0.003	% FSR
	Non-Linearity Temperature Coefficient (Note 3)	Operating Temperature Range		1	2	ppm/°C

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V^+ = 5V$, $V_{REF} = 10V$, $T_A = 25^\circ C$ unless otherwise specified.) (Continued)

Symbol	Parameter		Test Conditions	Limits			Unit
				Min	Typ	Max	
	Gain Error	J	Test Figure 4 (Notes 1 and 2)			0.024	% FSR
		K				0.012	% FSR
		L				0.006	% FSR
	Gain Error Temperature Coefficient (Note 3)			2	8		ppm/ $^\circ C$
	Monotonicity (Note 3)	J		12			Bits
		K		13			Bits
		L		14			Bits
I _{OLK}	I _{OUT} Leakage Current		T _A = +25 $^\circ C$ Operating Temperature Range			10 60	nA
PSRR	Power Supply Rejection		T _A = +25 $^\circ C$, $\Delta V^+ = \pm 10\%$ Operating Temperature Range		10	100	ppm/V
						150	
	Output Current Settling Time				1		μs
	Feedthrough Error	ICL7134U	V _{REF} = $\pm 10V$, 2kHz Sinewave		250		μV -p-p
		ICL7134B			500		
Z _{REF}	Reference Input Resistance		V _{RFL} = V _{RFM} (Unipolar Mode)	4.0		10	k Ω
C _{OUT}	Output Capacitance		DAC Register = All 0's		160		pF
			DAC Register = All 1's		235		
	Output Noise		Equivalent Johnson Res.		7		k Ω
V _{INL}	Low State Input		Operating Temperature Range			0.8	V
V _{INH}	High State Input		Operating Temperature Range	2.4			V
I _{lin}	Logic Input Current		0 \leq V _{IN} \leq V ⁺			1.0	μA
C _{lin}	Logic Input Capacitance		(Note 3)		15		pF
V ⁺	Supply Voltage Range (Note 4)		Functional Operation	3.5		6.0	V
I ⁺	Supply Current (Note 5)		(Excluding Ladder) (Note 5)		1.0	2.5	mA
	Long Term Stability		1000 Hours, +125 $^\circ C$ (Note 3)		10		ppm/month

NOTES: 1. Full-Scale Range (FSR) is 10V for unipolar mode, 20V ($\pm 10V$) for bipolar mode.

2. Using internal feedback and reference inverting resistors.

3. Guaranteed by design, not production tested.

4. Full scale tested to 0.040% FSR.

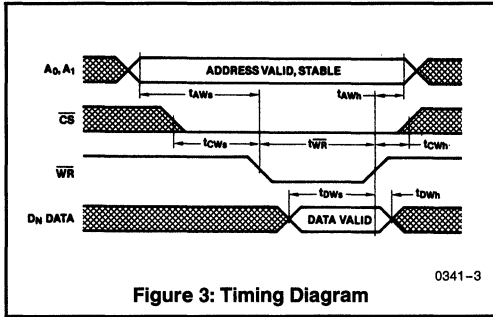
5. D0-D13 connected to 2.4V.

AC CHARACTERISTICS ($V^+ = 5V$, $T_A = 25^\circ C$, see Timing Diagram)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{AWs}	Address-WRite Set-Up Time		100			ns
t _{AWh}	Address-WRite Hold Time	(Note 3)	0			
t _{CWs}	Chip Select-WRite Set-Up Time	(Note 3)	0			
t _{CWh}	Chip Select-WRite Hold Time	(Note 3)	0			
t _{WR}	WRite Pulse Width Low		200			
t _{DWs}	Data-WRite Set-Up Time		200			
t _{DWh}	Data-WRite Hold Time	(Note 3)	0			

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NOTE: All typical values have been characterized but are not tested.



DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a straight line function between end points. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n}) (V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}] [V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within $\frac{1}{2}$ LSB for a given digital input stimulus, i.e., 0 to full-scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Table 1: Pin Descriptions

Pin	Symbol	Description	
1	\overline{CS}	Chip Select (active low). Enables register write.	
2	\overline{WR}	WRite, (active low). Writes in register. Equivalent to \overline{CS} .	
3	D_0	Bit 0	Least significant Input Data Bits (High = True) Most significant.
4	D_1	Bit 1	
5	D_2	Bit 2	
6	D_3	Bit 3	
7	D_4	Bit 4	
8	D_5	Bit 5	
9	D_6	Bit 6	
10	D_7	Bit 7	
11	D_8	Bit 8	
12	D_9	Bit 9	
13	D_{10}	Bit 10	
14	D_{11}	Bit 11	
15	D_{12}	Bit 12	
16	D_{13}	Bit 13	
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{RFL}	V_{REF} for lower bits.	
19	R_{INV}	Summing node for reference inverting amplifier.	
20	V_{RFM}	V_{REF} for MSB only (bipolar).	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force lines. Use to carry current from internal Analog GrouND connections. Tied internally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive voltage.	
27	A_1	Address 1	Control register lines
28	A_0	Address 0	

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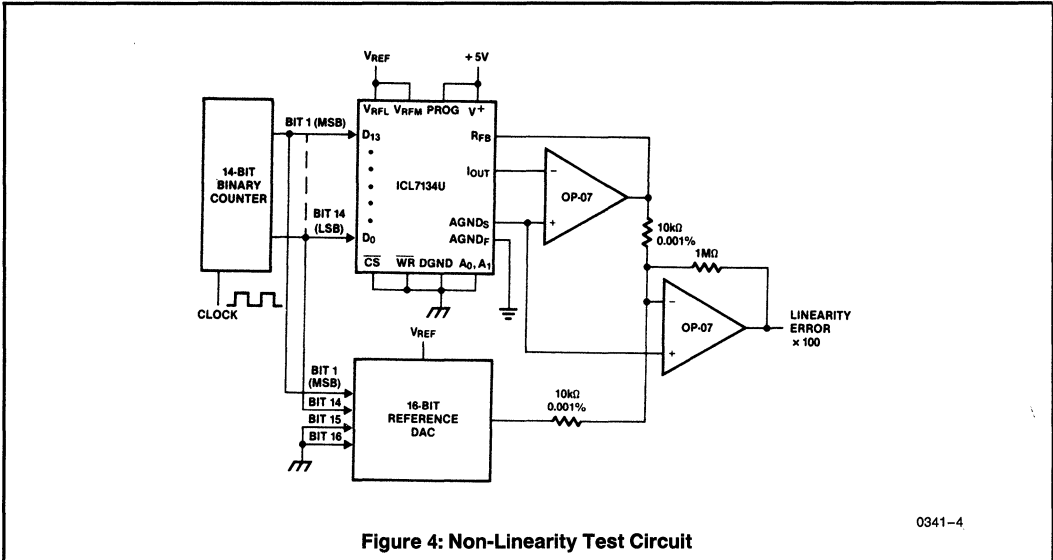


Figure 4: Non-Linearity Test Circuit

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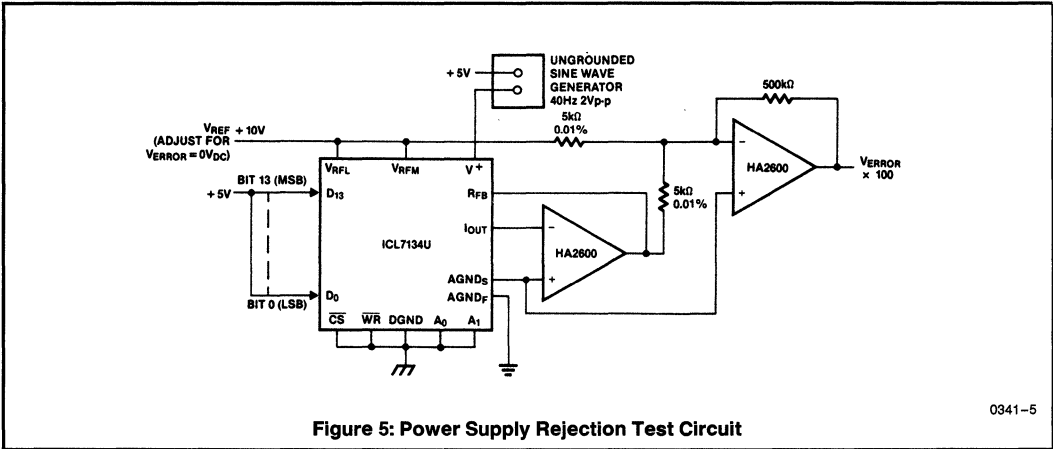


Figure 5: Power Supply Rejection Test Circuit

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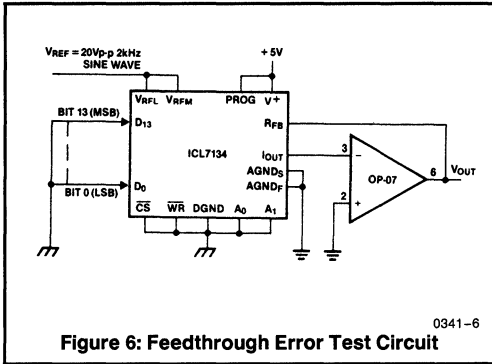


Figure 6: Feedthrough Error Test Circuit

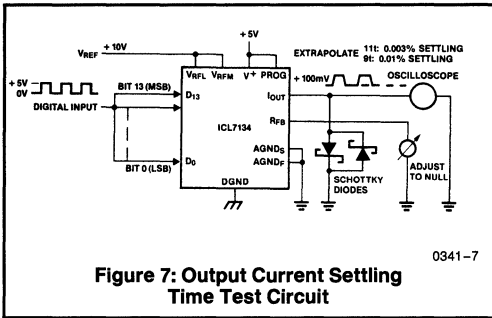


Figure 7: Output Current Settling Time Test Circuit

Analog Section

The ICL7134 inherently provides both unipolar and bipolar operation. The bipolar application circuit (Figure 8) requires one additional op-amp but no external resistors. The two on-chip resistors, R_{IN1} and R_{IN2} , together with the op-amp, form a voltage inverter which drives the MSB reference terminal, V_{RFM} , to $-V_{REF}$, where V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL} . This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF} , and the R_{IN} pin is left unconnected.

Since the PROM correction codes required are different for bipolar and unipolar operation, the ICL7134 is available in two different versions; the ICL7134U, which is corrected for unipolar operation, and the ICL7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from 'R' in the unipolar device to '2R' in the bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

Digital Section

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations: 1) load the LS-buffer register with the data at inputs D_0 to D_7 ; 2) load the MS-buffer register with the data at inputs D_8 to D_{13} ; 3) load the DAC register with the contents of the MS and LS-buffer registers and 4) load the DAC register directly from the data input pins (see Table 2). The \overline{CS} and \overline{WR} pins must be low to allow data transfers to occur. When direct loading is selected (\overline{CS} , \overline{WR} , A_0 and A_1 low) the registers are transparent, and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to V^+ (+5V).

Table 2: Data Loading Controls

Control I/P				ICL7134 Operation
A_0	A_1	\overline{CS}	\overline{WR}	
X	X	X	1	No operation, device not selected.
X	X	1	X	
0	0	0	0	Load all registers from data bus.
0	1	0	0	Load LS register from data bus.
1	0	0	0	Load MS register from data bus.
1	1	0	0	Load DAC register from MS and LS register.

Note: Data is latched on LO-HI transition of either \overline{WR} or \overline{CS} .

DETAILED DESCRIPTION

The ICL7134 consists of a 14-bit primary DAC, two PROM controlled correction DACs, input buffer registers, and microprocessor interface logic (Figure 2). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC, or G-DAC, diverts up to 2% of the feedback resistor's current to Analog GounND and reduces the gain error to less than 1 LSB, or 0.006%. The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC, or C-DAC. For every combination of the primary DAC's 5 most significant bits, a different C-DAC code is selected. This allows correction of superposition errors, caused by bit interaction on the primary resistor ladder's current output bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method which corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging. These packaging shifts limit the accuracy that can be achieved using wafer level correction methods such as laser trimming, which has also been found to degrade the time stability of thin film resistors at the 14-bit level.

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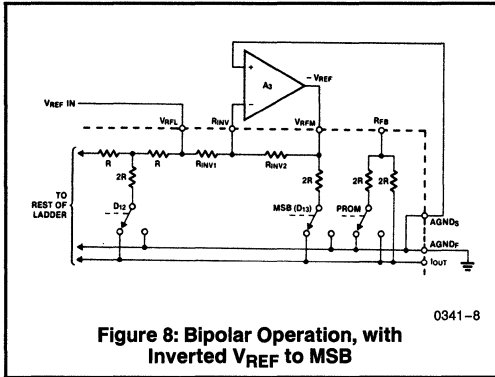


Figure 8: Bipolar Operation, with Inverted V_{REF} to MSB

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APPLICATIONS

General Recommendations
GROUND LOOPS

Careful consideration must be given to ground loops in any 14-bit accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, the $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 9. Thus output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

OPERATIONAL AMPLIFIER SELECTION

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than $25\mu V$) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10V range also requires that the output amplifier has a high open loop gain ($A_{VOL} > 400k$ for effective input offset less than $25\mu V$).

The reference inverting amplifier used in the bipolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than $50\mu V$), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the Analog Ground line (op-amp A_2 in Figure 11). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than $50\mu V$).

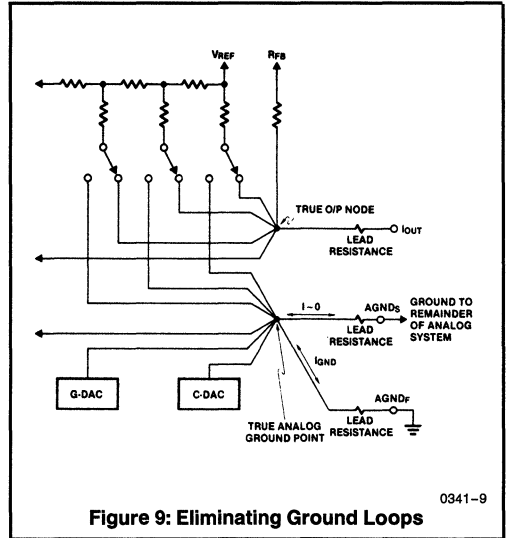


Figure 9: Eliminating Ground Loops

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The op-amp requirements can be readily met by use of an ICL7650 chopper stabilized device. For faster settling time, an HA26XX can be used with an ICL7650 providing automatic offset null (see A053 for details).

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/ $^{\circ}C$) resistors or trim-pots should be selected.

POWER SUPPLIES

The V^+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V^+ , which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V^+ for proper operation.

Unipolar Binary Operation (ICL7134U)

The circuit configuration for unipolar mode operation (ICL7134U) is shown in Figure 10. With positive and negative V_{REF} values the circuit is capable of two-quadrant multiplication. The "digital input code/analog output value" table for unipolar mode is given in Table 3. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers. For applications where the output reference ground point is established somewhere other than at the DAC, the circuit of Figure 11 can be used. Here, op-amp A_2 removes the slight error due to IR voltage drop between the internal Analog Ground node and the external ground connection. For 13-bit or lower accuracy, omit A_2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.

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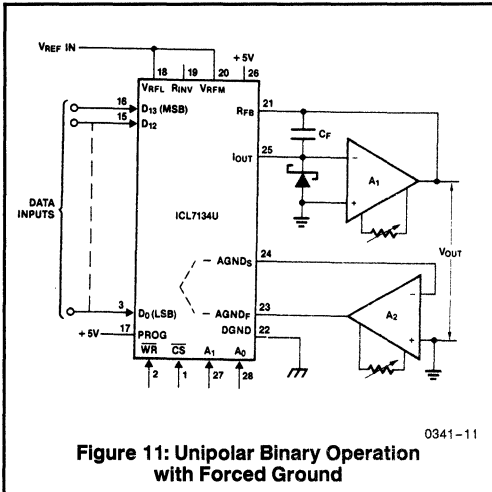
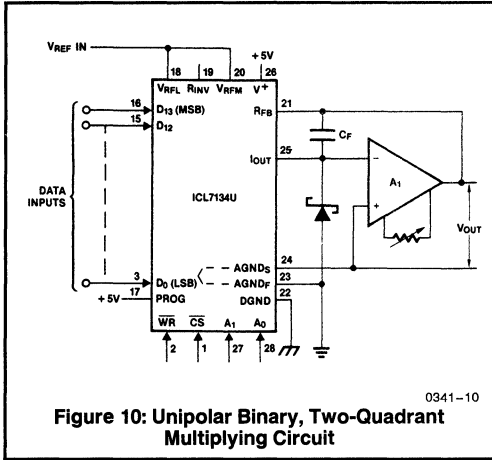


Table 3: Code Table — Unipolar Binary Operation

Digital Input	Analog Output
1111111111111111	$-V_{REF}(1 - \frac{1}{2}^{14})$
1000000000000001	$-V_{REF}(\frac{1}{2} + \frac{1}{2}^{14})$
1000000000000000	$-V_{REF}/2$
0111111111111111	$-V_{REF}(\frac{1}{2} - \frac{1}{2}^{14})$
0000000000000001	$-V_{REF}(\frac{1}{2}^{14})$
0000000000000000	0

ZERO OFFSET ADJUSTMENT

1. Connect all data inputs and \overline{WR} , \overline{CS} , A_0 and A_1 to DGND.
2. Adjust offset zero-adjust trim-pot of the operational amplifier A_2 , if used, for a maximum of $0V \pm 50\mu V$ at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of the output op-amp, A_1 , for a maximum of $0V \pm 50\mu V$ at V_{OUT} .

GAIN ADJUSTMENT (OPTIONAL)

1. Connect all data inputs to V^+ , connect \overline{WR} , \overline{CS} , A_0 and A_1 to DGND.
2. Monitor V_{OUT} for a $-V_{REF}(1 - \frac{1}{2}^{14})$ reading.
3. To decrease V_{OUT} , connect a series resistor of 100Ω or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT} , connect a series resistor of 100Ω or less between A_1 output and the R_{FB} terminal (pin 21).

Bipolar (2's Complement) Operation (ICL7134B)

The circuit configuration for bipolar mode operation (ICL7134B) is shown in Figure 12. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. The "digital input code/analog output value" table for bipolar mode is given in Table 4. Amplifier A_3 , together with internal resistors R_{INV1} and R_{INV2} , forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the ICL7134B's feedback resistance is switched to $2R$ under PROM control, so that the bipolar output range is $+V_{REF}$ to $-V_{REF}(1 - \frac{1}{2}^{13})$. Again, the grounding arrangement of Figure 11 can be used, if necessary.

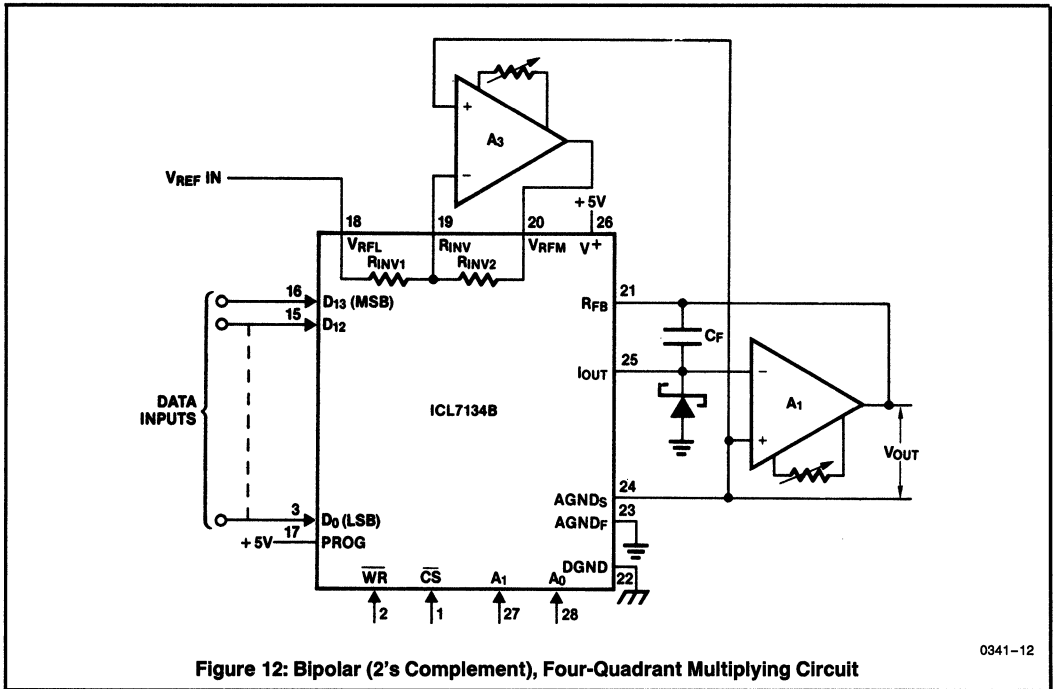
Table 4: Code Table — Bipolar (2's Complement) Operation

Digital Input	Analog Output
0111111111111111	$-V_{REF}(1 - \frac{1}{2}^{13})$
0000000000000001	$-V_{REF}(\frac{1}{2}^{13})$
0000000000000000	0
1111111111111111	$V_{REF}(\frac{1}{2}^{13})$
1000000000000001	$V_{REF}(1 - \frac{1}{2}^{13})$
1000000000000000	V_{REF}

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OFFSET ADJUSTMENT

1. Connect all data inputs and \overline{WR} , \overline{CS} , A_0 and A_1 to DGND.
2. Adjust the offset zero-adjust trim-pot of the operational amplifier A_2 , if used, for a maximum of $0V \pm 50\mu V$ at $AGND_S$.
3. Set data to 00000...00. Adjust the offset zero-adjust trim-pot of the output op-amp A_1 , for a maximum of $0V \pm 50\mu V$ at V_{OUT} .
4. Connect D_{13} (MSB) data input to V^+ .
5. Adjust the offset zero-adjust trim-pot of op-amp A_3 for a maximum of $0V \pm 50\mu V$ at the R_{INV} terminal (pin 19).

3. Monitor V_{OUT} for a $-V_{REF}$ ($1 - \frac{1}{2}1^3$) reading.
4. To increase V_{OUT} , connect a series resistor of 200Ω or less between the A_1 output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT} , connect a series resistor of 100Ω or less between the reference voltage and the V_{RFL} terminal (pin 18).

GAIN ADJUSTMENT (OPTIONAL)

1. Connect \overline{WR} , \overline{CS} , A_0 and A_1 to DGND.
2. Connect $D_0, D_1 \dots D_{12}$ to V^+ , D_{13} (MSB) to DGND.

Processor Interfacing

The ease of interfacing to a processor can be seen from Figure 13, which shows the ICL7134 connected to an 8035 or any other processor such as an 8049. The data bus feeds into both register inputs; three port lines, in combination with the \overline{WR} line, control the byte-wide loading into these registers and then the DAC register. A complete DAC set-up requires 4 write instructions to the port, to set up the address and \overline{CS} lines, and 3 external data transfers, one a dummy for the final transfer to the DAC register.

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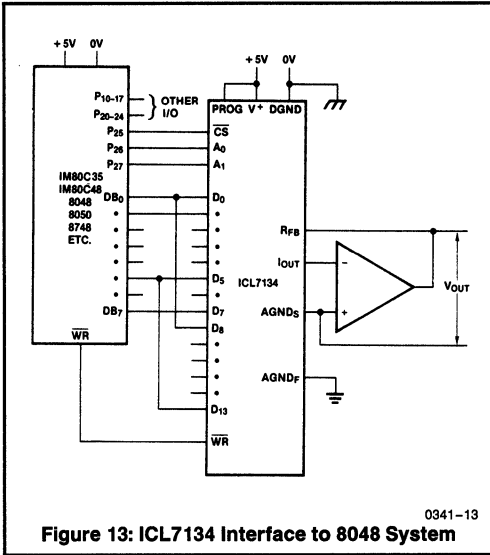


Figure 13: ICL7134 Interface to 8048 System

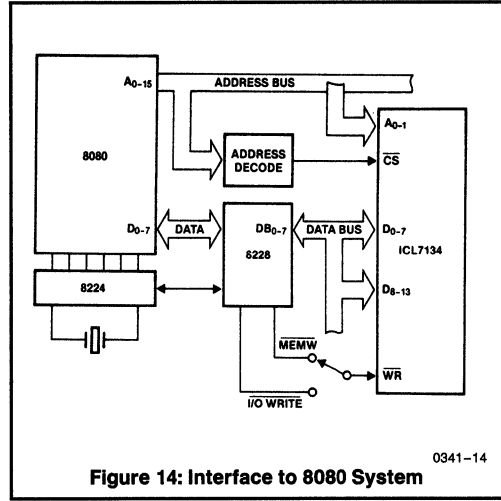


Figure 14: Interface to 8080 System

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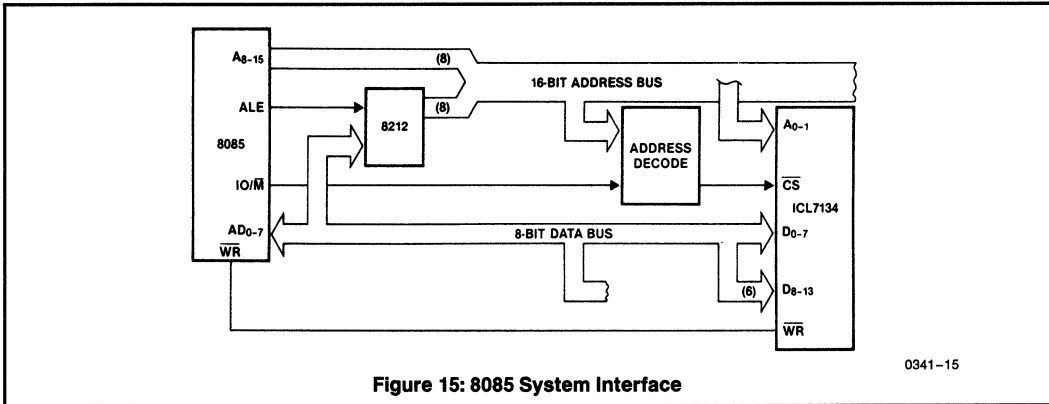


Figure 15: 8085 System Interface

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A similar arrangement can be used with an 8080A, 8228, and 8224 chip set. Figure 14 shows the circuit, which can be arranged as a memory-mapped interface (using MEMW) or as an I/O-mapped interface (using I/O WRITE). See A020 and R005 for discussions of the relative merits of memory-mapped versus I/O-mapped interfacing, as well as some other ideas on interfacing with 8080 processors. The 8085 processor has a very similar interface, except that the control lines available are slightly different, as shown in Fig-

ure 15. The decoding of the IO/M line, which controls memory-mapped or I/O-mapped operation, is arbitrary, and can be omitted if not necessary. Neither the MC680X nor R650X processor families offer specific I/O operations. Figure 16 shows a suitable interface to either of these systems, using a direct connection. Several other decoding options can be used, depending on the other control signals generated in the system. Note that the R650X family does not require VMA to be decoded with the address lines.

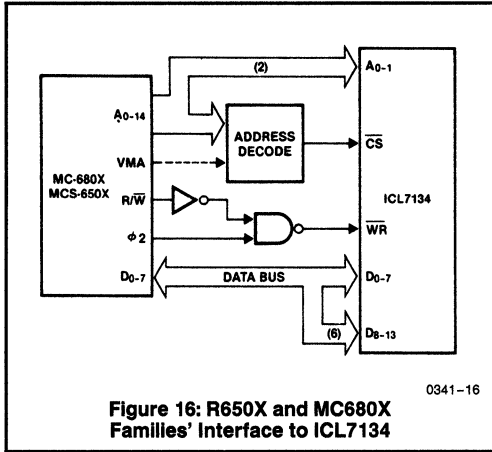


Figure 16: R650X and MC680X Families' Interface to ICL7134

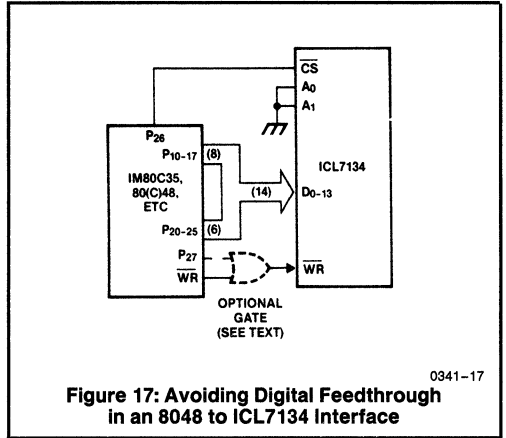


Figure 17: Avoiding Digital Feedthrough in an 8048 to ICL7134 Interface

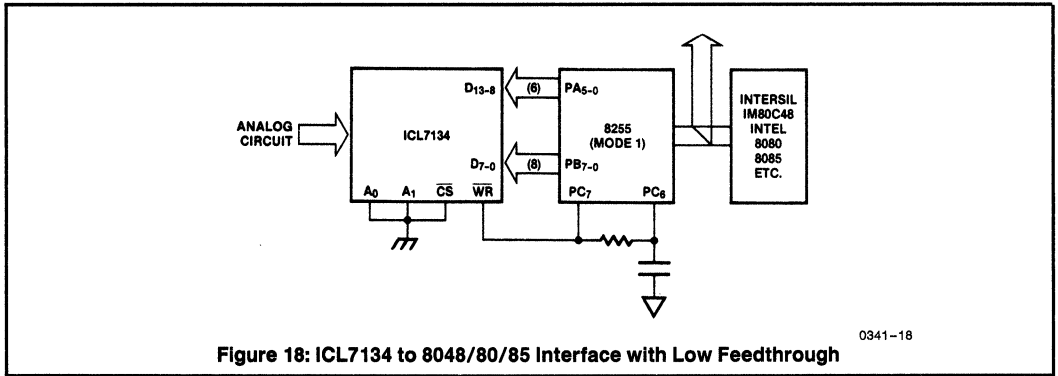


Figure 18: ICL7134 to 8048/80/85 Interface with Low Feedthrough

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Digital Feedthrough

All of the direct interfaces shown above can suffer from a capacitive coupling problem. The 14 data pins, and 4 control pins, all tied to active lines on a microprocessor bus, and in close proximity to the sensitive DAC circuitry, can couple pseudo-random spikes into the analog output. Careful board layout and shielding can minimize the problems (see **PC layout**), and clearly wire-wrap type sockets should never be used. Nevertheless, the inherent capacitance of the package alone can lead to unacceptable digital feedthrough in many cases. The only solution is to keep the digital input lines as inactive as possible. One easy way to do this is to use the peripheral interface circuitry available with all the systems previously discussed. These generally allow only 8 bits to be updated at any one time, but a little ingenuity will avoid difficulties with DAC steps that would result from partial updates. The problem can be solved for the 8048 family by tying the 14 port lines to the data input lines, with CS, A₀ and A₁ held low, and using only the \overline{WR} line to enter the data into the DAC (as shown in Figure 17). \overline{WR} is well separated from the analog lines on the ICL7134, and is usually not a very active line in 8048 systems. Additional "protection" can be achieved by gating the processor \overline{WR} line with another port line. The heavy use of port lines can be alleviated by use of the IM82C43 port expander. The same type of technique can be employed in the 8080/85 systems by using an 8255 PIA (Peripheral Interface adapter) (Figure 18) and in the MC680X and R650X systems by using an MC6820 (R6520) PIA.

Successive Approximation A/D Converters

Figure 19 shows an ICL7134B-based circuit for a bipolar input high speed A/D converter, using two AM25L03s to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2605 front-end amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7650 is probably ad-

visible (see A053). The clock, using two Schmitt trigger TTL gates, runs at a slower rate for the first 8 bits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; if fewer bits are required, it can be moved up accordingly. The circuit will free-run if the HOLD/RUN input is held low, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS output indicates when the device is operating, and the falling edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D₁₃) on an ICL7134U to pin 14 on the first AM25L03, deleting the reference inversion amplifier A₄, and tying V_{REFM} to V_{RFL}.

PC BOARD LAYOUT

Great care should be taken in the board layout to minimize ground loop and similar "hidden resistor" problems, as well as to minimize digital signal feedthrough. A suitable layout for the immediate vicinity of the ICL7134 is shown in Figure 20, and may be used as a guide.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

- A016** "Selecting A/D Converters," by Dave Fullagar.
- A017** "The Integrating A/D Converter," by Lee Evans.
- A018** "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.
- A020** "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.
- A021** "Power A/D Converters Using the ICH8510," by Dick Wilenken.
- A030** "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.
- R005** "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Most of these are available in the Intersil Data Acquisition Handbook, together with other material.

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NOTE: All typical values have been characterized but are not tested.

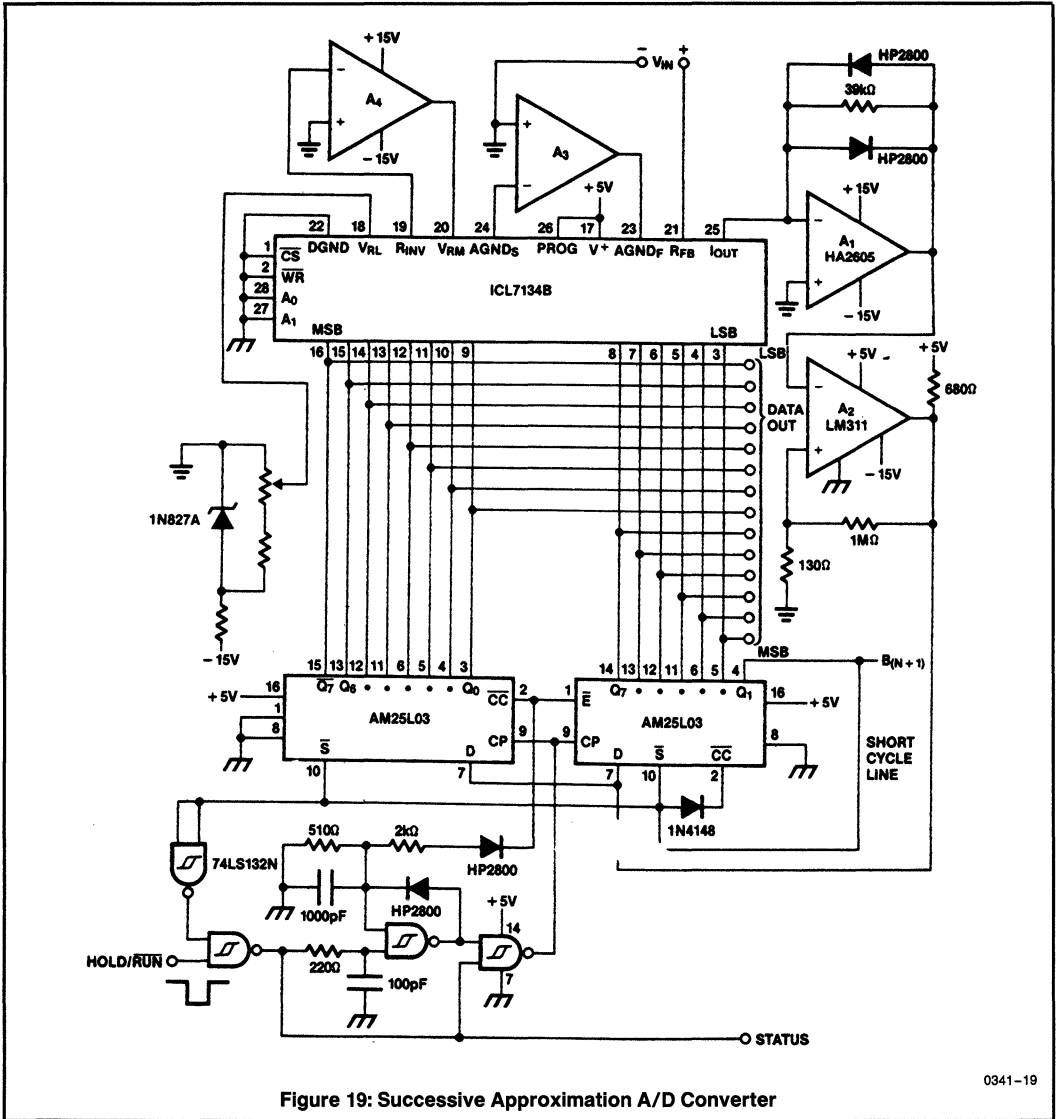
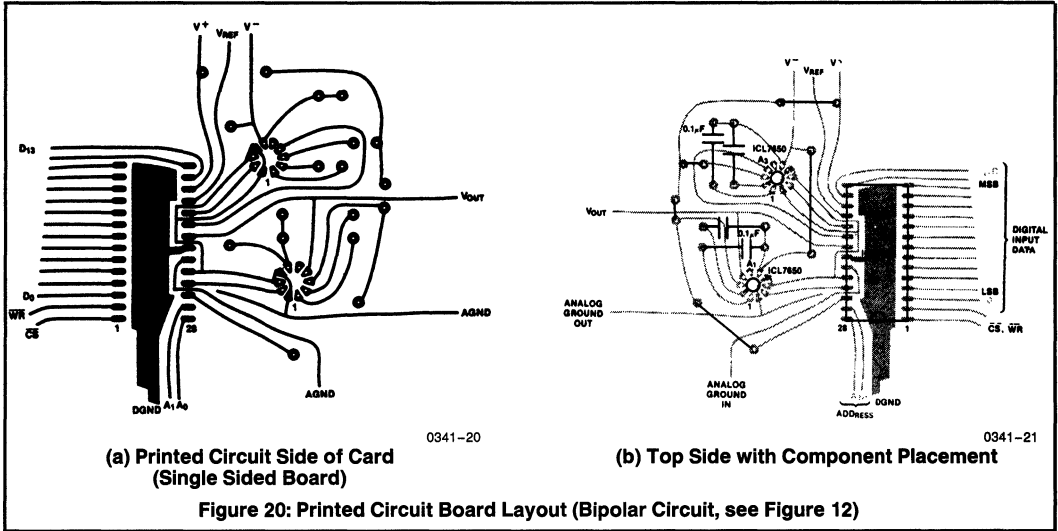


Figure 19: Successive Approximation A/D Converter

0341-19

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IM2110

256 x 12 Color Lookup Table and DAC



PRELIMINARY
Subject To Change Without Notice

GENERAL DESCRIPTION

The IM2110 is designed specifically for color graphics, and integrates a 256 x 12 color lookup table, three 4-bit DACs, and a microprocessor interface.

The color lookup table is stored in a RAM and may be written asynchronously by an 8- or 16-bit microprocessor. Three overlay registers are provided for overlaying cursors, grids, text, etc. The chip is capable of simultaneously displaying 256 out of 4096 colors at a 25 MHz rate, for a 640 x 480 non interlaced display.

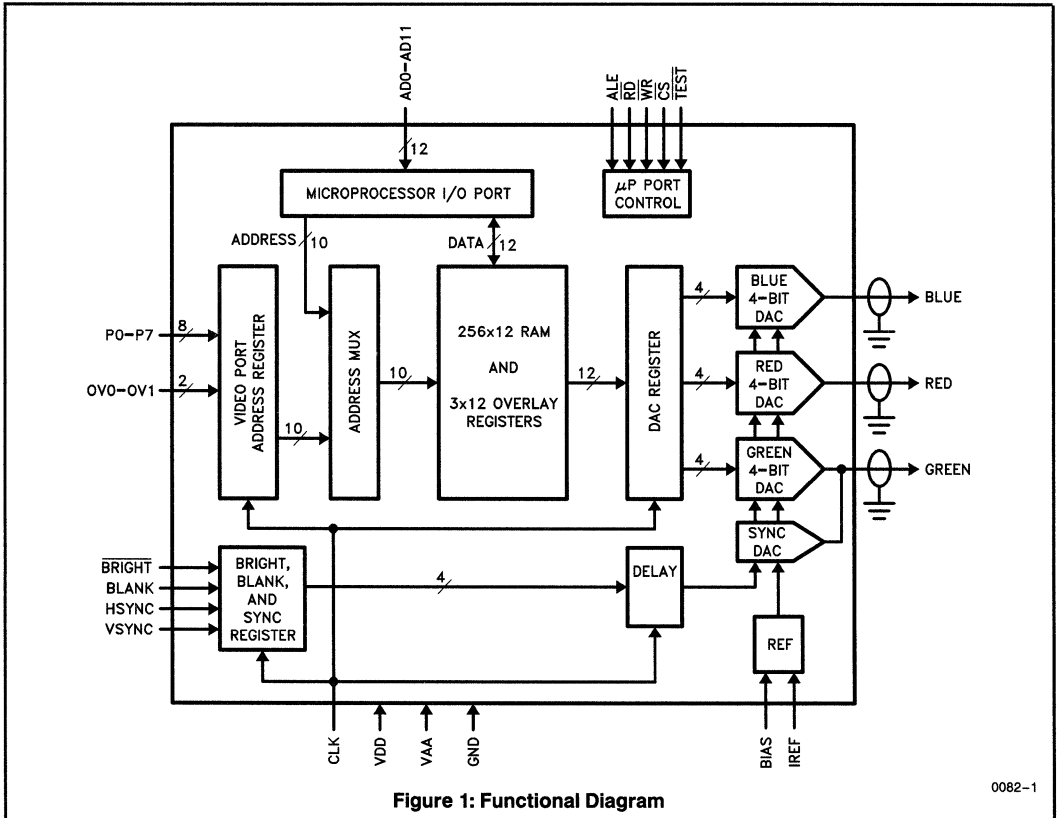
The IM2110 generates RS-343-A compatible red, green and blue analog signals, and is capable of driving doubly-terminated 75Ω coaxial cables directly.

FEATURES

- Interfaces Easily to 8- and 16-Bit Microprocessors
- Interfaces to 640 x 480 Non Interlaced Color Displays at 25 MHz
- 256 x 12 Color Palette
- 3 Overlay Registers
- Triple 4-Bit D/A Converters
- On-Chip Temperature-Compensated Reference
- DAC Inputs for Blank, Vsync, Hsync, Bright
- 40-Pin DIP/44 Pin PLCC
- PGA Compatible

ORDERING INFORMATION

Part Number	Temperature	Package
IM2110CPL	0°C to +70°C	40-Pin Plastic
IM2110CP44	0°C to +70°C	44-Pin PLCC



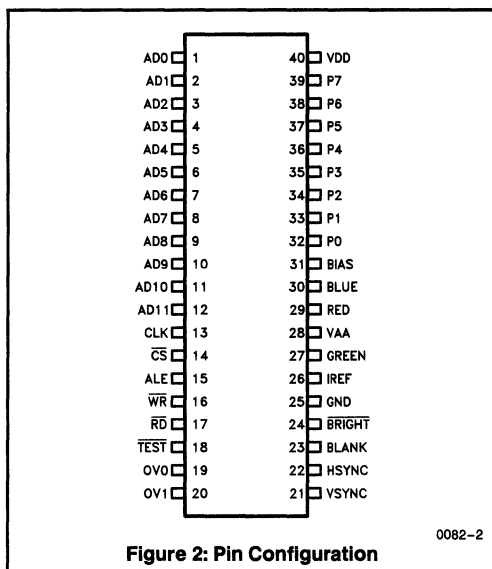
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ABSOLUTE MAXIMUM RATINGS

Supply Voltages	6.0V
V_{IH} (Input Logic "1" Voltage)	2.0V to $V_{DD} + 0.5V$
V_{IL} (Input Logic "0" Voltage)	-0.5V to 0.8V
Power Dissipation (Plastic Package)	600 mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}, V_{AA}	Positive Supply Voltage	4.5		5.5	V
T_A	Ambient Temperature	0		+70	°C
	Resistive Load on DAC Outputs		37.5		Ω
	Capacitive Load on DAC Outputs		50		pF
RSET	Full Scale Adjust Resistor		1050		Ω

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units
I_{CC}	Average Power Supply Current			150	mA
	DAC Resolution			4	Bits
	DAC Accuracy		Guaranteed		
	Integral Linearity	-1/2		+1/2	LSB
	Differential Linearity	-1/4		+1/4	LSB
	Monotonicity				
	Zero Offset	-1/8		+1/8	LSB
	Gain Error (Adjustable to Zero)	-1/2		+1/2	LSB
	Differential Accuracy (between Different Outputs on Same Device)	-1		+1	LSB
	DAC Output Characteristics				
	Full Scale Output Current (Green)		26.7		mA
	Full Scale Output Current (Red, Blue)		19.05		mA
V_O	Maximum Output Voltage		2.0		V
	REFERENCE				
I_{REF}	Reference Current (at I_{REF} Pin)	1.0		-1.2	mA
	Reference Voltage (at I_{REF} Pin)			1.4	V
	Voltage Temperature Coefficient		200		ppm/°C
	Power Supply Rejection ($V_{AA} = V_{DD} = 5V \pm 5\%$)		1.0		%VREF

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AC Test Conditions

Input Pulse Levels 0.4V to 2.4V

Input Rise & Fall Times 5 ns maximum

Input Timing Reference Level 1.5V

AC CHARACTERISTICS $V_{DD} = 5V \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Units
t_{CHCH}	Clock Period	38			ns
t_{CLCH}	Clock Width Low	10			ns
t_{CHCL}	Clock Width High	10			ns
	Clock Rise & Fall Times			5	ns
t_{AC}	Pixel Address (or OVERLAY, BLANK, SYNC, BRIGHT) Set-Up Time	10			ns
t_{CA}	Pixel Address (or OVERLAY, BLANK, SYNC, BRIGHT) Hold Time	10			ns
t_{CDA}	Clock to DAC Output (Note 1)			33	ns
	DAC Full Scale Settling Time (Note 2)		15		ns
	DAC 10–90% Rise Time (Note 3)		8		ns
	DAC Output Glitch Energy		50		pVs
t_{LL}	ALE Width	35			ns
t_{AL}	Address (and \overline{CS}) to Latch Set-Up Time	15			ns
t_{LA}	Address (and \overline{CS}) Hold Time after Latch	15			ns
t_{LW}	Latch to WRITE	–10			ns
t_{WW}	WRITE Pulse Width	80			ns
t_{AW}	Data to WRITE Set-Up Time	90			ns
t_{WA}	Data Hold Time after WRITE	0			ns
t_{WL}	WRITE to next ALE	20			ns
t_{LE}	ALE to ENABLE	25			ns
t_{EW} , t_{EE}	WRITE Duration	80			ns
t_{AR}	Address Float to READ	10			ns
t_{RR}	READ Pulse Width	130			ns
t_{RL}	READ to next ALE	30			ns
t_{RD}	Valid Data from READ			100	ns
t_{RF}	Data Valid after READ			30	ns

NOTE 1: To 0.2V on Red and Blue outputs, to 0.45V on Green output.

2: To within $\frac{1}{2}$ LSB of final value.

3: Capacitive load on DAC output of 10pF maximum.

PIN DESCRIPTION

Pin Name	Pin Number	Description
AD0–AD12	1–12	Microprocessor Address/Data. The 8 bits of RAM address and the 2 bits of overlay address are latched into the IM2110 when ALE is High. The 8-bit or 12-bit data is then written into the RAM and the overlay registers or read from them, depending on the state of \overline{WR} and \overline{RD} .
P0–P7	32–39	Pixel address. The address on these pins is latched on the first rising edge of the clock and decoded to select one of 256 colors stored in the color lookup table.

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PIN DESCRIPTION (Continued)

Pin Name	Pin Number	Description															
CLK	13	Pixel clock. Latches P0–P7, 0V0, 0V1, HSYNC, VSYNC, BLANK and $\overline{\text{BRIGHT}}$. Transfers address information from the input latches to the RAM decoder, and transfers RAM data from the DAC registers to the DAC inputs. Two clock transitions plus the DAC settling time are required from data address input to a valid output.															
$\overline{\text{CS}}$	14	Chip select for microprocessor interface (active low). $\overline{\text{CS}}$ is latched on the falling edge of ALE. When $\overline{\text{CS}}$ is low, the microprocessor port is enabled, and the DAC outputs go to the reference black level. (However, if the HYSNC, VSYNC or BLANK signals are applied, the DAC outputs are set to those respective levels).															
ALE	15	Address Latch Enable. Latches AD0–AD9 inputs into address registers when High, and the state of $\overline{\text{CS}}$ into the CS register on the falling edge. Used as the "AS" control with a Motorola microprocessor.															
$\overline{\text{WR}}$	16	Write. Logic "0" selects Write operation. Used as the "READ/WRITE" pin with a Motorola microprocessor.															
$\overline{\text{RD}}$	17	Read. Logic "0" selects Read operation onto the microprocessor bus, for manufacturer's testing purposes only. Used as the "ENABLE" or "DATA STROBE" control with a Motorola microprocessor.															
$\overline{\text{TEST}}$	18	Test. Logic "0" enables operation in test mode. Used for manufacturer's testing purposes only. This pin should always be tied to V_{DD} .															
0V0, 0V1	19, 20	<p>Overlay select. Enable and select one of the three overlay registers for Video Read. When accessing the overlay registers, P0–P7 are ignored.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>0V1</th> <th>0V0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Color Table RAM</td> </tr> <tr> <td>0</td> <td>1</td> <td>Overlay Register 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Overlay Register 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Overlay Register 3</td> </tr> </tbody> </table>	0V1	0V0		0	0	Color Table RAM	0	1	Overlay Register 1	1	0	Overlay Register 2	1	1	Overlay Register 3
0V1	0V0																
0	0	Color Table RAM															
0	1	Overlay Register 1															
1	0	Overlay Register 2															
1	1	Overlay Register 3															
VSYNC, HSYNC	21, 22	Green Vertical and Horizontal Sync. These two signals are exclusive-ORed inside the chip, to produce a composite SYNC signal. SYNC resets all DAC registers and forces all outputs to 0V. These inputs have priority over data inputs from the RAM and the overlay registers.															
BLANK	23	DAC Blanking. Logic "1" resets all DAC registers. Red and Blue outputs fall to 0V, Green output falls to 286 mV (blanking levels). This input has priority over data inputs from the RAM and the overlay registers.															
$\overline{\text{BRIGHT}}$	24	10% Bright. Logic "0" turns on an additional current source in each DAC. This produces an overbright pixel when a "White" input (all 1's) is applied to the DAC inputs.															
I_{REF}	26	Reference Current. A resistor is connected from this pin to Ground in order to set a 1 LSB current. The nominal voltage output at this pin is 1.2V, and the nominal value of the resistor should be 1050 Ω for a 37.5 Ω output termination.															
BIAS	31	Internal current source bias is provided with a temperature compensated reference. This pin is used for compensating the Bias line. 0.1 μF and 0.01 μF capacitors are normally connected in parallel from this pin to V_{AA} .															
R, G, B	29, 27, 30	Red, Green, and Blue Current Outputs. These analog outputs are intended to drive a minimum load of 37.5 Ω . If terminated with a 75 Ω resistor and a coaxial cable with 75 Ω impedance, reflection is minimized by matched termination of the cable. The full scale current needed at these outputs is adjusted with the resistor at I_{REF} .															
V_{DD}	40	Digital 5V positive supply.															
V_{AA}	28	Analog 5V positive supply, providing the high DAC output current. $V_{AA} = V_{DD}$.															
GND	25	Digital and analog ground.															

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NOTE: All typical values have been characterized but are not tested.

FUNCTIONAL DESCRIPTION

Microprocessor Interface

As illustrated in the functional diagram, the IM2110 has a 256 x 12 RAM and three 12-bit overlay registers. The MPU bus interface allows the writing of data into the RAM and the overlay registers, and operates asynchronously with the video data.

The device can be addressed either through the 12-bit microprocessor interface for writing data, or through the 8-bit video interface for transferring data to the video outputs. The microprocessor port is selected when Chip Select is active, and the video port is selected otherwise.

An 8-bit status register must be written to first, after power is applied to the part, in order to set an "8-bit" or a "12-bit" mode. Depending on the value stored at bit D0 in this register, data to the RAM and the overlay registers will be written 8 or 12 bits at a time. See Table for address mapping.

The lowest four data bits (D0-D3) contain the Red intensity information, the next four bits (D4-D7) contain the Blue intensity information, and the highest four bits (D8-D11) contain the Green intensity information.

When writing to the IM2110, the state of \overline{CS} and the address are latched on the falling edge of ALE. Data is then transferred when \overline{WR} is low.

An Intel microprocessor may be used as described above. A Motorola microprocessor may be used by taking into account the following pin correspondence (see timing diagrams, Figure 3 and Figure 4):

Intel	Motorola
ALE	AS
\overline{RD}	E or DS
\overline{WR}	R/W

While the microprocessor port is selected, all the DAC outputs are set to the reference 'Black' level, unless the 'BLANK', 'VSYNC' or 'HSYNC' signals are applied.

The content of the RAM (but not of the overlay registers) can be read back onto the AD bus, 12 bits at a time. This feature is used primarily for testing the part. The timing diagram and the specifications for this Read function are supplied for information purposes only. Note that in this mode the video clock must be operating at a frequency at least double that of ALE. (See Figure 5.)

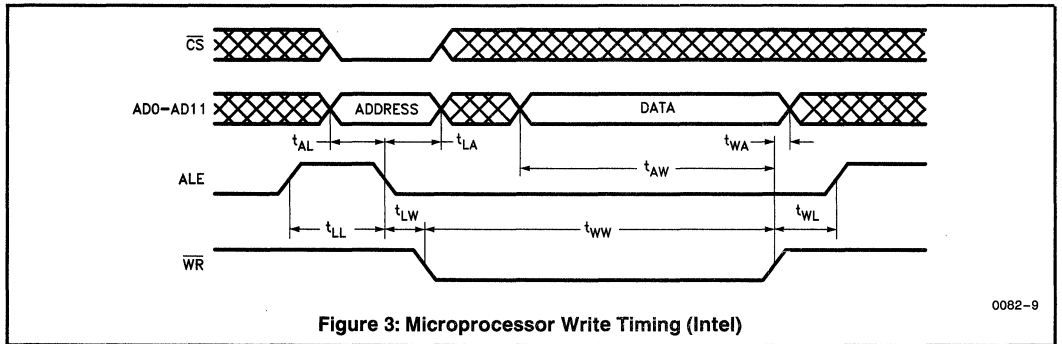


Figure 3: Microprocessor Write Timing (Intel)

0082-9

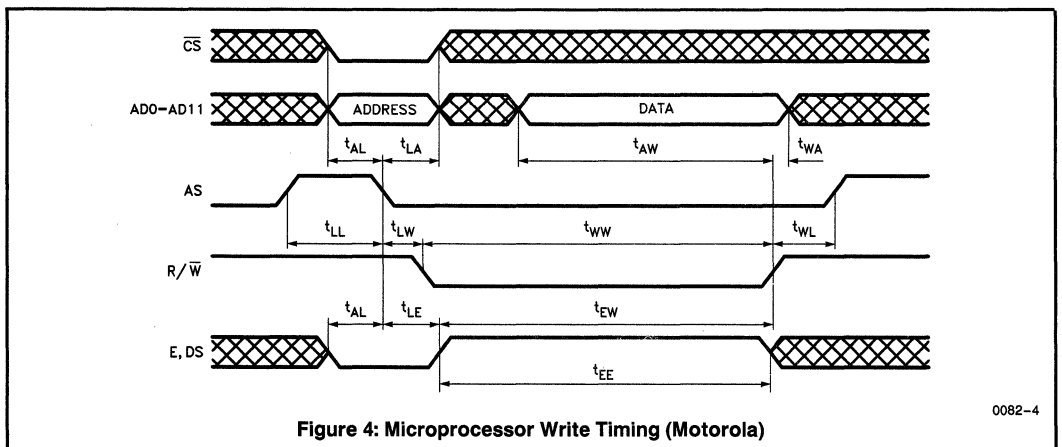


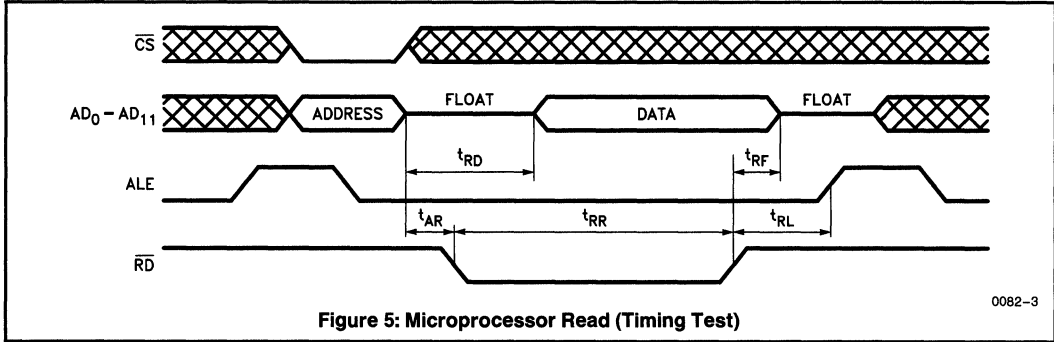
Figure 4: Microprocessor Write Timing (Motorola)

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NOTE: All typical values have been characterized but are not tested.

FUNCTIONAL DESCRIPTION (Continued)



ADDRESS MAP

Table 1

Address (AD ₀ -AD ₉)	12-Bit Mode		8-Bit Mode	
	Location	Data	Location	Data
000h	ram 0	D0-D11	ram 0	D0-D7
001h	ram 1	D0-D11	ram 1	D0-D7
002h	ram 2	D0-D11	ram 2	D0-D7
003h	ram 3	D0-D11	ram 3	D0-D7
•	•	•	•	•
•	•	•	•	•
0FEh	ram 254	D0-D11	ram 254	D0-D7
0FFh	ram 255	D0-D11	ram 255	D0-D7
100h	ram 0	D0-D11	ram 0	D8-D11
101h	ram 1	D0-D11	ram 1	D8-D11
•	•	•	•	•
•	•	•	•	•
1FEh	ram 254	D0-D11	ram 254	D8-D11
1FFh	ram 255	D0-D11	ram 255	D8-D11
201h	ovly 1	D0-D11	ovly 1	D0-D7
202h	ovly 2	D0-D11	ovly 2	D0-D7
203h	ovly 3	D0-D11	ovly 3	D0-D7
301h	ovly 1	D0-D11	ovly 1	D8-D11
302h	ovly 2	D0-D11	ovly 2	D8-D11
303h	ovly 3	D0-D11	ovly 3	D8-D11
3FFh	status register	D0-D7	status register	D0-D7
other locations	unused		unused	

4

Status register: D0 = 1: 12 bit mode. D0 = 0: 8 bit mode. All other bits unused. When an address is loaded, the levels on AD₁₀-AD₁₁ are indifferent. In the 8-bit mode, the data for D₀-D₇ must be present on AD₀-AD₇, and the data for D₈-D₁₁ on AD₀-AD₃. The levels on the other AD pins are indifferent.

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FUNCTIONAL DESCRIPTION (Continued)

Color Lookup Table

As illustrated in Figure 6, 8 bits of lookup table address and 2 bits of overlay address are latched into the address registers on the rising edge of the clock. On the following rising edge, the 12 bits of color information are latched into the DAC registers, decoded, and used to turn on or off the DAC current sources. If OV0 or OV1 is High, the information in the overlay registers overrides the pixel data on P0–P7. The overlay registers allow the use of additional bit planes in the frame buffers and may be controlled by external character, cursor or grid logic.

Bright, Blank, Sync

These inputs are also sampled on the rising edge of the clock, and internally pipelined to maintain synchronization with the data (see Table 3).

When BRIGHT is active, the intensity of the color addressed in the RAM or the overlay registers is increased by a value of 10% of the Reference White level.

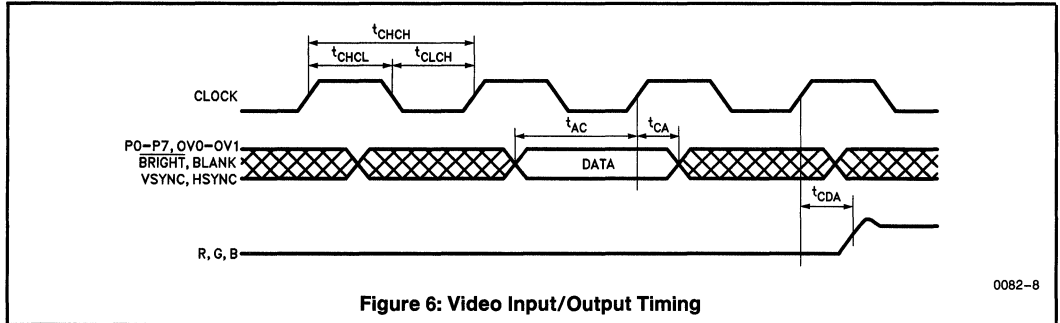


Figure 6: Video Input/Output Timing

0082-8

Table 2

	Green		Red, Blue	
	(mV)	(mA)	(mV)	(mA)
Peak White	1071	28.56	785	20.93
Reference White	1000	26.67	714	19.04
Reference Black	357	9.52	71	1.89
Blanking	286	7.62	0	0
Sync	0	0	0	0

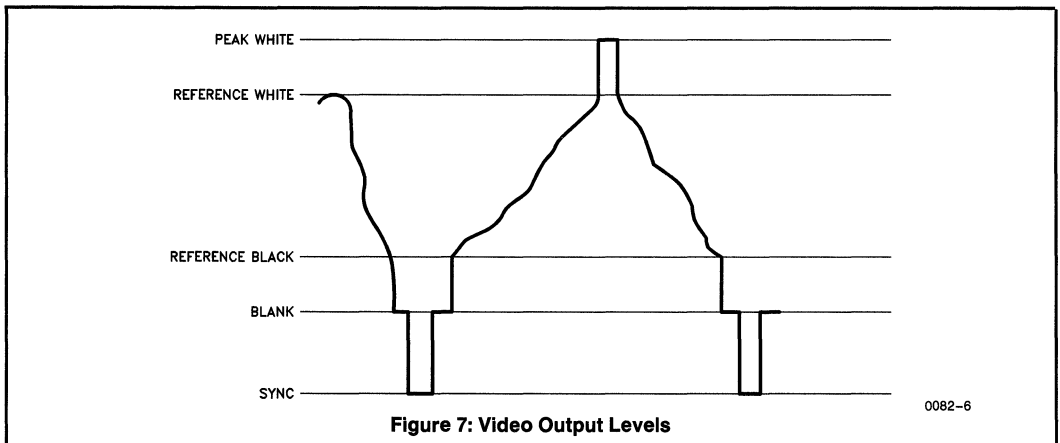


Figure 7: Video Output Levels

0082-6

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TRUTH TABLE

Table 3. Voltage and Current Output with Standard Setup
(adjusted for Green Reference White level = 1000 mV, 37.5Ω load on outputs)

BRIGHT	BLANK	HSYNC	VSYNC	OV0	OV1	P0-P7	Data	Level
0	0	0	0	0	0	addr	255	peak white
1	0	0	0	0	0	addr	255	ref white
						•	•	•
						•	•	•
						•	•	•
1	0	0	0	0	0	addr	0	ref black
1	0	0	0	1	0	X	(ovly1)	
1	0	0	0	0	1	X	(ovly2)	
1	0	0	0	1	1	X	(ovly3)	
X	1	0	0	X	X	X	X	blank
X	X	1	1	X	X	X	X	blank
X	X	0	1	X	X	X	X	sync
X	X	1	0	X	X	X	X	sync

Voltage Reference

The internal band gap reference provides a temperature compensated voltage bias to all three DAC's. Full scale output current is set by using the reference and an external resistor. The reference voltage at I_{REF} divided by the resistance from I_{REF} to GND is equal to a nominal one LSB of DAC current. An R_{SET} resistor consisting of a 500Ω fixed resistor in series with a 1 kΩ variable resistor should be used to adjust the full scale output voltage for a doubly-terminated 75Ω system. This adjustment eliminates any gain error and its range is wide enough to guarantee 1V peak-to-peak Green output (Sync tip to Reference White level). Selection of R_{SET} for RS343A output is made by using the equation:

$$R_{SET} = \frac{V_{ref} \times R(\text{load})}{42.86 \text{ mV}} \quad (42.86 \text{ mV} = 1 \text{ LSB})$$

With a nominal 1.2V reference voltage, R_{SET} will be 1050Ω for a 37.5Ω (doubly terminated) system and 2100Ω for a 75Ω system. Matching the temperature coefficients of R_{SET} and the load resistors will provide a system with an output voltage temperature coefficient of typically 200 ppm/°C.

The internal voltage generated for current source bias is present at the BIAS pin. 0.1 μF and 0.01 μF capacitors are connected in parallel from BIAS to VAA.

D/A CONVERTERS

Each DAC consists of 15 equal-weight current sources providing the gray scale output. This configuration guarantees monotonicity, reduces glitch energy, and ensures high integral and differential linearity. In addition, SETUP and BRIGHT current sources are included for RS343A output and cursor display options. The Green DAC has an additional SYNC current source, for RS343A compatibility.

The 12 bits of color information, in combination with the SYNC, BLANK or BRIGHT selected at the time of address input, are used to form the composite output current. This current, through output loads from 37.5Ω to 75Ω, provides the 1 Vp-p RS343A output voltage.

An on-chip temperature-compensated reference and external resistor set the full scale output current of all three DAC's. A current of one LSB (1.143 mA for 37.5Ω output load) is sourced from IREF. Varying R_{SET} adjusts the full scale output and LSB weight.

Reference Adjustment Procedure

A Reference White must be present at the DAC outputs. The R_{SET} resistor at IREF can then be adjusted to precisely set this output voltage. The following procedure may be used:

- 1) Write all 1's to Overlay register 1. The video clock need not be active.
- 2) Transfer the data into the DAC registers by moving the video clock from Low to High at least twice, while maintaining the following levels on the video input pins:

P0-P7	X
OV0	1
OV1	0
<u>BRIGHT</u>	1
BLANK	0
VSYNC	0
HSYNC	0
- 3) Measure the voltage at the Green output, and adjust the resistor value at IREF until that voltage is 1.000V.

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NOTE: All typical values have been characterized but are not tested.

PC BOARD LAYOUT CONSIDERATIONS

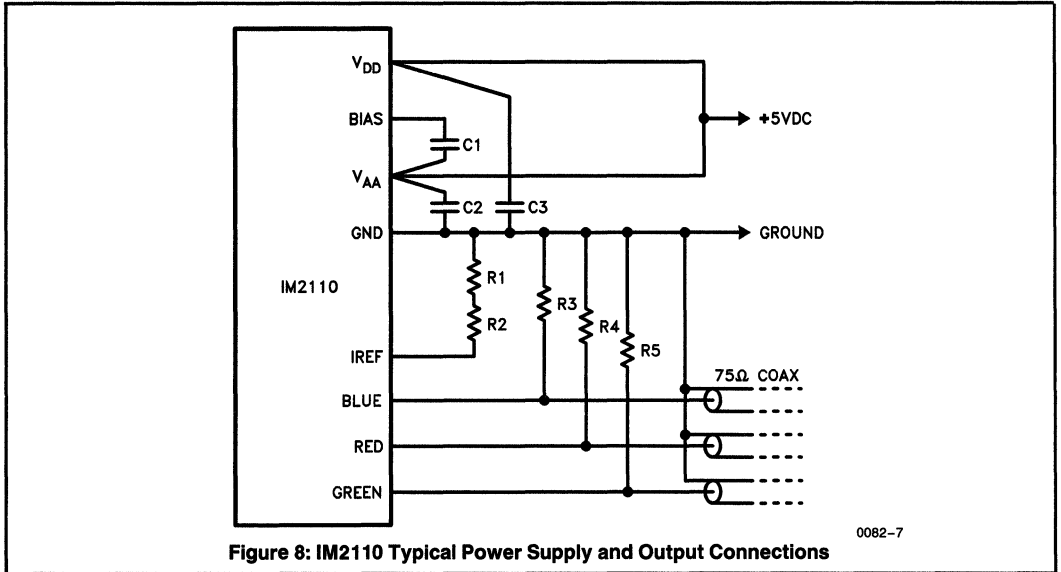


Figure 8: IM2110 Typical Power Supply and Output Connections

R1: 500Ω metal film resistor

R2: 1 kΩ cermet potentiometer

C1, C2, C3: 0.1 μF and 0.01 μF monolithic ceramic capacitors in parallel

R3, R4, R5: 75Ω 1% metal film resistor

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NOTE: All typical values have been characterized but are not tested.

Section 5 — Power Supply Supervisory

ICL7660	5-1
ICL7660S	5-10
ICL7662	5-20
ICL7663	5-28
ICL7663S	5-37
ICL7665	5-44
ICL7665S	5-53
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ICL7673	5-71
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ICL7660

CMOS Voltage Converter



ICL7660

GENERAL DESCRIPTION

The Intersil ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of -1.5V to -10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input. Note that an additional diode is required for $V_{SUPPLY} > 6.5V$.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

An enhanced direct replacement for this part called ICL7660S will become available shortly and will be more appropriate for new designs.

FEATURES

- Simple Conversion of +5V Logic Supply to $\pm 5V$ Supplies
- Simple Voltage Multiplication ($V_{OUT} = (-) nV_{IN}$)
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 98% Typical Power Efficiency
- Wide Operating Voltage Range 1.5V to 10.0V
- Easy to Use — Requires Only 2 External Non-Critical Passive Components

APPLICATIONS

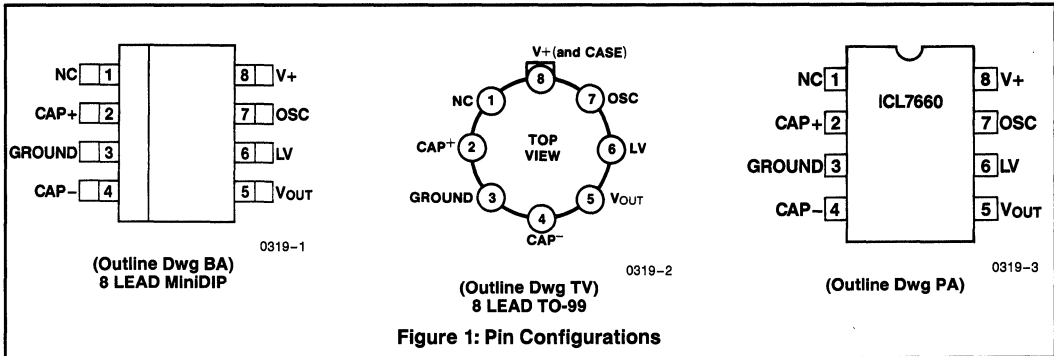
- On Board Negative Supply for Dynamic RAMs
- Localized μ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7660CTV	0° to +70°C	TO-99
ICL7660CBA	0°C to +70°C	8 PIN SOIC
ICL7660CPA	0° to +70°C	8 PIN MINI DIP
ICL7660MTV*	-55° to +125°C	TO-99

*Add /883B to part number if 883B processing is required.

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	10.5V
LV and OSC Input Voltage (Note 1)	-0.3V to (V \pm +0.3V) for V \pm < 5.5V (V \pm -5.5V) to (V \pm +0.3V) for V \pm > 5.5V
Current into LV (Note 1)	20 μ A for V \pm > 3.5V
Output Short Duration (V _{SUPPLY} \leq 5.5V)	Continuous
Power Dissipation (Note 2)	
ICL7660CTV	500mW
ICL7660CPA	300mW
ICL7660MTV	500mW

Operating Temperature Range

ICL7660M	-55°C to +125°C
ICL7660C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

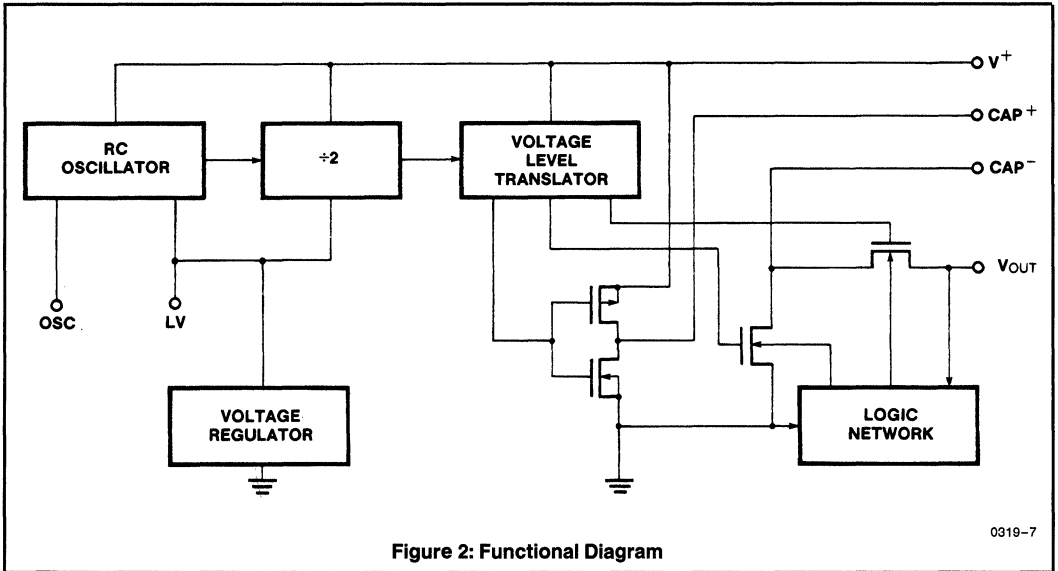


Figure 2: Functional Diagram

0319-7

OPERATING CHARACTERISTICS

V \pm = 5V, T_A = 25°C, C_{OSC} = 0, Test Circuit Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I \pm	Supply Current	R _L = ∞		170	500	μ A
V \pm _{H1}	Supply Voltage Range - Hi (D _X out of circuit) (Note 3)	0°C \leq T _A \leq 70°C, R _L = 10k Ω , LV Open -55°C \leq T _A \leq 125°C, R _L = 10k Ω , LV Open	3.0		6.5 5.0	V V
V \pm _{L1}	Supply Voltage Range - Lo (D _X out of circuit)	MIN \leq T _A \leq MAX, R _L = 10k Ω , LV to GROUND	1.5		3.5	V
V \pm _{H2}	Supply Voltage Range - Hi (D _X in circuit)	MIN \leq T _A \leq MAX, R _L = 10k Ω , LV Open	3.0		10.0	V
V \pm _{L2}	Supply Voltage Range - Lo (D _X in circuit)	MIN \leq T _A \leq MAX, R _L = 10k Ω , LV to GROUND	1.5		3.5	V

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NOTE: All typical values have been characterized but are not tested.

OPERATING CHARACTERISTICS

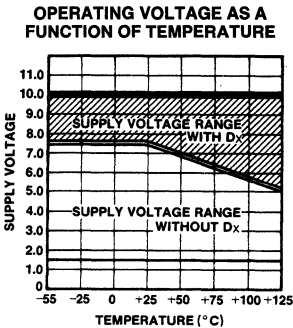
V+ = 5V, TA = 25°C, COSC = 0, Test Circuit Figure 3 (unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
ROUT	Output Source Resistance	IOUT = 20mA, TA = 25°C		55	100	Ω
		IOUT = 20mA, 0°C ≤ TA ≤ +70°C			120	Ω
		IOUT = 20mA, -55°C ≤ TA ≤ +125°C (Note 3)			150	Ω
		V+ = 2V, IOUT = 3mA, LV to GROUND 0°C ≤ TA ≤ +70°C			300	Ω
		V+ = 2V, IOUT = 3mA, LV to GROUND, -55°C ≤ TA ≤ +125°C, DX in circuit (Note 3)			400	Ω
fOSC	Oscillator Frequency		10		kHz	
PEf	Power Efficiency	RL = 5kΩ	95	98		%
VOUEf	Voltage Conversion Efficiency	RL = ∞	97	99.9		%
ZOSC	Oscillator Impedance	V+ = 2 Volts		1.0		MΩ
		V = 5 Volts		100		kΩ

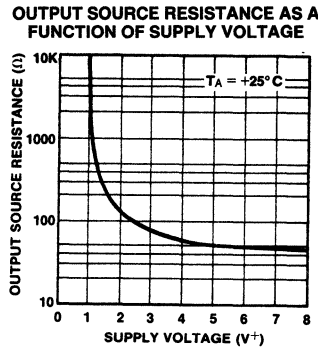
- Notes: 1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.
 2. Derate linearly above 50°C by 5.5mW/°C.
 3. ICL7660M only.

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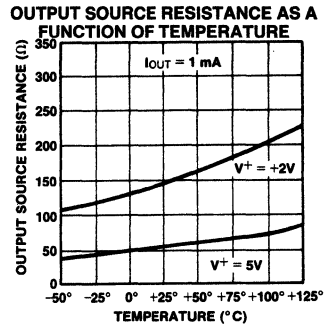
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)



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0319-9



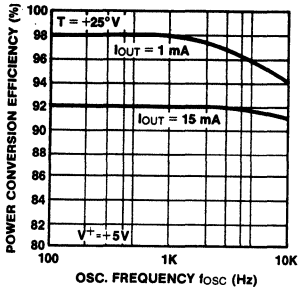
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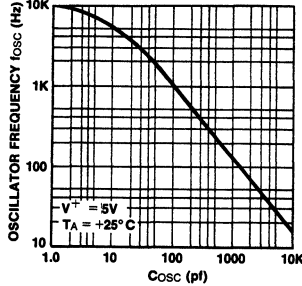
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



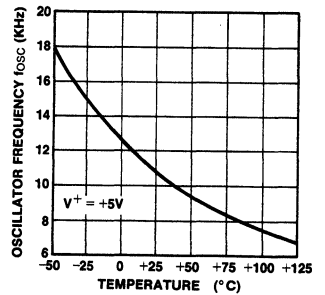
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FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



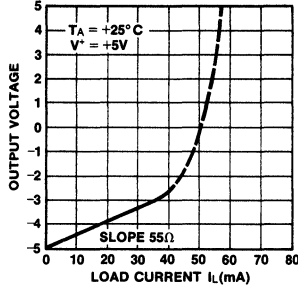
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UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



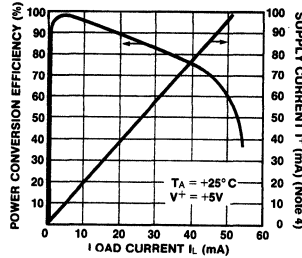
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OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



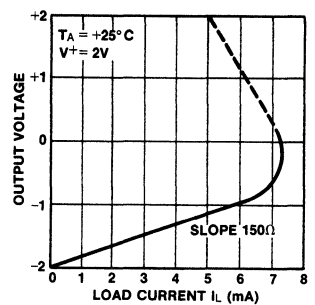
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SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



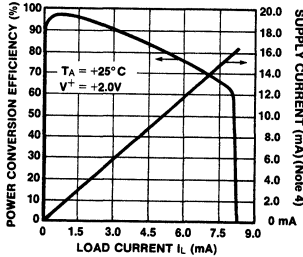
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OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



0319-16

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

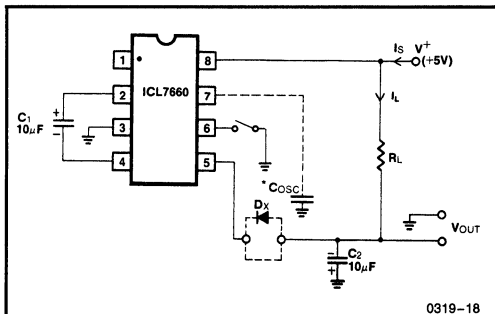


0319-17

NOTE 4. These curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \approx 2 V_{IN}$, $I_S \approx 2 I_L$, so $V_{IN} \cdot I_S \approx V_{OUT} \cdot I_L$.

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NOTE: All typical values have been characterized but are not tested.



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- NOTES:**
- For large values of C_{OSC} ($> 1000\mu F$) the values of C_1 and C_2 should be increased to $100\mu F$.
 - D_X is required for supply voltages greater than 6.5V @ $-55^\circ C \leq T_A \leq +70^\circ C$; refer to performance curves for additional information.

Figure 3: ICL7660 Test Circuit

DETAILED DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive $10\mu F$ polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+ , for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+ , assuming ideal switches and no load on C_2 . The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

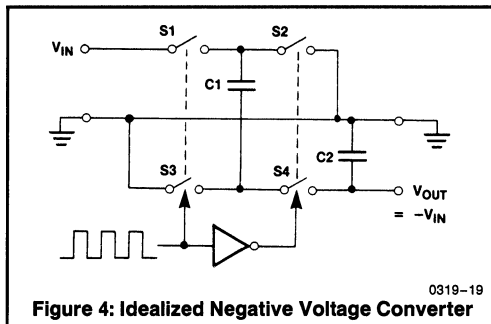
In the ICL7660, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

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NOTE: All typical values have been characterized but are not tested.



0319-19

Figure 4: Idealized Negative Voltage Converter

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

- The drive circuitry consumes minimal power.
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

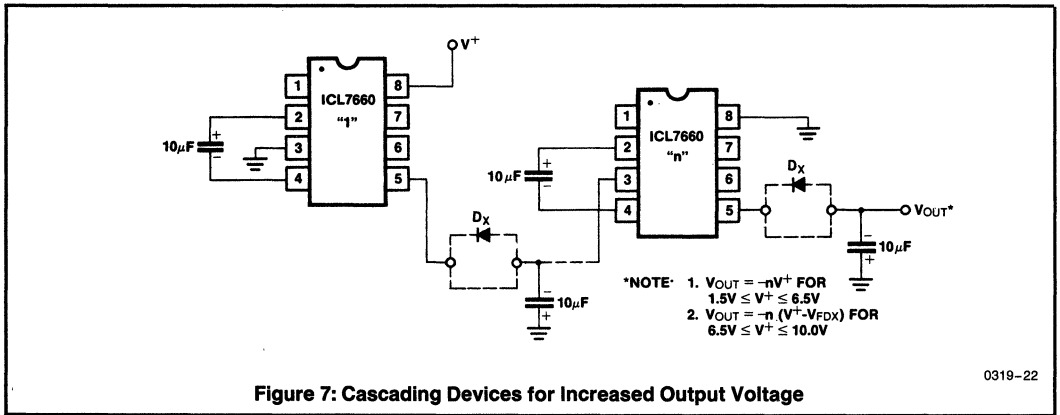
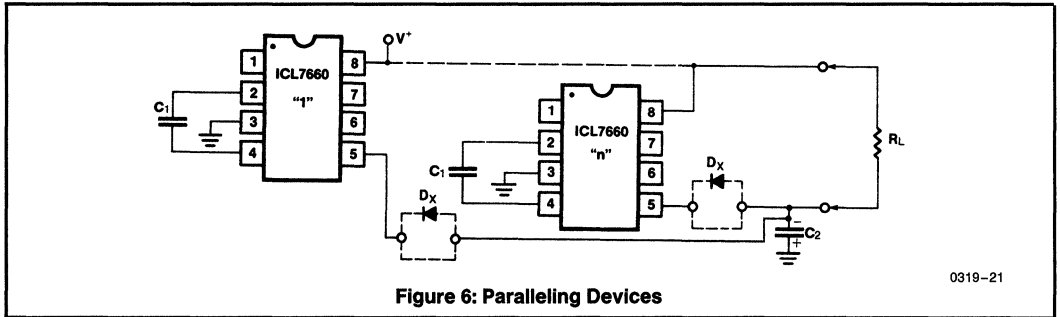
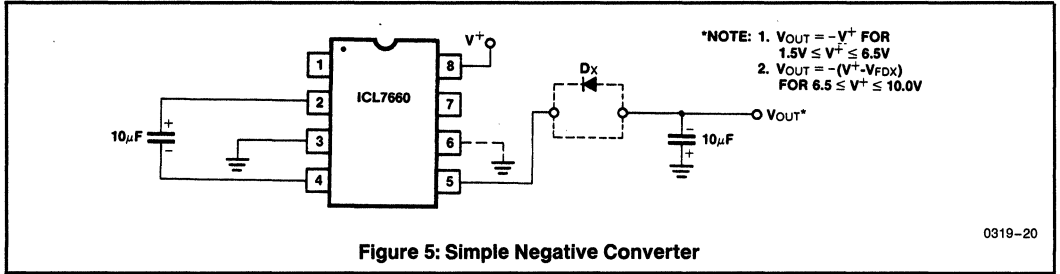
$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L , there will be a substantial difference in the voltages V_1 and V_2 . Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
- Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
- When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
- Add diode D_X as shown in Figure 3 for high-voltage, elevated temperature applications.
- Add capacitor ($\sim 0.1\mu F$, disc) from pin 8 to ground to limit rate of rise of input voltage to approximately $2V/\mu s$.

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NOTE: All typical values have been characterized but are not tested.

CONSIDERATIONS FOR HIGH VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (storage & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latchup of the ICL7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latchup can be achieved by adding a general purpose diode in series with the ICL7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +10.0 volts is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 55 ohms. Thus for a load current of -10mA and a supply voltage of +5 volts, the output voltage will be -4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$, where:

$$C = C_1 = C_2$$

$$\text{which gives } \frac{1}{\omega C} = \frac{1}{2\pi f_{PUMP} \times 10^{-5}} \approx 3 \text{ ohms}$$

for $C = 10\mu\text{F}$ and $f_{PUMP} = 5\text{kHz}$ ($1/2$ of oscillator frequency)

Paralleling Devices

Any number of ICL7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C₂, serves all devices while each device requires its own pump capacitor, C₁. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent possible device latchup, a 100kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V⁺ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be $1/2$ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

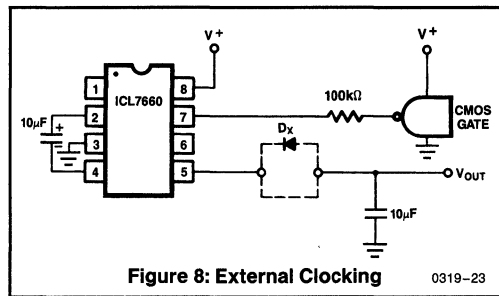


Figure 8: External Clocking

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It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C₁) and reservoir (C₂) capacitors; this is overcome by increasing the values of C₁ and C₂ by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V⁺ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C₁ and C₂ (from 10µF to 100µF).

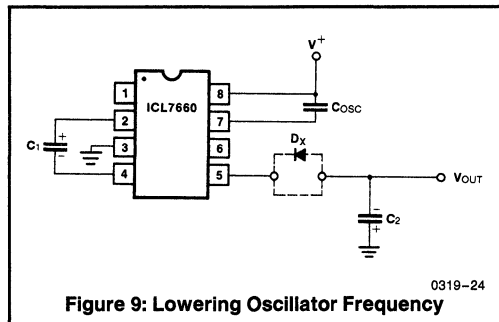


Figure 9: Lowering Oscillator Frequency

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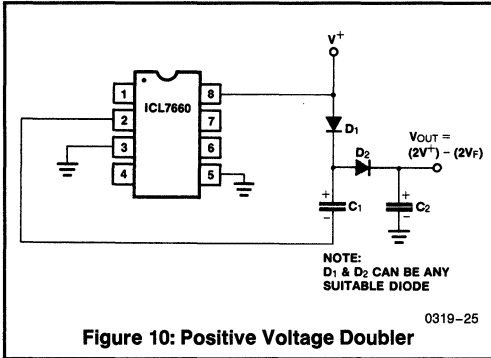


Figure 10: Positive Voltage Doubler

Positive Voltage Doubling

The ICL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 10. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2 . The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2 .

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

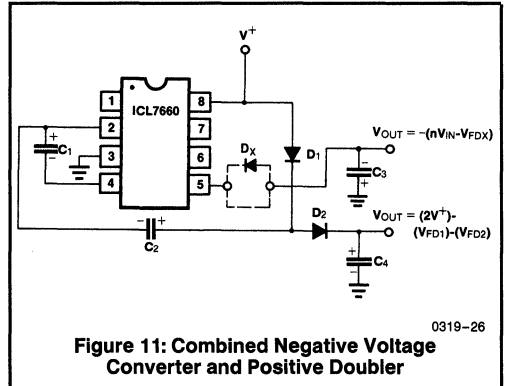


Figure 11: Combined Negative Voltage Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance ($\sim 250\Omega$).

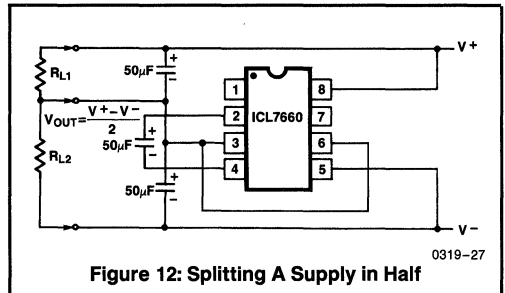


Figure 12: Splitting A Supply in Half

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NOTE: All typical values have been characterized but are not tested.

ICL7660S Super Voltage Converter



GENERAL DESCRIPTION

The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry-standard ICL7660 offering an **extended** operating supply voltage range up to 12V, **lower** supply current, and **ESD protection** exceeding 2000 volts. **No external diode** is needed for the ICL7660S. In addition, a **Frequency Boost pin** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in **bold italics** in the Electrical Characteristics section. **Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.**

The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of -1.5V to -12V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

FEATURES

- **Guaranteed Lower Max Supply Current for All Temperature Ranges**
- **Guaranteed Wider Operating Voltage Range** —1.5V to 12V
- **No External Diode Over Full Temperature and Voltage Range**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- **Guaranteed Minimum Power Efficiency of 96%**
- **Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%**
- **Enhanced ESD Protection > 2000V**
- **Improved SCR Latchup Protection**
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$**
- **Easy to Use—Requires Only 2 External Non-Critical Passive Components**
- **Improved Direct Replacement for Industry-Standard ICL7660 and Other Second-Source Devices**

APPLICATIONS

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems & Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter, $V_{OUT} = \pm V_S/2$**

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7660SCBA	0°C to +70°C	8-Pin SOIC
ICL7660SCPA	0°C to +70°C	8-Pin Minidip
ICL7660SIBA	0°C to +70°C	8-Pin SOIC
ICL7660SCTV	0°C to +70°C	TO-99
ICL7660SIPA	-25°C to +85°C	8-Pin Minidip
ICL7660SITV	-25°C to +85°C	TO-99
ICL7660SMTV*	-55°C to +125°C	TO-99

*Add /883B to part number if 883B processing is required.

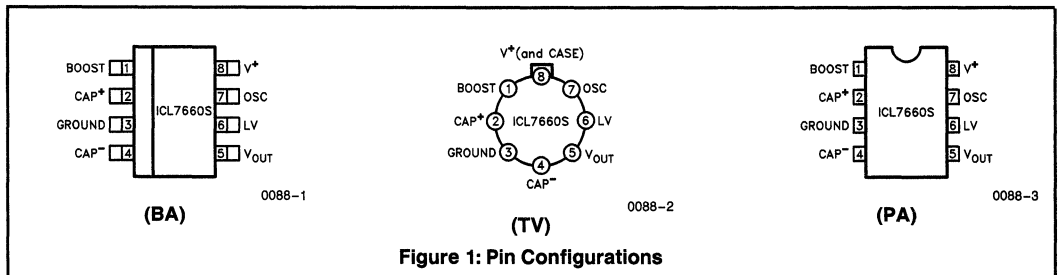


Figure 1: Pin Configurations

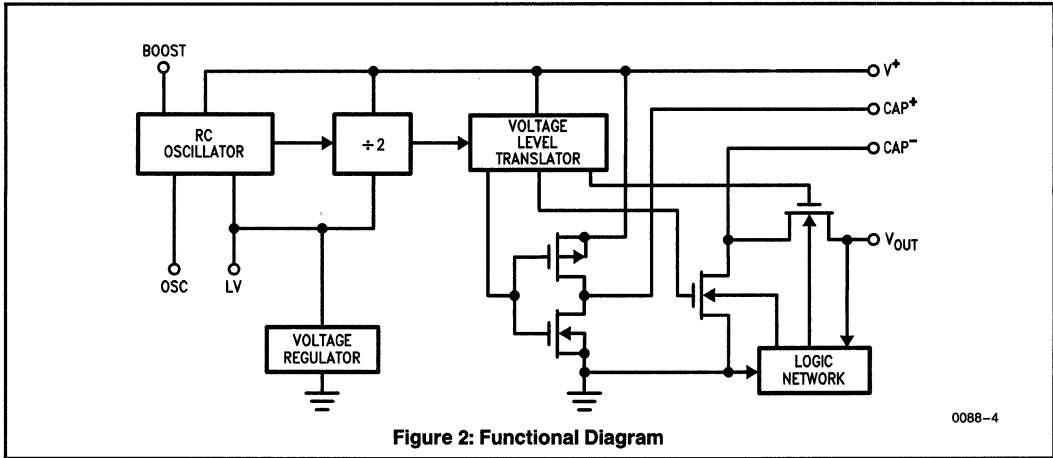
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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.0V
LV and OSC Input Voltage	
(Note 1)	-0.3V to (V ⁺ + 0.3V) for V ⁺ < 5.5V
	(V ⁺ - 5.5V) to (V ⁺ + 0.3V) for V ⁺ > 5.5V
Current into LV (Note 1)	.20 μA for V ⁺ > 3.5V
Output Short Duration (V _{SUPPLY} ≤ 5.5V)	Continuous
Power Dissipation (Note 2)	
ICL7660SCTV	500 mW
ICL7660SCPA	300 mW
ICL7660SCBA	300 mW
ICL7660SITV	500 mW
ICL7660SIPA	300 mW
ICL7660SIBA	300 mW
ICL7660SMTV	500 mW
Operating Temperature Range	
ICL7660SM	-55°C to +125°C
ICL7660SI	-25°C to +85°C
ICL7660SC	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
(Soldering, 10 sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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ELECTRICAL CHARACTERISTICS

V⁺ = 5V, T_A = 25°C, OSC = Free running, Test Circuit Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
<i>I</i> ⁺	<i>Supply Current</i> (Note 3)	R _L = ∞, 25°C 0°C < T _A < +70°C -25°C < T _A < +85°C -55°C < T _A < +125°C		80	160 180 180 200	μA
<i>V</i> _H ⁺	<i>Supply Voltage Range—Hi</i> (Note 4)	R _L = 10k, LV Open T _{min} < T _A < T _{max}	3.0		12	V
<i>V</i> _L ⁺	<i>Supply Voltage Range—Lo</i>	R _L = 10k, LV to GROUND T _{min} < T _A < T _{max}	1.5		3.5	V
<i>R</i> _{OUT}	<i>Output Source Resistance</i>	<i>I</i> _{OUT} = 20 mA, T _A = 25°C		60	100	Ω
		<i>I</i> _{OUT} = 20 mA, 0°C < T _A < +70°C			120	
		<i>I</i> _{OUT} = 20 mA, -25°C < T _A < +85°C			120	
		<i>I</i> _{OUT} = 20 mA, -55°C < T _A < +125°C			150	
		<i>I</i> _{OUT} = 3 mA, V ⁺ = 2V, LV = GND, 0°C < T _A < +70°C			250	
		<i>I</i> _{OUT} = 3 mA, V ⁺ = 2V, LV = GND, -25°C < T _A < +85°C			300	
		<i>I</i> _{OUT} = 3 mA, V ⁺ = 2V, LV = GND, -55°C < T _A < +125°C			400	
<i>f</i> _{OSC}	<i>Oscillator Frequency</i>	C _{OSC} = 0, Pin 1 Open or GND Pin 1 = V ⁺	5	10 35		kHz
<i>PEff</i>	<i>Power Efficiency</i>	R _L = 5 kΩ T _{min} < T _A < T _{max}	96 95	98 97		%
<i>V</i> _{OUT} <i>Eff</i>	<i>Voltage Conversion Efficiency</i>	R _L = ∞	99	99.9		%
Z _{OSC}	Oscillator Impedance	V ⁺ = 2V		1		MΩ
		V ⁺ = 5V		100		kΩ

NOTE 1: Connecting any terminal to voltages greater than V⁺ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660s.

2: Derate linearly above 50°C by 5.5 mW/°C.

3: In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5 pF.

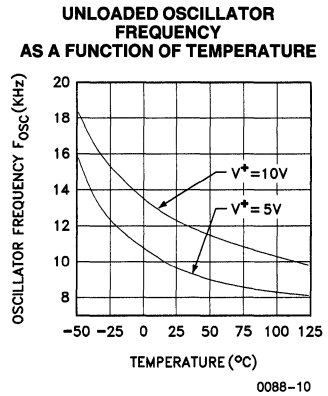
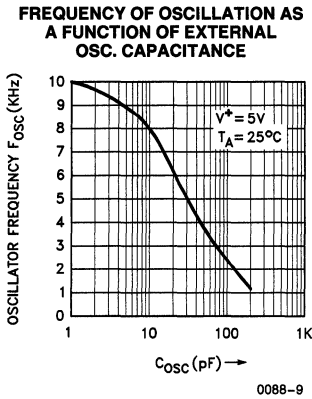
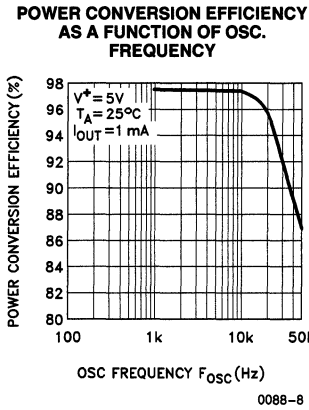
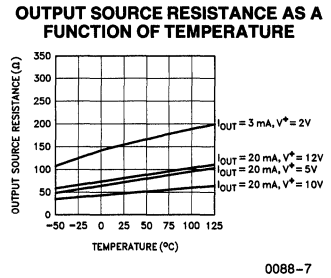
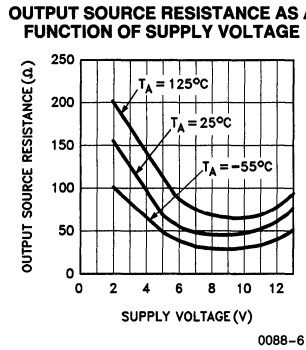
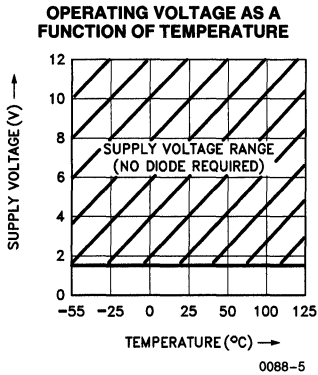
4: The Intersil ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

5: All significant improvements over the industry-standard ICL7660 are highlighted in **bold italics**.

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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)



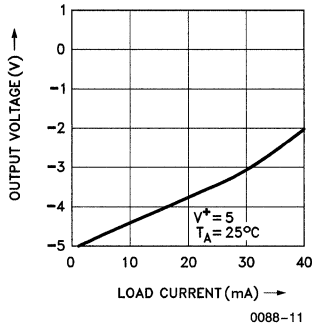
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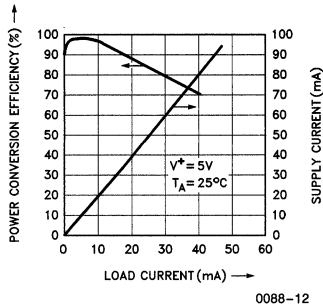
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

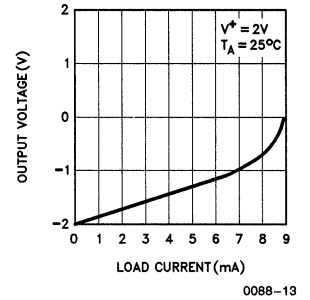
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



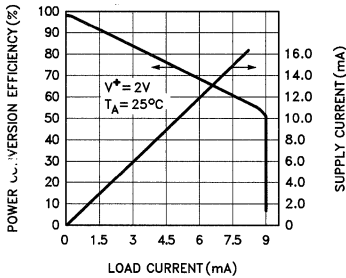
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



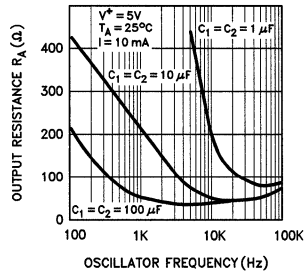
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



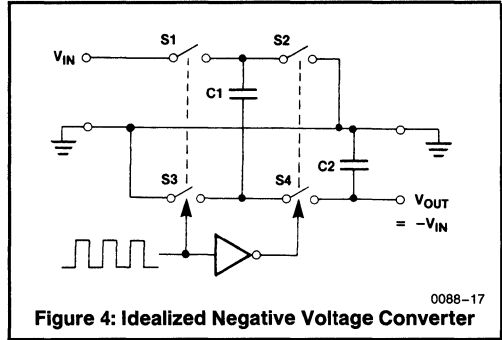
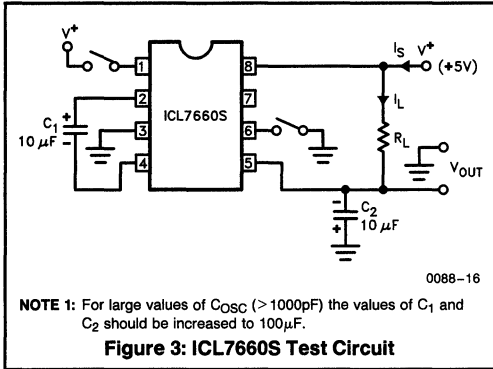
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



NOTE 4: These curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660S, to the negative side of the load. Ideally, $V_{OUT} \cong 2 V_{IN}$, $I_S \cong 2 I_L$, so $V_{IN} \cdot I_S \cong V_{OUT} \cdot I_L$.

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DETAILED DESCRIPTION

The ICL7660S contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive $10\mu F$ polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+ , for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+ , assuming ideal switches and no load on C_2 . The ICL7660S approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660S, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

- A The drive circuitry consumes minimal power.
- B The output switches have extremely low ON resistance and virtually no offset.
- C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2)$$

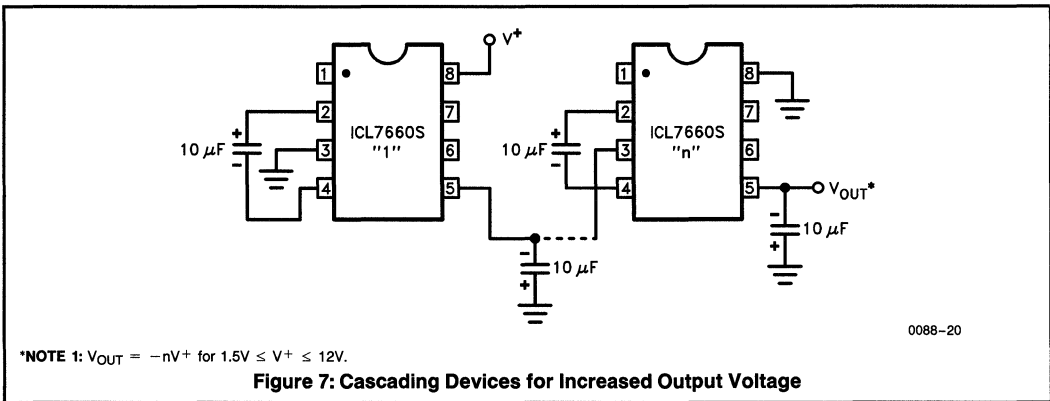
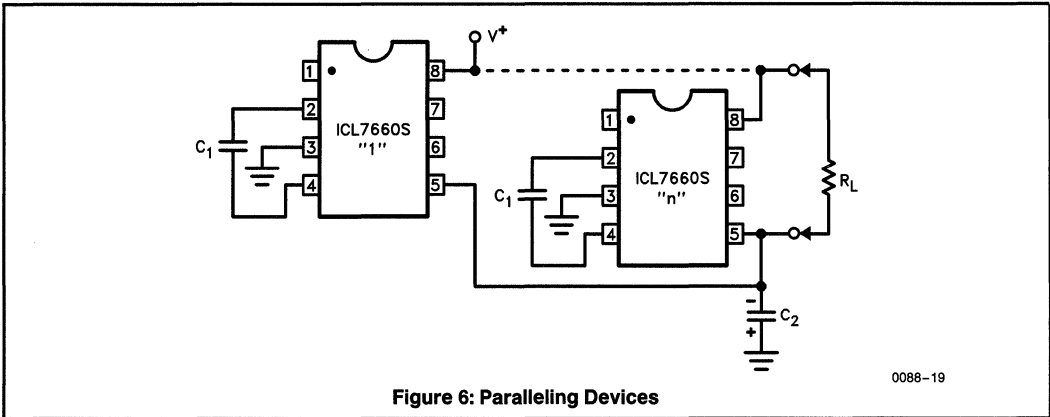
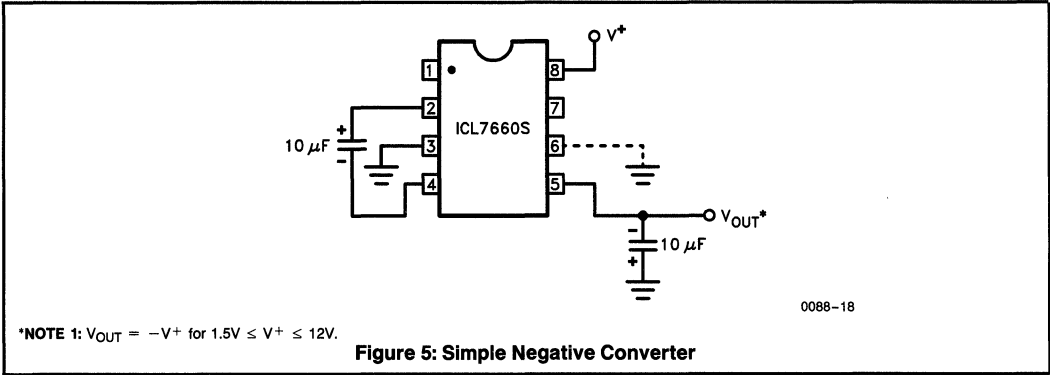
where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L , there will be a substantial difference in the voltages V_1 and V_2 . Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660S and the + terminal of C_2 must be connected to GROUND.

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TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 55 ohms. Thus for a load current of -10mA and a supply voltage of +5 volts, the output voltage will be -4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$, where:

$$C = C_1 = C_2$$

$$\text{which gives } \frac{1}{\omega C} = \frac{1}{2\pi f_{PUMP} \times 10^{-5}} \approx 3 \text{ ohms}$$

for $C = 10\mu\text{F}$ and $f_{PUMP} = 5\text{kHz}$ ($1/2$ of oscillator frequency)

Paralleling Devices

Any number of ICL7660S voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2 , serves all devices while each device requires its own pump capacitor, C_1 . The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660S)}}{n \text{ (number of devices)}}$$

Cascading Devices

The ICL7660S may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n (V_{IN}).$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S R_{OUT} values.

Changing the ICL7660S Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods described below.

By connecting the Boost Pin (Pin 1) to V^+ , the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately $3\frac{1}{2}$ times. The result is a decrease in the output impedance and ripple. This is of major importance for surface-mount applications where capacitor size and cost are critical. Smaller capacitors, e.g. $0.1\mu\text{F}$, can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 10\mu\text{F}$ or $100\mu\text{F}$. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent device latchup, a $100\text{k}\Omega$ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a $10\text{k}\Omega$ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be $1/2$ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

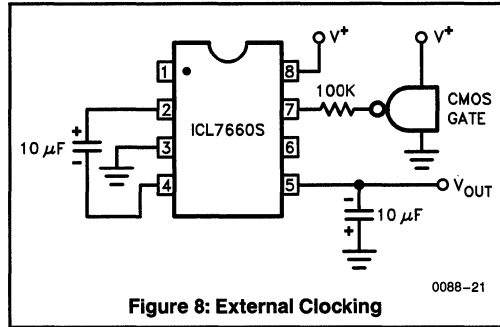


Figure 8: External Clocking

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It is also possible to increase the conversion efficiency of the ICL7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from $10\mu\text{F}$ to $100\mu\text{F}$).

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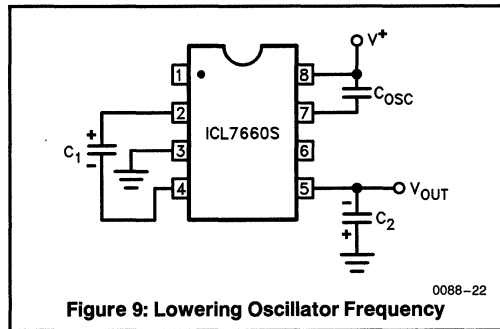
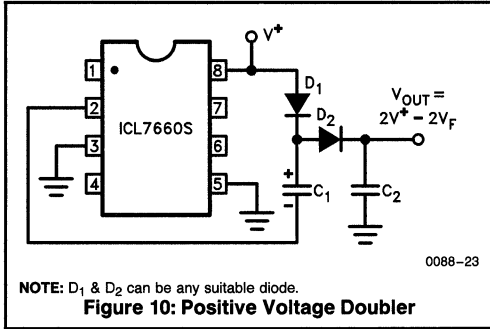


Figure 9: Lowering Oscillator Frequency

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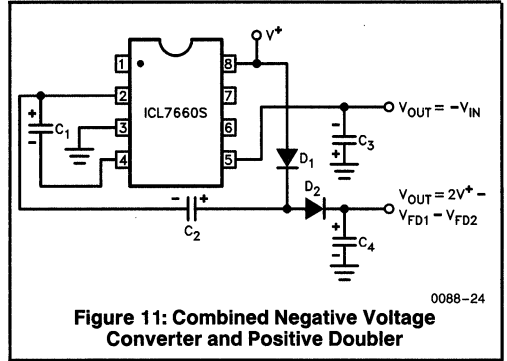
Positive Voltage Doubling

The ICL7660S may be employed to achieve positive voltage doubling using the circuit shown in Figure 10. In this application, the pump inverter switches of the ICL7660S are used to charge C₁ to a voltage level of V⁺ - V_F (where V⁺ is the supply voltage and V_F is the forward voltage drop of diode D₁). On the transfer cycle, the voltage on C₁ plus the supply voltage (V⁺) is applied through diode D₂ to capacitor C₂. The voltage thus created on C₂ becomes (2V⁺) - (2V_F) or twice the supply voltage minus the combined forward voltage drops of diodes D₁ and D₂.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V⁺ = 5 volts and an output current of 10mA it will be approximately 60 ohms.

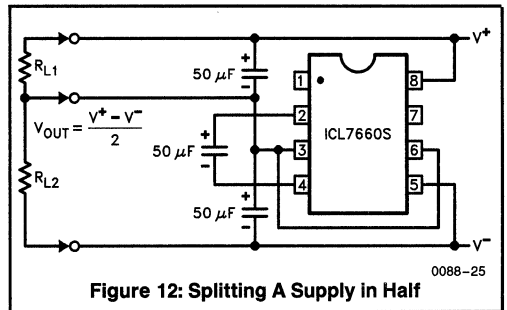
Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C₁ and C₃ perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C₂ and C₄ are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.



Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).



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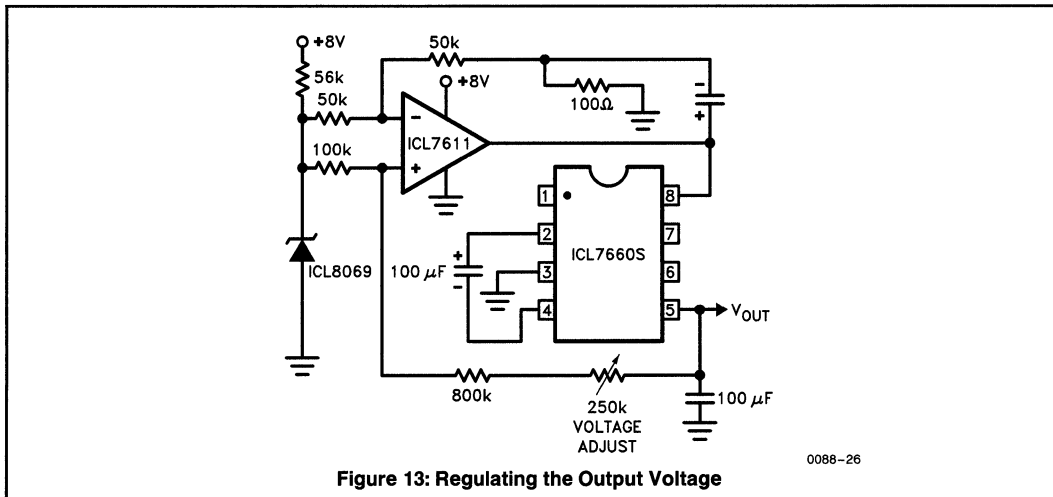
Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660S can be a problem, particularly if the load current varies substantially. The circuit of Figure 13 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommo-

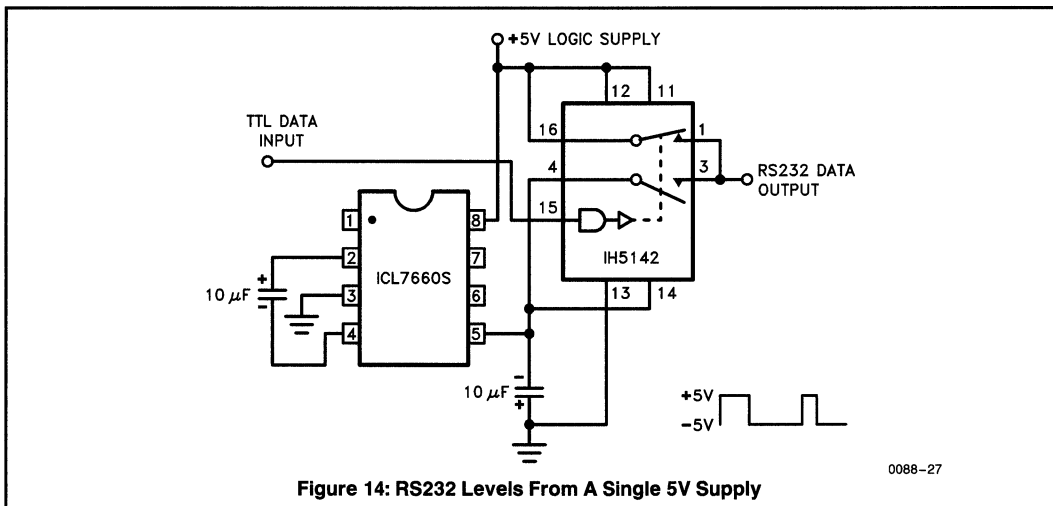
date the 7660S, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660S may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".



5



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NOTE: All typical values have been characterized but are not tested.

ICL7662 CMOS Voltage Converter



GENERAL DESCRIPTION

The Intersil ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10 to +20V), the LV pin is left floating to prevent device latchup.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7662CTV	0°C to +70°C	TO-99
ICL7662CPA	0°C to +70°C	8 PIN MINI DIP
ICL7662MTV*	-55°C to +125°C	TO-99

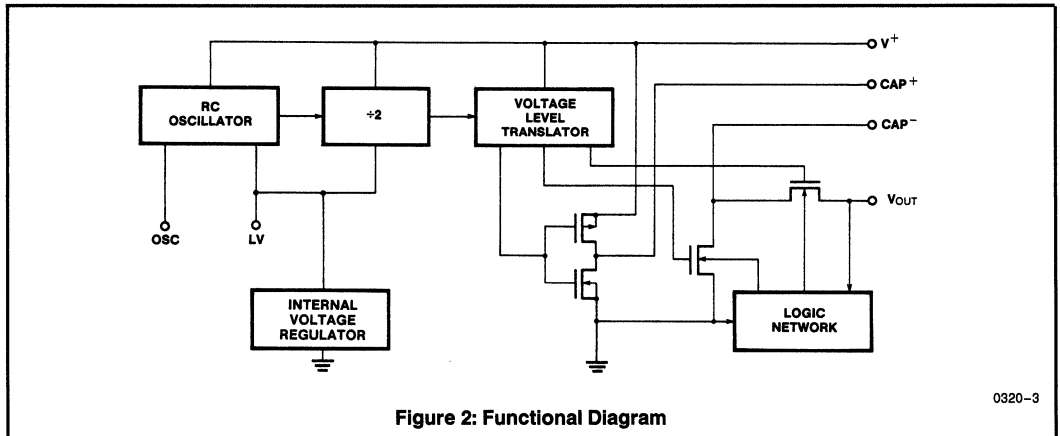
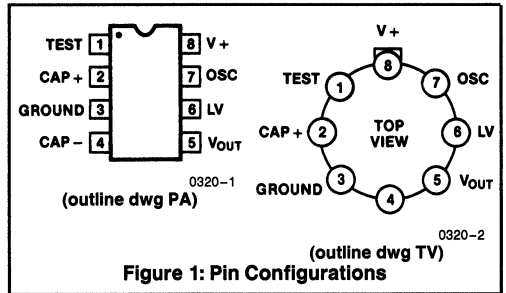
*Add /883B to Part Number for 883B Processing.

FEATURES

- No External Diode Needed Over Entire Temperature Range
- Pin Compatible With ICL7660
- Simple Conversion of +15V Supply to -15V Supply
- Simple Voltage Multiplication ($V_{OUT} = (-) nV_{IN}$)
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 96% Typical Power Efficiency
- Wide Operating Voltage Range 4.5V to 20.0V
- Easy to Use — Requires Only 2 External Non-Critical Passive Components

APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized μ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- Up to -20V for Op Amps



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	22V
Oscillator Input Voltage (Note 1)	-0.3V to (V ⁺ + 0.3V) for V ⁺ < 10V
	(V ⁺ - 10V) to (V ⁺ + 0.3V) for V ⁺ > 10V
Current into LV (Note 1)	20μA for V ⁺ > 10V
Output Short Duration	Continuous

Power Dissipation (Note 2)	
ICL7662CTY	500mW
ICL7662CPA	300mW
ICL7662MTY	500mW
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS V⁺ = 15V, T_A = 25°C, C_{OSC} = 0, unless otherwise stated. Test Circuit

Figure 3.

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
V ⁺ L	Supply Voltage Range—Lo	R _L = 10kΩ, LV = GND	Min < T _A < Max	4.5		11	V
V ⁺ H	Supply Voltage Range—Hi	R _L = 10kΩ, LV = Open	Min < T _A < Max	9		20	V
I ⁺	Supply Current	R _L = ∞, LV = Open	T _A = 25°C 0°C < T _A < +70°C -55°C < T _A < +125°C		.25 .30 .40	.60 .85 1.0	mA
R _O	Output Source Resistance	I _O = 20mA, LV = Open	T _A = 25°C 0°C < T _A < +70°C -55°C < T _A < +125°C		60 70 90	100 120 150	Ω
I ⁺	Supply Current	V ⁺ = 5V, R _L = ∞, LV = GND	T _A = 25°C 0°C < T _A < +70°C -55°C < T _A < +125°C		20 25 30	150 200 250	μA
R _O	Output Source Resistance	V ⁺ = 5V, I _O = 3mA, LV = GND	T _A = 25°C 0°C < T _A < +70°C -55°C < T _A < +125°C		125 150 200	200 250 350	Ω
F _{OSC}	Oscillator Frequency				10		kHz
P _{EFF}	Power Efficiency	R _L = 2kΩ	T _A = 25°C Min < T _A < Max	93 90	96 95		%
V _{OEF}	Voltage Conversion Effic.	R _L = ∞	Min < T _A < Max	97	99.9		%
I _{OSC}	Oscillator Sink or Source Current	V ⁺ = 5V (V _{OSC} = 0V to +5V) V ⁺ = 15V (V _{OSC} = +5V to +15V)			0.5 4.0		μA

NOTES: 1. Connecting any terminal to voltages greater than V⁺ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7662.

2. Derate linearly above 50°C by 5.5mW/°C.

3. Pin 1 is a Test pin and is not connected in normal use.

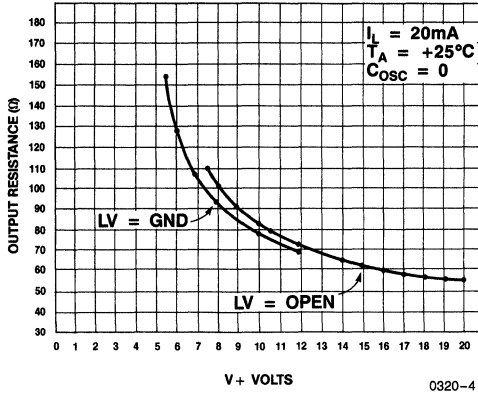
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NOTE: All typical values have been characterized but are not tested.

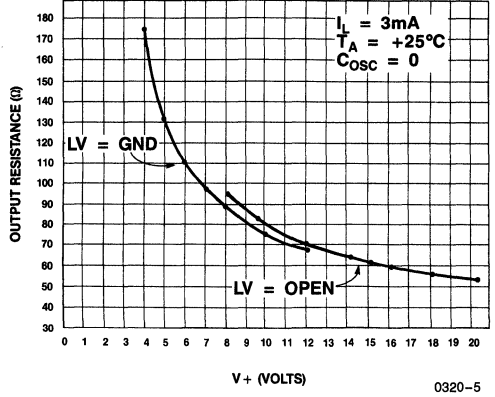
TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuit of Figure 3)

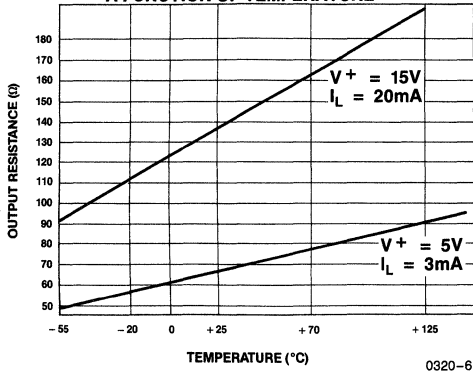
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



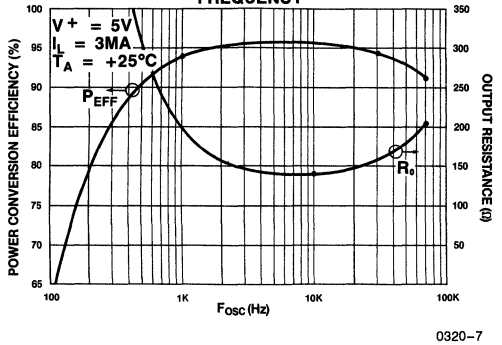
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



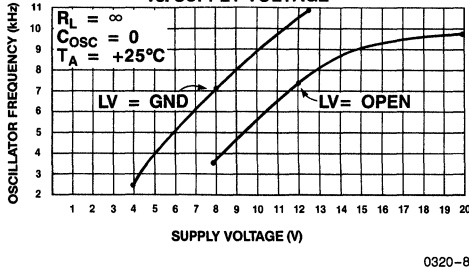
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



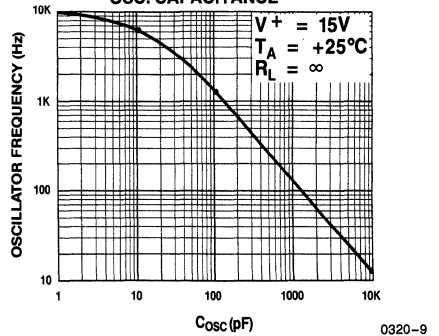
POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

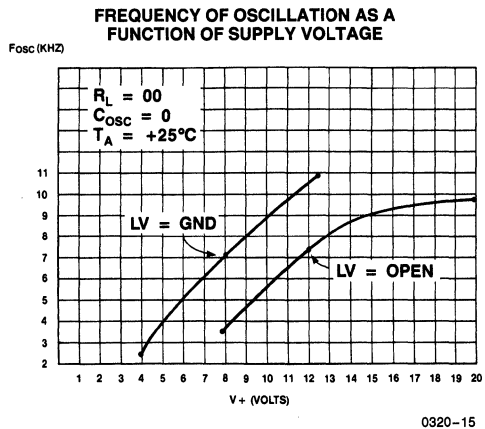
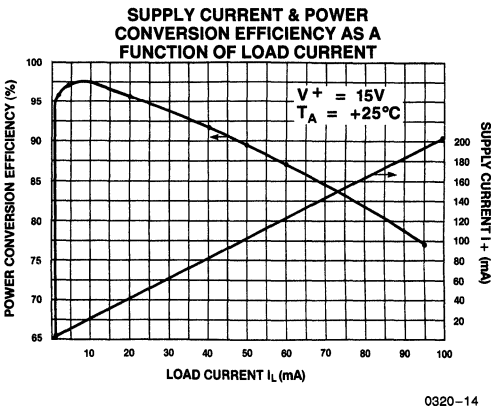
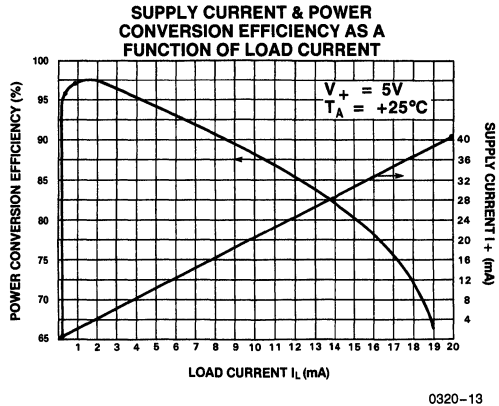
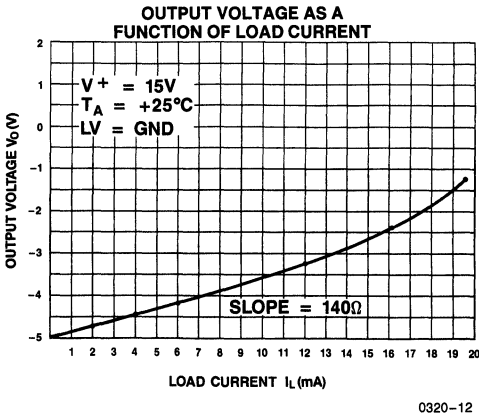
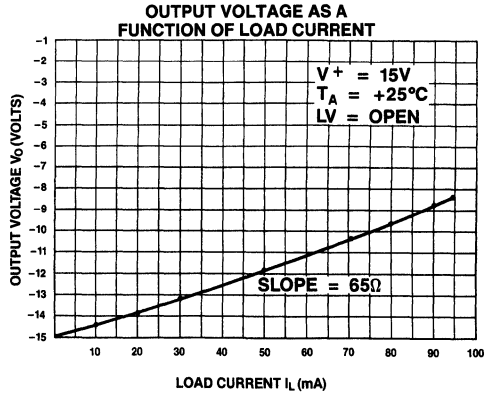
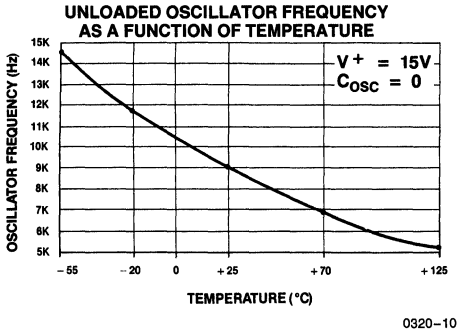


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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuit of Figure 3) (Continued)



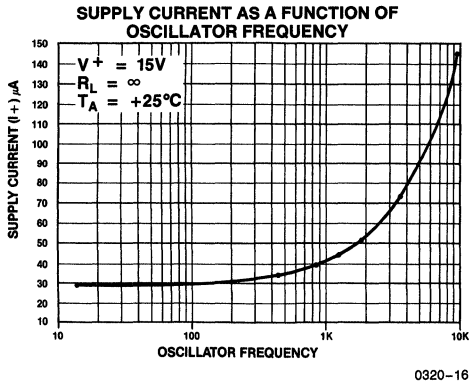
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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuit of Figure 3) (Continued)



NOTE 4.

Note that these curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load. Ideally, $V_{LOAD} \approx 2V_{IN}$, $I_S \approx 2 I_L$, so $V_{IN} \cdot I_S \approx V_{LOAD} \cdot I_L$

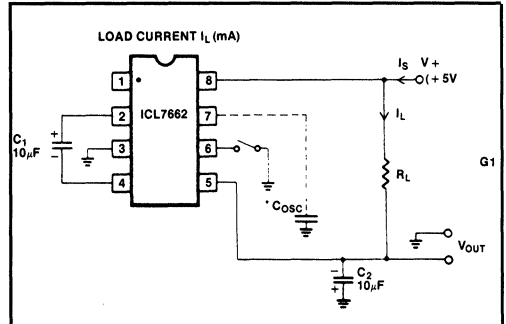
CIRCUIT DESCRIPTION

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive $10\mu F$ polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+ , for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+ , assuming ideal switches and no load on C_2 . The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 11 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.



NOTE: For large value of C_{OSC} ($> 1000\text{pf}$) the values of C_1 and C_2 should be increased to $100\mu F$.

Figure 3: ICL7662 Test Circuit

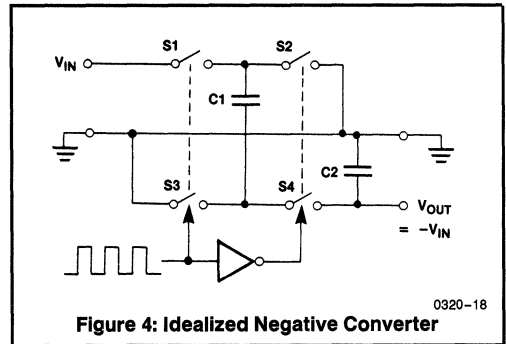


Figure 4: Idealized Negative Converter

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NOTE: All typical values have been characterized but are not tested.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

- A The drive circuitry consumes minimal power
- B The output switches have extremely low ON resistance and virtually no offset.
- C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L , there will be a substantial difference in the voltages V_1 and V_2 . Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 11 volts.
3. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7662 and the + terminal of C_2 must be connected to GROUND.

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 11 volts.

The output characteristics of the circuit in Figure 5 are those of a nearly ideal voltage source in series with 65 ohms. Thus for a load current of -10mA and a supply voltage of +15 volts, the output voltage will be 14.35 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$, where:

$$C = C_1 = C_2$$

$$\text{which gives } \frac{1}{\omega C} = \frac{1}{2\pi f_{\text{pump}} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\mu\text{F}$ and $f_{\text{pump}} = 5\text{kHz}$ ($\frac{1}{2}$ of oscillator frequency)

Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2 , serves all devices while each device requires its own pump capacitor, C_1 . The resultant output resistance would be approximately

$$R_{\text{OUT}} = \frac{R_{\text{OUT}} \text{ (of ICL7662)}}{n \text{ (number of devices)}}$$

Cascading Devices

The ICL7662 may be cascaded as shown to produce large negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{\text{OUT}} = -n (V_{\text{IN}}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 R_{OUT} values.

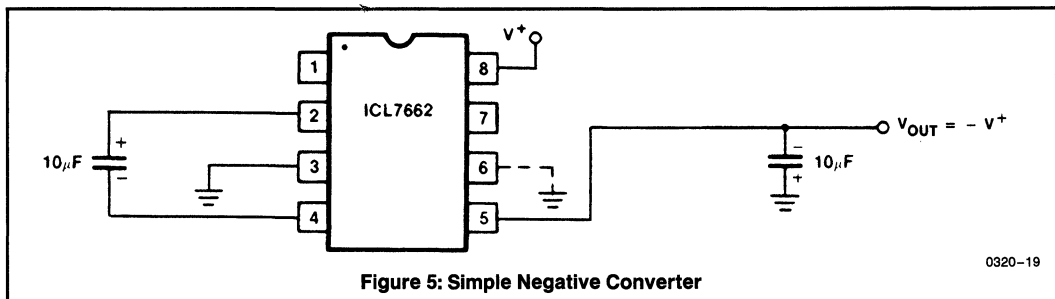


Figure 5: Simple Negative Converter

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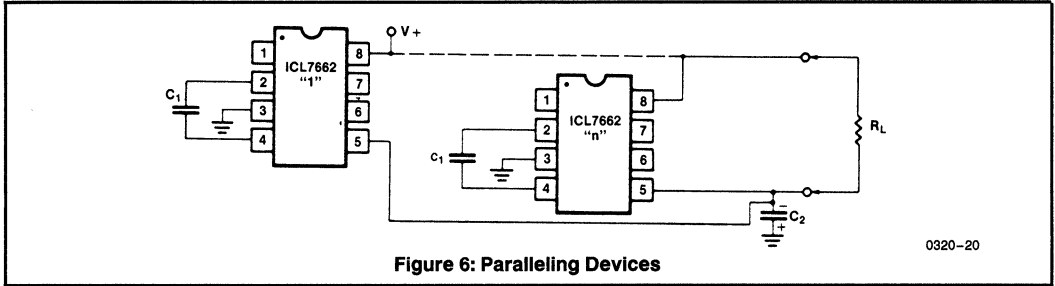


Figure 6: Paralleling Devices

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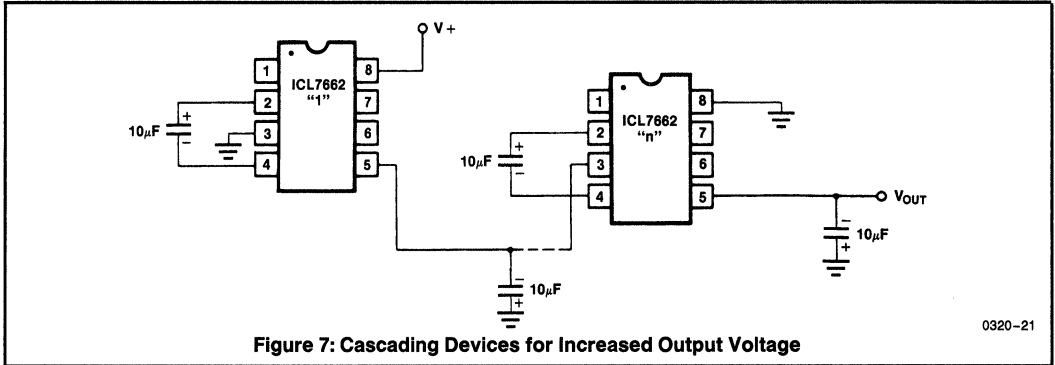


Figure 7: Cascading Devices for Increased Output Voltage

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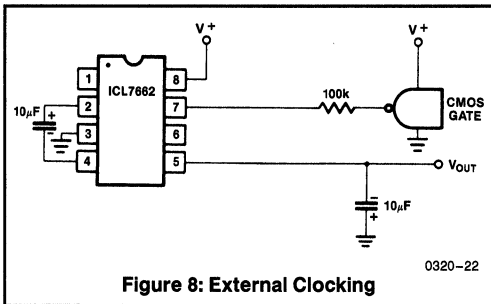


Figure 8: External Clocking

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It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC} , as shown in Figure 9. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 8. In order to prevent possible device latchup, a 100kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

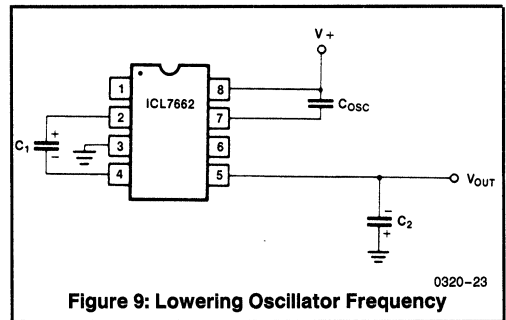


Figure 9: Lowering Oscillator Frequency

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NOTE: All typical values have been characterized but are not tested.

Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 10. In this application, the pump inverter switches of the ICL7662 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2 . The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2 .

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 15$ volts and an output current of 10mA it will be approximately 70 ohms.

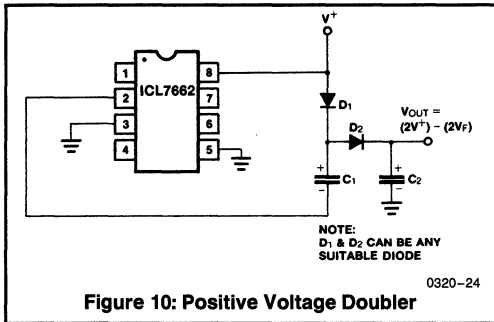


Figure 10: Positive Voltage Doubler

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 11 combines the functions shown in Figures 5 and 10 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

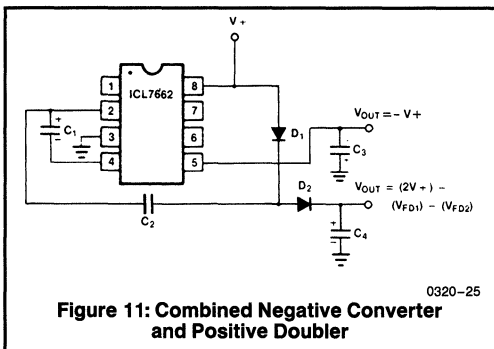


Figure 11: Combined Negative Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 7, +30V can be converted (via +15V, and -15V) to a nominal -30V, although with rather high series output resistance (~250Ω).

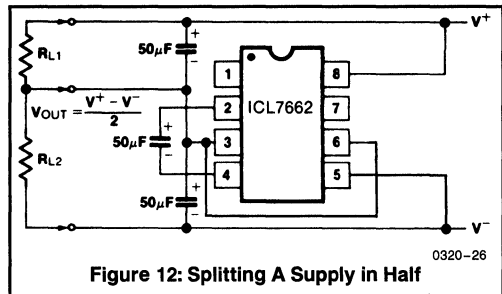


Figure 12: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 13 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

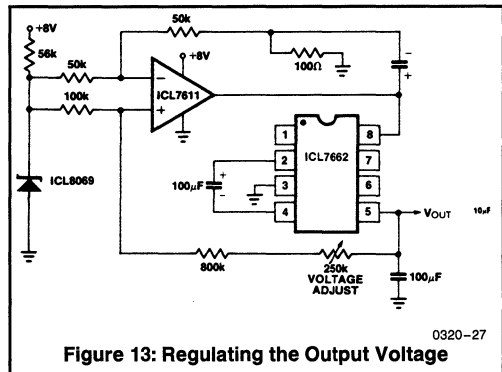


Figure 13: Regulating the Output Voltage

OTHER APPLICATIONS

Further information on the operation and use of the ICL7662 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

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NOTE: All typical values have been characterized but are not tested.

ICL7663 CMOS Programmable Micropower Voltage Regulators



GENERAL DESCRIPTION

The ICL7663 positive voltage regulator is a low-power, high-efficiency device which accepts inputs from 1.6V to 16V and provides adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4 μ A, regardless of load.

Output current sensing and remote shutdown are available, providing protection for the regulator and the circuits it powers. A unique feature is a negative temperature coefficient output. This can be used, for example, to efficiently tailor the voltage applied to a multiplexed LCD through the driver e.g., ICM7231/2/3 so as to extend the display operating temperature range many times.

An enhanced direct replacement for this part called ICL7663S is now available and is more appropriate for new designs.

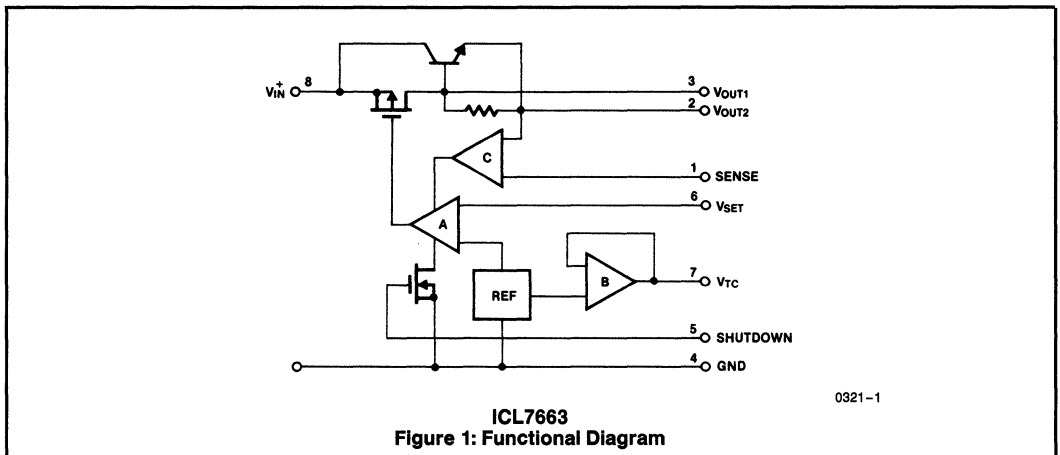
The ICL7663 is available in 8-pin plastic, TO-99 can, Cerdip, and SOIC packages.

FEATURES

- Ideal for Battery-Operated Systems: Less Than 4 μ A Typical Current Drain
- Will Handle Input Voltages From 1.6V to 16V
- Very Low Input-Output Differential Voltage
- 1.3V Bandgap Voltage Reference
- Up to 40mA Output Current
- Output Shutdown Via Current-Limit Sensing or External Logic Signal
- Output Voltages Programmable From 1.3V to 16V
- Output Voltages With Programmable Negative Temperature Coefficients

ORDERING INFORMATION

Positive Regulator		
Part Number	Temperature Range	Package
ICL7663CBA	0°C to +70°C	8-Lead SOIC
ICL7663CPA	0°C to +70°C	8-Lead MiniDIP
ICL7663CJA	0°C to +70°C	8-Lead Cerdip
ICL7663CTV	0°C to +70°C	8-Lead TO-99



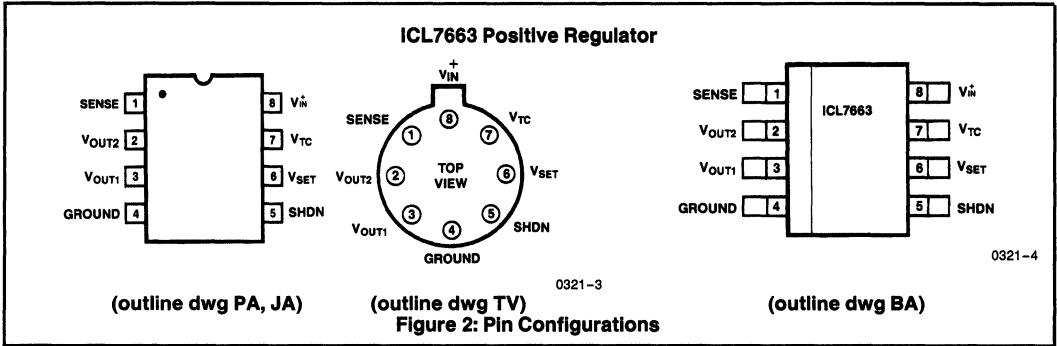
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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS, ICL7663 POSITIVE REGULATOR

Input Supply Voltage	+18V	Output Sinking Current (Terminal 7)	-10mA
Any Input or Output Voltage (Note 1) (Terminals 1, 2, 3, 5, 6, 7)	(GND -0.3V) to (V ⁺ _{IN} +0.3V)	Power Dissipation (Note 2)	
Output Source Current		MiniDIP	200mW
(Terminal 2)	50mA	TO-99 Can	300mW
(Terminal 3)	25mA	Operating Temperature Range	0°C to +70°C
		Storage Temperature	-65°C to +150°C
		Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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NOTE: All typical values have been characterized but are not tested.

ICL7663 ELECTRICAL CHARACTERISTICS

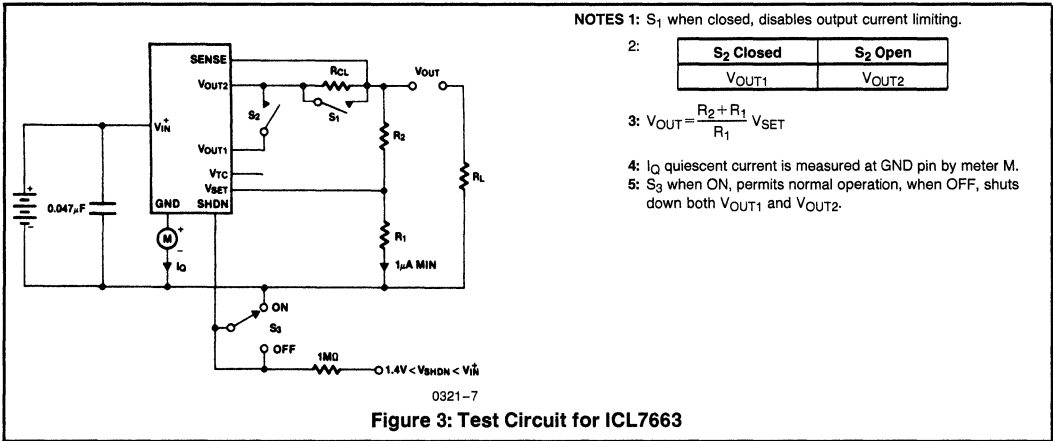
$V_{IN} = 9V$, $V_{OUT} = 5V$, $T_A = +25^\circ C$, unless otherwise specified. See Test Circuit Figure 3.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{IN}	Input Voltage	$T_A = +25^\circ C$ $0^\circ C \leq T_A \leq +70^\circ C$	1.5 1.6		16.0 16.0	V
I_Q	Quiescent Current	$\left\{ \begin{matrix} R_L = \infty \\ 1.4V \leq V_{OUT} \leq 8.5V \end{matrix} \right\}$ $V_{IN} = 16V$ $V_{IN} = 9V$		4.0 3.5	12 10	μA
V_{SET}	Reference Voltage		1.2	1.3	1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	$8.5V < V_{IN} < 9V$		± 200		ppm
$\frac{\Delta V_{SET}}{V_{SET} \Delta V_{IN}}$	Line Regulation	$2V < V_{IN} < 9V$		0.03		%/V
I_{SET}	V_{SET} Input Current			± 0.01	10	nA
I_{SHDN}	Shutdown Input Current			± 0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDNHI} : Both V_{OUT} Disabled V_{SHDNLO} : Both V_{OUT} Enabled	1.4		0.3	V
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold Voltage	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
R_{SAT}	Input-Output On-Resistance (Note 3)	$V_{IN} = 2V$ $V_{IN} = 9V$ $V_{IN} = 15V$		200 70 50		Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$\Delta I_{OUT1} = 100\mu A @ V_{OUT1} = 5V$ $\Delta I_{OUT2} = 10mA @ V_{OUT2} = 5V$		2.0 1.0		Ω
I_{OUT2}	Available Output Current (V_{OUT2})	$V_{IN} = 3V V_{OUT} = V_{SET}$ $V_{IN} = 9V V_{OUT} = 5V$ $V_{IN} = 15V V_{OUT} = 5V$	10 25 40			mA
V_{TC}	Negative-Tempco Output (Note 4)	Open-Circuit Voltage		0.9		V
I_{TC}		Maximum Sink Current	0	8	2.0	mA
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient of V_{TC} Output	Open Circuit		+ 2.5		mV/ $^\circ C$
$I_{L(min)}$	Minimum Load Current	(Includes V_{SET} Divider)	1.0			μA

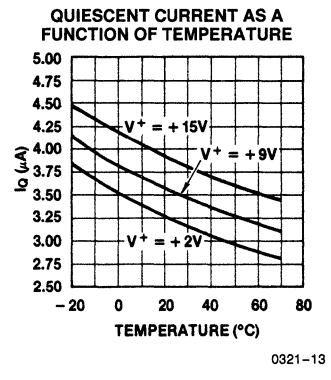
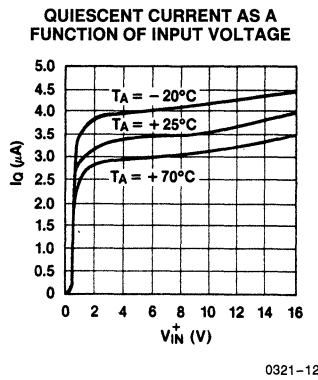
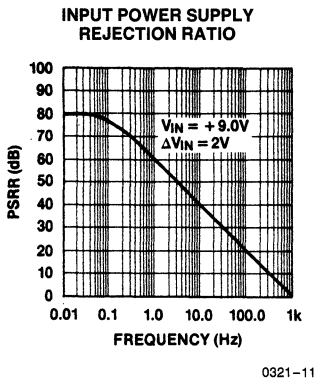
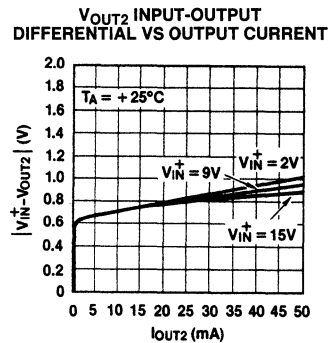
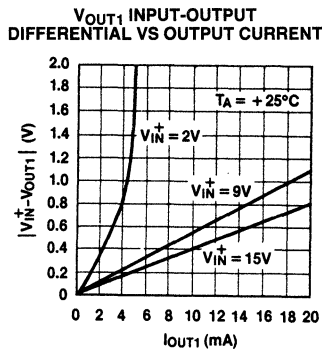
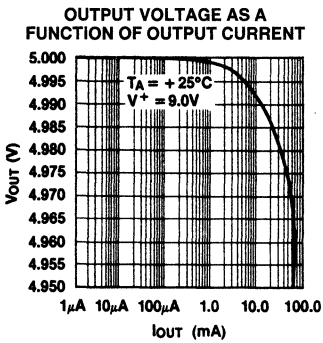
- NOTES:**
1. Connecting any terminal to voltages greater than ($V_{IN} + 0.3V$) or less than ($GND - 0.3V$) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.
 2. Derate linearly above $50^\circ C$ at $5mW/^\circ C$ for minidip and $7.5mW/^\circ C$ for TO-99 can.
 3. This parameter refers to the on-resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.
 4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET} , a negative coefficient results in the output voltage. See Figure 4 for details. Pin will not source current.

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NOTE: All typical values have been characterized but are not tested.



TYPICAL PERFORMANCE CHARACTERISTICS



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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The ICL7663 is a CMOS integrated circuit which contains all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the functional diagram (Figure 1), it can be seen that it contains a band-gap-type voltage reference of 1.3 Volts. This voltage, therefore, is the lowest output voltage the regulator can control. Error amplifier A drives a P-channel pass transistor which is sufficient for low (under about 5mA) currents. The high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via an MOS transistor of the appropriate polarity. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} line. Finally, the positive regulator has an output (V_{TC}) from a buffer amplifier (B), which can be used to generate programmable-temperature-coefficient output voltages.

The amplifiers, reference and comparator circuitry all operate at bias levels well below $1\mu\text{A}$ to achieve the extremely

low quiescent current. This does limit the dynamic response of the circuit, however, and transients are best dealt with outside the regulator loop.

BASIC OPERATION

The ICL7663 is designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as a low power device, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30mA clearly exceeds the power dissipation rating of the minidip: $(10-2)(30)(10^{-3})=240\text{mW}$. The test circuit illustrates proper use of the device.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or non-operation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

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NOTE: All typical values have been characterized but are not tested.

Input Voltages — The regulator accepts working inputs of 1.4V to 18V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulator, where internal operating currents are in the nanoampere range. The 0.047μF capacitor on the device side of the switch will limit inputs to a safe level around 2V/μs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDown pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulator by RC filtering, zener protection, or even fusing.

Output Voltages — The resistor divider R₂/R₁ is used to scale the reference voltage, V_{SET}, to the desired output using the formula V_{OUT} = (1 + R₂/R₁) V_{SET}. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. Because of the low leakage current of the V_{SET} terminal, these resistors can be tens of megohms for minimum additional quiescent drain current. However, some load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1μA. This can include the current for R₂ and R₁.

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal.

Output Currents — For the ICL7663, low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Where higher currents are needed, use V_{OUT2} (V_{OUT1} should be left open in this case).

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing — The on-chip comparator (C in the block diagrams) permits shutdown of the regulator output in the event of excessive current drain. As the test circuit shows, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2}, and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.7V) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.

Logic-Controllable Shutdown — When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it/s required. This usually means switches, with their unreliable contacts. Instead, the ICL7663 can be shut down by a logic signal, leaving only I_Q (under 4μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less

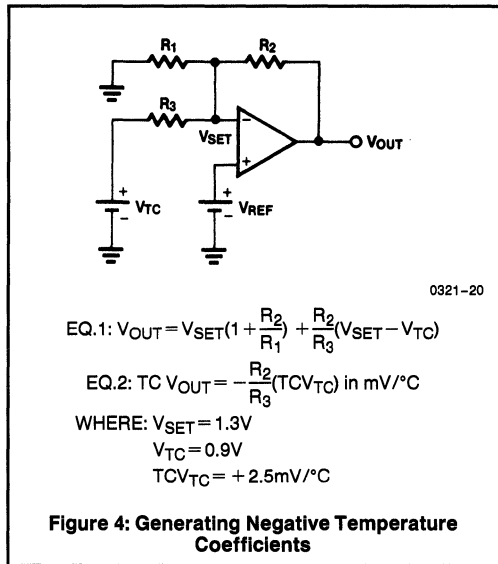
than 0.3V will keep the regulator ON, and a voltage level of more than 1.4V but less than V_{IN}⁺ will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V_{IN}⁺), the current from this signal should be limited to 100μA maximum by a high-value (1MΩ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

Additional Circuit Precautions — The regulator has poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

$$I = C \frac{\Delta V}{\Delta t}, C = I_{OUT} \frac{(20 \times 10^{-3})}{0.9 V_{OUT}} = 0.022 \frac{I_{OUT}}{V_{OUT}}$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see "Current-Limit Sensing").

Producing Output Voltages With Negative Temperature Coefficients — The ICL7663 has an additional output which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R₂/R₃ ratio (see Figure 4 and its design equations).



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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

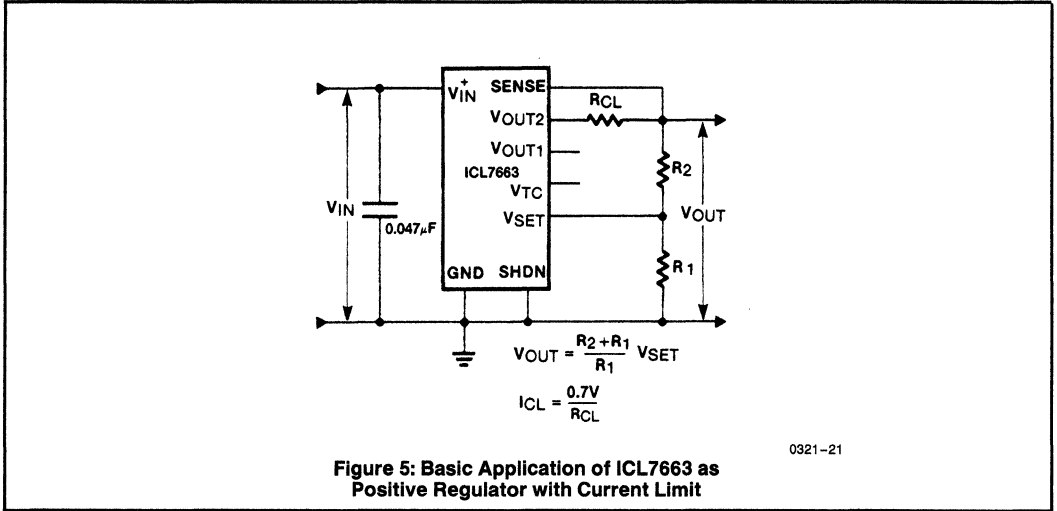


Figure 5: Basic Application of ICL7663 as Positive Regulator with Current Limit

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NOTE: All typical values have been characterized but are not tested.

ICL7663B ADDENDUM TO THE ICL7663 DATASHEET

This Addendum to the standard ICL7663 datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7663B devices. The following table indicates those limits to which the ICL7663B is tested and/or guaranteed operational.

ICL7663B POSITIVE REGULATOR ORDERING INFORMATION

Positive Regulator		
ICL7663BCBA	0°C to 70°C	8-pin S.O.I.C.
ICL7663BCJA	0°C to 70°C	8-pin CERDIP
ICL7663BCPA	0°C to 70°C	8-pin MiniDIP
ICL7663BCTV	0°C to 70°C	TO-99

ABSOLUTE MAXIMUM RATINGS ICL7663B

Input Supply Voltage +12V
 Any Input or Output Voltage (Note 1) Terminals 1, 2, 3, 4, 5, 6, 7) (GND - 0.3V) to (V⁺_{IN} + 0.3V)
 Output Source Current
 (Terminal 2) 50mA
 (Terminal 3) 25mA

Output Sinking Current (Terminal 7) -10mA
 Power Dissipation (Note 2)
 MiniDIP 200mW
 TO-99 Can 300mW

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7663B OPERATING CHARACTERISTICS V⁺_{IN} = 9V, V_{OUT} = 5V, T_A = +25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V ⁺ _{IN}	Input Voltage	T _A = +25°C 20°C ≤ T _A ≤ +70°C	1.5 1.6		10 10	V
I _Q	Quiescent Current	{ R _L = ∞ 1.4V ≤ V _{OUT} ≤ 8.5V }		3.5	10	μA
V _{SET}	Reference Voltage		1.2	1.3	1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	8.5V < V ⁺ _{IN} < 9V		± 200		ppm
$\frac{\Delta V_{SET}}{V_{SET} \Delta V_{IN}}$	Line Regulation	2V < V ⁺ _{IN} < 9V		0.03		%/V
I _{SET}	V _{SET} Input Current			± 0.01	10	nA
I _{SHDN}	Shutdown Input Current			± 0.01	10	nA
V _{SHDN}	Shutdown Input Voltage	V _{SHDNHI} : Both V _{OUT} Disabled V _{SHDNLO} : Both V _{OUT} Enabled	1.4		0.3	V
I _{SENSE}	Sense Pin Input Current			0.01	10	nA
V _{CL}	Sense Pin Input Threshold Voltage	V _{CL} = V _{OUT2} - V _{SENSE} (Current-Limit Threshold)		0.7		V
R _{SAT}	Input-Output Saturation Resistance (Note 3)	V ⁺ _{IN} = 2V V ⁺ _{IN} = 9V		200 70		Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	ΔI _{OUT1} = 100μA @ V _{OUT1} = 5V ΔI _{OUT2} = 10mA @ V _{OUT2} = 5V		2 1		Ω
I _{OUT2}	Available Output Current (V _{OUT2})	V ⁺ _{IN} = 3V V _{OUT} = V _{SET} V ⁺ _{IN} = 9V V _{OUT} = 5V	10 25			mA

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NOTE: All typical values have been characterized but are not tested.

ICL7663B OPERATING CHARACTERISTICS $V^+_{IN}=9V, V_{OUT}=5V, T_A = +25^\circ\text{C}$, unless otherwise specified. (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{TC}	Negative-Tempco Output (Note 4)	Open-Circuit Voltage		0.9		V
I_{TC}		Maximum Sink Current	0	8	2	mA
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient	Open Circuit		+2.5		mV/°C
$I_{L(\min)}$	Minimum Load Current	(Includes V_{SET} Divider)			1	μA

NOTES: 1. Connecting any terminal to voltages greater than ($V^+_{IN} + 0.3V$) or less than ($\text{GND} - 0.3V$) may cause destructive device latchup. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663B power-up.

2. Derate linearly above 50°C at $5\text{mW}/^\circ\text{C}$ for minidip and $7.5\text{mW}/^\circ\text{C}$ for TO-99 can.

3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET} , a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

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ICL7663S

CMOS Programmable Micropower Positive Voltage Regulator



ICL7663S

GENERAL DESCRIPTION

The Intersil ICL7663S Super Programmable Micropower Voltage Regulator is a low power, high efficiency positive voltage regulator which accepts 1.6V to 16V inputs and provides adjustable outputs from 1.3V to 16V at currents up to 40mA.

It is a direct replacement for the industry standard ICL7663B offering *wider* operating voltage and temperature ranges, *improved* output accuracy (ICL7663SA), *better* temperature coefficient, *guaranteed* maximum supply current, *guaranteed* line and load regulation, and *ESD protection* in excess of 2000V on all pins. All improvements are highlighted in **bold italics** in the electrical characteristics section. **Critical parameters are guaranteed over the entire commercial and industrial temperature ranges.** The ICL7663S/SA programmable output voltage is set by two external resistors. The 1% reference accuracy of the ICL7663SA eliminates the need for trimming the output voltage in most applications.

The ICL7663S is well suited for battery powered supplies, featuring 4μA quiescent current, low V_{IN} to V_{OUT} differential, output current sensing and logic input level shutdown control. In addition, the ICL7663S has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for LCD displays.

The ICL7663S is available in either an 8-pin plastic, TO-99 can, CERDIP, or SOIC package.

FEATURES

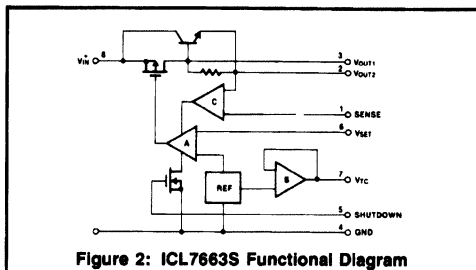
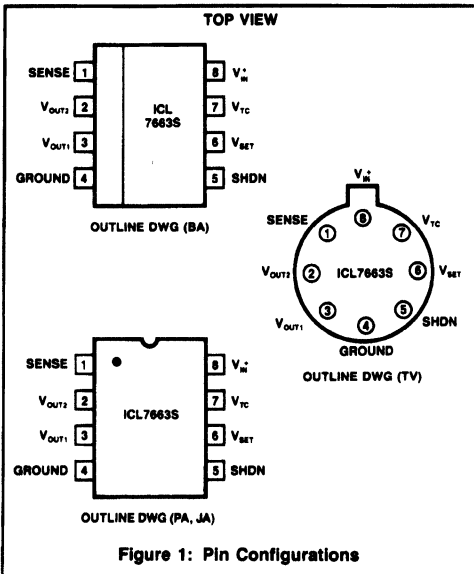
- **Guaranteed 10μA** maximum quiescent current over all temperature ranges
- **Wider operating voltage range** — 1.6V to 16V
- **Guaranteed** line and load regulation over *entire* operating temperature range.
- **Optional**
 - 1% output voltage accuracy (ICL7663SA)
 - Output voltage programmable from 1.3V to 16V
 - Improved temperature coefficient of output voltage
 - 40mA minimum output current with current limiting
 - Output voltages with programmable negative temperature coefficients.
- Output shutdown via current-limit sensing or external logic level
- Low input-to-output voltage differential
- Improved direct replacement for industry standard ICL7663B and other second-source products
- Enhanced ESD protection >2000V

APPLICATIONS

- Low-Power Portable Instrumentation
- **Pagers**
- Handheld Instruments
- LCD Display Modules
- Remote Data Loggers
- Battery-Powered Systems

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7663SCBA ICL7663SCPA ICL7663SCJA ICL7663SCTV ICL7663SACPA ICL7663SACJA ICL7663SACTV	0°C to +70°C	8 Lead SOIC 8 Lead Minidip 8 Lead CERDIP TO-99 8 Lead Minidip 8 Lead CERDIP TO-99
ICL7663SIBA ICL7663SIPA ICL7663SIIA ICL7663SITV ICL7663SAIPA ICL7663SAIIA ICL7663SAITV	-25°C to +85°	8 Lead SOIC 8 Lead Minidip 8 Lead CERDIP TO-99 8 Lead Minidip 8 Lead CERDIP TO-99



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NOTE: All typical values have been characterized but are not tested.

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ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage.....	+ 18V
Any Input or Output Voltage (Note 1) (Terminals 1,2,3,5,6,7,).....	($V_{IN} + 0.3$) to (GND - 0.3)V
Output Source Current (Terminal 2).....	50mA
(Terminal 3).....	25mA
Output Sinking Current (Terminal 7).....	- 10mA
Lead Temperature (Soldering, 10 sec).....	300°C
Storage Temperature Range.....	- 65° to 150°C
Operating Temp. Range	
ICL7663SC.....	0°C to + 70°C
ICL7663SI.....	- 25°C to + 85°C
Total Power Dissipation (Note 2)	
SOIC.....	200mW
Minidip.....	200mW
TO-99 Can.....	300mW
CERDIP.....	500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Specifications below applicable to both ICL7663S and ICL7663SA unless otherwise stated. $V_{IN} = 9V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise stated. See Test Circuit, Figure 3.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}^+	Input Voltage	ICL7663S				
		TA = 25°C	1.5		16	V
		0°C < TA < 70°C	1.6		16	V
		-25°C < TA < +85°C	1.6		16	
		ICL7663SA				
		0°C < TA < +70°C	1.6		16	V
		-25°C < TA < +85°C	1.6		16	
I_O	Quiescent Current	1.4V < V_{OUT} < 8.5V, No Load				
		$V_{IN}^+ = 9V$ 0°C < TA < 70°C			10	µA
		-25°C < TA < +85°C			10	
		$V_{IN}^+ = 16V$ 0°C < TA < 70°C			12	µA
		-25°C < TA < +85°C			12	
V_{SET}	Reference Voltage	$I_{OUT1} = 100\mu A$, $V_{OUT} = V_{SET}$				
		ICL7663S TA = 25°C	1.2	1.3	1.4	V
		ICL7663SA TA = 25°C	1.275	1.29	1.305	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient	0°C < TA < 70°C		100		ppm
		-25°C < TA < +85°C		100		ppm
$\frac{\Delta V_{SET}}{V_{SET} \Delta V_{IN}}$	Line Regulation	2V < V_{IN} < 15V				
		0°C < TA < 70°C		0.03	0.3	%/V
		-25°C < TA < 85°C		0.03	0.3	%/V
I_{SET}	V_{SET} Input Current	0°C < TA < 70°C		0.01	10	nA
		-25°C < TA < 85°C		0.01	10	nA

Notes:

- Connecting any terminal to voltages greater than ($V_{IN}^+ + 0.3V$) or less than (GND - 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663S power-up.
- Derate linearly above 50°C at 5mW/°C for Plastic Minidip, 7.5mW/°C for TO-99 can, and 10mW/°C for CERDIP.

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{SHDN}	Shutdown Input Current			± 0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDN} HI: Both V_{OUT} Disabled V_{SHDN} LO: Both V_{OUT} Enabled	1.4		0.3	V V
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold			0.5		V
R_{SAT}	Input-Output Saturation Resistance <i>Note 3</i>	$V^+_{IN} = 2V, I_{OUT1} = 1mA$ $V^+_{IN} = 9V, I_{OUT1} = 2mA$ $V^+_{IN} = 15V, I_{OUT1} = 5mA$		170 50 35	350 100 70	Ω Ω Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$1mA < I_{OUT2} < 20mA$ $50\mu A < I_{OUT1} < 5mA$		1 2	3 10	Ω Ω
I_{OUT2}	Available Output Current (V_{OUT2})	$3V < V_{IN} < 16V, V_{IN} - V_{OUT2} = 1.5V$	40			mA
V_{TC}	Negative Tempcco	Open - Circuit Voltage		0.9		V
I_{TC}	Output (Note 4)	Maximum Sink Current	0	8	2.0	mA
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient	Open Circuit		+2.5		mV/°C
I_L (MIN)	Minimum Load Current	(includes V_{SET} Divider) $T_A = 25^\circ C$ $0^\circ C < T_A < +70^\circ C$ $-25^\circ C < T_A < +85^\circ C$		0.2 0.2	1.0 5.0 5.0	μA μA μA

Notes:

- This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.
- This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET} , a negative coefficient results in the output voltage. See Figure 4 for details. Pin will not source current.
- All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V.
- All significant improvements over the industry standard ICL7663 are highlighted in **bold italics**.

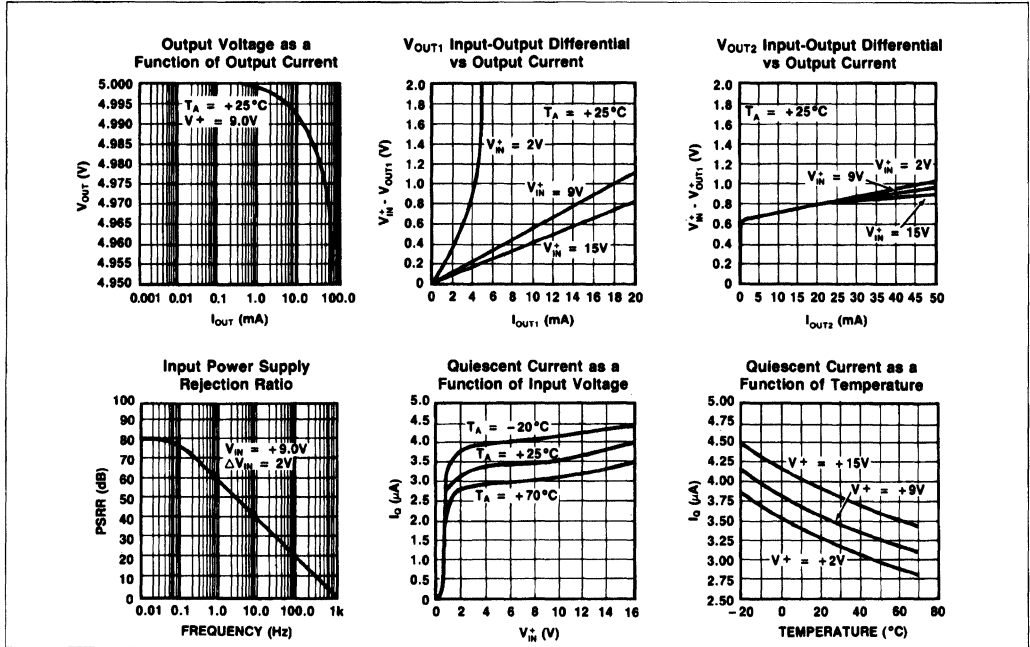
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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



DETAILED DESCRIPTION

The ICL7663S is a CMOS integrated circuit incorporating all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the functional diagram (Figure 2), the main blocks are a bandgap-type voltage reference, an error amplifier, and an output driver with both PMOS and NPN pass transistors.

The bandgap output voltage, trimmed to $1.29\text{V} \pm 15\text{mV}$ for the ICL7663SA, and the input voltage at the V_{SET} terminal are compared in amplifier A. Error amplifier A drives a P-channel pass transistor which is sufficient for low (under about 5mA) currents. The high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via a N-channel MOS transistor. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} terminal. The ICL7663S has an output (V_{TC}) from a buffer amplifier (B), which can be used in combination with amplifier A to generate programmable-temperature-coefficient output voltages.

The amplifiers, reference and comparator circuitry all operate

at bias levels well below $1\mu\text{A}$ to achieve extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

BASIC OPERATION

The ICL7663S is designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30mA clearly exceeds the power dissipation rating of the minidip:

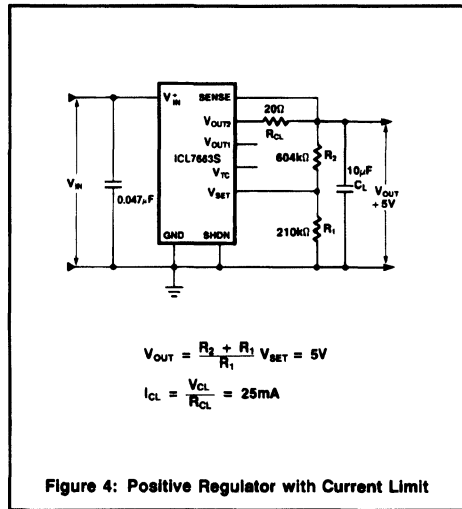
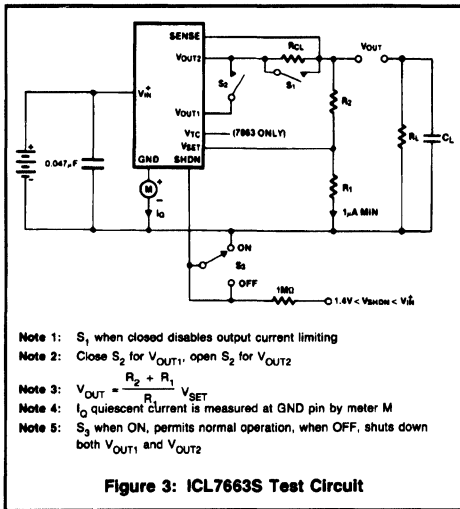
$$(10-2) (30) (10^{-3}) = 240\text{mW}$$

The circuit of Figure 4 illustrates proper use of the device.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or nonoperation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

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NOTE: All typical values have been characterized but are not tested.



Input Voltages—The ICL7663S accepts working inputs of 1.5V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047µF capacitor on the device side of the switch will limit inputs to a safe level around 2V/µs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDown pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output Voltages—The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET} , to the desired output using the formula $V_{OUT} = (1 + R_2/R_1) V_{SET}$. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. In most applications the potentiometer may be eliminated by using the ICL7663SA. The ICL7663SA has V_{SET} voltage guaranteed to be 1.29V±15mV and when used with ±1% tolerance resistors for R_1 and R_2 the initial output voltage will be within ±2.7% of ideal.

The low leakage current of the V_{SET} terminal allows R_1 and R_2 to be tens of megohms for minimum additional quiescent drain current. However, some load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1µA. This can include the current for R_2 and R_1 .

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal. The input-output differential increases to 1.5V when using V_{OUT2} .

Output Currents—Low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Where higher currents are needed, use V_{OUT2} (V_{OUT1} should be left open in this case).

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High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing—The on-chip comparator (C in Figure 2) permits shutdown of the regulator output in the event of excessive current drain. As Figure 4 shows, a current-limiting resistor, R_{CL} , is placed in series with V_{OUT2} and the SENSE terminal is connected to the load side of R_{CL} . When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.5V) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL} .

Logic-Controllable Shutdown—When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it is required. This usually means switches, with their unreliable contacts. Instead, the ICL7663S can be shut down by a logic signal, leaving only I_Q (under 4µA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663S will keep the regulator ON, and a voltage level of more than 1.4V but less than V^+_{IN} will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V^+_{IN}) the current from this signal should be limited to 100µA maximum by a high-value (1MΩ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

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NOTE: All typical values have been characterized but are not tested.

Additional Circuit Precautions—This regulator has poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

$$I = C \frac{\Delta V}{\Delta t}, C = I_{OUT} \frac{(20 \times 10^{-3})}{0.9V_{OUT}} = 0.022 \frac{I_{OUT}}{V_{OUT}}$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see "Current-Limit Sensing").

Producing Output Voltages With Negative Temperature Coefficients—The ICL7663S has an additional output which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. (The TC of the output voltage is controlled by the R₂/R₃ ratio (see Figure 5 and its design equations).

APPLICATIONS

Boosting Output Current with External Transistor

The maximum available output current from the ICL7663S is 40mA. To obtain output currents greater than 40mA, an external NPN transistor is used connected as shown in Figure 6.

Generating a Temperature Compensated Display Drive Voltage

Temperature has an important effect in the variation of threshold voltage in multiplexed LCD displays. As temperature rises, the threshold voltage goes down. For applications where the display temperature varies widely, a temperature compensated display voltage, V_{DISP}, can be generated using the ICL7663S. This is shown in Figure 7 for the ICM7233 triplexed LCD display driver.

Generating Regulated Split Supplies from a Single Supply

To generate regulated +5V and -5V supplies from a single supply, the ICL7660S and ICL7664 are used with the ICL7663S, as shown in Figure 8. The ICL7660S inverts the +9V input voltage to -9V. Then, the ICL7664S negative voltage regulator uses the -9V to generate a regulated -5V output, while the ICL7663S positive voltage regulator regulates the +9V input to a constant +5V output.

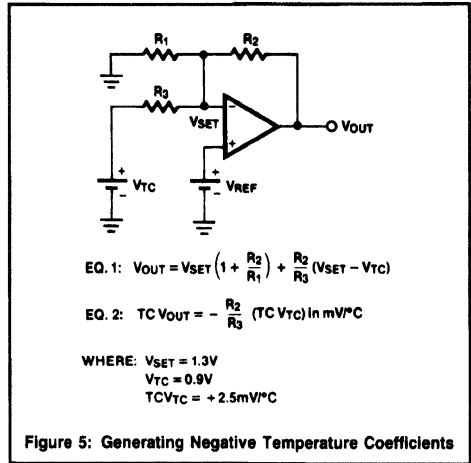


Figure 5: Generating Negative Temperature Coefficients

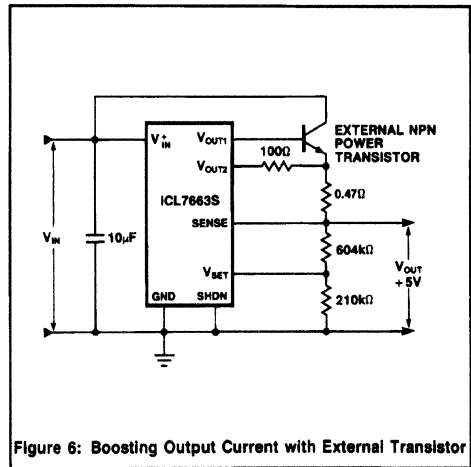


Figure 6: Boosting Output Current with External Transistor

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APPLICATIONS

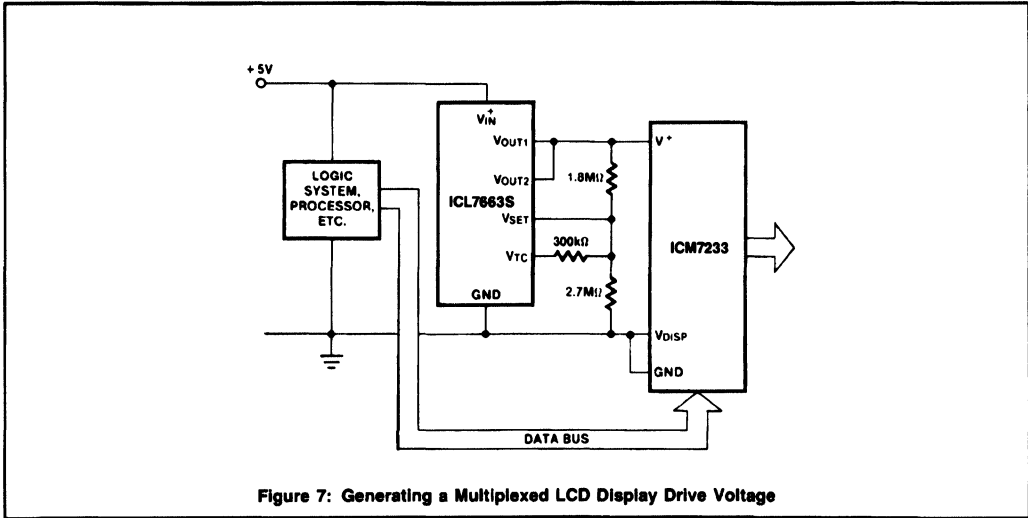


Figure 7: Generating a Multiplexed LCD Display Drive Voltage

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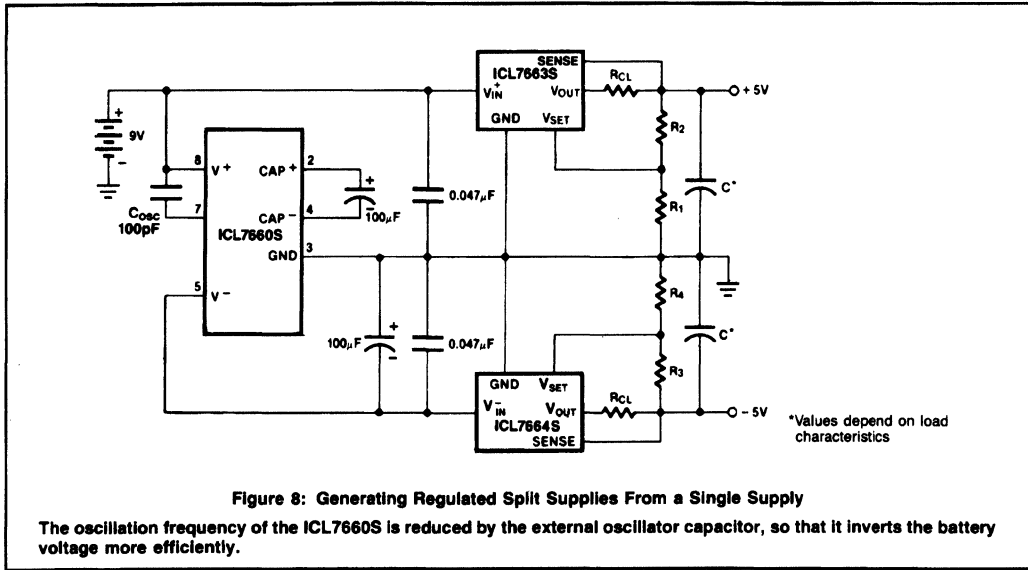


Figure 8: Generating Regulated Split Supplies From a Single Supply

The oscillation frequency of the ICL7660S is reduced by the external oscillator capacitor, so that it inverts the battery voltage more efficiently.

*Values depend on load characteristics

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ICL7665

Micropower Under/Over Voltage Detector



GENERAL DESCRIPTION

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only 3µA typical for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. Typical applications are battery-backup computer memories, battery-operated medical devices, radiation dosimeters, pocket pagers, portable calibrators, test instruments, and charging systems.

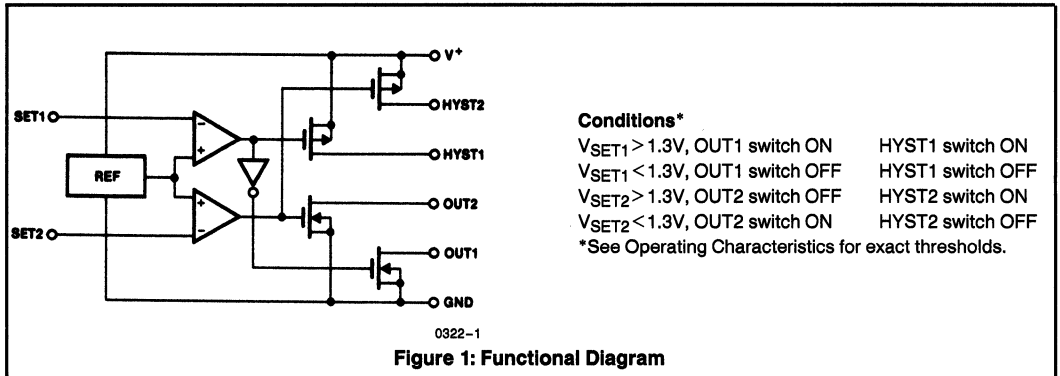
An enhanced direct replacement for this part called ICL7665s will become available shortly and will be more appropriate for new designs.

FEATURES

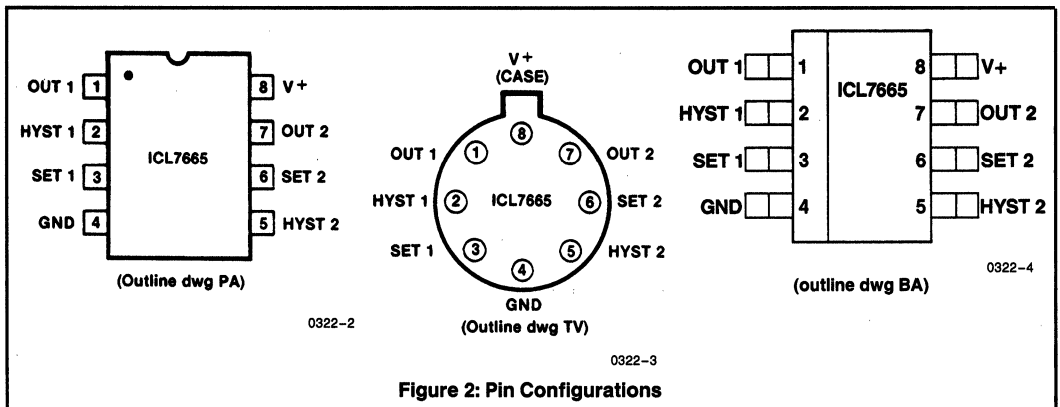
- Exceptionally Low Supply Current (<3µA Typ)
- Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels
- Accurate On-Chip Bandgap Reference
- Up to 20mA Output Current Sinking Ability
- Wide Supply Voltage Range

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7665CPA	0°C to +70°C	8 Lead MiniDIP
ICL7665CTV	0°C to +70°C	8 Lead TO-99
ICL7665CBA	0°C to 70°C	8 Lead SOIC
ICL7665CJA	0°C to 70°C	8 Lead CERDIP



Conditions*
 VSET1 > 1.3V, OUT1 switch ON HYST1 switch ON
 VSET1 < 1.3V, OUT1 switch OFF HYST1 switch OFF
 VSET2 > 1.3V, OUT2 switch OFF HYST2 switch ON
 VSET2 < 1.3V, OUT2 switch ON HYST2 switch OFF
 *See Operating Characteristics for exact thresholds.



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -0.3V to +18V
 Output Voltages OUT1 and OUT2 (with respect to GND)
 (Note 2) -0.3V to +18V
 Output Voltages HYST1 and HYST2 (with respect to V+)
 (Note 2) +0.3V to -18V
 Input Voltages SET1 and SET2
 (Note 2) (GND-0.3V) to (V+ +0.3V)

Maximum Sink Output Current OUT1 and OUT2 25mA
 Maximum Source Output Current HYST1
 and HYST2 -25mA
 Power Dissipation (Note 1) 200mW
 Operating Temperature Range 0°C to +70°C
 Storage Temperature Range -55°C to +125°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC OPERATING CHARACTERISTICS

(V+ = 5V, TA = +25°C, unless otherwise specified. See Test Circuit

Fig. 4)

Symbol	Parameter	Test Conditions	Limits			Units		
			Min	Typ	Max			
V+	Operating Supply Voltage	TA = +25°C 0°C ≤ TA ≤ +70°C	1.6 1.8		16 16	V		
I+	Supply Current	GND ≤ VSET1, VSET2 ≤ V+ All Outputs Open Circuit V+ = 2V V+ = 9V V+ = 15V		2.5 2.6 2.9	10 10 15	μA		
VSET1 VSET2	Input Trip Voltage		1.15 1.2	1.3 1.3	1.45 1.4	V		
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of VSET			±200		ppm/°C		
$\frac{\Delta V_{SET}}{\Delta V_S}$	Supply Voltage Sensitivity of VSET1, VSET2	ROUT1, ROUT2, RHYST1, RHYST2 = 1MΩ		0.004		%/V		
IOLK IHLK	Output Leakage Currents on OUT and HYST	VSET = 0V or VSET ≥ 2V		10 -10	200 -100	nA		
IOLK IHLK		V+ = 9V, TA = 70°C V+ = 9V, TA = 70°C			2000 -500			
VOUT1 VOUT1 VOUT1	Output Saturation Voltages	V+ = 2V, VSET1 = 2V, IOUT1 = 2mA V+ = 5V, VSET1 = 2V, IOUT1 = 2mA V+ = 9V, VSET1 = 2V, IOUT1 = 2mA		0.2 0.1 0.06	0.5 0.3 0.2	V		
VHYST1 VHYST1 VHYST1		V+ = 2V, VSET1 = 2V, IHYST1 = -0.5mA V+ = 5V, VSET1 = 2V, IHYST1 = -0.5mA V+ = 9V, VSET1 = 2V, IHYST1 = -0.5mA		-0.15 -0.05 -0.02	-0.3 -0.15 -0.10			
VOUT2 VOUT2 VOUT2		V+ = 2V, VSET2 = 0V, IOUT2 = 2mA V+ = 5V, VSET2 = 0V, IOUT2 = 2mA V+ = 9V, VSET2 = 0V, IOUT2 = 2mA		0.2 0.15 0.11	0.5 0.3 0.25			
VHYST2 VHYST2 VHYST2		V+ = 2V, VSET2 = 2V, IHYST2 = -0.2mA V+ = 5V, VSET2 = 2V, IHYST2 = -0.5mA V+ = 9V, VSET2 = 2V, IHYST2 = -0.5mA		-0.25 -0.43 0.35	-0.8 -1.0 -1.0			
ISET		VSET Input Leakage Current	GND ≤ VSET ≤ V+		0.01		10	nA
ΔVSET		ΔVSET Input for Complete Output Change	ROUT = 4.7kΩ, RHYST = 20kΩ VOUTLO = 1% V+, VOUTH = 99% V+		1			mV
VSET1-VSET2		Difference in Trip Voltages	ROUT, RHYST = 1MΩ		±5		±50	
		Output/Hysteresis Difference	ROUT, RHYST = 1MΩ		±1			

NOTES: 1. Derate above ±25°C ambient temperature at 4mW/°C.

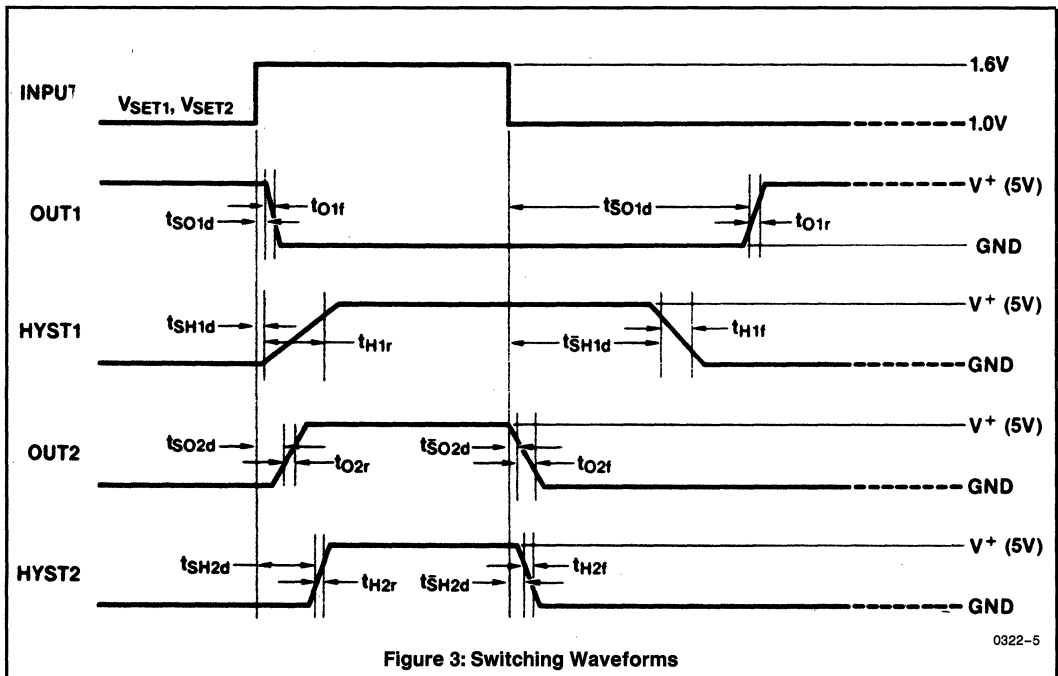
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V+ +0.3V) or less than (GND-0.3V) may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

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NOTE: All typical values have been characterized but are not tested.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	Output Delay Time Input Going HI	V_{SET} Switched from 1.0V to 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		70 80 120 230		μs
t_{SO1d} t_{SH2d} t_{SO2d} t_{SH2d}	Output Delay Time Input Going LO	V_{SET} Switched from 1.6V to 1.0V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		1040 610 70 30		μs
t_{O1r} t_{O2r} t_{H1r} t_{H2r}	Output Rise Times	V_{SET} Switched between 1.0V and 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		120 80 330 25		μs
t_{O1f} t_{O2f} t_{H1f} t_{H2f}	Output Fall Times	V_{SET} Switched between 1.0V and 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$		30 60 180 30		μs



0322-5

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NOTE: All typical values have been characterized but are not tested.

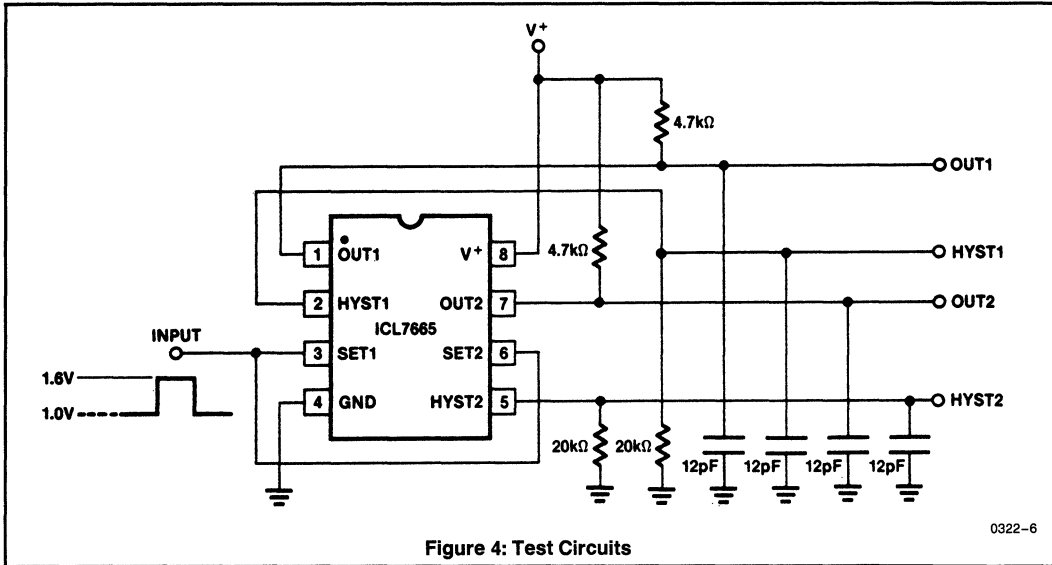


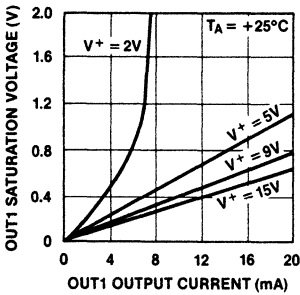
Figure 4: Test Circuits

0322-6

TYPICAL PERFORMANCE CHARACTERISTICS

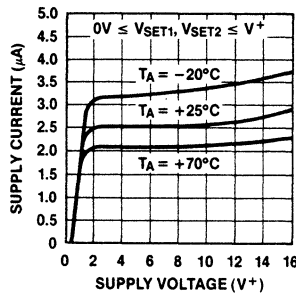
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OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



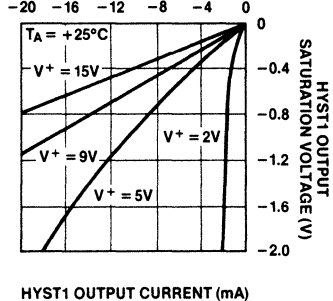
0322-7

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



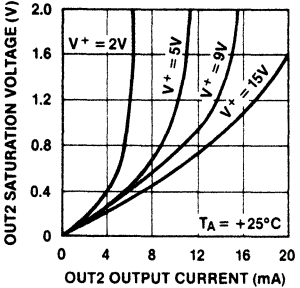
0322-8

HYST1 OUTPUT SATURATION VOLTAGE VS HYST1 OUTPUT CURRENT



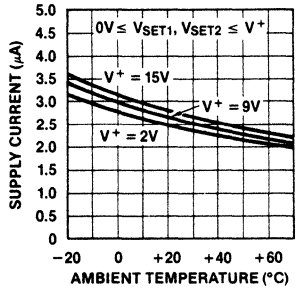
0322-9

OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



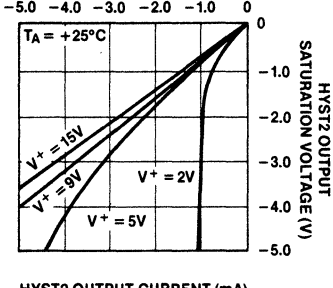
0322-10

SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



0322-11

HYST2 OUTPUT SATURATION VOLTAGE VS HYST2 OUTPUT CURRENT



0322-12

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

As shown in the Functional Diagram, the ICL7665 consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal, so V_{SET1} will generally not quite equal V_{SET2} .

The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

PRECAUTIONS

Junction-isolated CMOS devices like the ICL7665 have an inherent SCR or 4-layer PNP structure distributed

throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low current analog circuits, such as the ICL7665, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed $100V/\mu s$ in such a circuit. A low-impedance capacitor (e.g. $0.05\mu F$ disc ceramic) between the V^+ and GROUND pins of the ICL7665 can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V^+ , the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

APPLICATIONS

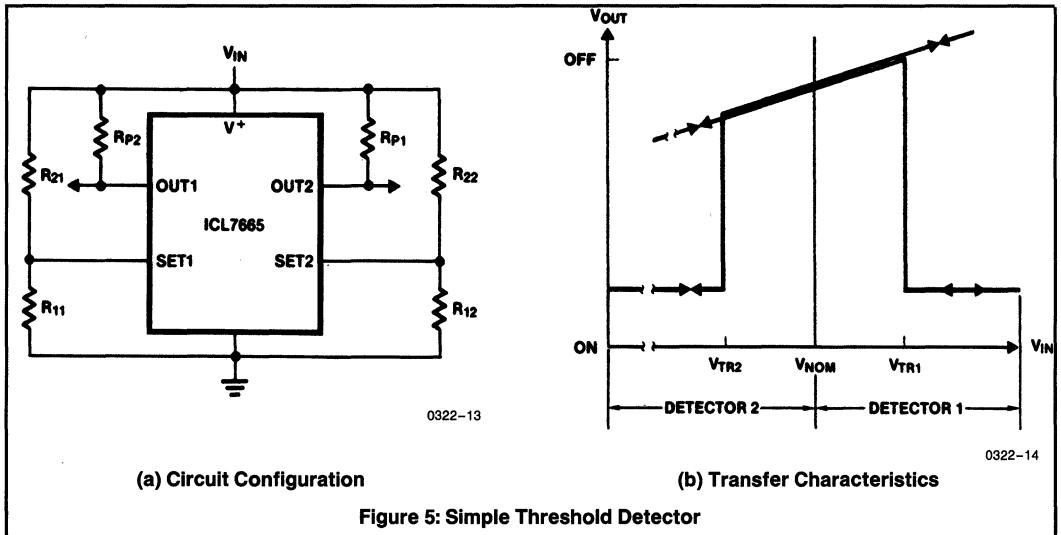


Figure 5: Simple Threshold Detector

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NOTE: All typical values have been characterized but are not tested.

Figure 5 shows the simplest connection of the ICL7665 for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2} . If the voltage rises above V_{NOM} as much as V_{TR1} , OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are, from Figure 1(a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})}; \quad V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value of V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1}$$

and

$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2.}$$

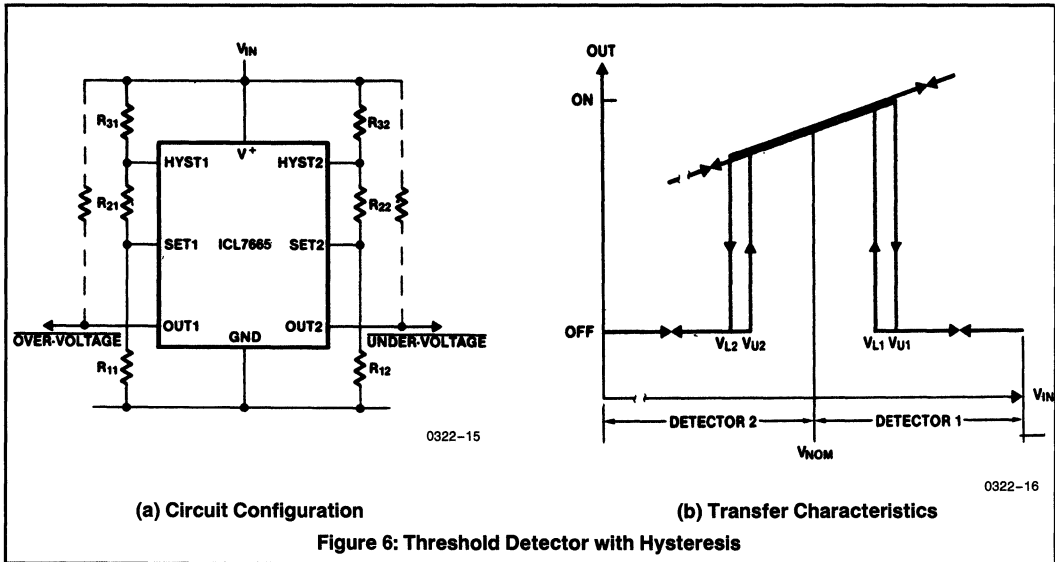
Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF con-

ditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Figure 6(a) shows how to set up such hysteresis, while Figure 6(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n} , R_{2n} and R_{3n} , until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n} , a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 7. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100k Ω .



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NOTE: All typical values have been characterized but are not tested.

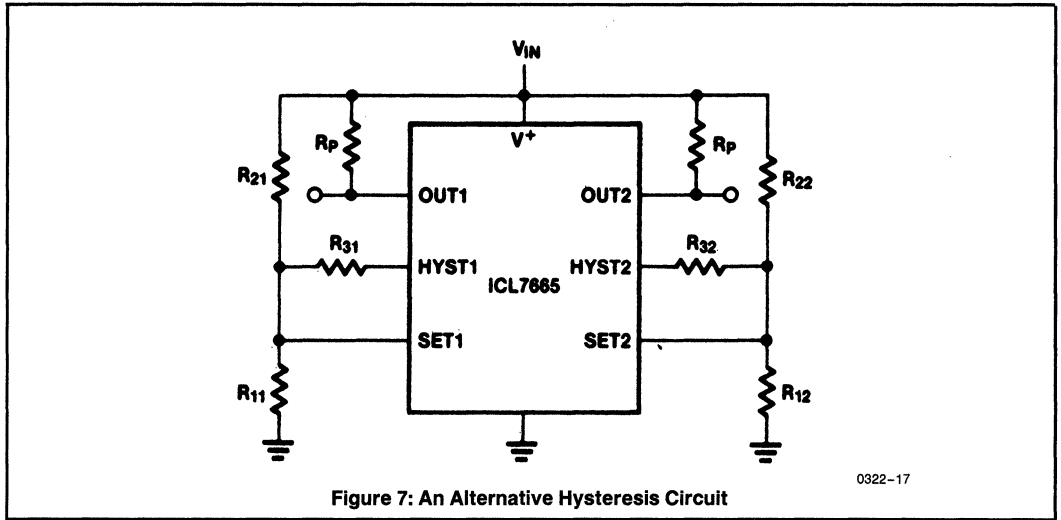


Figure 7: An Alternative Hysteresis Circuit

0322-17

Table 1. Set-Point Equations

<p>a) NO HYSTERESIS</p>	<p>Over-Voltage $V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$</p> <p>Under-Voltage $V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$</p>
<p>b) HYSTERESIS PER FIGURE 6A</p>	<p>Over-Voltage $V_{TRIP} \quad V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$</p> <p>$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$</p> <p>Under-Voltage $V_{TRIP} \quad V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$</p> <p>$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$</p>
<p>c) HYSTERESIS PER FIGURE 7</p>	<p>Over-Voltage $V_{TRIP} \quad V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$</p> <p>$V_{L1} = \frac{R_{11} + \frac{R_{21} R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$</p> <p>$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$</p> <p>Under-Voltage $V_{TRIP} \quad V_{L2} = \frac{R_{12} + \frac{R_{22} R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$</p>

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NOTE: All typical values have been characterized but are not tested.

ICL7665B ADDENDUM TO THE ICL7665 DATASHEET

This Addendum to the standard ICL7665B datasheet describes changes and/or modifications to the DC Operating characteristics applicable to the ICL7665B device. The following table indicates those limits to which the ICL7665B is tested and/or guaranteed operational.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7665BCPA	0 to +70°C	8 Lead MiniDIP
ICL7665BCTV	0 to +70°C	8 Lead TO-99
ICL7665BCJA	0 to +70°C	8-Lead CERDIP
ICL7665BCBA	0 to +70°C	8-Lead S.O.I.C.

ABSOLUTE MAXIMUM RATINGS, ICL7665B

Supply Voltage -0.3V to +12V
 Output Voltages OUT1 and OUT2 (with respect to GND)
 (Note 2) -0.3V to +12V
 Output Voltages HYST1 and HYST2 (with respect to V+)
 (Note 2) +0.3V to -12V
 Input Voltages SET1 and SET2
 (Note 2) (GND -0.3V) to (V+ +0.3V)

Maximum Sink Output Current OUT1 and OUT2 25mA
 Maximum Source Output Current HYST1
 and HYST2 -25mA
 Power Dissipation (Note 1) 200mW
 Operating Temperature Range 0 to +70°C
 Storage Temperature Range -55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS V+ = 5V, TA = +25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V+	Operating Supply Voltage	TA = +25°C 0 ≤ TA ≤ +70°C	1.6 1.8		10 10	V
I+	Supply Current	GND ≤ VSET1, VSET2 ≤ V+ All Outputs Open Circuit V+ = 2V V+ = 9V		2.5 2.6	10 10	μA
VSET1 VSET2	Input Trip Voltage		1.15 1.2	1.3 1.3	1.45 1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of VSET			±200		ppm/°C
$\frac{\Delta V_{SET}}{\Delta V_S}$	Supply Voltage Sensitivity of VSET1, VSET2	ROUT1, ROUT2, RHYST1, RHYST2 = 1MΩ		0.004		%/V
IOLK IHLK	Output Leakage Currents on OUT and HYST	VSET = 0V or VSET ≥ 2V		10 -10	200 -100	nA
IOLK IHLK		V+ = 9V, TA = 70°C V+ = 9V, TA = 70°C			2000 -500	

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NOTE: All typical values have been characterized but are not tested.

DC OPERATING CHARACTERISTICS $V^+ = 5V, T_A = +25^\circ C$, unless otherwise specified. (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{OUT1} V_{OUT1} V_{OUT1}	Output Saturation Voltages	$V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA$		0.2	0.5	V
		$V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA$		0.1	0.3	
		$V^+ = 9V, V_{SET1} = 2V, I_{OUT1} = 2mA$		0.06	0.25	
V_{HYST1} V_{HYST1} V_{HYST1}		$V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = -0.5mA$		-0.15	-0.3	
		$V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = -0.5mA$		-0.05	-0.15	
		$V^+ = 9V, V_{SET1} = 2V, I_{HYST1} = -0.5mA$		-0.02	0.15	
V_{OUT2} V_{OUT2} V_{OUT2}		$V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA$		0.2	0.5	
		$V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA$		0.15	0.3	
		$V^+ = 9V, V_{SET2} = 0V, I_{OUT2} = 2mA$		0.11	0.3	
V_{HYST2} V_{HYST2} V_{HYST2}		$V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = -0.2mA$		-0.25	-0.8	
		$V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = -0.5mA$		-0.43	-1	
		$V^+ = 9V, V_{SET2} = 2V, I_{HYST2} = -0.5mA$		0.35	-1	
I_{SET}	V_{SET} Input Leakage Current	$GND \leq V_{SET} \leq V^+$		0.01	10	nA
ΔV_{SET}	ΔV_{SET} Input for Complete Output Change	$R_{OUT} = 4.7k\Omega, R_{HYST} = 20k\Omega$ $V_{OUTLO} = 1\% V^+, V_{OUTH} = 99\% V^+$		1		mV
$V_{SET1} - V_{SET2}$	Difference in Trip Voltages	$R_{OUT}, R_{HYST} = 1M\Omega$		± 5	± 50	
	Output/Hysteresis Difference	$R_{OUT}, R_{HYST} = 1M\Omega$		± 1		

NOTES: 1. Derate above $\pm 25^\circ C$ ambient temperature at 4mW/ $^\circ C$.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than $(V^+ + 0.3V)$ or less than $(GND - 0.3V)$ may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665B be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to $\pm 0.5mA$ and voltages must not exceed those defined above.

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NOTE: All typical values have been characterized but are not tested.

ICL7665S

CMOS Micropower Over/Under Voltage Detector



GENERAL DESCRIPTION

The ICL7665S Super CMOS Micropower Over/Under Voltage Detector contains two low power, individually programmable voltage detectors on a single CMOS chip. Requiring typically $3\mu\text{A}$ for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors. An internal bandgap-type reference provides an accurate threshold voltage while operating from any supply in the 1.6V to 16V range.

The Intersil ICL7665S, Super Programmable Over/Under Voltage Detector is a direct replacement for the industry standard ICL7665B offering *wider* operating voltage and temperature ranges, *improved* threshold accuracy (ICL7665SA), and temperature coefficient, *guaranteed* maximum supply current, and *ESD protection* in excess of 2000V on all pins. All improvements are highlighted in bold italics in the electrical characteristics section. *All critical parameters are guaranteed over the entire commercial and industrial temperature ranges.*

FEATURES

- Guaranteed $10\mu\text{A}$ Maximum Quiescent Current over Temperature
- Guaranteed Wider Operating Voltage Range over Entire Operating Temperature Range
- 2% Threshold Accuracy (ICL7665SA)
- Dual Comparator with Precision Internal Reference
- 100 ppm/ $^{\circ}\text{C}$ Temperature Coefficient of Threshold Voltage
- Improved Direct Replacement for Industry-Standard ICL7665B and Other Second-Source Devices
- Up to 20mA Output Current Sinking Ability
- Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels
- Enhanced ESD Protection, >2000V

APPLICATIONS

- Pocket Pagers
- Portable Instrumentation
- Charging Systems
- Memory Power Back-Up
- Battery-Operated Systems
- Portable Computers
- Level Detectors

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665SCBA ICL7665SCPA ICL7665SCJA ICL7665SCTV ICL7665SACPA ICL7665SACJA ICL7665SACTV	0°C to $+70^{\circ}\text{C}$	8 Lead SOIC 8 Lead Minidip 8 Lead CERDIP TO-99
ICL7665SIBA ICL7665SIPA ICL7665SIJA ICL7665SITV ICL7665SAIPA ICL7665SAJA ICL7665SAITV	-25°C to $+85^{\circ}\text{C}$	8 Lead SOIC 8 Lead Minidip 8 Lead CERDIP TO-99

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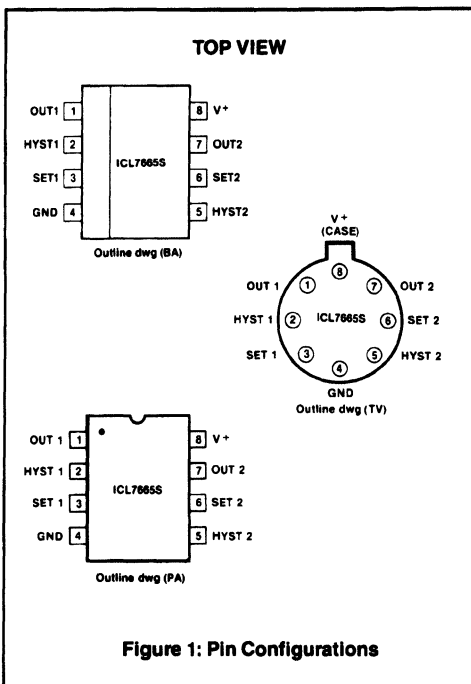


Figure 1: Pin Configurations

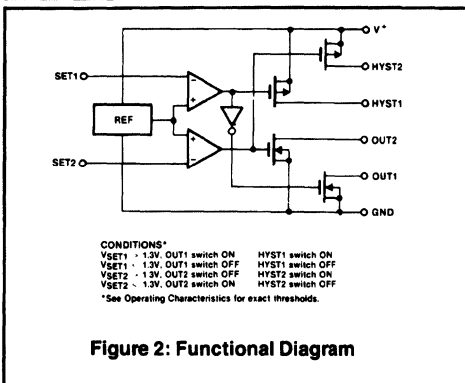


Figure 2: Functional Diagram

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2)	-0.3V to +18V
Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2)	-0.3V to +18V
Output Voltages HYST1 and HYST2 (with respect to V ⁺) (Note 2)	-0.3V to +18V
Input Voltages SET1 and SET2 (Note 2)	(GND-0.3V) to (V ⁺ +0.3V)
Maximum Sink Output OUT1 and OUT2	25mA
Maximum Source Output Current HYST1 and HYST2	-25mA

Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
ICL7665SC	0°C to 70°C
ICL7665SI	-25°C to +85°C
Total Power Dissipation (Note1)	
SOIC	200mW
Minidip	200mW
TO-99 Can	300mW
CERDIP	500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: The specifications below are applicable to both the ICL7665S and ICL7665SA unless otherwise stated.

V⁺ = 5V, T_A = 25°C, Test circuit Figure 3 unless otherwise stated.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V ⁺	Operating Supply Voltage	ICL7665S T _A = 25°C 0°C ≤ T _A ≤ +70°C -25°C ≤ T _A ≤ +85°C ICL7665SA 0°C ≤ T _A ≤ +70°C -25°C ≤ T _A ≤ +85°C	1.6 1.8 1.8		16 16 16	V
I ⁺	Supply Current	GND ≤ V _{SET1} , V _{SET2} ≤ V ⁺ All Outputs Open Circuit 0°C ≤ T _A ≤ +70°C V ⁺ = 2V V ⁺ = 9V V ⁺ = 15V -25°C ≤ T _A ≤ +85°C V ⁺ = 2V V ⁺ = 9V V ⁺ = 15V		2.5 2.6 2.9 2.5 2.6 2.9	10 10 10 10 10 10	μA
V _{SET1} V _{SET2} V _{SET1} V _{SET2}	Input Trip Voltage	ICL7665S ICL7665SA	1.15 1.2	1.3 1.3	1.45 1.4	V
$\frac{\Delta V_{SET}}{\Delta T}$	Temperature Coefficient of V _{SET}	ICL7665S ICL7665SA		200 100		ppm
$\frac{\Delta V_{SET}}{\Delta V_S}$	Supply Voltage Sensitivity of V _{SET1} , V _{SET2}	R _{OUT1} , R _{OUT2} , R _{HYST1} , R _{HYST2} = 1MΩ 2V ≤ V ⁺ ≤ 10V		0.03		%/V
I _{OLK} I _{HLK} I _{OLK} I _{HLK}	Output Leakage Currents of OUT and HYST	V _{SET} = 0V or V _{SET} ≥ 2V V ⁺ = 15V, T _A = 70°C		10 -10	200 -100 2000 -500	nA
V _{OUT1} V _{OUT1} V _{OUT1}	Output Saturation Voltages	V _{SET1} = 2V, I _{OUT1} = 2mA V ⁺ = 2V V ⁺ = 5V V ⁺ = 15V		0.2 0.1 0.06	0.5 0.3 0.2	V

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (cont.): The specifications below are applicable to both the ICL7665S and ICL7665SA unless otherwise stated.
 $V^+ = 5V, T_A = 25^\circ C$, Test circuit Figure 3 unless otherwise stated.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{HYST1} V_{HYST1} V_{HYST1}	Output Saturation Voltages	$V_{SET1} = 2V, I_{HYST1} = -0.5mA$ $V^+ = 2V$ $V^+ = 5V$ $V^+ = 15V$		-0.15 -0.05 -0.02	-0.13 -0.15 -0.10	V V V
V_{OUT2} V_{OUT2} V_{OUT2}	Output Saturation Voltages	$V_{SET2} = 0V, I_{OUT2} = 2mA$ $V^+ = 2V$ $V^+ = 5V$ $V^+ = 15V$		0.2 0.15 0.11	0.5 0.3 0.25	V V V
V_{HYST2} V_{HYST2}	Output Saturation Voltages	$V_{SET2} = 2V$ $V^+ = 2V, I_{HYST2} = -0.2mA$ $V^+ = 5V, I_{HYST2} = -0.5mA$ $V^+ = 15V, I_{HYST2} = -0.5mA$		-0.25 -0.43 -0.35	-0.8 -1.0 -0.8	V V V
I_{SET}	V_{SET} Input Leakage Current	$GND < V_{SET} < V^+$		± 0.01	± 10	nA
ΔV_{SET}	Δ Input for Complete Output Change	$R_{OUT} = 4.7k\Omega, R_{HYST} = 20k\Omega$ $V_{OUTLO} = 1\% V^+, V_{OUTHl} = 99\% V^+$ <i>ICL7665S</i> <i>ICL7665SA</i>		1.0 0.1		mV mV
$V_{SET1} - V_{SET2}$	Difference in Trip Voltages	$R_{OUT}, R_{HYST} = 1M\Omega$		± 5	± 50	mV
	Output/Hysteresis Difference	$R_{OUT}, R_{HYST} = 1M\Omega$ <i>ICL7665S</i> <i>ICL7665SA</i>		± 1 ± 0.1		mV mV

- NOTE 1:** Derate above $\pm 25^\circ C$ ambient temperature at 4mW/ $^\circ C$.
2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than $(V^+ + 0.3V)$ or less than $(GND - 0.3V)$ may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665S be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to $\pm 0.5mA$ and voltages must not exceed those defined above.
3: All significant improvements over the industry-standard ICL7665 are highlighted in bold italics.

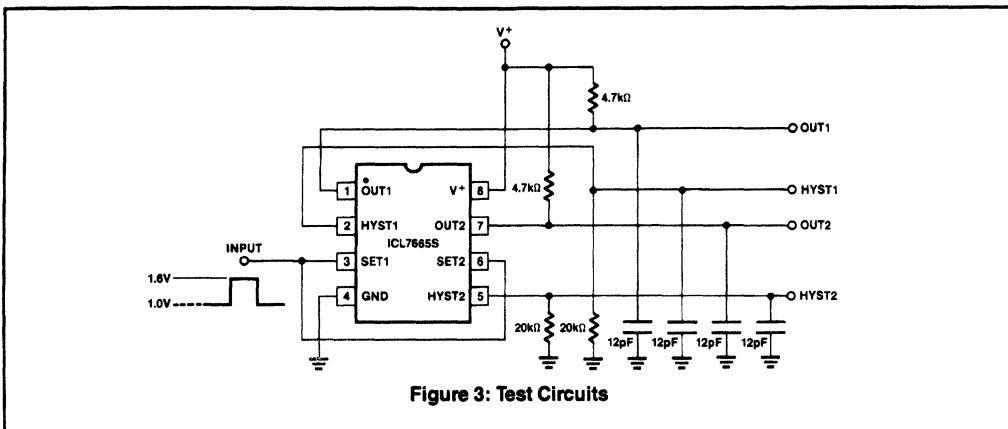


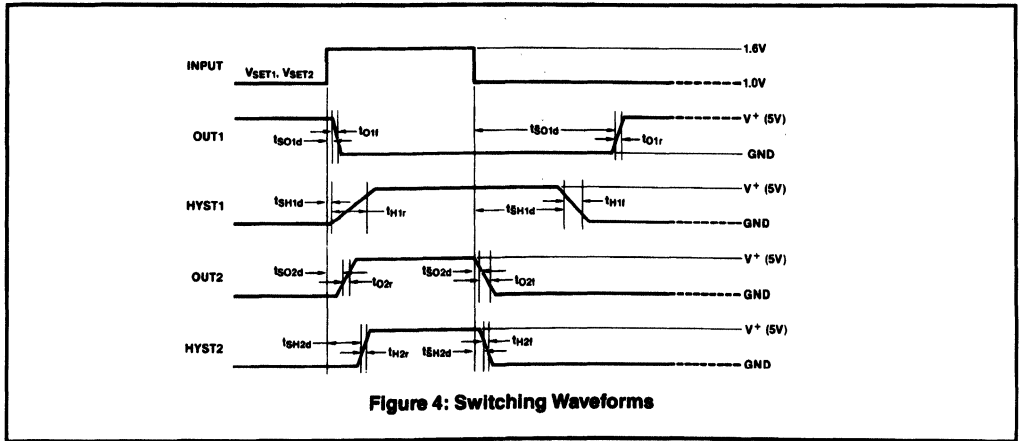
Figure 3: Test Circuits

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NOTE: All typical values have been characterized but are not tested.

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A.C. ELECTRICAL CHARACTERISTICS

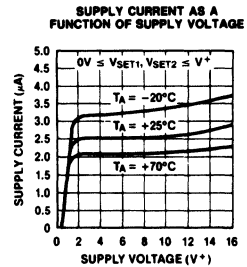
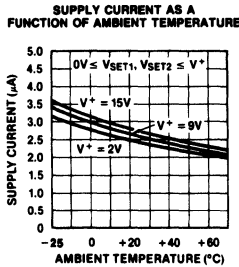
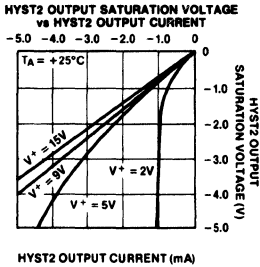
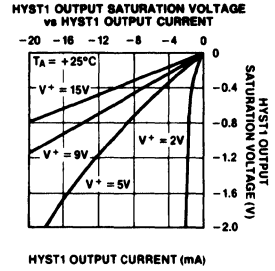
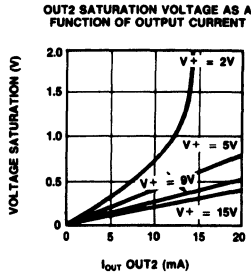
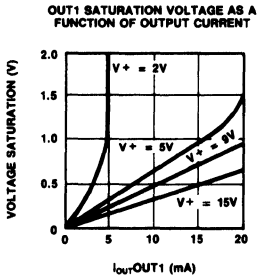
Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	Output Delay Times Input Going HI	V_{SET} Switched between 1.0V to 1.6V $R_{OUT} = 4.7k\Omega, C_L = 12pF$ $R_{HYST} = 20k\Omega, C_L = 12pF$		85 90 55 55		μs
t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	Input Going LO	V_{SET} Switched between 1.6V to 1.0V $R_{OUT} = 4.7k\Omega, C_L = 12pF$ $R_{HYST} = 20k\Omega, C_L = 12pF$		75 80 60 60		μs
t_{O1r} t_{O2r} t_{H1r} t_{H2r}	Output Rise Times	V_{SET} Switched between 1.0V to 1.6V $R_{OUT} = 4.7k\Omega, C_L = 12pF$ $R_{HYST} = 20k\Omega, C_L = 12pF$		0.6 0.8 7.5 0.7		μs
t_{O1f} t_{O2f} t_{H1f} t_{H2f}	Output Fall Times	V_{SET} Switched between 1.0V to 1.6V $R_{OUT} = 4.7k\Omega, C_L = 12pF$ $R_{HYST} = 20k\Omega, C_L = 12pF$		0.6 0.7 4 1.8		μs

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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

As shown in the Functional Diagram, Figure 2, the ICL7665S consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal so V_{SET1} will generally not quite equal V_{SET2} .

The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

PRECAUTIONS

Junction-isolated CMOS devices like the ICL7665S have an inherent SCR or 4-layer PNP structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very low current analog circuits, such as the ICL7665S, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed $100V/\mu s$ in such a circuit. A low-impedance capacitor (e.g. 0.05 μF disc ceramic) between the V⁺ and GrouND pins of the ICL7665S can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V⁺, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

SIMPLE THRESHOLD DETECTOR

Figure 5 shows the simplest connection of the ICL7665S for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2} . If the voltage rises above V_{NOM} as much as V_{TR1} , OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are from Figure 5 (a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})}; V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1}$$

and

$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

THRESHOLD DETECTOR WITH HYSTERESIS

Figure 6(a) shows how to set up such hysteresis, while Figure 6(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n} , R_{2n} , and R_{3n} , until the trip point is reached. As this value is

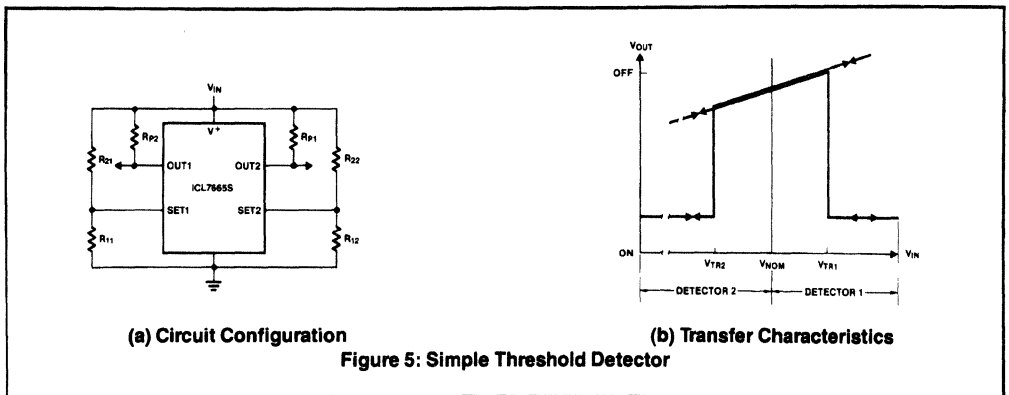
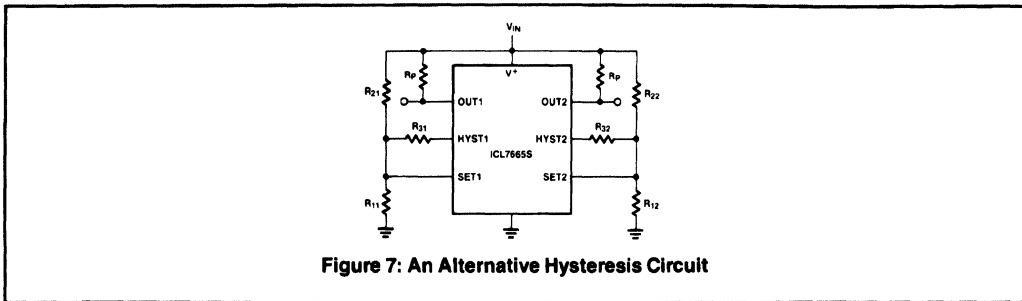
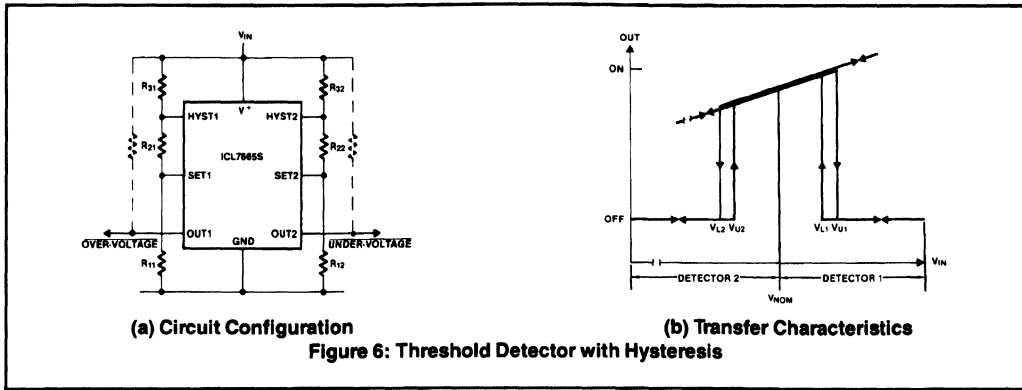


Figure 5: Simple Threshold Detector

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APPLICATIONS



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Table 1: Set-Point Equations

a) NO HYSTERESIS	
Over-Voltage V_{TRIP}	$= \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}	$= \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
b) HYSTERESIS PER FIGURE 6A	
Over-Voltage V_{TRIP}	$V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$
Under-Voltage V_{TRIP}	$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Under-Voltage V_{TRIP}	$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$
Under-Voltage V_{TRIP}	$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$

c) HYSTERESIS PER FIGURE 7	
Over-Voltage V_{TRIP}	$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Under-Voltage V_{TRIP}	$V_{L1} = \frac{R_{11} + \frac{R_{21}R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}	$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
Under-Voltage V_{TRIP}	$V_{L2} = \frac{R_{12} + \frac{R_{22}R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$

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THRESHOLD DETECTOR WITH HYSTERESIS (cont.)

passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n} , a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 7. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100k Ω .

APPLICATIONS

Single Supply Fault Monitor

Figure 8 shows an over/under-voltage fault monitor for a single supply. The over-voltage trip point is centered around 5.5V and the under-voltage trip point is centered around 4.5V. Both have

some hysteresis to prevent erratic output ON and OFF conditions. The two outputs are connected in a wired OR configuration with a pullup resistor to generate a power OK signal.

Multiple Supply Fault Monitor

The ICL7665S can simultaneously monitor several supplies when connected as shown in Figure 9. The resistors are chosen such that the sum of the currents through R_{21A} , R_{21B} , and R_{31} is equal to the current through R_{11} when the two input voltages are at the desired low voltage detection point. The current through R_{11} at this point is equal to $1.3V/R_{11}$. The voltage at the V_{SET} input depends on the voltage of both supplies being monitored. The trip voltage of one supply while the other supply is at the nominal voltage will be different than the trip voltage when both supplies are below their nominal voltages.

The other side of the ICL7665S can be used to detect the absence of negative supplies. The trip points for OUT1 depend on both the negative supply voltages and the actual voltage of the +5V supply.

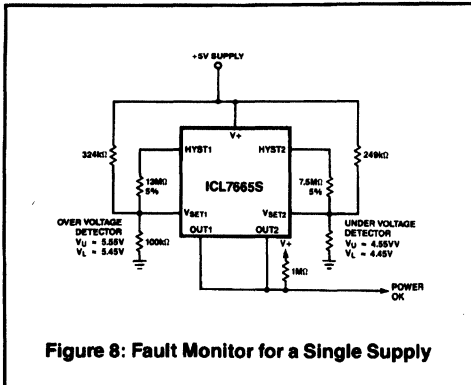


Figure 8: Fault Monitor for a Single Supply

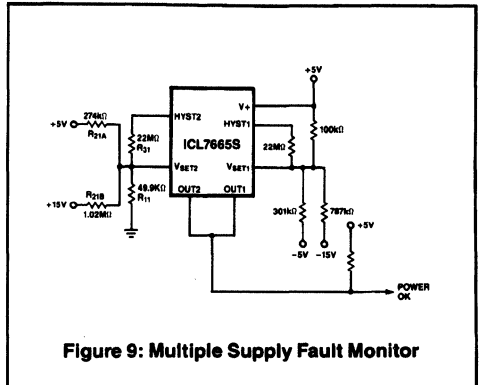


Figure 9: Multiple Supply Fault Monitor

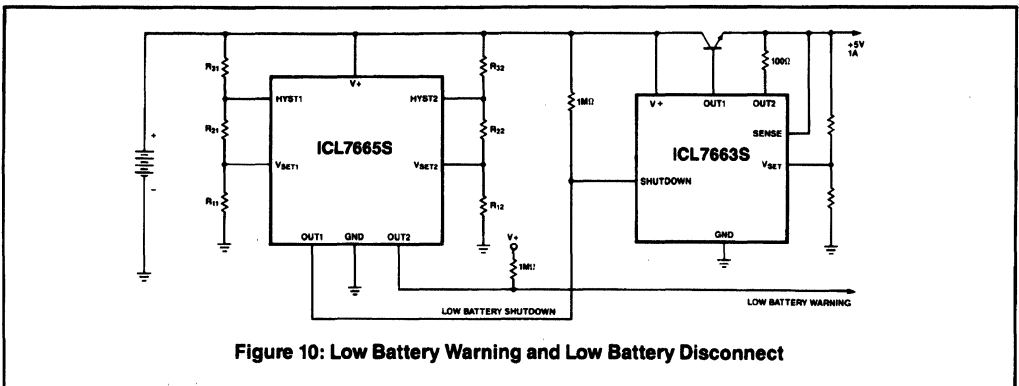


Figure 10: Low Battery Warning and Low Battery Disconnect

Combination Low Battery Warning and Low Battery Disconnect

When using rechargeable batteries in a system, it is important to keep the batteries from being overdischarged. The circuit shown in Figure 10 provides a low battery warning and also disconnects the low battery from the rest of the system to prevent damage to the battery. OUT1 is used to shutdown the ICL7663S when the battery voltage drops to the value where the load should be disconnected. As long as V_{SET1} is greater than 1.3V, OUT1 is low, but when V_{SET1} drops below 1.3V, OUT1 goes high, shutting off the ICL7663S. OUT2 is used for low battery warning. When V_{SET2} is greater than 1.3V, OUT2 is high and the low battery warning is on. When V_{SET2} drops below 1.3V, OUT2 is low and the low battery warning goes off. The trip voltage for low battery warning can be set higher than the trip voltage for shutdown to give advance low battery warning before the battery is disconnected.

Power Fail Warning and Powerup/Powerdown Reset

Figure 11 shows a power fail warning circuit with powerup/powerdown reset. When the unregulated DC input is above the trip point, OUT1 is low. When the DC input drops below the trip point, OUT1 shuts OFF and the power fail warning goes high. The voltage on the input of the 7805 decays at a rate of $1/OUT/C$. Since the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will provide a certain amount of warning before the 5V output begins to drop.

The ICL7665S OUT2 is used to prevent a microprocessor from writing spurious data to a CMOS battery backup memory by causing OUT2 to go low when the 7805 5V output drops below the ICL7665S trip point.

Simple High/Low Temperature Alarm

Figure 12 illustrates a simple high/low temperature alarm which uses the ICL7665S with an NPN transistor. The voltage at the top of R_1 is determined by the V_{BE} of the transistor and the position of R_1 's wiper arm. This voltage has a negative temperature coefficient. R_1 is adjusted so that V_{SET2} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the high temperature alarm. When this occurs, OUT2

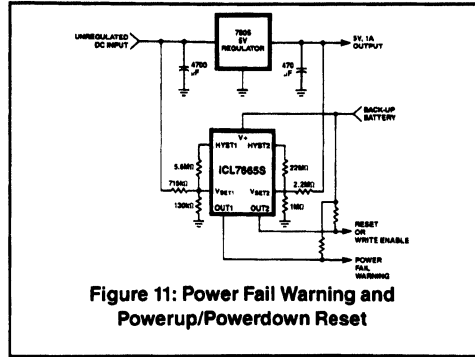


Figure 11: Power Fail Warning and Powerup/Powerdown Reset

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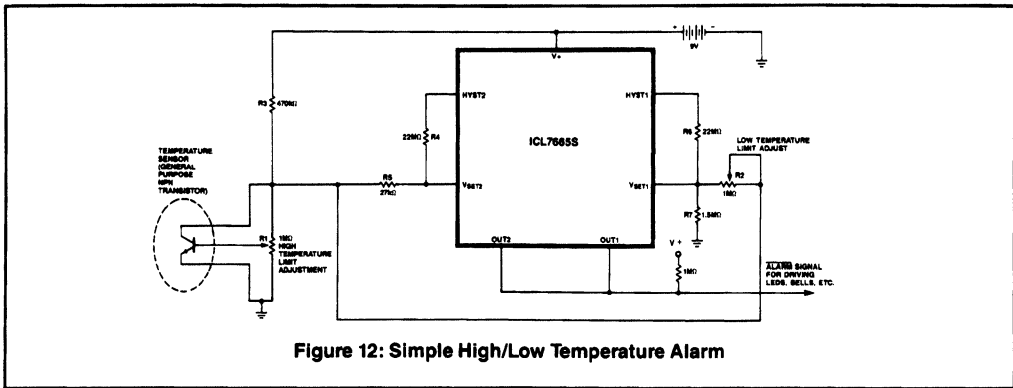


Figure 12: Simple High/Low Temperature Alarm

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NOTE: All typical values have been characterized but are not tested.

goes low. R_2 is adjusted so that V_{SET1} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the low temperature alarm. When the temperature drops below this limit, OUT1 goes low.

AC Power Fail and Brownout Detector

Figure 13 shows a circuit that detects AC undervoltage by monitoring the secondary side of the transformer. The capacitor, C_1 , is charged through R_1 when OUT1 is OFF. With a normal 110 VAC input to the transformer, OUT1 will discharge C_1 once every cycle, approximately every 16.7 ms. When the AC input voltage is reduced, OUT1 will stay OFF, so that C_1 does not discharge. When the voltage on C_1 reaches 1.3V, OUT2 turns OFF and the power fail warning goes high. The time constant, R_1C_1 , is chosen such that it takes longer than 16.7 ms to charge C_1 1.3V.

For a more comprehensive AC power fail circuit, refer to Inter-sil's new ICL7677 monolithic power fail detector.

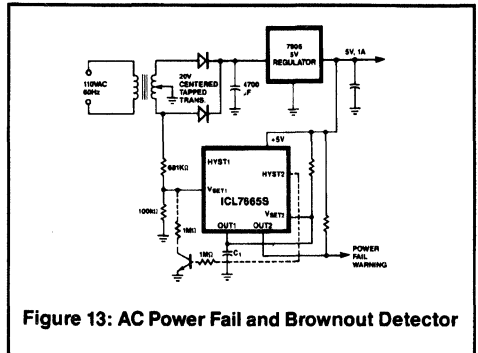


Figure 13: AC Power Fail and Brownout Detector

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ICL7667

Dual Power MOSFET Driver



ICL7667

GENERAL DESCRIPTION

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control IC's.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7667CBA ICL7667CPA ICL7667CJA ICL7667CTV	0°C to +70°C	8-Pin SOIC 8-Pin Plastic 8-Pin Cerdip TO-99 Can
ICL7667MTV* ICL7667MJA*	-55°C to +125°C	TO-99 Can 8-Pin Cerdip

*Add /883B to Part Number for 883B processing.

FEATURES

- Fast Rise and Fall Times
— 30ns With 1000pF Load
- Wide Supply Voltage Range
— $V_{CC} = 4.5$ to 15V
- Low Power Consumption
— 4mW With Inputs Low
— 120mW With Inputs High
- TTL/CMOS Input Compatible Power Driver
— $R_{OUT} = 7\Omega$ typ
- Direct Interface With Common PWM Control IC's
- Pin Equivalent to DS0026/DS0056; TSC426

TYPICAL APPLICATIONS

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

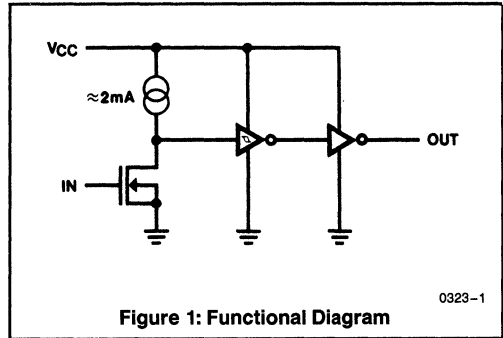


Figure 1: Functional Diagram

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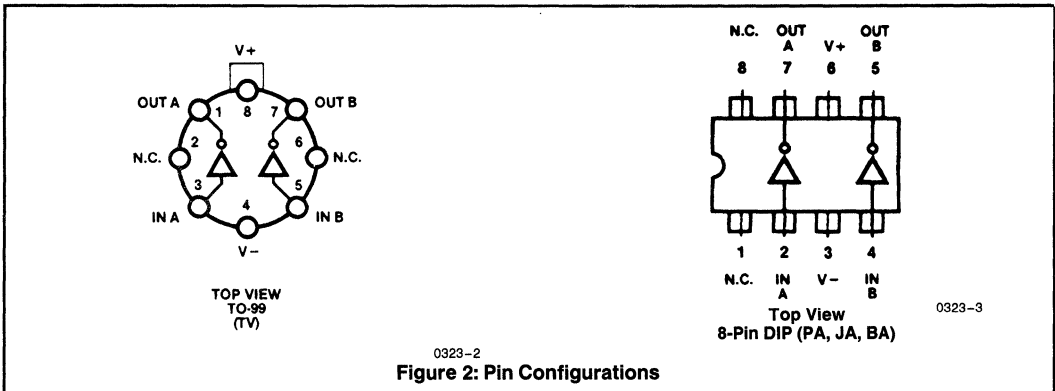


Figure 2: Pin Configurations

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ to V^- 15V
 Input Voltage ($V^- - 0.3V$) to ($V^+ + 0.3V$)
 Package Dissipation, $T_A = 25^\circ C$ 500mW
 Linear Derating Factors
 TO-99 Plastic Cerdip
 6.7mW/ $^\circ C$ 5.6mW/ $^\circ C$ 6.7mW/ $^\circ C$
 above $50^\circ C$ above $36^\circ C$ above $50^\circ C$

Storage Temperature $-65^\circ C$ to $+150^\circ C$
 Operating Temperature Range
 ICL7667C $0^\circ C$ to $+70^\circ C$
 ICL7667M $-55^\circ C$ to $+125^\circ C$
 Lead Temperature (Soldering, 10sec) $300^\circ C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (STATIC)

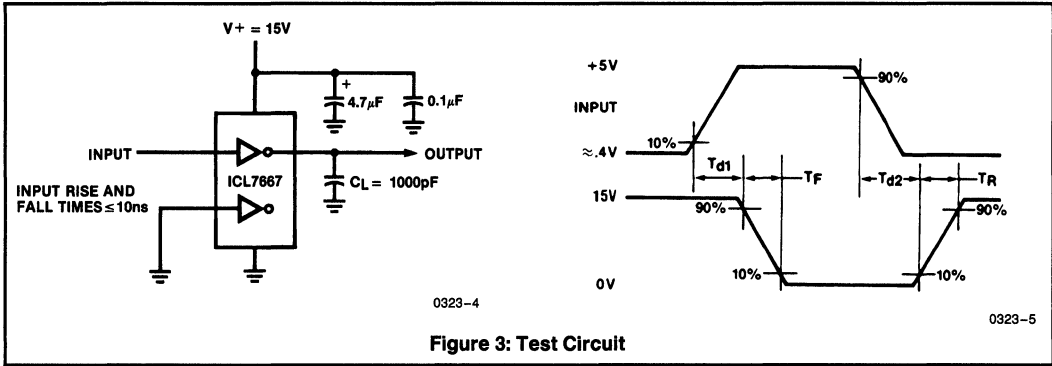
Symbol	Parameter	Test Conditions	ICL7667C,M			ICL7667M			Units
			$T_A = 25^\circ C$			$-55^\circ C \leq T_A \leq +125^\circ C$			
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Logic 1 Input Voltage	$V_{CC} = 4.5V$	2.0			2.0			V
V_{IH}	Logic 1 Input Voltage	$V_{CC} = 15V$	2.0			2.0			V
V_{IL}	Logic 0 Input Voltage	$V_{CC} = 4.5V$			0.8			0.5	V
V_{IL}	Logic 0 Input Voltage	$V_{CC} = 15V$			0.8			0.8	V
I_{IL}	Input Current	$V_{CC} = 15V, V_{IN} = 0V$ and $15V$	-0.1		0.1	-0.1		0.1	μA
V_{OH}	Output Voltage High	$V_{CC} = 4.5V$ and $15V$	$V_{CC} - 0.05$	V_{CC}		$V_{CC} - 0.1$			V
V_{OL}	Output Voltage Low	$V_{CC} = 4.5V$ and $15V$		0	0.05			0.1	V
R_{OUT}	Output Resistance	$V_{IN} = V_{IL}, I_{OUT} = -10 mA,$ $V_{CC} = 15V$		7	10			12	Ω
R_{OUT}	Output Resistance	$V_{IN} = V_{IH}, I_{OUT} = 10mA,$ $V_{CC} = 15V$		8	12			13	Ω
I_{CC}	Power Supply Current	$V_{CC} = 15V, V_{IN} = 3V$ both inputs		5	7			8	mA
I_{CC}	Power Supply Current	$V_{CC} = 15V, V_{IN} = 0V$ both inputs		150	400			400	μA

ELECTRICAL CHARACTERISTICS (DYNAMIC)

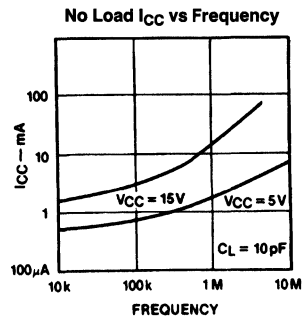
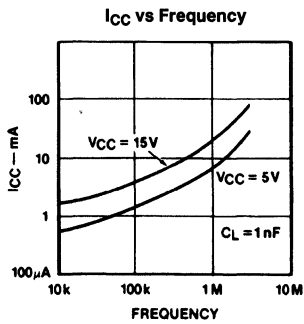
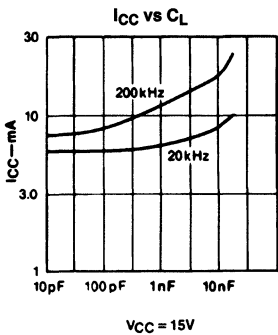
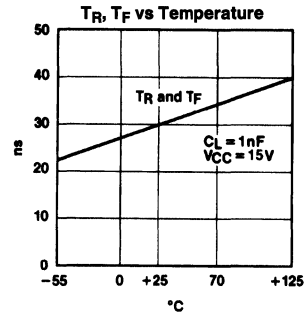
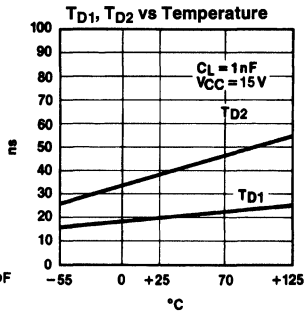
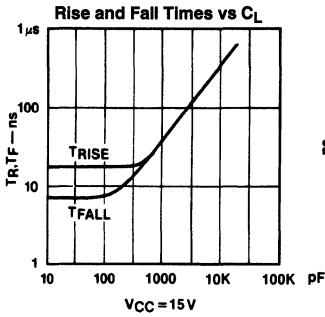
Symbol	Parameter	Test Conditions	ICL7667C,M			ICL7667M			Units
			$T_A = 25^\circ C$			$-55^\circ C \leq T_A \leq +125^\circ C$			
			Min	Typ	Max	Min	Typ	Max	
T_{D2}	Delay Time	Figure 3		35	50			60	ns
T_R	Rise Time	Figure 3		20	30			40	ns
T_F	Fall Time	Figure 3		20	30			40	ns
T_{D1}	Delay Time	Figure 3		20	30			40	ns

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Typical Performance Characteristics



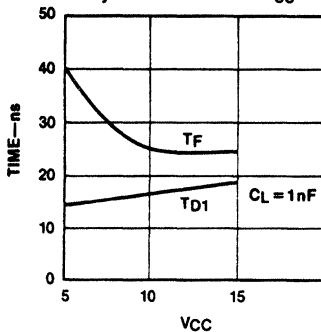
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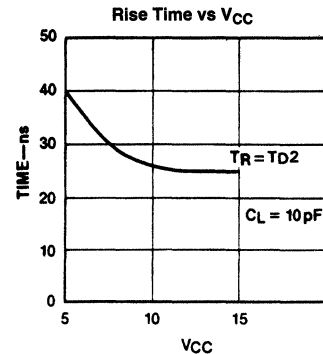
NOTE: All typical values have been characterized but are not tested.

Typical Performance Characteristics (Continued)

Delay and Fall Times vs V_{CC}



0923-12



0923-13

DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOS-FETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at $V_{CC}=15V$, the propagation delays and specifications are almost independent of V_{CC} .

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

INPUT STAGE

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V_{CC} voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5 - 15V V_{CC} range. Being CMOS, the inputs draw less than 1 μ A of current over the entire input voltage range of ground to V_{CC} . The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50 - 100mV at the input, is generated by positive feedback around the second stage.

OUTPUT STAGE

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V_{CC} . At $V_{CC}=15V$, the output impedance of the inverter is typically 7 Ω . The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal

power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1 μ s.

APPLICATION NOTES

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

GROUNDING

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

BYPASSING

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7 μ F tantalum capacitor in parallel with a low inductance 0.1 μ F capacitor is usually sufficient bypassing.

OUTPUT DAMPING

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

- 1) Reduce inductance by making printed circuit board traces as short as possible.
- 2) Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
- 3) Use a 10 to 30 Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
- 4) Use good bypassing techniques to prevent supply voltage ringing.

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NOTE: All typical values have been characterized but are not tested.

POWER DISSIPATION

The power dissipation of the ICL7667 has three main components:

- 1) Input inverter current loss
- 2) Output stage crossover current loss
- 3) Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.2mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

Where C = Load Capacitance

f = Frequency

In cases where the load is a power MOSFET and the gate drive requirements are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_G V_{CC} f$$

Where Q_G = Charge required to switch the gate, in Coulombs.

f = Frequency

POWER MOS DRIVER CIRCUITS POWER MOS DRIVER REQUIREMENTS

Because it has a very high peak current output, the ICL7667 excels at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 4 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and

is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

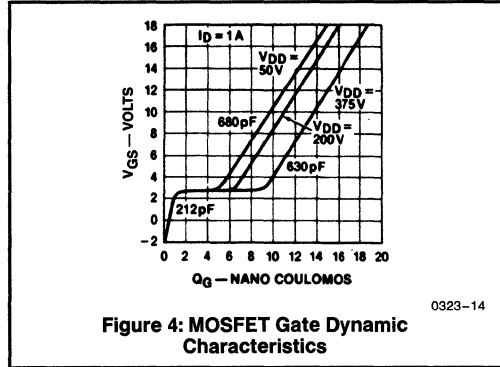


Figure 4: MOSFET Gate Dynamic Characteristics

DIRECT DRIVE OF MOSFETS

Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speed-up capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

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TRANSFORMER COUPLED DRIVE OF MOSFETS

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 6 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low outputs can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

BUFFERED DRIVERS FOR MULTIPLE MOSFETS

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{gs} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

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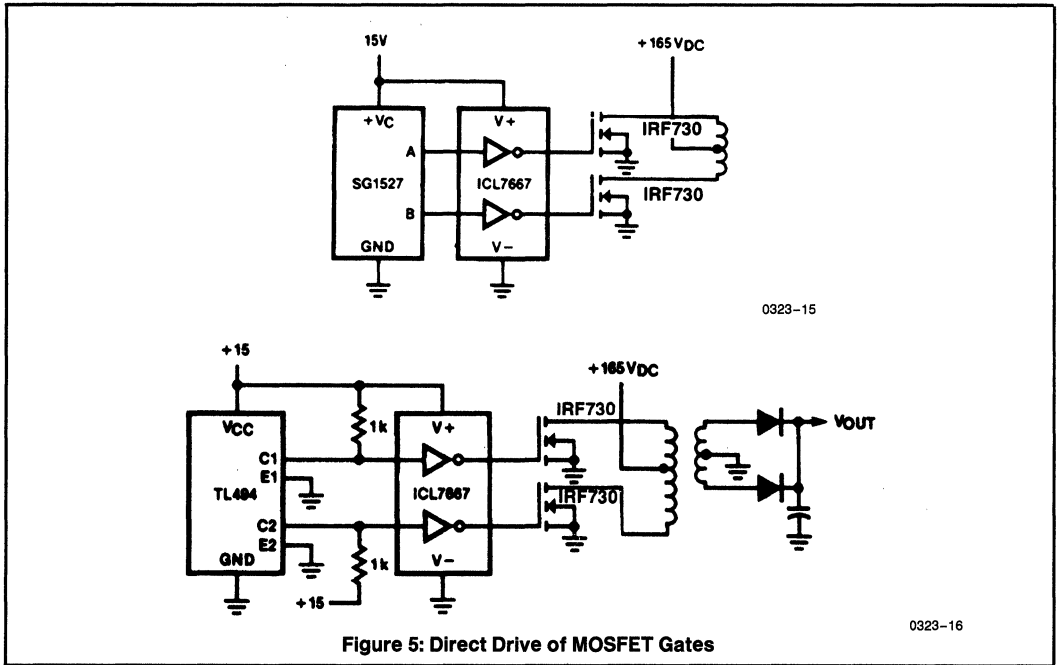


Figure 5: Direct Drive of MOSFET Gates

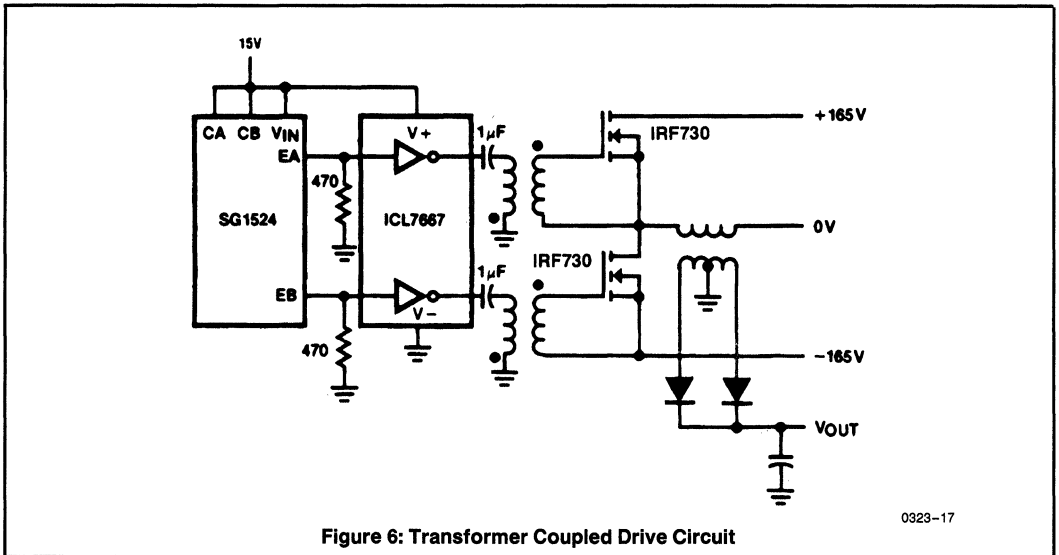


Figure 6: Transformer Coupled Drive Circuit

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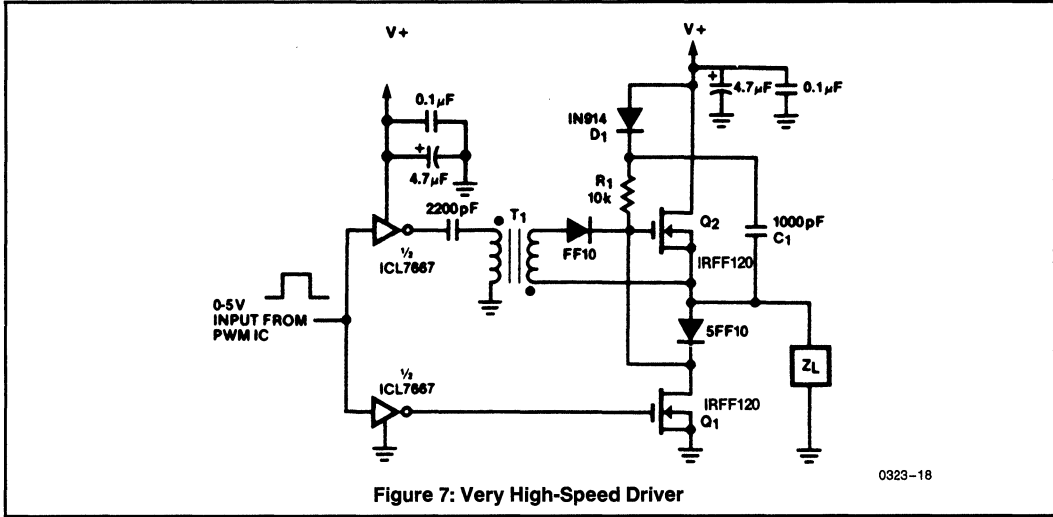


Figure 7: Very High-Speed Driver

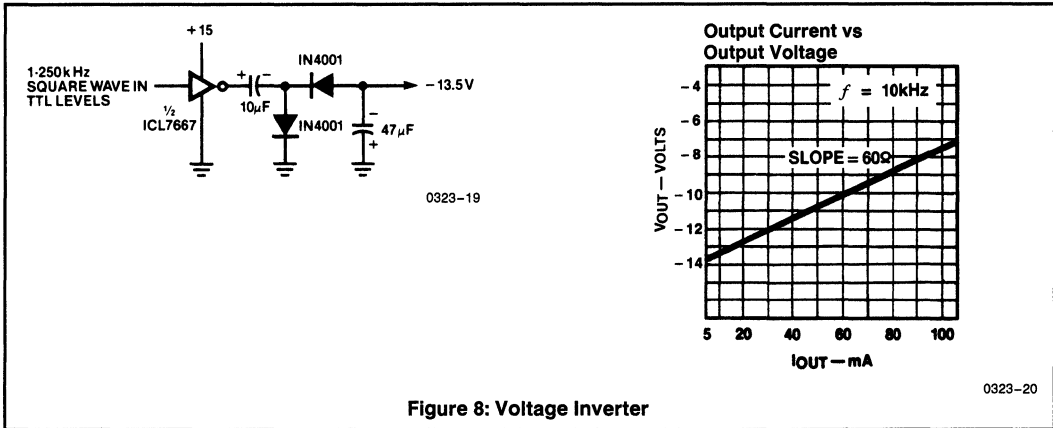


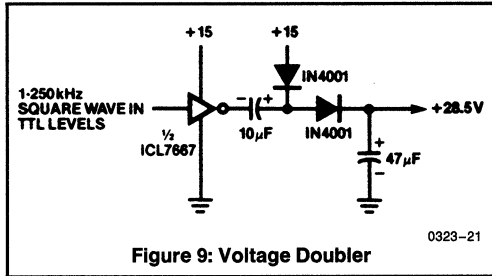
Figure 8: Voltage Inverter

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OTHER APPLICATIONS

RELAY AND LAMP DRIVERS

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

CHARGE PUMP OR VOLTAGE INVERTERS AND DOUBLERS

The low output impedance and wide V_{CC} range of the ICL7667 make it well suited for charge pump circuits. Figure

8 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 9, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

CLOCK DRIVER

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

ICL7673

Automatic Battery Back-up Switch



ICL7673

GENERAL DESCRIPTION

The Intersil ICL7673 is a monolithic CMOS battery back-up circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

The ICL7673 is available in either an 8-pin plastic minidip package or a TO-99 metal can.

FEATURES

- Automatically Connects Output to The Greater Of Either Input Supply Voltage
- If Main Power to External Equipment Is Lost, Circuit Will Automatically Connect Battery Backup
- Reconnects Main Power When Restored
- Logic Indicator Signaling Status Of Main Power
- Low Impedance Connection Switches
- Low Internal Power Consumption
- Wide Supply Range: 2.5 to 15 Volts
- Low Leakage Between Inputs
- External Transistors May Be Added If Very Large Currents Need to Be Switched

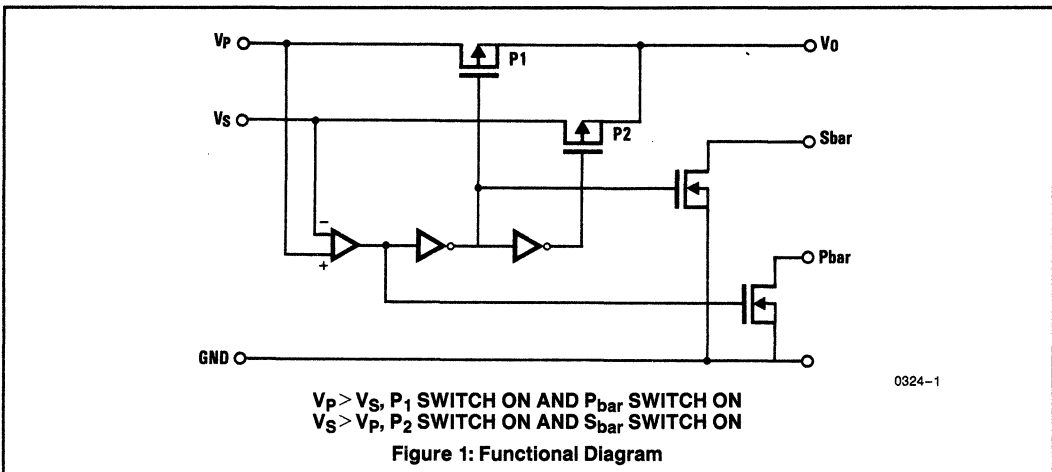
APPLICATIONS

- On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs
- Over/Under Voltage Detector
- Peak Voltage Detector
- Other Uses:
 - Portable Instruments, Portable Telephones, Line Operated Equipment

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ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7673CPA	0°C to +70°C	8-pin minidip
ICL7673CBA	0°C to +70°C	8-pin SOIC
ICL7673ITV	-25°C to +85°C	8-pin TO-99



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ABSOLUTE MAXIMUM RATINGS

Input Supply (V_P or V_S) Voltage	-0.3 to +18V
Output Voltages P_{bar} and S_{bar}	-0.3 to +18V
Peak Current	
Input V_P (@ $V_P=5V$) (note 1)	38mA
Input V_S (@ $V_S=3V$)	30mA
P_{bar} or S_{bar}	150mA
Continuous Current	
Input V_P (@ $V_P=5V$) (note 1)	38mA
Input V_S (@ $V_S=3V$)	30mA
P_{bar} or S_{bar}	50mA

Package Dissipation 300mW

Linear Derating Factors

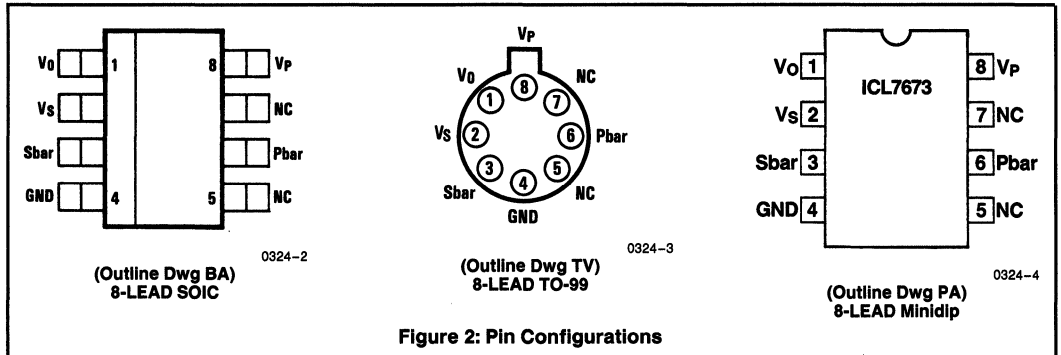
TO-99	PLASTIC
5.7mW/°C	6.1mW/°C
above 50°C	above 36°C

Operating Temperature Range:

ICL7673C	0°C to +70°C
ICL7673I	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1. Derate above 25°C by 0.38mA/°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_P	INPUT VOLTAGE	$V_S = 0$ volts $I_{load} = 0mA$	2.5	-	15	V
V_S		$V_P = 0$ volts $I_{load} = 0mA$	2.5	-	15	
I^+	QUIESCENT SUPPLY CURRENT	$V_P = 0$ volts $V_S = 3$ volts $I_{load} = 0mA$	-	1.5	5	μA
$R_{ds(on)P1}$	SWITCH RESISTANCE P1 (NOTE 2)	$V_P = 5$ volts $V_S = 3$ volts $I_{load} = 15mA$	-	8	15	Ω
		@ T _A = 85°C	-	16	-	
		$V_P = 9$ volts $V_S = 3$ volts $I_{load} = 15mA$	-	6	-	Ω
		$V_P = 12$ volts $V_S = 3$ volts $I_{load} = 15mA$	-	5	-	Ω

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$T_{C(P1)}$	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P1	$V_P = 5$ volts $V_S = 3$ volts $I_{load} = 15\text{mA}$	-	0.5	-	%/ $^\circ\text{C}$
$R_{ds(on)P2}$	SWITCH RESISTANCE P2 (NOTE 2)	$V_P = 0$ volts $V_S = 3$ volts $I_{load} = 1\text{mA}$	-	40	100	Ω
		@ $T_A = 85^\circ\text{C}$	-	60	-	
		$V_P = 0$ volts $V_S = 5$ volts $I_{load} = 1\text{mA}$	-	26	-	Ω
		$V_P = 0$ volts $V_S = 9$ volts $I_{load} = 1\text{mA}$	-	16	-	Ω
$T_{C(P2)}$	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P2	$V_P = 0$ volts $V_S = 3$ volts $I_{load} = 1\text{mA}$	-	0.7	-	%/ $^\circ\text{C}$
$I_{L(PS)}$	LEAKAGE CURRENT (V_P to V_S)	$V_P = 5$ volts $V_S = 3$ volts $I_{load} = 10\text{mA}$	-	0.01	20	nA
		@ $T_A = 85^\circ\text{C}$	-	35	-	
$I_{L(SP)}$	LEAKAGE CURRENT (V_S to V_P)	$V_P = 0$ volts $V_S = 3$ volts $I_{load} = 1\text{mA}$	-	0.01	50	nA
		@ $T_A = 85^\circ\text{C}$	-	120	-	
$V_{O Pbar}$	OPEN DRAIN OUTPUT SATURATION VOLTAGES	$V_P = 5$ volts $V_S = 3$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	-	85	400	mV
		@ $T_A = 85^\circ\text{C}$	-	120	-	
		$V_P = 9$ volts $V_S = 3$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	-	50	-	mV
		$V_P = 12$ volts $V_S = 3$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	-	40	-	mV
$V_{O Sbar}$		$V_P = 0$ volts $V_S = 3$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	-	150	400	mV
		@ $T_A = 85^\circ\text{C}$	-	210	-	
		$V_P = 0$ volts $V_S = 5$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	-	85	-	mV
		$V_P = 0$ volts $V_S = 9$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	-	50	-	mV

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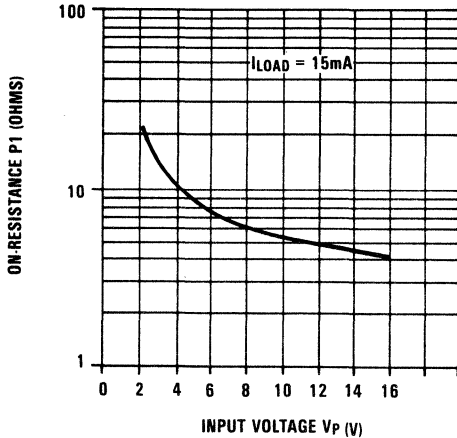
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$I_{L\ Pbar}$	OUTPUT LEAKAGE CURRENTS OF Pbar AND Sbar	$V_P = 0$ volts $V_S = 15$ volts $I_{load} = 0\text{mA}$	-	50	500	nA
		@ $T_A = 85^\circ\text{C}$	-	900	-	
$I_{L\ Sbar}$		$V_P = 15$ volts $V_S = 0$ volts $I_{load} = 0\text{mA}$	-	50	500	nA
		@ $T_A = 85^\circ\text{C}$	-	900	-	
$V_P - V_S$	SWITCHOVER UNCERTAINTY FOR COMPLETE SWITCHING OF INPUTS AND OPEN DRAIN OUTPUTS.	$V_S = 3$ volts $I_{sink} = 3.2\text{mA}$ $I_{load} = 0\text{mA}$	9d		0	V

NOTE 2. The minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

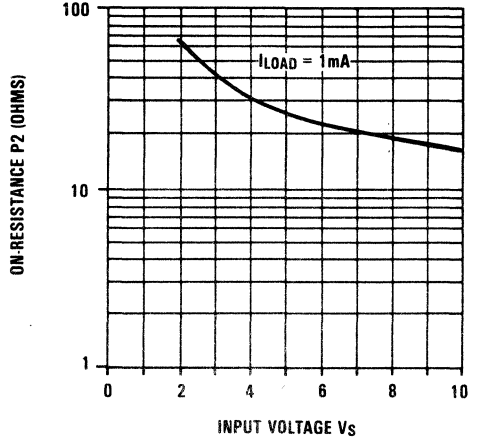
TYPICAL PERFORMANCE CHARACTERISTICS

ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V_P



0324-5

ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V_S



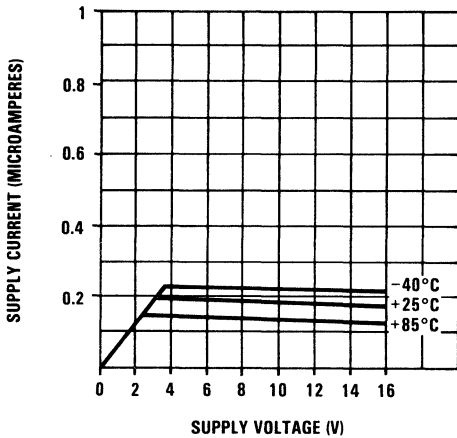
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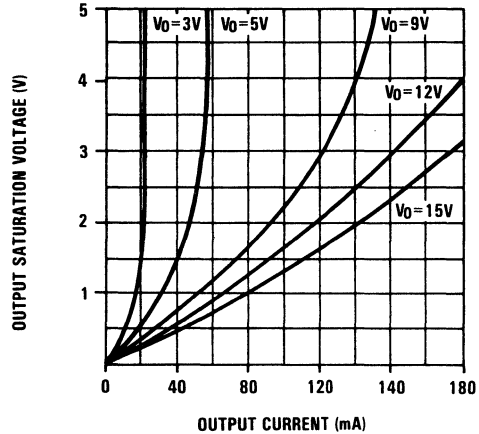
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



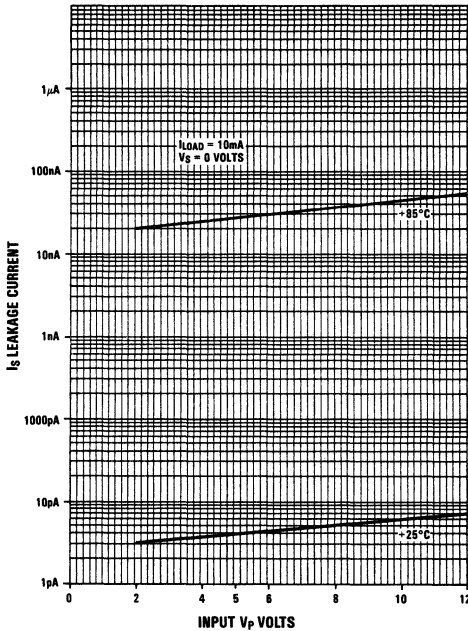
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Pbar OR Sbar SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



0324-8

IS LEAKAGE CURRENT VP TO VS AS A FUNCTION OF INPUT VOLTAGE



0324-9

DETAILED DESCRIPTION

As shown in the functional diagram (Figure 1), the ICL7673 includes a comparator which senses the input voltages V_P and V_S . The output of the comparator drives the first inverter and the open-drain N-channel transistor P_{bar} . The first inverter drives a large P-channel switch, P1, a second inverter, and another open-drain N-channel transistor, S_{bar} . The second inverter drives another large P-channel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V_P and V_S must not be allowed to float, and, the difference in the two supplies must be greater than 50 millivolts. The leakage current through the reverse biased parasitic diode of switch P2 is very low.

OUTPUT VOLTAGE

The output operating voltage range is 2.5 to 15 volts. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V_O . The ON-resistance of the P-channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5 volts, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50 microseconds.

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NOTE: All typical values have been characterized but are not tested.

INPUT VOLTAGE

The input operating voltage range for V_P or V_S is 2.5 to 15 volts. The input supply voltage (V_P or V_S) slew rate should be limited to 2 volts per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a $0.047\mu\text{F}$ disc ceramic can be used to reduce the rate-of-rise.

STATUS INDICATOR OUTPUTS

The N-channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

APPLICATIONS

A typical discrete battery backup circuit is illustrated in Figure 3. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 4, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 5. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663S micropower voltage regulator as shown in Figure 6.

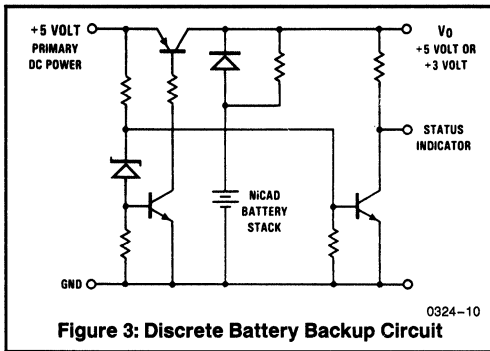


Figure 3: Discrete Battery Backup Circuit

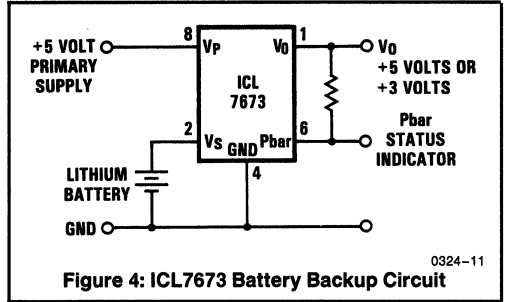


Figure 4: ICL7673 Battery Backup Circuit

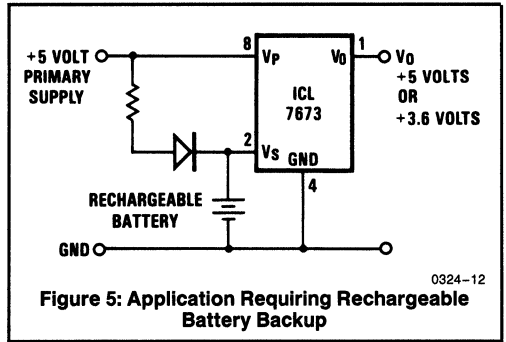


Figure 5: Application Requiring Rechargeable Battery Backup

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

A typical application, as illustrated in Figure 7, would be a microprocessor system requiring a 5 volt supply. In the event of primary supply failure, the system is powered down, and a 3 volt battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to V_P and V_S , with the circuit output V_O supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than V_S and connect, via its internal MOS switches, V_P to output V_O . The backup input, V_S will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect V_P from V_O , and connect V_S .

Figure 8 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input V_P and open drain output S_{bar} through a resistor as illustrated in Figure 9. For high power applications hysteresis can be applied as shown in Figure 10.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 11. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

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NOTE: All typical values have been characterized but are not tested.

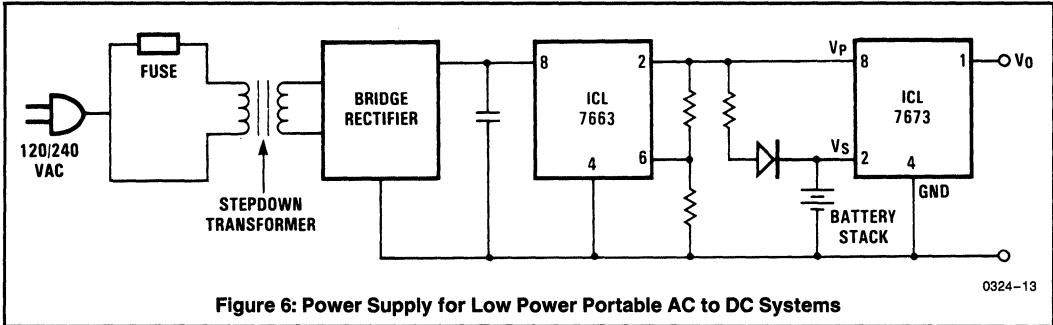


Figure 6: Power Supply for Low Power Portable AC to DC Systems

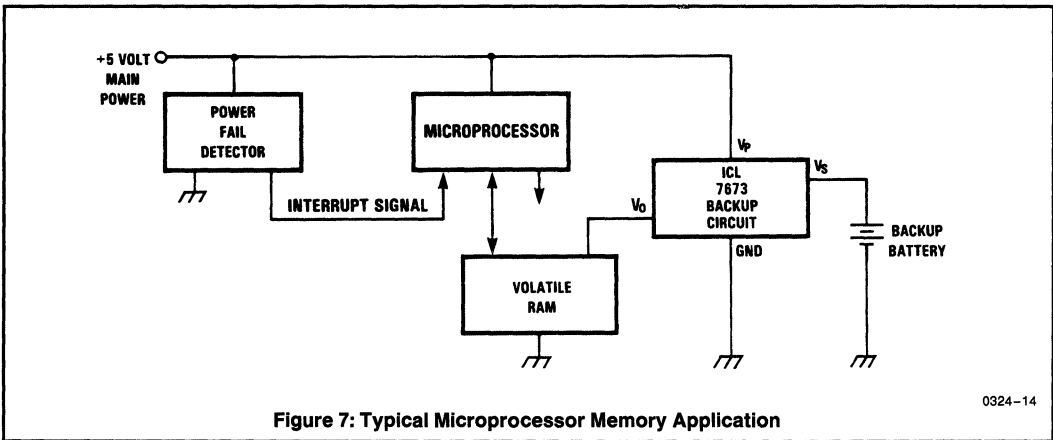


Figure 7: Typical Microprocessor Memory Application

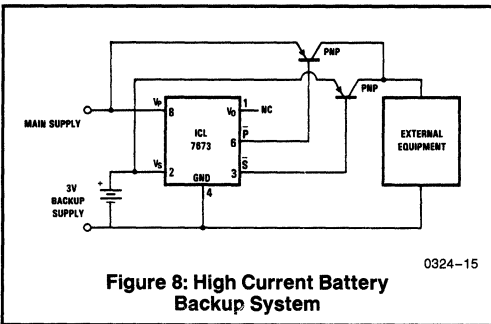


Figure 8: High Current Battery Backup System

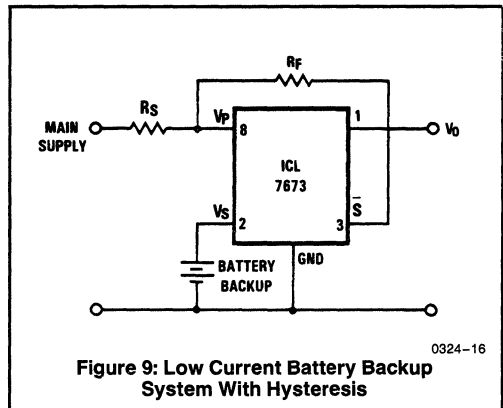
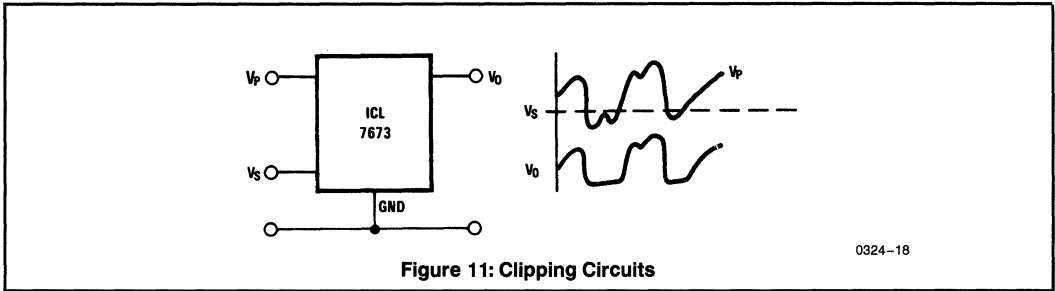
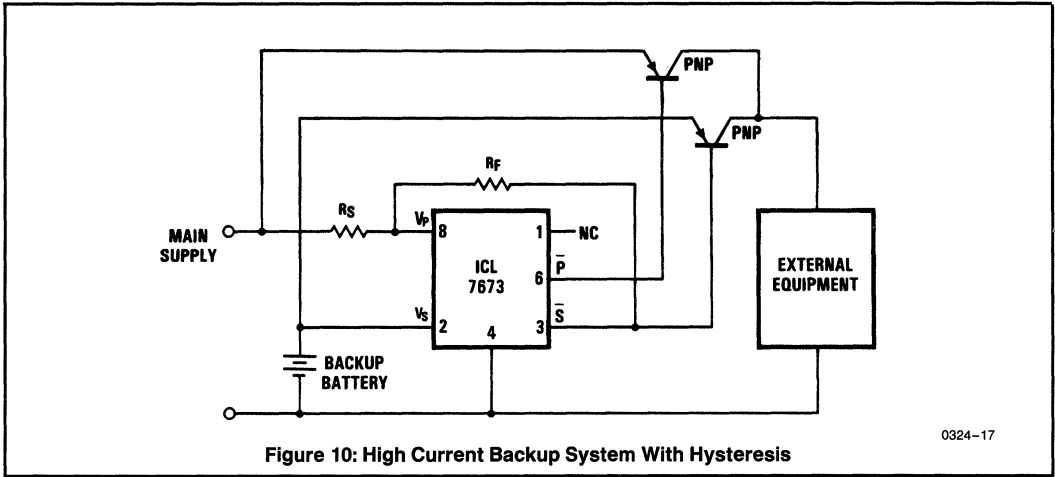


Figure 9: Low Current Battery Backup System With Hysteresis

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ICL7675/ICL7676

Switched-Mode Power Supply Controller Set



ICL7675/ICL7676

GENERAL DESCRIPTION

The ICL7675/7676 two-chip set provides the necessary control circuitry for regulation of a single-ended, transformer coupled, flyback type switching power supply. Specifically designed to operate in this type of configuration, the Intersil controller chip set is trimmed to provide a regulated 5V output.

The two chips comprise a primary side controller and a secondary side controller. Referring to Figure 3, the output of the primary side controller drives the power MOSFET switch in the primary leg of the transformer. The switch is always turned off at a time corresponding to the falling edge of the internal system clock at a frequency of 50kHz. Following an initial soft-start cycle, the switch is turned on at a time corresponding to a pulse received from the secondary side controller via a pulse transformer. The secondary side controller detects the power switch turn-off at the secondary of the transformer and initiates a time-out sequence with a duration directly proportional to the output voltage being sensed. A pulse generated at the end of the time-out period is fed back through the pulse transformer to the primary side controller, thereby completing the control loop.

Power for the primary side controller may be taken from the high voltage DC input to the power transformer via a resistor which feeds current to the on-chip zener diode. This eliminates the need for a separate power supply for the controller. Excessive current in the power MOSFET switch is detected at one end of a resistor in series with the source of the MOSFET, forcing the primary side controller into the soft-start mode.

FEATURES

- Output Voltage of 5V ± 5% Under All Conditions
- Simple Low Current Pulse Transformer Feedback
- Power Switch Over-Current Protection
- Soft-Start
- No Off-Chip Trimming Required
- Minimum External Components
- Low Supply Current
- Output Duty Cycle—5% to 75%

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7675CPA	0°C to +70°C	8 Lead MINIDIP
ICL7675CJA	0°C to +70°C	8 Lead CERDIP
ICL7675IPA	-25°C to +85°C	8 Lead MINIDIP
ICL7675IJA	-25°C to +85°C	8 Lead CERDIP
ICL7675MJA	-55°C to +125°C	8 Lead CERDIP
ICL7676CPA	0°C to +70°C	8 Lead MINIDIP
ICL7676CJA	0°C to +70°C	8 Lead CERDIP
ICL7676IPA	-25°C to +85°C	8 Lead MINIDIP
ICL7676IJA	-25°C to +85°C	8 Lead CERDIP
ICL7676MJA	-55°C to +125°C	8 Lead CERDIP

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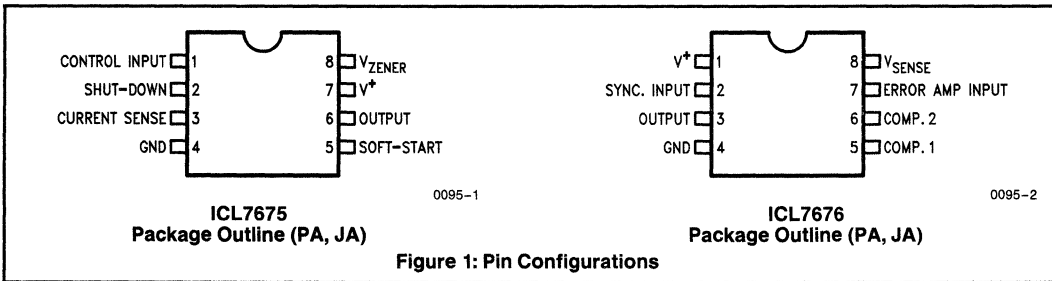


Figure 1: Pin Configurations

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ICL7675/ICL7676



ABSOLUTE MAXIMUM RATINGS

ICL7675
 Supply Voltage (V^+ to GND)16V
 Voltage on any pin($V^+ + 0.3$) to (GND - 0.3) V

ICL7676
 Supply Voltage (V_{sense} to GND)16V
 Voltage on any pin($V_{sense} + 0.3$) to (GND - 0.3) V

ICL7675 & ICL7676

Lead Temperature (Soldering, 10 sec)300°C
 Storage Temperature Range -65°C to +150°C

Operating Temperature Range

ICL767XC0°C to +70°C
 ICL767XI-25°C to +85°C
 ICL767XM-55°C to +125°C
 Continuous Total Power Dissipation ($T_A = 25^\circ\text{C}$)
 CERDIP Package500 mW
 Plastic Package375 mW

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

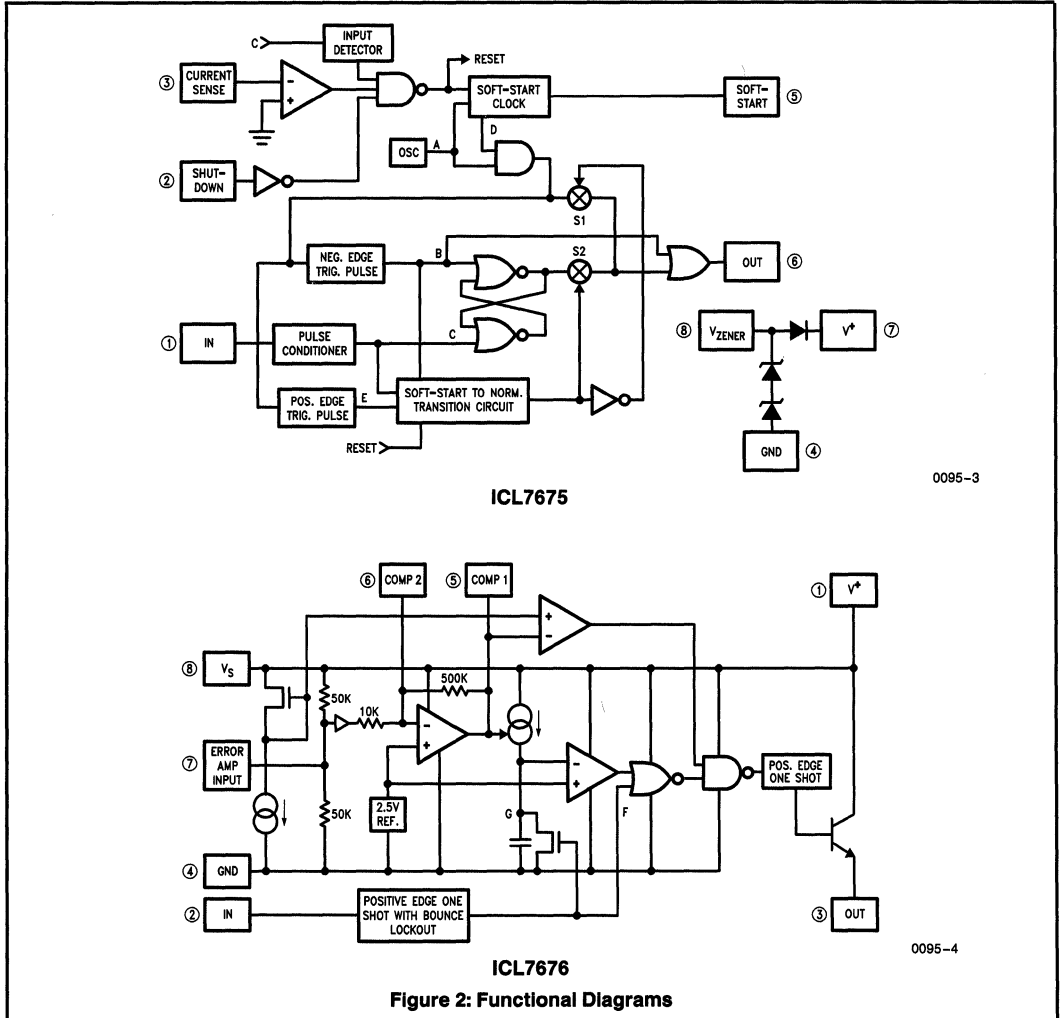


Figure 2: Functional Diagrams

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ICL7675

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: Pins 1, 2, 3, and 4 are connected to GND;

 Pin 7 is connected to V⁺; all other pins are open; V⁺ = 13.5V

Parameter	Test Conditions	Limits											Units	
		T _A = +25°C			0°C < T _A < +70°C			-25°C < T _A < +85°C			-55°C < T _A < +125°C			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ		Max
Oscillator:														
Frequency		42		58	41		59	40		60	38		62	kHz
Temp. Stability						0.1			0.1			0.1		%/°C
Output:														
Fall Time (Note 1)	R _O = 10M, C _O = 500 pF		100	150			170			180			200	ns
Rise Time (Note 1)	R _O = 10M, C _O = 500 pF		100	150			170			180			200	ns
Voltage	Output Low, I _O = -5 mA		0.2	0.3			0.33			0.35			0.40	V
	Output High, I _O = +5 mA	12.8			12.8			12.7			12.6			V
Control Input:														
Leakage Current			0.01	10			50			50			100	nA
Threshold		9.5		11.0	9.0		11.0	8.5		11.5	8.5		12.0	V
Shut-Down:														
Leakage Current			0.01	10			50			50			100	nA
Threshold		9.5		11.5	9.4		11.8	9.3		12.0	9.2		12.5	V
Soft-Start:														
Time-out	Open Pin		8											ms
Current Limiting:														
Sense Voltage		420		600	390		630	370		640	300		700	mV
Sense Voltage Temperature Coefficient						0.6			0.6			0.6		mV/°C
V _{zener} :														
Forward Voltage (Pin 8)		13.5	13.8	14.3										V
Forward Voltage Temperature Coefficient						7			7			7		mV/°C
V ⁺ Supply Voltage (Pin 7)			13.2											V
Supply Current	No Output Load			1.2			1.3			1.4			1.5	mA

NOTE 1: This parameter is guaranteed by design and is not tested in production.

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ICL7676

ELECTRICAL CHARACTERISTICS

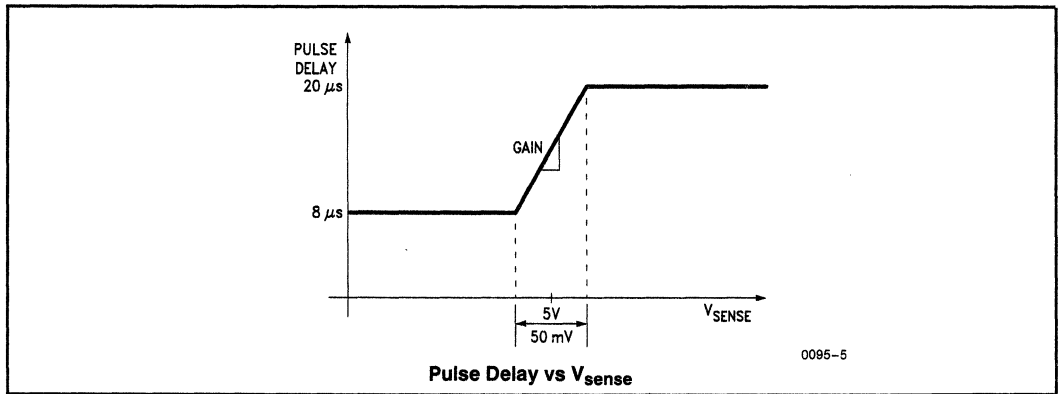
Unless otherwise stated: Pins 2 and 4 are connected to GND; Pins 1 and 8 are connected to V_{sense} ; all other pins are open; $V^+ = 5V$

Parameter	Test Conditions	Limits												Units
		$T_A = +25^\circ C$			$0^\circ C < T_A < +70^\circ C$			$-25^\circ C < T_A < +85^\circ C$			$-55^\circ C < T_A < +125^\circ C$			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply: Output Voltage	15 μs Pulse Delay (Note 2)	4.9		5.1										V
Temp. Stability					100			100			100			mV
Sync Input: Threshold		1.2		2.4	1.2		2.4	1.2		2.4	1.2		2.4	V
Leakage			0.01	10			50			50			100	nA
Output: Voltage	Output High	4.35			4.3			4.2			4.1			V
Pulse Current		15			14			12			10			mA
Pulse Width		0.55		1.0	0.5		1.0	0.4		1.0	0.25		1.0	μs
Min. Pulse Delay	50kHz Clock at Input			9			9			10			12	μs
Max. Pulse Delay	50kHz Clock at Input	20			20			20			20			μs
Gain	Time-Out/ V_{sense}	90	140		70			60			50			$\mu s/V$
V_{sense} Input Current (Note 3)	$V_{sense} = 5.0V$, No Load			1.0			1.1			1.2			1.5	mA

NOTE 2: This corresponds to a 25% duty cycle at the output of the ICL7675.

3: This parameter is equivalent to device supply current.

TYPICAL PERFORMANCE CHARACTERISTICS



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ICL7675/ICL7676



DETAILED DESCRIPTION

Refer to the system schematic (Figure 3), timing diagram (Figure 4) and the individual controller functional diagrams (Figure 2) for the following discussion.

Secondary Side Controller

The secondary side controller, ICL7676, is required to provide an output pulse that will cause the primary side controller, ICL7675, to turn the MOSFET power switch on in the primary leg of the power supply transformer. This pulse must occur at a time such that the resultant switch duty cycle causes the output of the power supply to be regulated at precisely 5V. The circuit accomplishes this by amplifying the difference between a fraction of the output voltage and an internally generated reference voltage and using that output to control a ramp generator. When the output of the ramp generator reaches the reference voltage level, a comparator triggers a monostable giving a fixed width pulse at the output of the controller. A positive transition at the power supply transformer secondary, corresponding to power switch turn-off, triggers a one-shot with a bounce lock-out feature that prevents any false triggering due to excessive ringing at this node. The output of this one-shot resets the ramp generator by turning on a MOS transistor across the ramp capacitor. Also, if the ramp voltage has not reached the comparator threshold, the one-shot triggers the output monostable. This ensures that a pulse is sent to the primary side controller every cycle. Variations in the output voltage are detected and cause an increase or decrease in the current supplied to the ramp capacitor. This causes a change in the capacitor ramp rate at point G in Figure 2 and a consequent change in the time when the comparator threshold crossover occurs, generating an output pulse from the ICL7676. The output pulse's position is thereby modulated relative to the input trigger in direct proportion to the power supply voltage. The direction of change is such that when the resultant duty cycle at the output of the ICL7675 corrects the power supply voltage, a negative feedback control loop is formed that maintains the desired output voltage.

Primary Side Controller

The primary side controller, ICL7675, must process the incoming pulse from the secondary side controller, ICL7676, and combine this with the internally generated oscillator waveform to produce a driving signal for the MOSFET switch. Initially, however, a soft-start circuit determines the driving signal waveform. Therefore, there must also be a circuit which directs the orderly transition from soft-start to

normal operation. When the power supply is first turned on, a power-up-reset circuit initializes the soft-start clock and sets switch S1 on and switch S2 off, as shown in Figure 2. The soft-start's slowly increasing duty cycle waveform is fed through an AND gate and through switch S1 to the output buffer. Meanwhile, the transition circuit continuously monitors the relative position in time between the incoming pulse from the secondary side controller and the leading edge from the clock waveform. When the duty cycle of the soft-start clock has increased to the point where its positive edge occurs earlier than the input pulse, then the transition circuit gives control of the output switch drive to the feedback loop by turning off S1 and turning on S2. Now the negative edge of the clock resets the flip-flop, turning off the power switch, and the input pulse sets the flip-flop, turning on the power switch. The negative edge of the soft-start clock is synchronized to the negative edge of the oscillator and occurs at a fixed frequency of 50kHz. The soft-start clock's output duty cycle gradually increases from zero to 100%, but when ANDed with the 75% duty cycle waveform of the oscillator, the maximum duty cycle of the resultant waveform is limited to 75% as well.

Soft-Start Cycle

The soft-start cycle time is fixed at about 15 ms. It can be increased somewhat by adding capacitance to pin 5. If no pulse is received from the secondary side controller, the primary side controller will reset, initiating the soft-start sequence. It will continue to recycle through the soft-start sequence until a pulse is received. As long as a pulse is received within one eighth cycle after the falling edge of the system clock, an approximately 0.5 μ s pulse will appear at the output to drive the power switch. This allows for delays in the feedback loop which might cause the controlling pulse to arrive late.

Other Features

The external resistor R2, connected between the I_{sense} pin and ground and placed in series with the power MOSFET switch, senses an over-current fault condition, tripping a comparator which shuts down the output. After the fault condition has been removed, the power supply will pass through the soft-start cycle before returning to normal operation. There is also a shut-down pin that when forced high will shut down the output. An on-chip zener diode and rectifying diode combination, connected through a dropping resistor to the high DC input voltage of the power supply, provides power to the circuit.

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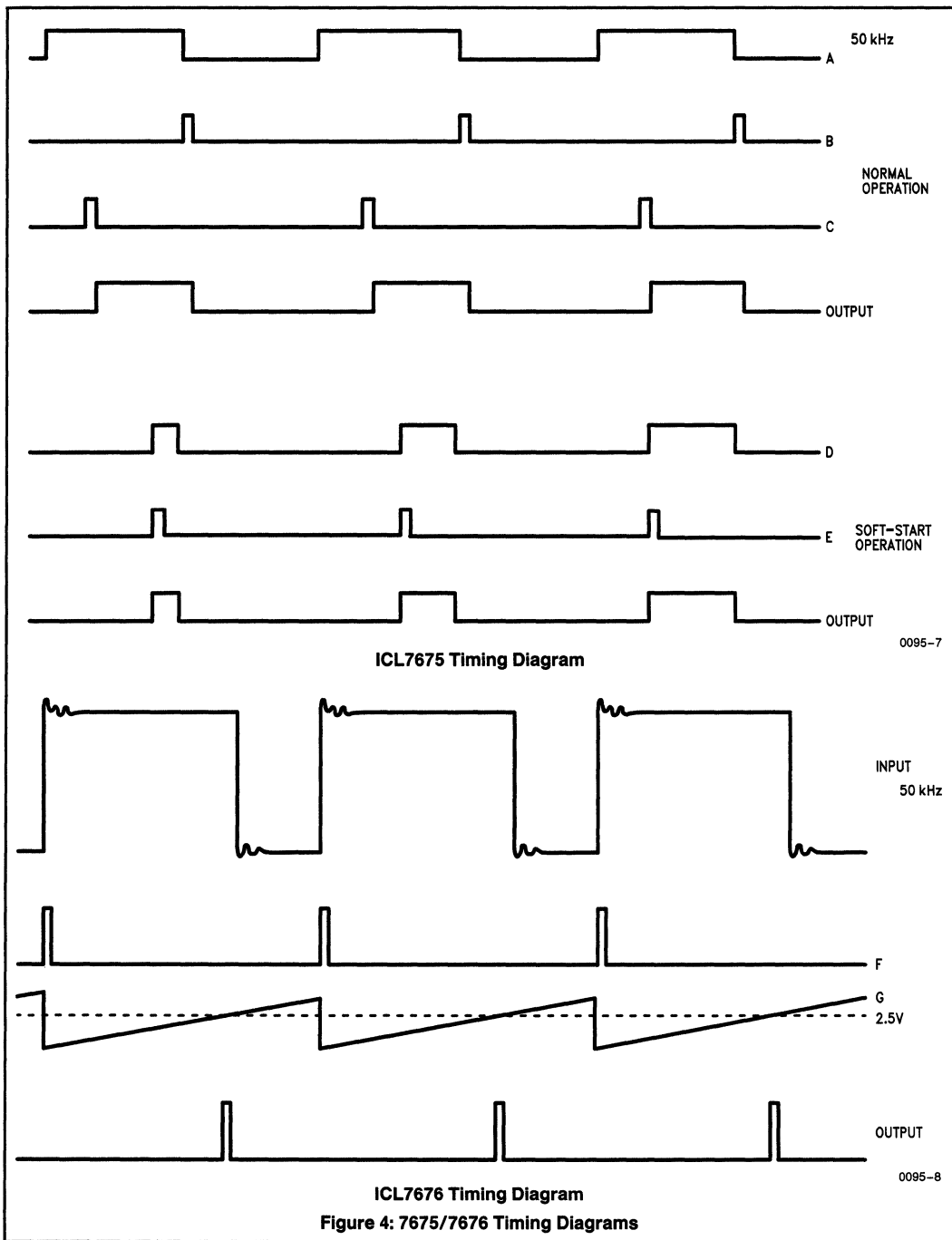


Figure 4: 7675/7676 Timing Diagrams

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APPLICATIONS

Refer to the system schematic (Figure 3) for the following discussion of a flyback converter.

The input bridge rectifier and filter circuit converts the 115V AC line to 163V DC. The unregulated high voltage DC is applied across a GE IRF 821 Power FET (Q1) and the primary of transformer L1. The Power FET acts as a switch, opening and closing in response to the gate drive signal from the output of the ICL7675 controller. When Q1 opens, the energy stored in L1 is transferred to the secondary and through diode D6 into C7. This is characteristic of the flyback converter. The ICL7676 monitors the voltage across C7 and sends a variable time delay pulse through pulse transformer L3 to the ICL7675 with a delay proportional to the voltage sensed. The ICL7675 translates the pulse into a variable duty-cycle 50kHz output signal which drives the gate of the Power FET Q1 "ON" and "OFF" thereby closing the negative feedback loop.

The flyback converter topology is best suited for power levels below 150W due to the high ripple current produced across capacitor C7. This topology is favored because of its simplicity. Output voltage control is achieved by varying the ratio of ON to OFF time for Q1, and can be expressed as follows:

$$V_0 = V_{C1} N \frac{t_{on}}{t_{off}} - V_{D6} - I_0 R_S$$

where:

- V_{C1} = Voltage across C1
- V_{D6} = Forward drop across D6
- I_0 = Output current
- R_S = Output series resistance
- N = Turns ratio of L1 (secondary/primary)

This applies for continuous mode operation where the current in L1 never falls to zero during a clock cycle. For light loads, discontinuous conduction may occur. The primary inductance of L1 required to assure continuous mode operation at a light load $I_{0(min)}$ is:

$$L_p = \frac{t_{on(min)}^2 \times V_{C1(max)} \times f}{2(V_0 + V_{D6} + I_0 R_S) I_{0(min)}}$$

For $I_{0(min)}$ = 10% of full load at high line:

$$L_p = \frac{(6 \times 10^{-6})^2 \times (185)^2 \times (50 \times 10^3)}{(2)(6)(1)} = 5.1 \text{ mH}$$

This inductance can be obtained on a gapped ferrite 'E' core which offers an excellent (performance)/(cost) ratio. The air gap is required to prevent saturation at low line and maximum current.

Neglecting voltage spikes due to leakage inductance, drain to source voltage stress for Q1 is:

$$V_{ds} = \frac{V_0 + V_{D6} + I_0 R_S}{N} + V_{C1}$$

A turns ratio $N = 1/14$ limits V_{ds} to a safe value at high line. A catch winding clamps voltage spikes across the Power FET at turn off. The winding should be bifilar wound with the primary to minimize leakage inductance. An electrostatic shield will improve isolation between primary and secondary.

The network composed of L2 and C8 at the output provides additional filtering by attenuating high frequency spikes and ripple. The corner frequency for the LC filter is approximately 20kHz which effectively attenuates 50kHz and higher order harmonics. Inductor L2 is shunted by 3.9Ω R7 to reduce the output "Q" and minimize output ringing. For critical damping: $R = \sqrt{L/C}$. Diode D6 is a fast recovery Schottky diode. It has a low V_d and is snubbed by resistor R6 and capacitor C6 to limit the dV/dt and overshoot. The diode D5 is also a fast recovery diode which is connected to the catch winding of transformer L1. This protects the power FET Q1 from potentially damaging voltage spikes.

Switching Losses

Power FETs behave like ideal switches and are very well suited for high frequency switching power supply applications. The fast turn-on and turn-off of the power MOSFET results in very low switching losses. In this application the turn-off losses are essentially zero, due in part to the presence of snubber network C4 and R4. And the worst case turn-on losses are less than two watts.

Energy: $W = \int_0^t V_{ds}(t) I_d(t) dt$

where: $V_{ds}(t) = 10^9 t$
 $I_d(t) = 12.5 \times 10^6 t$
 $W = 12.5 \times 10^{15} \int_0^{200 \text{ ns}} t^2 dt$

Integrating:

$$W = 12.5 \times 10^{15} \frac{t^3}{3} \quad \text{where: } t = 200 \times 10^{-9}$$

and Power:

$$P = W \times F \quad \text{where: } F = 50 \text{ kHz}$$

$$\text{Power} = 12.5 \times 10^{15} \left[\frac{(2 \times 10^{-7})^3}{3} \right] 5 \times 10^4$$

$$= 1.67 \text{ Watts}$$

Because the power MOSFET has very high current gain it can be driven directly from the ICL7675. This is highly advantageous because it simplifies the circuitry and reduces overall system manufacturing costs.

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Control Loop Design

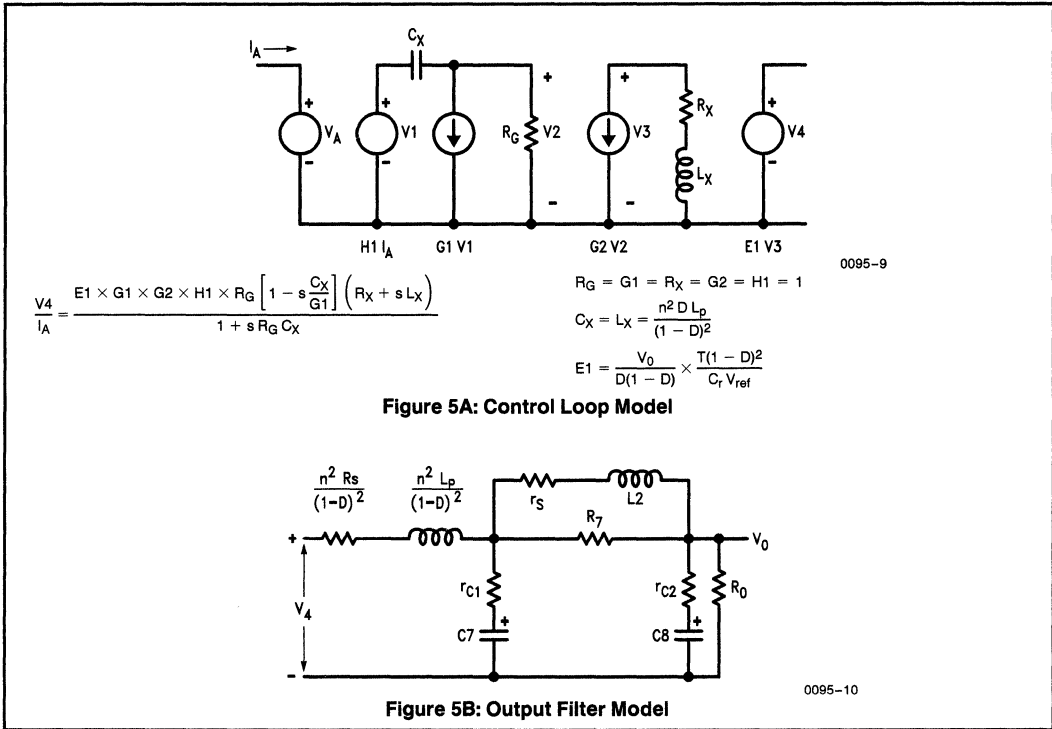
The control loop for a transformer coupled flyback converter is similar to the boost converter from which it is derived. The presence of an LC resonant filter with its steep 180 degree phase rolloff and a right-half plane zero in the loop transfer function makes frequency compensation a non-trivial exercise. However, the design of the control loop can be made easier if not simpler with the proper tools. The mathematical equation representing the power mesh equivalent transfer function may be reduced to a model which can be entered into SPICE, a widely used circuit simulation program, or any other simulation software being used. The equation for the modulator-power mesh portion of the control loop may be expressed as:

$$\frac{V_0}{D(1-D)} \left[1 - \frac{sn^2DL_p}{(1-D)^2 R_0} \right] \frac{T(1-D)^2}{C_r V_{ref}}$$

where:

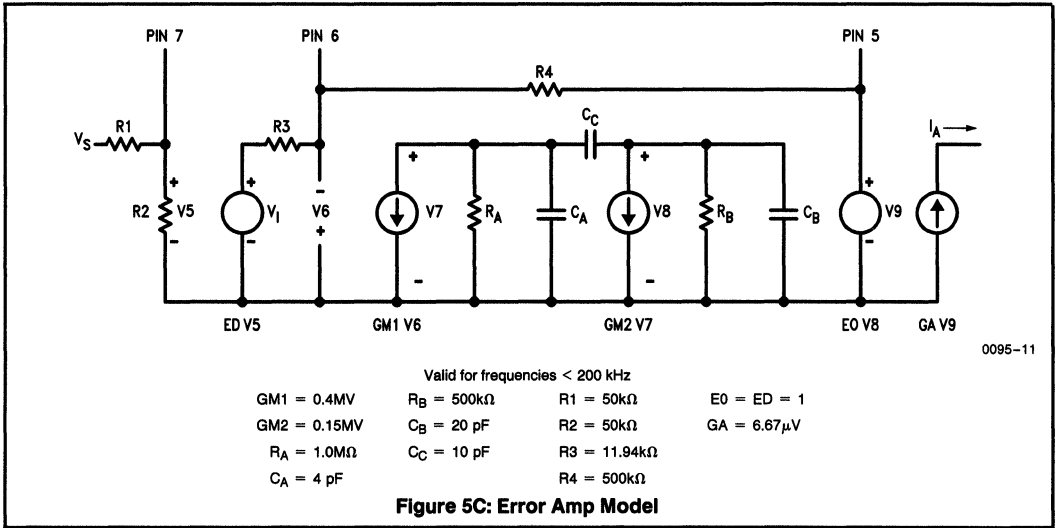
- D = Duty cycle
- n = Transformer turns ratio
- L_p = Primary inductance
- R₀ = Load resistance
- T = Clock period
- C_r = Internal ramp capacitance = 40 pF
- V_{ref} = Internal reference voltage = 2.5V

A model representing this equation is shown in Figure 5A. Combined with the output filter shown in Figure 5B, and the error amp shown in Figure 5C, a computer simulation can be used to determine the optimum combination of components for a stable design that still provides adequate response to external disturbances. Note that in the output filter, the effective primary inductance and inductor series resistance are multiplied by n²/(1-D)². In the example here, a combination of lead compensation provided by C11 and lag compensation provided by R10 and C10 gave the desired response.



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ICL7677

Power Fail Detector*



ICL7677

GENERAL DESCRIPTION

The ICL7677 is a power fail detector, an important enhancement in a power supply circuit. It is designed to give the fastest possible power fail indication. The part can be used on the primary side of the power supply with opto-isolators transmitting the fault indication to the equipment in the secondary side. Alternatively, this part can be used on the secondary side of the power supply to monitor power supply conditions, with the ability to drive TTL/CMOS logic at the fault indicating outputs.

The ICL7677 as a primary side power fail detector can simultaneously monitor the a.c. line voltage, the reservoir capacitor voltage, the primary side current and ambient temperature. The part as a secondary side power fail detector can simultaneously monitor up to two DC voltages, one load current and ambient temperature. Only a few external passive components are required.

The circuit has an on-chip bandgap voltage reference to conveniently program the detection thresholds. However, an external voltage reference can be used if preferred.

There are four fault indicating outputs. These are "no fault", "under-voltage", "over-voltage", and "over-temperature or over-current". Thus, these outputs allow straight forward diagnosis of power failure. Moreover, the "no fault" indicator alone is sufficient for low cost systems to indicate failure using only one opto-isolator.

The part allows the user to program time delays for various faults, preventing false indications due to spikes or noise. It also displays a unique output state while the supply is turning ON, until the applied voltage reaches its nominal voltage range.

The ICL7677 can be powered by a 5V voltage source, or current fed via a resistor, as it has its own voltage regulator.

FEATURES

- Simultaneous Monitoring of the AC Line, Reservoir Capacitor Voltage, Ambient Temperature and Primary Side Current When Used on Primary Side.
- Simultaneous Monitoring of Two DC Voltages, Temperature, and One Load Current When Used on the Secondary Side
- Programmable Thresholds for Over-Voltage, Under-Voltage, and Over-Temperature Detection
- Programmable Delay Time for All Faults to Avoid False Indication Due to Noise or Line Spikes
- On Chip Voltage Reference and Voltage Regulator; An External Voltage Reference Can be Used If Desired
- Unique Output State for the Start-Up phase
- Outputs are Logically Combined to Optimize Power Fail Indication and Indicate Source of Power Failure
- Outputs Can Drive Low-Current Opto-Isolators and TTL/MOS Logic Directly

APPLICATIONS

- Switching Power Supplies, Both Primary Side and Secondary Side Power Fail Detector
- Linear Power Supplies, DC to DC Converters

ORDERING INFORMATION

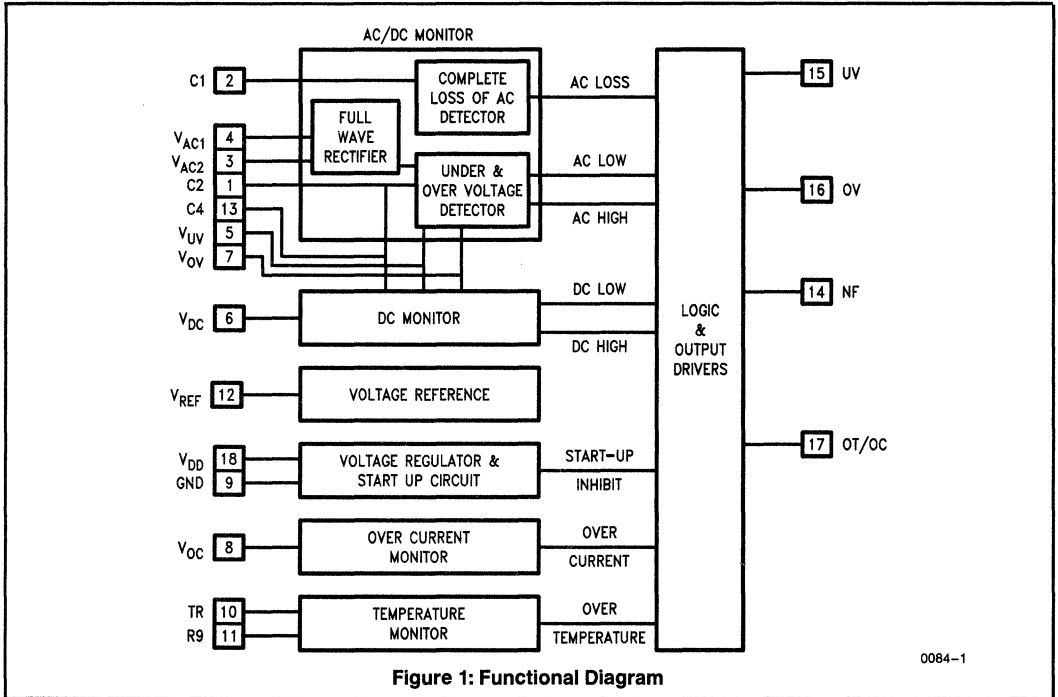
Part Number	Operating Temperature	Package
ICL7677CPN	0°C to +70°C	18 Lead Plastic
ICL7677CJN	0°C to +70°C	18 Lead Cerdip
ICL7677IPN	-25°C to +85°C	18 Lead Plastic
ICL7677IJN	-25°C to +85°C	18 Lead Cerdip
ICL7677MJN	-55°C to +125°C	18 Lead Cerdip

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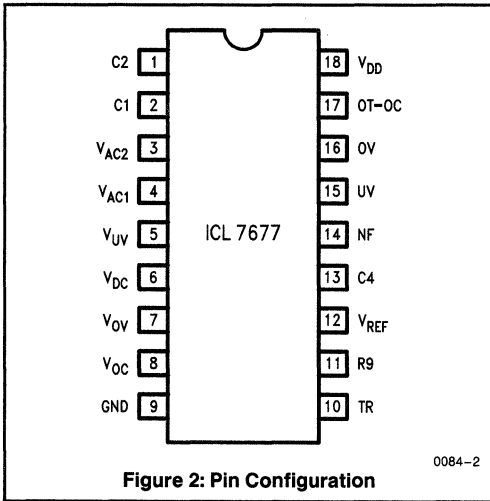
*Patent Pending

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NOTE: All typical values have been characterized but are not tested.



0084-1



0084-2

Pin	Symbol	Function
1	C2	Delay capacitor for AC under voltage fault.
2	C1	Delay capacitor for immediate power loss fault.
3	V _{AC2}	One input of AC/DC monitor.
4	V _{AC1}	Other input of AC/DC monitor.
5	V _{UV}	Low threshold level.
6	V _{DC}	Input of DC monitor.
7	V _{OV}	High threshold level.
8	V _{OC}	Input to sense over current.
9	GND	Chip supply ground or V _{SS} .
10	TR	Thermistor.
11	R9	Bias resistor.
12	V _{REF}	Reference voltage.
13	C4	Delay capacitor to prevent false alarms due to noise.
14	NF	No fault output.
15	UV	Under voltage output.
16	OV	Over voltage output.
17	OT-OC	Over temperature or over current output.
18	V _{DD}	Positive chip supply or V ⁺ .

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage9V
Supply Current ($V_{SUPPLY} = 9V$)20 mA
Input Voltage at Any Pin	$V^- - 0.3V$ to $V^+ + 0.3V$
Power Dissipation		
CERDIP Package	500 mW
Plastic Package	375 mW
Storage Temperature	-65°C to +150°C
Operating Temperature Range		
ICL7677C	0°C to +70°C
ICL7677I	-25°C to +85°C
ICL7677M	-55°C to +125°C
Lead Temperature (Soldering, 10s)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Circuit in Figure 3, S1 S3 S4 open, S2 S5 closed, unless otherwise specified.

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$			$T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$			Units
			ICL7677			ICL7677C			ICL7677I			ICL7677M			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I ⁺	Supply Current	$V_{DD} = 4V$			0.75			0.75			0.8			1.0	mA
		$V_{DD} = 6V$			8.5			8.5			9.0			10.0	
V _{DD}	Internally Regulated Supply Voltage	I ⁺ = 4 mA	5.5		6.1	5.5		6.1	5.5		6.1	5.3		6.3	V
I _{IN}	Input Current	$V_{DD} = 4V$ and 6V		20	80		20	80		20	100		20	100	μA
	Input Leakage V _{DC}	$V_{DD} = 4V$ and 6V			50			50			50			100	nA
	V _{UV} , V _{OV} , V _{OC}				50			50			50			100	
V _{REF}	Reference Voltage	$V_{DD} = 4V$ and 6V No Load, S1 Open	1.23	1.254	1.278	1.23		1.28	1.23		1.284	1.2		1.31	V
		100 μA Load, S1 Closed	1.23	1.254	1.278	1.23		1.28	1.23		1.284	1.2		1.31	
	Reference Tempco						100			100			100	ppm/°C	
V _{OUT}	ON Output Voltage	$V_{DD} = 4V$, I _{OUT} = 40 μA	2.4			2.4			2.4			2.4		V	
"ON"	All Four Drivers	$V_{DD} = 6V$, I _{OUT} = 40 μA	2.4			2.4			2.4			2.4			
I _{OUT}	ON Output Current	$V_{DD} = 4V$, V _{OUT} = 0.7V	0.8		1.3	0.8		1.3	0.8		1.3	0.7		1.4	mA
		$V_{DD} = 6V$, V _{OUT} = 0.7V	1.4		2.2	1.4		2.2	1.4		2.2	1.3		2.3	
V _{OUT}	OFF Output Current	$V_{DD} = 4V$, I _{OUT} = -1.6 mA	0		0.4	0		0.4	0		0.4	0		0.4	V
		$V_{DD} = 6V$, I _{OUT} = -1.6 mA	0		0.4	0		0.4	0		0.4	0		0.4	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

Test Circuit in Figure 3, S1 S3 S4 open, S2 S5 closed, unless otherwise specified.

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = 0°C to +70°C			T _A = -25°C to +85°C			T _A = -55°C to +125°C			Units
			ICL7677			ICL7677C			ICL7677I			ICL7677M			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{bias}	Bias Current	V _{DD} = 4V S2 Closed, S1 Open V _{DD} = 6V	3.6		6.0	3.6		6.0	3.3		6.5	3.0		7.0	μA
			8.0		12.4	8.0		12.4	7.7		12.8	7.4		13.4	
I _{temp}	Thermistor Short-Circuit Current	S2, S5 Open S3, S4 Closed V _{DD} = 4V and 6V	9.5		10.5	9.2		11.0	9.0		12.0	9.0		13.0	μA
I _{temp}	Thermistor Current	S2, S5 Open S3 Closed V _{DD} = 4V and 6V	9.5		10.5	9.2		10.5	9.0		10.5	8.0		11.0	μA
V _{TH}	Threshold Voltage at Over-Current Sensing	V _{DD} = 4V and 6V	205		245	203		247	199		251	195		255	mV
T1	Immediate Loss of Power Delay	(Fig. 4) V _{DD} = 5V C1, C2, C4 Connected C1, C2, C4 Not Connected	330	410	490	330		490	330		520	330		550	μs
T3	AC Under-Voltage Delay	(Fig. 5) V _{DD} = 5V C1, C2, C4 Connected C1, C2, C4 Not Connected	6.61	8.26	9.91	6.61		9.91	6.61		10.0	6.61		11.0	ms
					50			60			60			70	μs
T5	AC Over-Voltage Delay	(Fig. 6) V _{DD} = 5V C1, C2, C4 Connected C1, C2, C4 Not Connected	174	215	256	174		256	174		300	174		300	μs
					40			40			40			50	
T7	DC Under-Voltage Delay	(Fig. 7) V _{DD} = 5V C1, C2, C4 Connected C1, C2, C4 Not Connected	174	215	256	174		256	174		300	174		300	μs
					30			30			30			40	
T9	DC Over-Voltage Delay	(Fig. 8) V _{DD} = 5V C1, C2, C4 Connected C1, C2, C4 Not Connected	174	215	256	174		256	174		300	174		300	μs
					30			30			30			40	
T11	Over-Temperature Delay	Fig. 9, V _{DD} = 5V			50			60			60			70	μs
T13	Over-Current Delay	Fig. 10, V _{DD} = 5V			40			40			40			60	μs
T2	Recovery Times From Correction of Faults	Fig. 4-10, V _{DD} = 5V			40			40			40			50	μs
T4					40			40			40			50	μs
T6					40			40			40			50	μs
T8					40			40			40			50	μs
T10					40			40			40			50	μs
T12					40			40			40			50	μs
T14					40			40			40			60	μs

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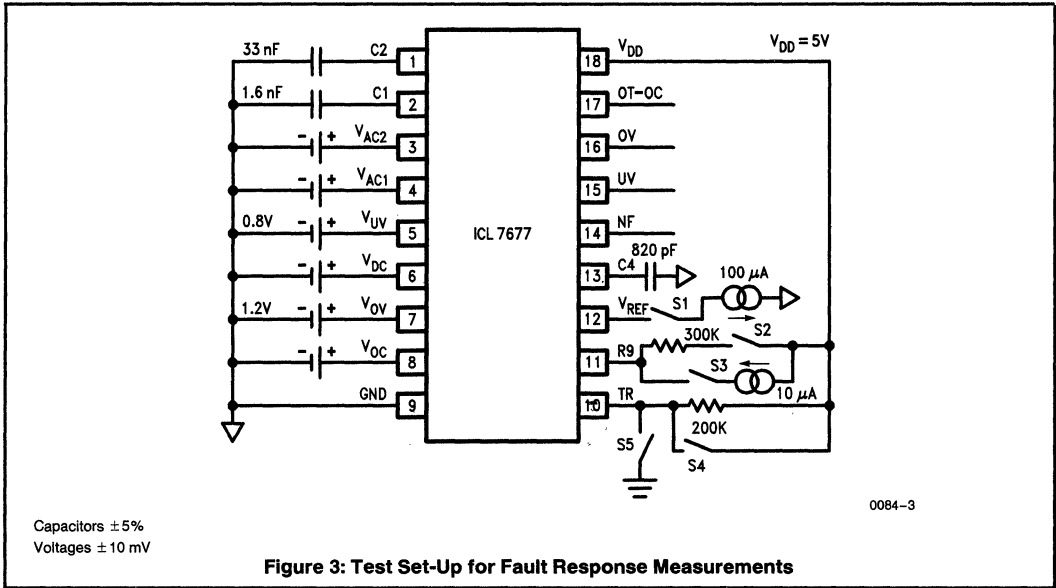


Figure 3: Test Set-Up for Fault Response Measurements

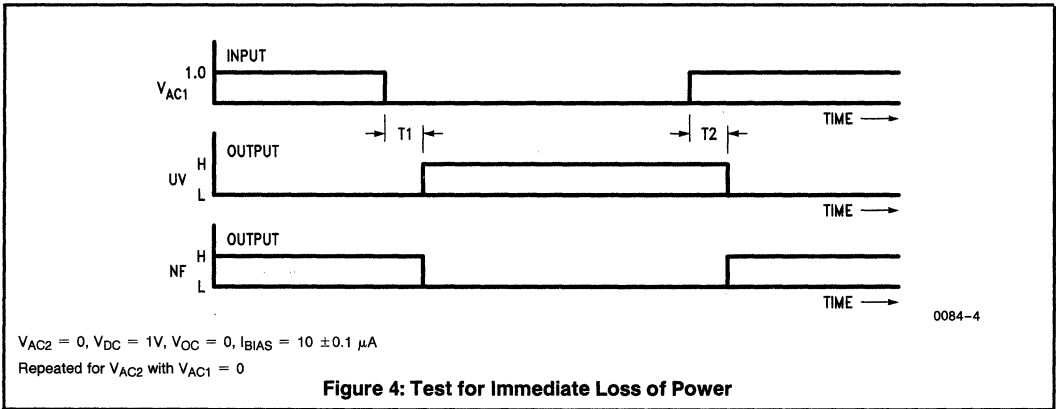


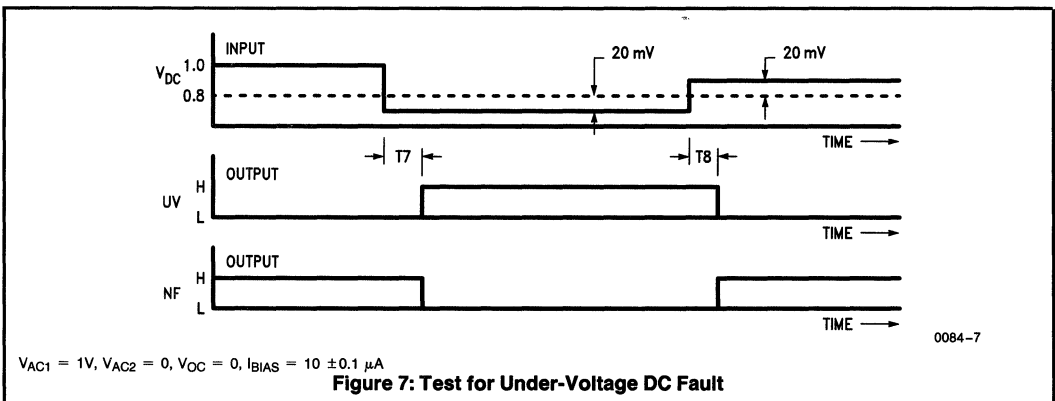
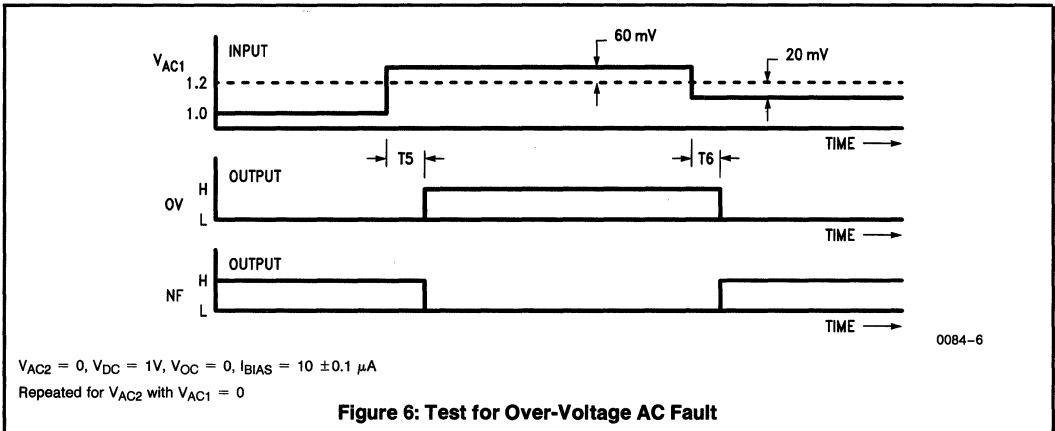
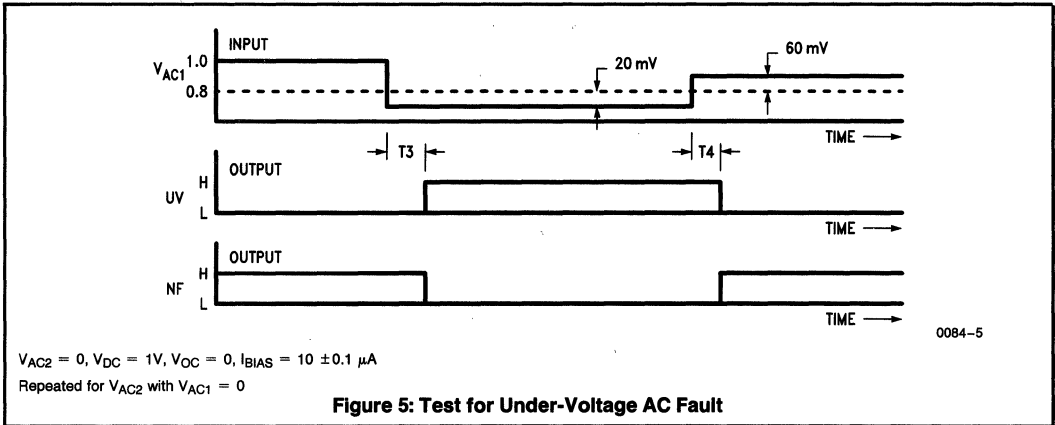
Figure 4: Test for Immediate Loss of Power

$V_{AC2} = 0$, $V_{DC} = 1V$, $V_{OC} = 0$, $I_{BIAS} = 10 \pm 0.1 \mu A$
 Repeated for V_{AC2} with $V_{AC1} = 0$

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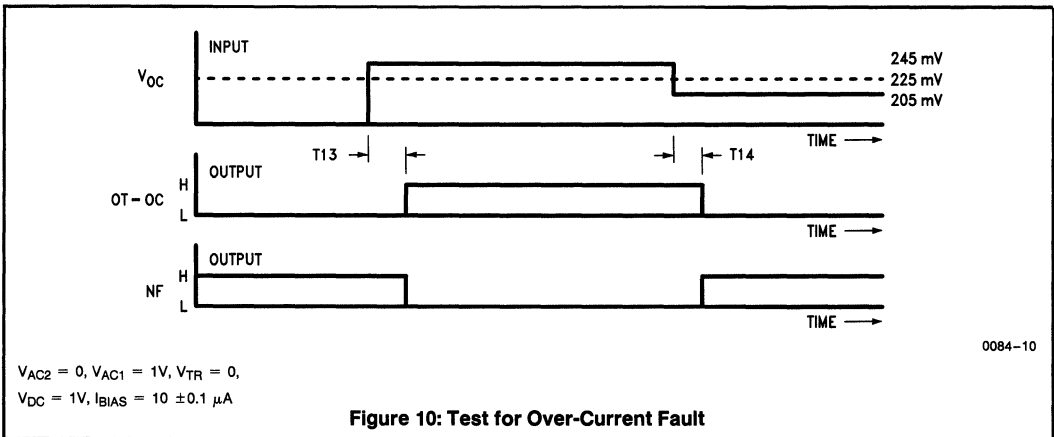
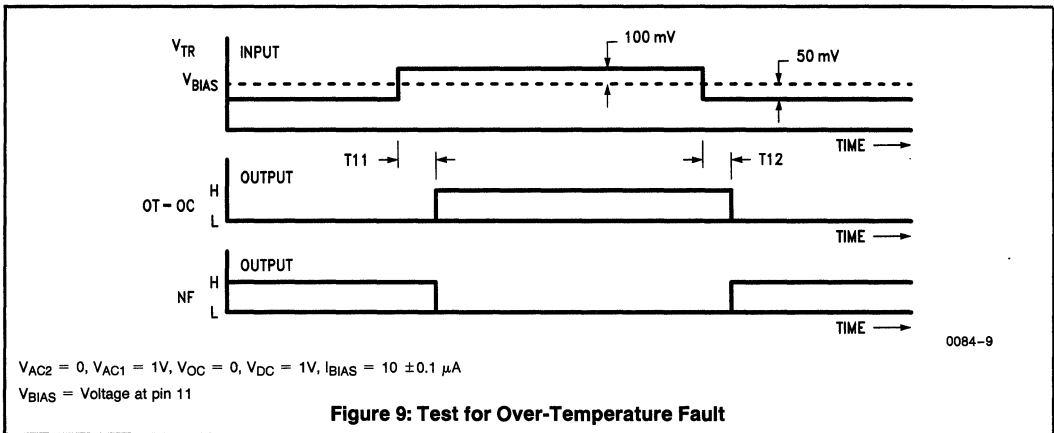
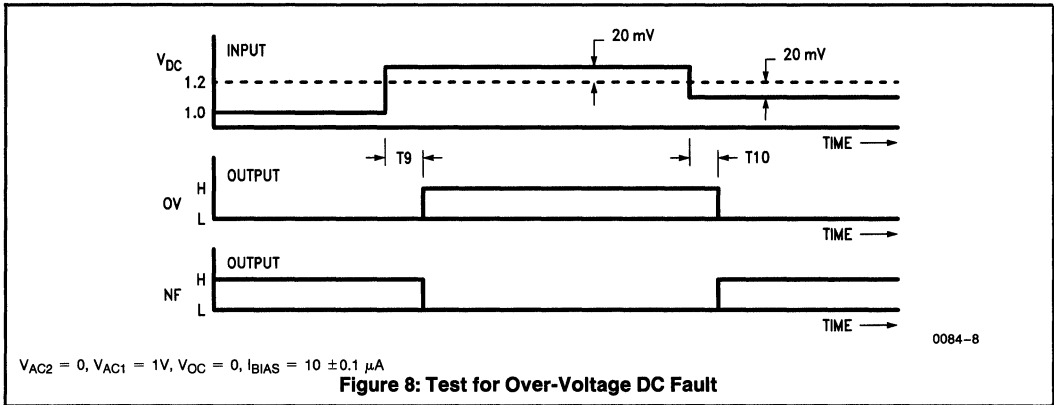
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DETAILED DESCRIPTION

Functional Diagram

The functional diagram of the ICL7677 is shown in Figure 1. The circuit contains an AC/DC monitor, DC monitor, current monitor, temperature monitor, logic and output drivers, regulator, start up circuit, and voltage reference circuit.

AC/DC Monitor

The AC/DC monitor is primarily designed to monitor the line, but can also monitor DC signals if the chip is used on the regulated side of the supply. As an AC monitor, it detects the following fault conditions;

1. Complete and immediate loss of power.
2. Reduction in voltage.
3. Excessive voltage.

The detection of complete loss of power is explained by considering Figure 11. The AC line voltage is divided by external resistors connected to pins 3 & 4 and converted to a full wave rectified form on chip. The figure shows that the amplitude of the signal is close to zero for a very brief period during each cycle. This period of time, t , is governed by the amplitude and frequency of the signal, and the threshold voltage, V_{ZERO} , which is approximately 22% of the internal reference voltage, V_{REF} . If the signal remains below V_{ZERO} for a duration much longer than t , this is interpreted as a loss of AC power. The user can program the allowed time duration by simply changing the external capacitor at pin 2 to suit the particular AC frequency employed. The absolute differential signal threshold between V_{AC1} (pin 4) and V_{AC2} (pin 3) is $276mV \pm 20mV$.

The detection of reduction in AC voltage can be checked only on the peak values. Two threshold values are defined using external resistors together with either the on-chip voltage reference at pin 12 or an external reference. Low threshold (V_{UV}) and high threshold (V_{OV}) are developed at pins 5 & 7 respectively. It is obvious from Figure 11 that the signal crosses the low threshold value every half cycle. Thus, the absence of the signal crossing the low threshold

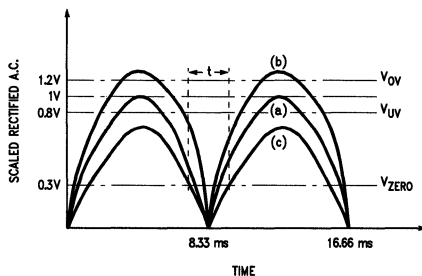
indicates a reduction in AC voltage. The fault detection is based on the fact that the maximum time duration when the signal is below the low threshold value is half the time period. Thus, detection of the signal below the threshold for a period longer than this indicates that there is a reduction in voltage. Again, the allowed time duration is user programmable to work with different line frequencies. This time duration is varied by the external capacitor C2.

Finally, excessive voltage is detected when the AC voltage crosses the upper threshold value as shown in Figure 11. The threshold must be exceeded for longer than a user defined delay to be interpreted as a fault condition. This feature reduces the probability of false alarm due to short harmless voltage spikes. The length of the delay is controlled by the external capacitor, C4, on pin 13.

As an auxiliary DC monitor, used on the secondary side of the supply, pin 3 is grounded and pin 4 is connected to the resistively divided DC voltage as shown in Figure 15. In this case, the time constant that was previously related to the line frequency, set by the capacitor on pin 1, is now used for spike suppression. Pin 2 should be tied to V_{DD} to disable the loss of AC detector. There is no circuit change for over-voltage detection.

DC Monitor

The DC monitor detects the under- and over-voltage on the monitored node by dividing down the DC voltage using two resistors and applying it to pin 6. The divided DC voltage is compared with V_{UV} and V_{OV} which are at pins 5 & 7 respectively. When the supply voltage drops below the lower threshold value for a time duration more than the user programmed delay, an under-voltage condition is present. Similarly, when the supply voltage goes above the upper threshold value for a similar time duration, then an over-voltage condition is indicated. The purpose of the programmed time delay is to reduce false alarms due to noise, and is the same value that was chosen for AC over-voltage, set by the capacitor, C4, on pin 13.



0084-12

Figure 11: Definition of AC Faults
Curve a: Nominal Voltage.
Curve b: Over-Voltage AC.
Curve c: Under-Voltage AC.

Calculation of time while AC voltage is below V_{ZERO} :
 If lowest nominal voltage = 0.8V,
 then max. time below 0.3V is $t = 2[\text{Arc sin}(0.3/0.8)]/120\pi$
 = 2.04 ms

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Current Monitor

The user may detect excessive current through the primary transformer winding in Figure 12 by placing a sensing resistor in the source or emitter of the switching transistor. The chip threshold at pin 8 is 225mV ±20mV. Similarly, it can be used on the secondary side as shown in Figure 15 in the application section.

Temperature Monitor

Temperature monitoring requires an external thermistor at pin 10 and a low tempo resistor at pin 11. This resistor is used to set the bias current, which is recommended to be between 5µA and 20µA. The chip supplies two equal currents and compares the voltages across the thermistor and the resistor. The user can now program a trip temperature where the thermistor resistance is going to equal or be slightly less than the resistor. At this temperature an internal comparator will switch. This feature allows the user to shut the system off if the temperature rises above the allowed range due to an overload or an absence of air flow. There is a hysteresis of 30mV ±10mV in the comparator to prevent oscillation.

Chip Power Supply Section and Voltage Reference

The system can work either as a current or voltage driven circuit ("current fed mode" and "voltage fed mode"). There is a shunt voltage regulator which uses a bandgap reference to set up a 5.8V ±0.2V internal chip supply. The chip is powered from a high voltage in the current fed mode through a resistor at pin 18. The system can alternatively be powered by a 4V to 5.5V DC power source connected directly to pin 18. The same bandgap reference can be used to define the thresholds for the fault monitor circuit.

Chip Initialization

When the power supply is first turned on, all outputs will be low; but this situation will readily be identified as a start up mode, since in normal use, one of the LED's will always be on. The NF output will turn ON when the monitored DC voltage reaches the nominal range. This prevents false fault indication during power up mode.

Logic and Fault Outputs

The circuit outputs are designed for driving opto-isolators, and are particular logic combinations of the outputs of the different monitors. When the chip is used on the primary side of the power supply, the outputs are as follows;

Output	Pin #	Function
Under-Voltage	15	UV = Loss of AC or Low AC or Low DC
Over-Voltage	16	OV = AC Over-Voltage or DC Over-Voltage
Over-Temperature	17	OT-OC = Over-Temperature or Over-Current
No Fault	14	NF = None of the Above Faults

As described, the same chip can be employed on the secondary side of the power supply system and monitor up to two DC voltages, as illustrated in Figure 15. The DC1 is connected to AC monitor and DC2 is connected to DC monitor. The temperature sensor may be retained. In this case the outputs are as follows;

Output	Pin #	Function
Under-Voltage	15	UV = Low DC1 or Low DC2
Over-Voltage	16	OV = Over-Voltage of DC1 or DC2
Over-Temperature	17	OT-OC = Over-Temperature or Over-Current
No Fault	14	NF = None of the Above Faults

System Performance

The key aspect of the system performance is the accuracy of the threshold levels. The system performance is presented with the following assumptions.

1. Resistors and capacitors are 1% accurate;
2. V_{REF} accuracy is ±2%;
3. System is connected as shown in Figure 12.

Error in AC UV & OV Detection	Error
Resistor divider error from inputs, R1, R2, R3, R4	1% + 1%
V _{REF} error	2%
Resistor divider error (V _{UV} or V _{OV}), R7, R8	1% + 1%
Internal comparator offset at inputs: 7.5 mV	0.75%
Internal resistor mismatch	1% + 1%
Total worst case error	8.75%
The RMS error of threshold voltage	3.25%

Error in DC UV & OV Detection	Error
Resistor divider error from inputs, R5, R6	1% + 1%
V _{REF} error	2%
Resistor divider error (V _{UV} or V _{OV}), R7, R8	1% + 1%
Internal comparator offset at inputs: 2.5 mV	0.25%
Total worst case error	6.25%
The RMS error of threshold voltage	2.84%

Over-Current Detection Error	Error
Resistor error, R11	1%
Internal comparator offset: 7.5 mV	3%
Fixed internal level error	5%
Total worst case error	9%
The RMS error of threshold current	6%

Over-Temperature Detection Error	Error
Resistor R9 error	1%
Thermistor RT error	5%
Overdrive at pin 10 referred to pin 11: 40 mV	2%
Total worst case error	8%
The RMS error	5.5%
For 85°C trip temperature, degrees of error	4.7°C - 6.8°C

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TYPICAL APPLICATIONS

Primary Side Power Fail Detector

Figure 12 shows a primary side power fail detector implementation.

The following is an example of the component calculations for the system.

Assume:

- A. Nominal AC voltage is 120V rms or 170V peak and the frequency is 60 Hz.
- B. Indications of over- and under-voltage occur with $\pm 25\%$ variations.
- C. Over-temperature is indicated when the temperature is above 85°C.
- D. Over-current is indicated when the current in the transformer primary winding exceeds 2A.
- E. Opto-isolator needs at least 0.8mA for its operation.

Calculations for resistor values:

Set $V_{OV} = V_{REF} = 1.254V$, then

$$V_{UV} = (75\%/125\%) \times V_{REF} = 0.752V$$

Choose V_{REF} current to be $10\mu A$, well within the spec. of $100\mu A$, then

$$R7 = V_{UV}/10\mu A = 75K$$

$$R8 = (V_{REF} - V_{UV})/10\mu A = 50K$$

The scaled AC and DC peak values are nominally 1V. The resistors are chosen with a power dissipation of $1/4$ watt.

The current through R1 and R2 should be less than

$$0.25 \text{ watts}/170V = 1.47mA, \text{ and}$$

$$R2/(R1 + R2) = 1V/170V, \text{ therefore,}$$

$R1 = 169K$ and $R2 = 1K$ will satisfy these conditions.

Calculating R3, R4, R5, and R6 in a similar manner gives $R3 = 169K$, $R4 = 1K$, $R5 = 169K$, $R6 = 1K$.

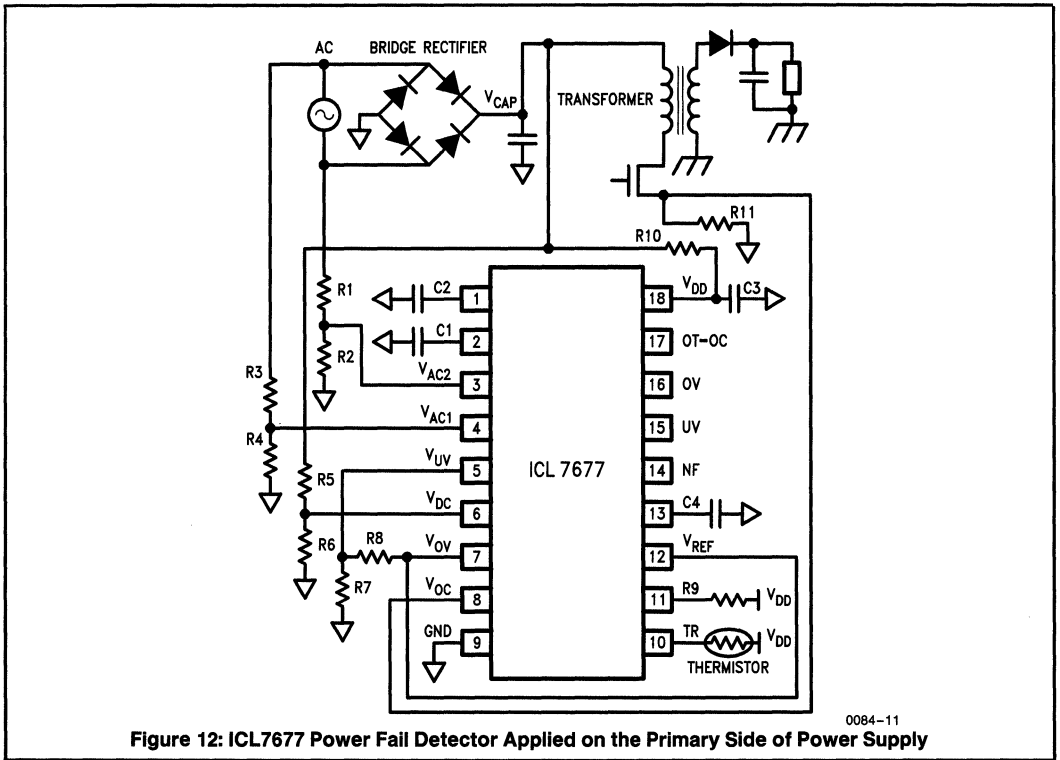


Figure 12: ICL7677 Power Fail Detector Applied on the Primary Side of Power Supply

0084-11

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NOTE: All typical values have been characterized but are not tested.

The resistors can then be corrected to preferred values.

For the current fed mode,

$$R10 = (V_R - V_{DD})/I_s$$

- where V_R = minimum expected reservoir voltage
- V_{DD} = supply voltage
- I_s = minimum supply current for the system.

The peak reservoir voltage is 170V, therefore the minimum expected reservoir voltage is $0.75 \times 170V$. In the current fed mode, $V_{DD} = 5.8V$. Because the chip requires less than 1.5mA and the output current for the opto-isolators is 0.8mA, 3mA should be sufficient for the system.

Therefore,

$$R10 = (0.75 \times 170V - 5.8V)/3 mA = 40K$$

Figure 13 shows the typical curve for bias current versus R9. Choosing R9 = 300kΩ results in a bias current of approximately 10μA. For temperature monitoring, a thermistor is then selected which is equal to or less than 300kΩ at 85°C.

The limit for over-current in the primary circuit is 2A. Therefore,

$$R11 = 245mV/2A = 0.12Ω.$$

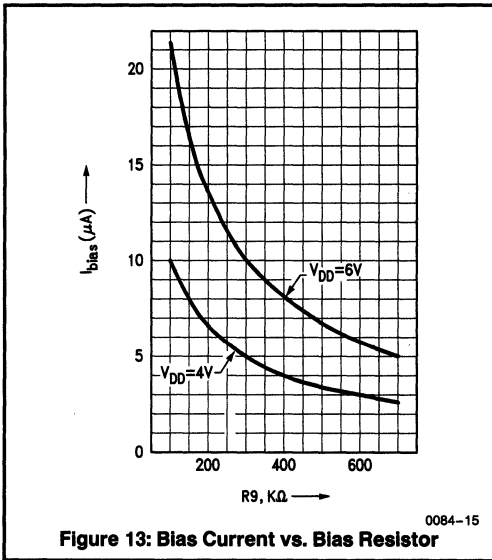


Figure 13: Bias Current vs. Bias Resistor

Calculations for capacitor values:

Assume the following time delays for fault indications:

(a) Loss of power:

The maximum time the signal will be below V_{zero} is

$$t = 2 \arcsin (V/A)/2\pi f$$

where A = lowest nominal peak value = 0.8V

$$V = V_{zero} = 0.3V$$

$$f = \text{frequency} = 60 \text{ Hz.}$$

$$\begin{aligned} \text{Therefore, } t &= 2[\arcsin (0.3/0.8)]/120(3.14) \\ &= 2.04 \text{ ms} \end{aligned}$$

The time delay for loss of power is therefore chosen to be 2.5 ms.

(b) Low AC: 12 ms, based on 8.33 ms half cycle time.

(c) High DC, high AC and low DC: 1.0 ms

Glitches less than 1 ms on the AC and DC supplies will then be ignored.

The time delay for fault detection is calculated as shown below and in Figure 14.

$$T = (C \times V_{DD}/2 \div I_{bias}) + 10 \mu s.$$

where T = time delay

C = delay capacitance

I_{bias} = bias current

$V_{DD}/2$ = voltage swing at comparator

10 μs = typical system delay.

Now, $C = T \times I_{bias}/(V_{DD}/2)$

where $I_{bias} = 10 \mu A$

$$V_{DD}/2 = 2.9V$$

$$\text{Therefore, } C_1 = 2.5 \text{ ms} \times 10 \mu A / 2.9V = 8.6 \text{ nF}$$

$$C_2 = 12 \text{ ms} \times 10 \mu A / 2.9V = 41.4 \text{ nF}$$

$$C_4 = 1.0 \text{ ms} \times 10 \mu A / 2.9V = 3.45 \text{ nF}$$

A 20μF capacitor is recommended for the decoupling capacitor, C3. If the reservoir voltage goes to zero abruptly, the load current of the part will be about 2 mA so it can sustain power to the part for approximately 15 ms.

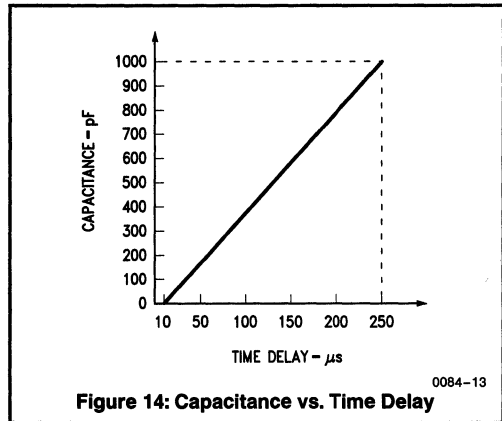


Figure 14: Capacitance vs. Time Delay

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NOTE: All typical values have been characterized but are not tested.

Secondary Side Power Fail Detector

The ICL7677 power fail detector can be applied on the secondary side as shown in Figure 15. Calculations for the external components follow the same procedure used in the primary side application.

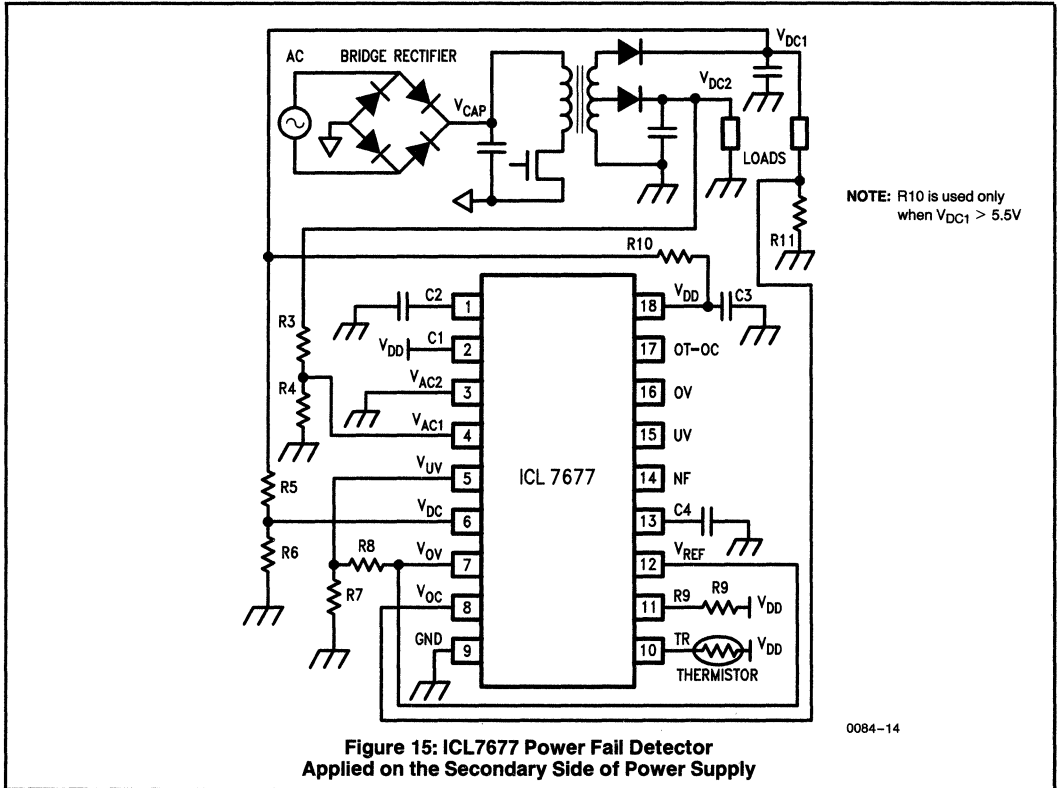


Figure 15: ICL7677 Power Fail Detector Applied on the Secondary Side of Power Supply

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NOTE: All typical values have been characterized but are not tested.

ICL7680

+5V to $\pm 15V$ Voltage Converter/Regulator



ICL7680

PRELIMINARY
Subject To Change Without Notice

GENERAL DESCRIPTION

The Intersil ICL7680 voltage converter provides the necessary control circuitry for independent regulation of both a single-ended, boost type and boost-buck (inverting) type switched-mode power supply. Specifically designed to operate in these two configurations, the ICL7680 is trimmed to provide both a +15V and -15V output with a +5V input voltage.

The internal circuitry is divided into two similar sections sharing a common voltage reference and oscillator: one for the boost stage and another for the inverting stage. Each section contains an error amplifier, comparator, and output logic which provide a standard pulse-width modulated output drive to an external transistor switch. The boost section senses the positive power supply output voltage via an internal thin film resistor divider which is trimmed for +15V. This voltage is user adjustable by adding an external resistor. Similarly, the inverting section senses the negative power supply output voltage at the input of an inverting amplifier that is trimmed for -15V.

The output logic provides the proper phase to drive an N-channel MOSFET on the boost side and a P-channel MOSFET on the inverting side. Although bipolar devices could be used, the chip is optimized for MOSFET drive and these devices will give higher efficiency.

For overcurrent protection, an internal comparator senses the voltage across an external resistor between the chip input supply pin and the current sense pin, shutting the circuit down for a voltage exceeding the limit.

Oscillator frequencies of 25 kHz, 50 kHz, or 100 kHz can be set with the three-state frequency select pin connected to GND left open, or connected to V_{IN} respectively. The sync pin can be overdriven, allowing the circuit to be run from an external system clock.

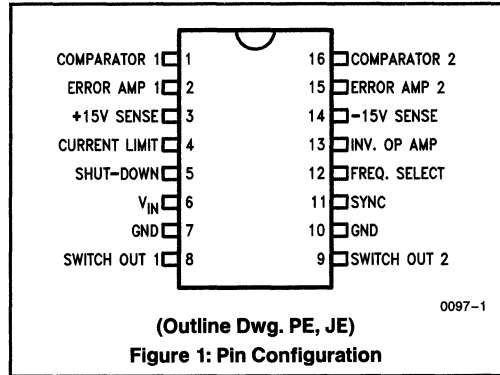
FEATURES

- Dual Output Voltages of $\pm 15V \pm 5\%$ Under All Conditions
- Output Voltage Externally Adjustable
- Input Current Sensing
- Three Frequency Oscillator, Selectable with a Single Pin
- Sync Pin Available
- No Off-Chip Trimming Required
- Minimum External Components
- Low Supply Current
- Built-In Latchup Protection

ORDERING INFORMATION

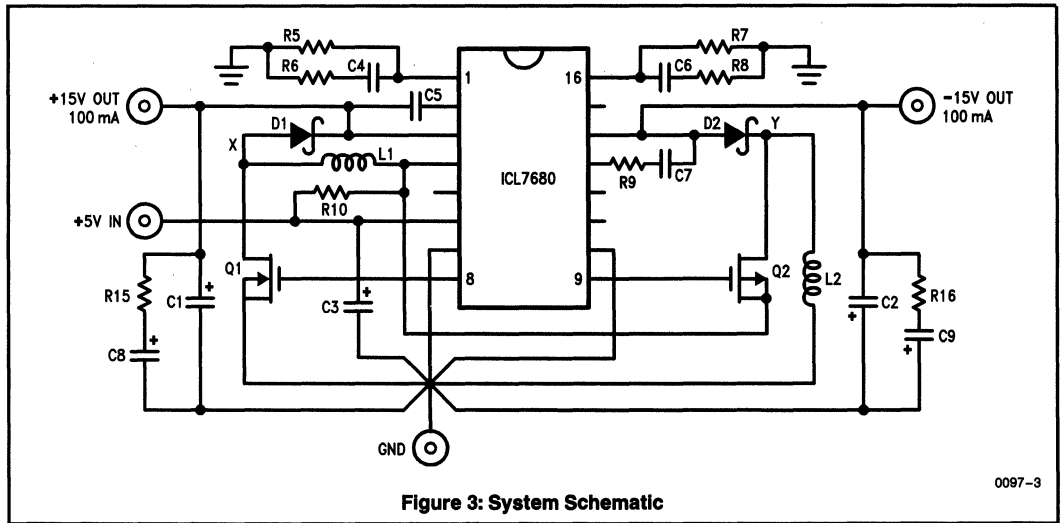
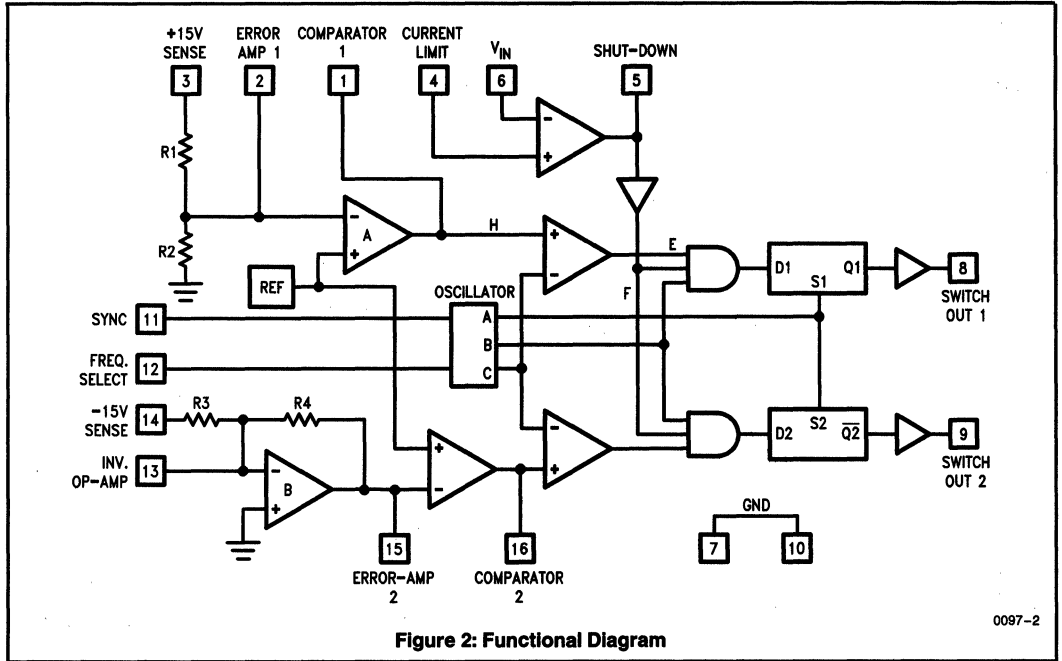
Part Number	Temperature Range	Package
ICL7680CPE	0°C to +70°C	16 Pin Plastic
ICL7680CJE		16 Pin CERDIP
ICL7680IJE	-25°C to +85°C	16 Pin CERDIP
ICL7680MJE	-55°C to +125°C	16 Pin CERDIP

5



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NOTE: All typical values have been characterized but are not tested.

ICL8211/ICL8212 Programmable Voltage Detector



ICL8211/ICL8212

GENERAL DESCRIPTION

The Intersil ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0°C to +70°C	8 lead Mini DIP
ICL8211CBA	0°C to +70°C	8 lead SOIC
ICL8211CTY	0°C to +70°C	TO-99 Can
ICL8211MTY*	-55°C to +125°C	TO-99 Can
ICL8212CPA	0°C to +70°C	8 lead Mini DIP
ICL8212CBA	0°C to +70°C	8 lead SOIC
ICL8212CTY	0°C to +70°C	TO-99 Can
ICL8212MTY*	-55°C to +125°C	TO-99 Can

* Add /883B to part number if 883B processing is required.

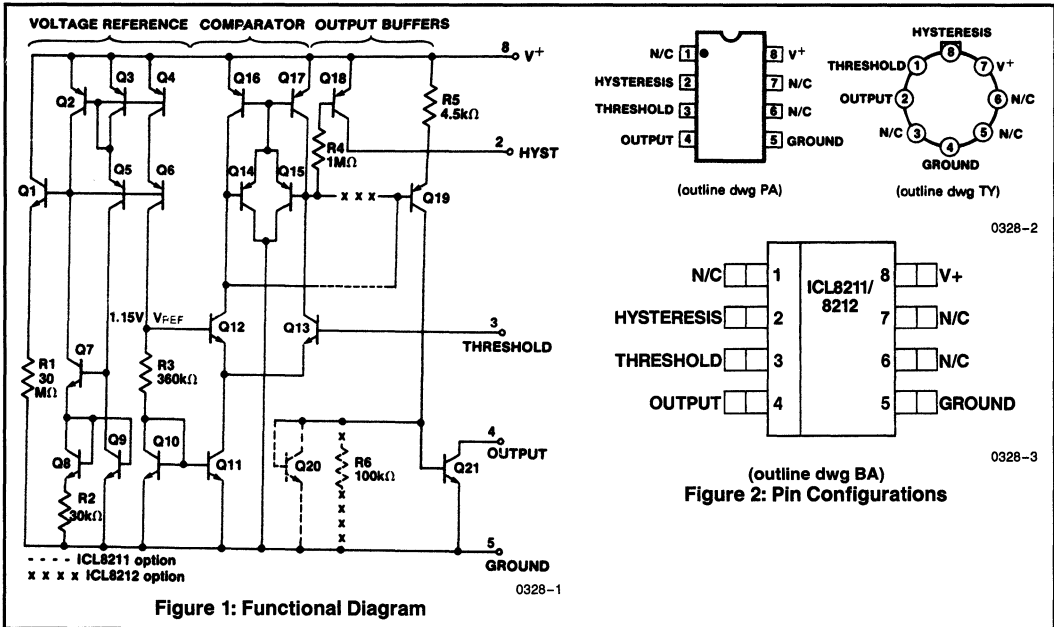
FEATURES

- High Accuracy Voltage Sensing and Generation: Internal Reference 1.15 Volts Typical
- Low Sensitivity to Supply Voltage and Temperature Variations
- Wide Supply Voltage Range: Typ. 1.8 to 30 Volts
- Essentially Constant Supply Current Over Full Supply Voltage Range
- Easy to Set Hysteresis Voltage Range
- Defined Output Current Limit — ICL8211
High Output Current Capability — ICL8212

APPLICATIONS

- Low Voltage Sensor/Indicator
- High Voltage Sensor/Indicator
- Non Volatile Out-of-Voltage Range Sensor/Indicator
- Programmable Voltage Reference or Zener Diode
- Series or Shunt Power Supply Regulator
- Fixed Value Constant Current Source

5



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NOTE: All typical values have been characterized but are not tested.

ICL8211/ICL8212



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	−0.5 to +30 volts
Output Voltage	−0.5 to +30 volts
Hysteresis Voltage	+0.5 to −10 volts
Threshold Input Voltage	−30 to +30 volts with respect to GROUND and +0 to −30 volts with respect to V+
Current into Any Terminal	±30mA

Power Dissipation (Note 1 & 2)	300mW
Operating Temperature Range:	
ICL8211M/8212M	−55°C to +125°C
ICL8211C/8212C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/8212MTY products. Derate linearly at −10mW/°C for ambient temperatures above 100°C.

NOTE 2: Derate linearly above 50°C by −10mW/°C for ICL8211C/8212C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

ELECTRICAL CHARACTERISTICS (V+ = 5V, TA = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	ICL8211			ICL8212			Units
			Min	Typ	Max	Min	Typ	Max	
I+	Supply Current	2.0 < V+ < 30 VT = 1.3V VT = 0.9V	10 50	22 140	40 250	50 10	110 10	250 20	μA μA
VTH	Threshold Trip Voltage	IOUT = 4mA VOUT = 2V	0.98 0.98 1.00	1.15 1.145 1.165	1.19 1.19 1.20	1.00 1.00 1.05	1.15 1.145 1.165	1.19 1.19 1.20	V V
VTHP	Threshold Voltage Disparity Between Output & Hysteresis Output	IOUT = 4mA IHYST = 7μA		−8.0			−0.5		mV
VSUPPLY	Guaranteed Operating Supply Voltage Range (Note 5)	+25°C 0 to +70°C −55°C to +125°C	2.0 2.2 2.8		30 30 30	2.0 2.2 2.8		30 30 30	V V
VSUPPLY	Typical Operating Supply Voltage Range	+25°C +125°C −55°C	1.8 1.4 2.5		30 30 30	1.8 1.4 2.5		30 30 30	V V
ΔVTH/ΔT	Threshold Voltage Temperature Coefficient	IOUT = 4mA VOUT = 2V		+200			+200		ppm/°C
ΔVTH/ΔV+	Variation of Threshold Voltage with Supply Voltage	ΔV+ = 10% at V+ = 5V		1.0			1.0		mV
ITH	Threshold Input Current	VTH = 1.15V VTH = 1.00V		100 5	250		100 5	250	nA nA
IOLK	Output Leakage Current	VOUT = 30V VOUT = 30V VOUT = 5V VOUT = 5V			10 1		10 1		μA μA μA
VSAT	Output Saturation Voltage	IOUT = 4mA		0.17	0.4		0.17	0.4	V V
Ioh	Max Available Output Current	(Note 3 & 4) VOUT = 5V −55°C ≤ TA ≤ 125°C	4	7.0	12 15	15 12	35		mA mA
Ihys	Hysteresis Leakage Current	V+ = 10V VHYST = V−			0.1			0.1	μA
Vhys (max)	Hysteresis Sat Voltage	IHYST = −7μA measured with respect to V+		−0.1	−0.2		−0.1	−0.2	V
Ihys (max)	Max Available Hysteresis Current		−15	−21		−15	−21		μA

NOTES: 3. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.

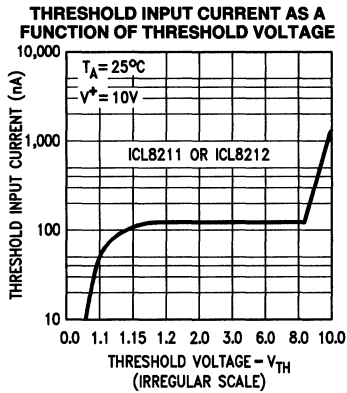
4. The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.

5. Threshold Trip Voltage is 0.80V(min) to 1.30V(max).

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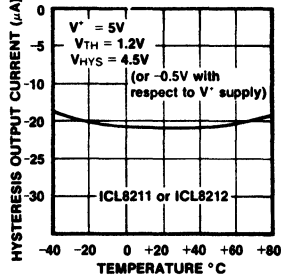
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS COMMON TO ICL8211 AND ICL8212



0328-4

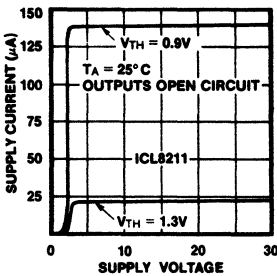
HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



0328-5

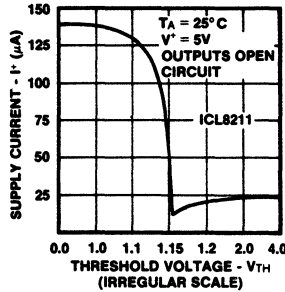
TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



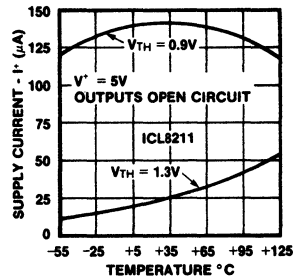
0328-6

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



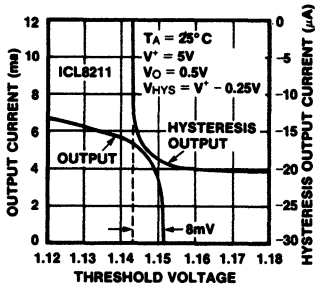
0328-7

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



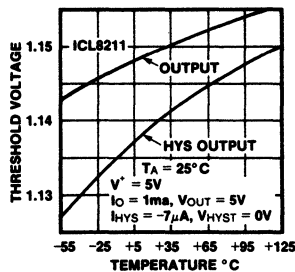
0328-8

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



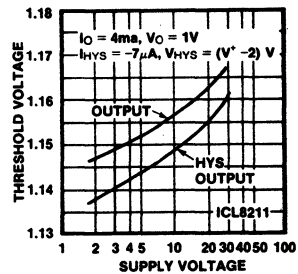
0328-9

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



0328-10

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



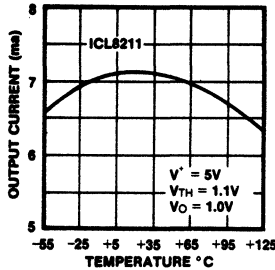
0328-11

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NOTE: All typical values have been characterized but are not tested.

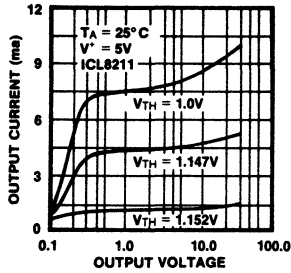
TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY (Continued)

OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



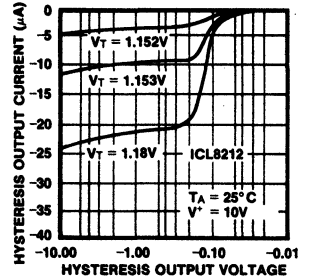
0328-12

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



0328-13

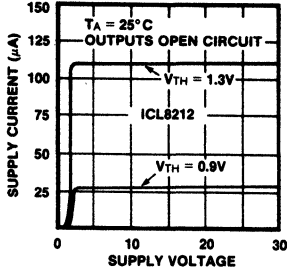
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



0328-14

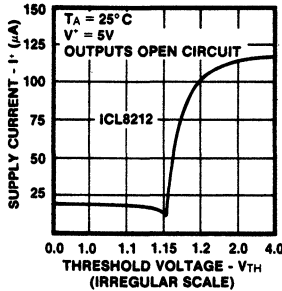
TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



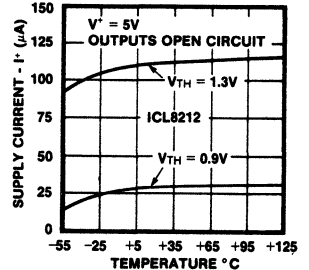
0328-15

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



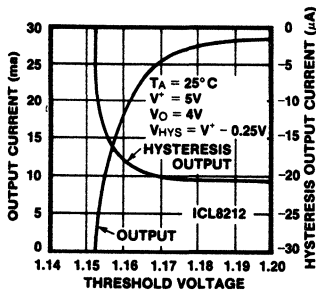
0328-16

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



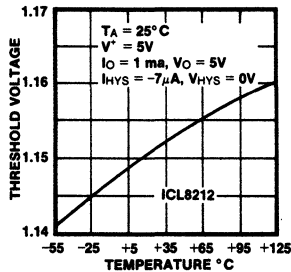
0328-17

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



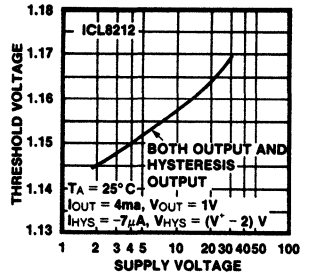
0328-18

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



0328-19

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



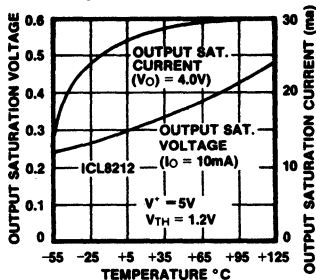
0328-20

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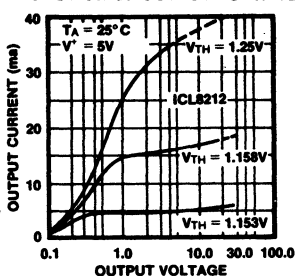
TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY (Continued)

OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



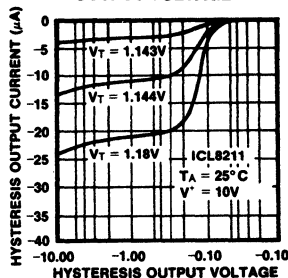
0328-21

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



0328-22

HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



0328-23

DETAILED DESCRIPTION

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 thru Q_{10} and R_1 , R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per $^{\circ}\text{C}$).

Components Q_2 thru Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9 , and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$I_C (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ln 7$$

or approximately $1\mu\text{A}$ at 25°C

Where k = Boltzman's constant

q = charge on an electron

and T = absolute temperature in $^{\circ}\text{K}$

Transistors Q_5 , Q_6 , and Q_7 assure that the V_{CE} of Q_3 , Q_4 , and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant source; there being two stable states for this type of circuit — either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2 ; Q_{10} is matched to Q_9 . Thus the I_C and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8 . To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.15 = V_{BE} (Q_8 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ln 7$$

which provides $\frac{R_3}{R_2} = 12$ (approx.)

The total supply current consumed by the voltage reference section is approximately $6\mu\text{A}$ at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17} . The outputs from the comparator are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to $100\mu\text{A}$.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7mA , whereas for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21} , resulting in a maximum available collector current of the order of 30mA . It is advisable to externally limit this current to 25mA or less.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

General Information

THRESHOLD INPUT CONSIDERATIONS

Although any voltage between -5V and V^+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about $+6$ volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

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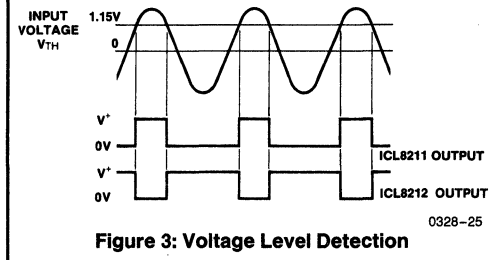
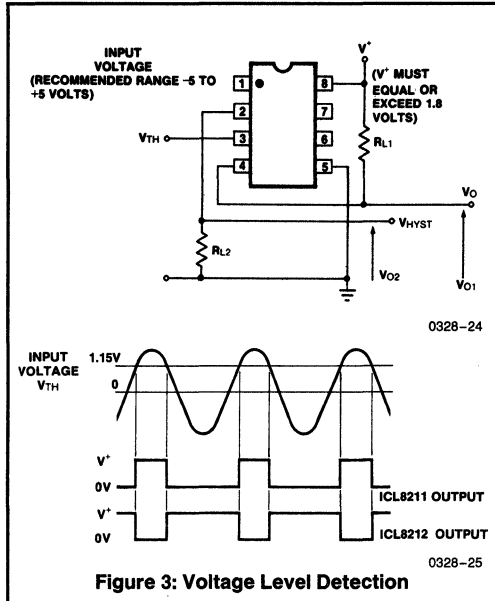


Figure 3: Voltage Level Detection

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 3 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10µA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

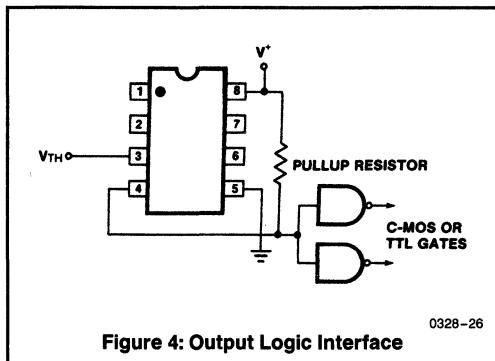


Figure 4: Output Logic Interface

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for VTH. For high accuracy, currents as large as 50µA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6µA may be considered without a great loss of accuracy. 6µA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

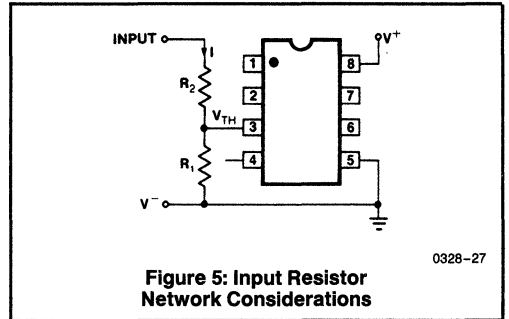


Figure 5: Input Resistor Network Considerations

Case 1. High accuracy required, current in resistor network unimportant Set $I = 50\mu A$ for $V_{TH} = 1.15$ volts
 $\therefore R_1 \rightarrow 20k\Omega$.

Case 2. Good accuracy required, current in resistor network important Set $I = 7.5\mu A$ for $V_{TH} = 1.15$ volts
 $\therefore R_1 \rightarrow 150k\Omega$.

SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection — no hysteresis

Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 7 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

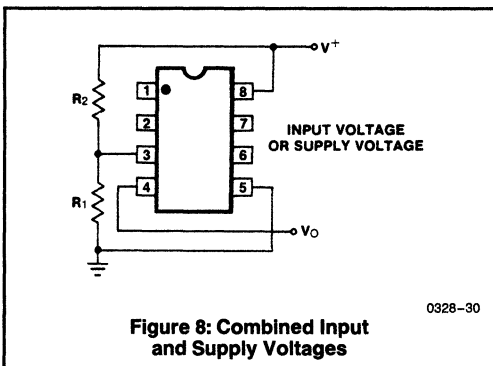
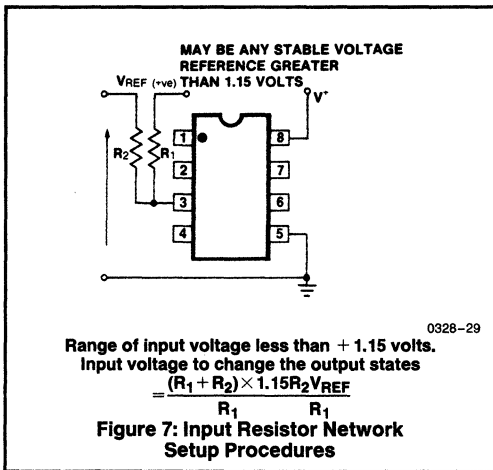
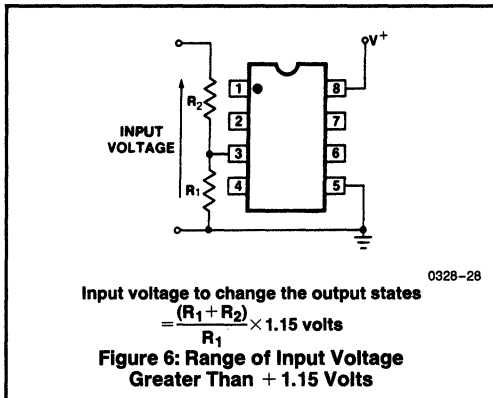
For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 8.

Conditions for correct operation of OUTPUT (terminal #4).

1. ICL8211
 $1.8V \leq V^+ \leq 30V$
2. ICL8212
 $0 \leq V^+ \leq 30V$

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NOTE: All typical values have been characterized but are not tested.



Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind

hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications — refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 9.

The circuit (a) of Figure 9 requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output, whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

Practical Applications

a) Low Voltage Battery Indicator

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35µA which will increase to 7mA when the lamp is turned on. R₃ will provide hysteresis if required.

b) |Non-Volatile| Low Voltage Detector

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S₁ the operating point changes to B and will remain at B until the supply voltage drops below V_{TR1}, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

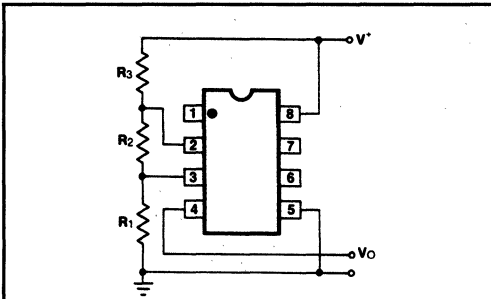
c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

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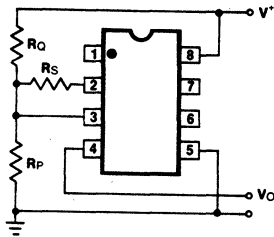
0328-31

Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2 \times 1.15)}{R_1} + 0.1 \right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



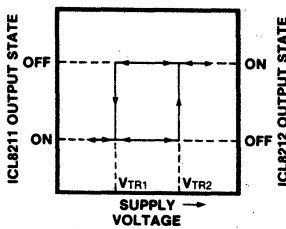
0328-32

Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + R_P \right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

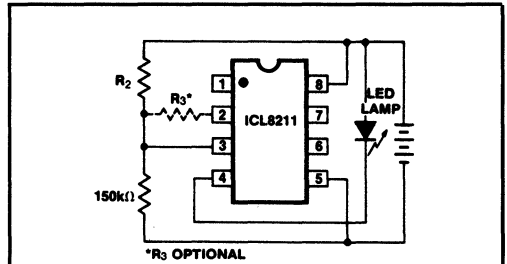
High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$

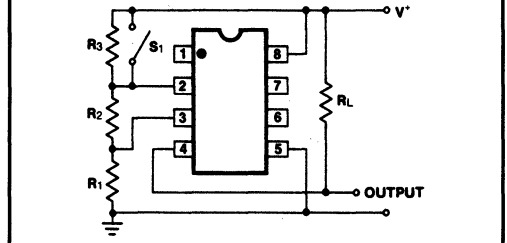


0328-33

Figure 9: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

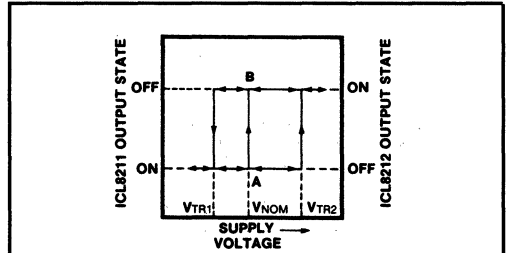


0328-34



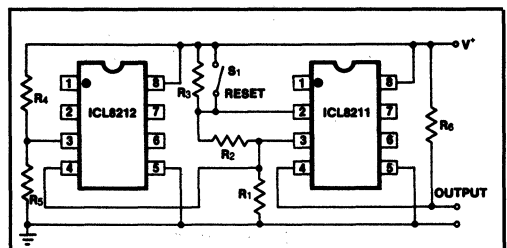
0328-35

Figure 10: Low Voltage Battery Indicator



0328-36

Figure 11: Low Voltage Detector and Memory



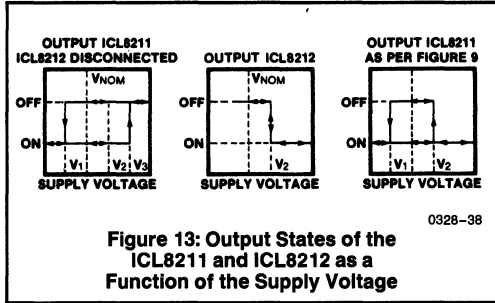
0328-37

Figure 12: Schematic of Recorder

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A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.



Referring to Figure 12, the ICL8212 is used to detect a voltage, V_2 , which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1 . Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 — the upper trip point of the ICL8211 much higher in voltage than V_2 .

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2 . Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2 .

d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately $25\mu\text{A}$ by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a $130\mu\text{A}$ constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

e) Zener or Precision Voltage Reference

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

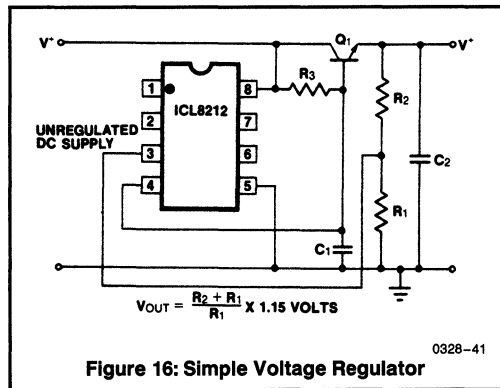
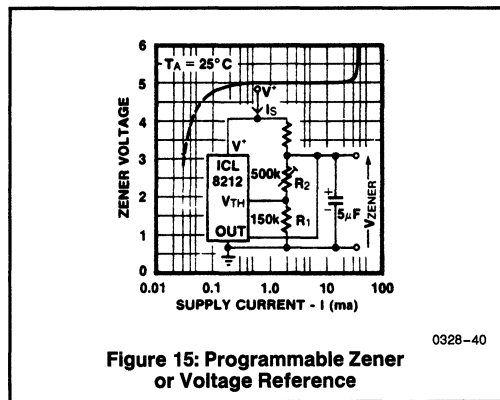
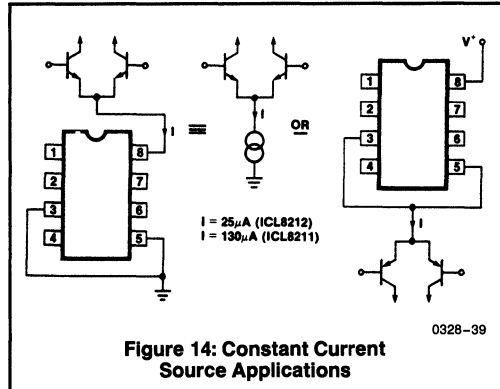
$$V_{\text{zener}} = \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts.}$$

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between $300\mu\text{A}$ and 25mA will range from 4 to 7Ω . The knee is sharper and occurs at a significantly lower current than other similar devices available.

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f) Precision Voltage Regulators

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2 . Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

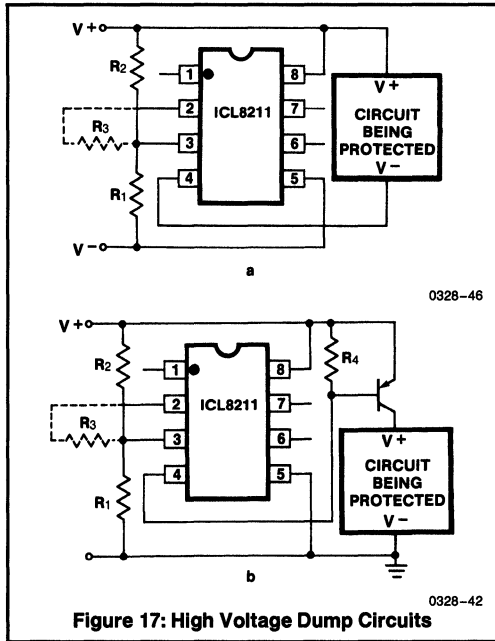


Figure 17: High Voltage Dump Circuits

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than

any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

g) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R₁ and R₂ set up the disconnect voltage and R₃ provides optional voltage hysteresis if so desired.

h) Frequency limit detectors

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R₃, R₄ and C₂ results in a slow output positive ramp. The negative range is much faster than the positive range. R₅ and R₆ provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C₃. The time constant of R₇ C₃ is much greater than R₄ C₂. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

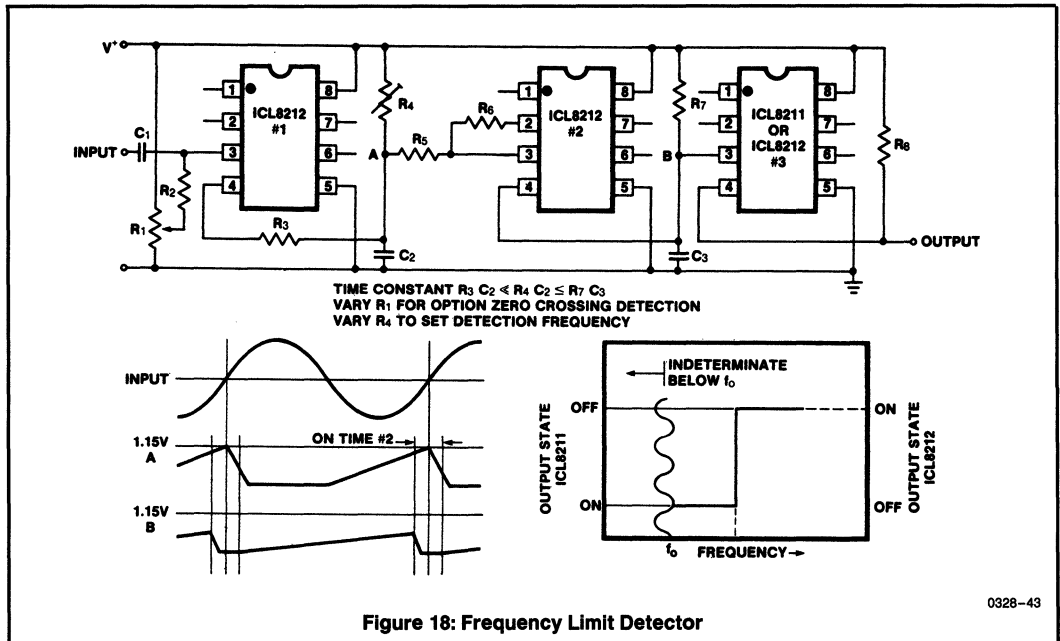


Figure 18: Frequency Limit Detector

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ICL8211/ICL8212



ICL8211/ICL8212

i) Switch bounce filter

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 19 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of $R_1 C_1$ to approximately the manufacturer's bounce time the output as terminal # 4 of the ICL8211/8212 will be a single transition of state per desired switch closure.

j) Low voltage power disconnect

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212" by D. Watson.

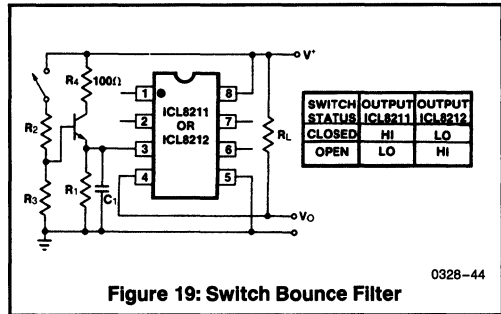


Figure 19: Switch Bounce Filter

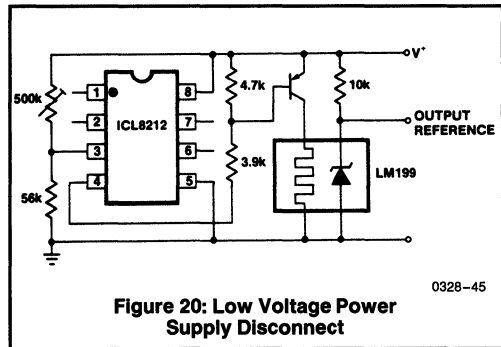


Figure 20: Low Voltage Power Supply Disconnect

5

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Section 6 — Special Analog

AD590	6-1
ICL8013	6-12
ICL8038	6-21
ICL8048	6-30
ICL8049	6-30
ICL8069	6-39

AD590

2-Wire Current Output Temperature Transducer



AD590

GENERAL DESCRIPTION

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing $1\mu\text{A}/^\circ\text{K}$ for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2 μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature-sensing application between -55°C and +150°C (0°C and 70°C for TO-92) in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance-measuring circuitry and cold-junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

FEATURES

- Linear Current Output: $1\mu\text{A}/^\circ\text{K}$
- Wide Range: -55°C to +150°C
- Two-Terminal Device: Voltage In/Current Out
- Laser Trimmed to $\pm 0.5^\circ\text{C}$ Calibration Accuracy (AD590M)
- Excellent Linearity: $\pm 0.5^\circ\text{C}$ Over Full Range (AD590M)
- Wide Power Supply Range: +4V to +30V
- Sensor Isolation From Case
- Low Cost

ORDERING INFORMATION

Non-Linearity (°C)	Part Number	Temperature Range	Package
± 3.0	AD590IH	-55°C to +150°C	TO-52
± 1.5	AD590JH	-55°C to +150°C	TO-52

6

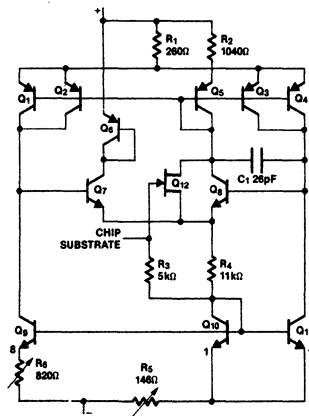


Figure 1: Functional Diagram

0318-1

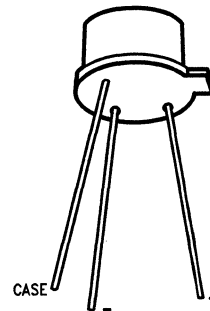


Figure 2: Pin Configurations

0318-2

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Forward Voltage (V^+ to V^-)	+44V	Rated Performance Temperature Range	
Reverse Voltage (V^+ to V^-)	-20V	TO-52	-55°C to +150°C
Breakdown Voltage (Case to V^+ or V^-)	$\pm 200\text{V}$	Lead Temperature (Soldering, 10sec)	+300°C
Storage Temperature Range	-65°C to +150°C		

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (Typical values at $T_A = +25^\circ\text{C}$, $V^+ = 5\text{V}$ unless otherwise noted)

Characteristics	AD590I	AD590J	Units
Output			
Nominal Output Current @ +125°C(298.2°K)	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	$\mu\text{A}/^\circ\text{K}$
Calibration Error @ +25°C (Notes 1, 5)	± 10.0 max	± 5.0 max	$^\circ\text{C}$
Absolute Error (-55°C to +150°C) (Note 7)			
Without External Calibration Adjustment	± 20.0 max	± 10.0 max	$^\circ\text{C}$
With External Calibration Adjustment	± 5.8 max	± 3.0 max	$^\circ\text{C}$
Non-Linearity (Note 6)	± 3.0 max	± 1.5 max	$^\circ\text{C}$
Repeatability (Notes 2, 6)	± 0.1 max	± 0.1 max	$^\circ\text{C}$
Long Term Drift (Notes 3, 6)	± 0.1 max	± 0.1 max	$^\circ\text{C}/\text{month}$
Current Noise	40	40	$\text{pA}/\sqrt{\text{Hz}}$
Power Supply Rejection:			
+4V < V^+ < +5V	0.5	0.5	$\mu\text{A}/\text{V}$
+5V < V^+ < +15V	0.2	0.2	$\mu\text{A}/\text{V}$
+15V < V^+ < +30V	0.1	0.1	$\mu\text{A}/\text{V}$
Case Isolation to Either Lead	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	V

- NOTES:**
- Does not include self heating effects.
 - Maximum deviation between +25°C reading after temperature cycling between -55°C and +150°C.
 - Conditions: Constant +5V, constant +125°C.
 - Leakage current doubles every +10°C.
 - Mechanical strain on package may disturb calibration of device.
 - Guaranteed. But not tested.
 - 55°C Guaranteed by testing @ +25°C and @ +150°C.

TRIMMING OUT ERRORS

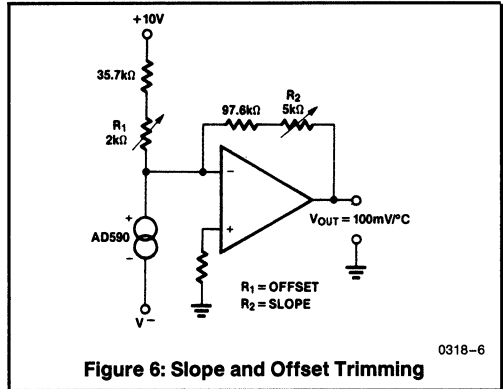
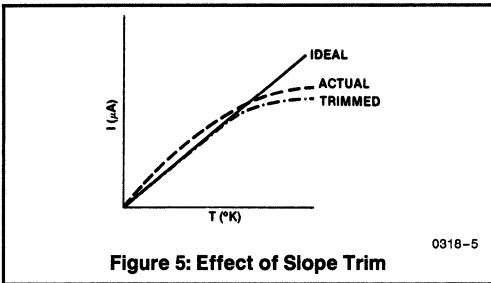
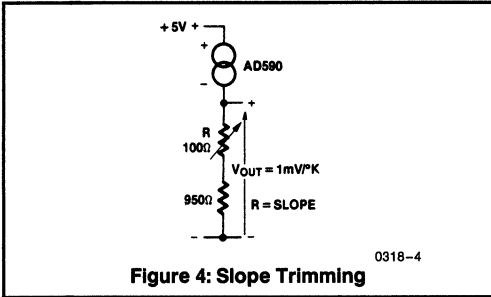
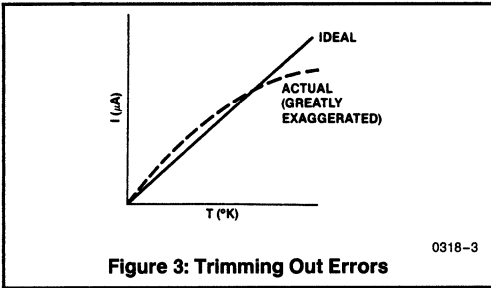
The ideal graph of current versus temperature for the AD590 is a straight line, but as Figure 3 shows, the actual shape is slightly different. Since the sensor is limited to the range of -55°C to +150°C, it is possible to optimize the accuracy by trimming. Trimming also permits extracting maximum performance from the lower-cost sensors.

The circuit of Figure 4 trims the slope of the AD590 output. The effect of this is shown in Figure 5.

The circuit of Figure 6 trims both the slope and the offset. This is shown in Figure 7. The diagrams are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over the whole range, or over any selected part of the range. In fact, it is possible to adjust the I-grade device to give less than 0.1°C error over the range 0°C to 90°C and less than 0.05°C error from 25°C to 60°C.

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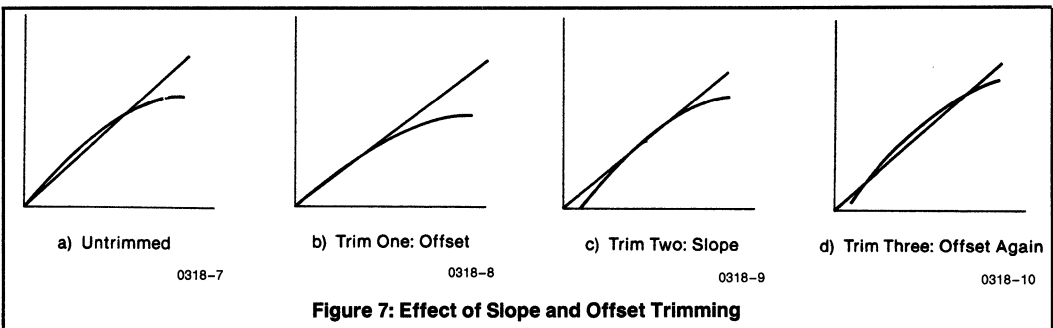
NOTE: All typical values have been characterized but are not tested.



ACCURACY

Maximum errors over limited temperature spans, with $V_s = +5V$, are listed by device grade in the following tables. The tables reflect the worst-case linearities, which invariably occur at the extremities of the specified temperature range. The trimming conditions for the data in the tables are shown in Figures 4 and 5.

All errors listed in the tables are $\pm^\circ C$. For example, if $\pm 1^\circ C$ maximum error is required over the $+25^\circ C$ to $+75^\circ C$ range (i.e., lowest temperature of $+25^\circ C$ and span of $50^\circ C$), then the trimming of a J-grade device, using the single-trim circuit (Figure 4), will result in output having the required accuracy over the stated range. An M-grade device with no trims will have less than $\pm 0.9^\circ C$ error, and an I-grade device with two trims (Figure 5) will have less than $\pm 0.2^\circ C$ error. If the requirement is for less than $\pm 1.4^\circ C$ maximum error, from $-25^\circ C$ to $+75^\circ C$ (100° span from $-25^\circ C$), it can be satisfied by an M-grade device with no trims, a K-grade device with one trim, or an I-grade device with two trims.



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I GRADE — MAXIMUM ERRORS, °C

Number of Trims	Temperature Span—°C	Lowest Temperature in Span—°C							
		-55	-25	0	+25	+50	+75	+100	+125
None	10	8.4	9.2	10.0	10.8	11.6	12.4	13.2	14.4
None	25	10.0	10.4	11.0	11.8	12.0	13.8	15.0	16.0
None	50	13.0	13.0	12.8	13.8	14.6	16.4	18.0	
None	100	15.2	16.0	16.6	17.4	18.8			
None	150	18.4	19.0	19.2					
None	205	20.0							
One	10	0.6	0.4	0.4	0.4	0.4	0.4	0.4	0.6
One	25	1.8	1.2	1.0	1.0	1.0	1.2	1.6	1.8
One	50	3.8	3.0	2.0	2.0	2.0	3.0	3.8	
One	100	4.8	4.5	4.2	4.2	5.0			
One	150	5.5	4.8	5.5					
One	205	5.8							
Two	10	0.3	0.2	0.1	*	*	0.1	0.2	0.3
Two	25	0.5	0.3	0.2	*	0.1	0.2	0.3	0.5
Two	50	1.2	0.6	0.4	0.2	0.2	0.3	0.7	
Two	100	1.8	1.4	1.0	2.0	2.5			
Two	150	2.6	2.0	2.8					
Two	205	3.0							

* Less than 0.05°C.

J GRADE — MAXIMUM ERRORS, °C

Number of Trims	Temperature Span—°C	Lowest Temperature in Span—°C							
		-55	-25	0	+25	+50	+75	+100	+125
None	10	4.2	4.6	5.0	5.4	5.8	6.2	6.6	7.2
None	25	5.0	5.2	5.5	5.9	6.0	6.9	7.5	8.0
None	50	6.5	6.5	6.4	6.9	7.3	8.2	9.0	
None	100	7.7	8.0	8.3	8.7	9.4			
None	150	9.2	9.5	9.6					
None	205	10.0							
One	10	0.3	0.2	0.2	0.2	0.2	0.2	0.2	0.3
One	25	0.9	0.6	0.5	0.5	0.5	0.6	0.8	0.9
One	50	1.9	1.5	1.0	1.0	1.0	1.5	1.9	
One	100	2.3	2.2	2.0	2.0	2.3			
One	150	2.5	2.4	2.5					
One	205	3.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.2	0.1	*	*	*	*	0.1	0.2
Two	50	0.4	0.2	0.1	*	*	0.1	0.2	*
Two	100	0.7	0.5	0.3	0.7	1.0			
Two	150	1.0	0.7	1.2					
Two	205	1.6							

* Less than ±0.05°C.

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NOTE: All typical values have been characterized but are not tested.

NOTES

1. Maximum errors over all ranges are guaranteed based on the known behavior characteristic of the AD590.
2. For one-trim accuracy specifications, the 205°C span is assumed to be trimmed at +25°C; for all other spans, it is assumed that the device is trimmed at the midpoint.
3. For the 205°C span, it is assumed that the two-trim temperatures are in the vicinity of 0°C and +140°C; for all other spans, the specified trims are at the endpoints.
4. In precision applications, the actual errors encountered are usually dependent upon sources of error which are often overlooked in error budgets. These typically include:
 - a. Trim error in the calibration technique used
 - b. Repeatability error
 - c. Long-term drift errors

Trim error is usually the largest error source. This error arises from such causes as poor thermal coupling between the device to be calibrated and the reference sensor; reference sensor errors; lack of adequate time for the device being calibrated to settle to the final temperature; radically different thermal resistances between the case and the surroundings ($R_{\theta CA}$) when trimming and when applying the device.

Repeatability errors arise from a strain hysteresis of the package. The magnitude of this error is solely a function of the magnitude of the temperature span over which the device is used. For example, thermal shocks between 0°C and 100°C involve extremely low hysteresis and result in repeatability errors of less than $\pm 0.05^\circ\text{C}$. When the thermal-shock excursion is widened to -55°C to $+150^\circ\text{C}$, the device will typically exhibit a repeatability error of $\pm 0.05^\circ\text{C}$ (± 0.10 guaranteed maximum).

Long-term drift errors are related to the average operating temperature and the magnitude of the thermal shocks experienced by the device. Extended use of the AD590 at temperatures above 100°C typically results in long-term drift of $\pm 0.03^\circ\text{C}$ per month; the guaranteed maximum is $\pm 0.10^\circ\text{C}$ per month. Continuous operation at temperatures below 100°C induces no measurable drifts in the device. Besides the effects of operating temperature, the severity of thermal shocks incurred will also affect absolute stability. For thermal-shock excursions less than 100°C, the drift is difficult to measure ($< 0.03^\circ\text{C}$). However, for 200°C excursions, the device may drift by as much as $\pm 0.10^\circ\text{C}$ after twenty such shocks. If severe, quick shocks are necessary in the application of the device, realistic simulated life tests are recommended for a thorough evaluation of the error introduced by such shocks.

TYPICAL APPLICATIONS

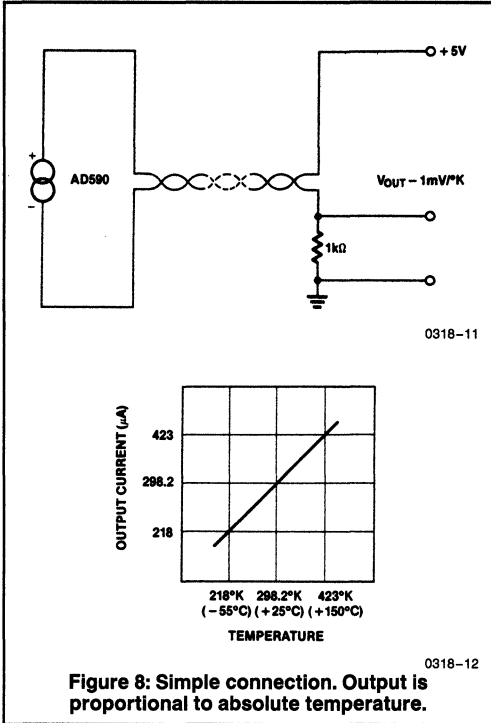


Figure 8: Simple connection. Output is proportional to absolute temperature.

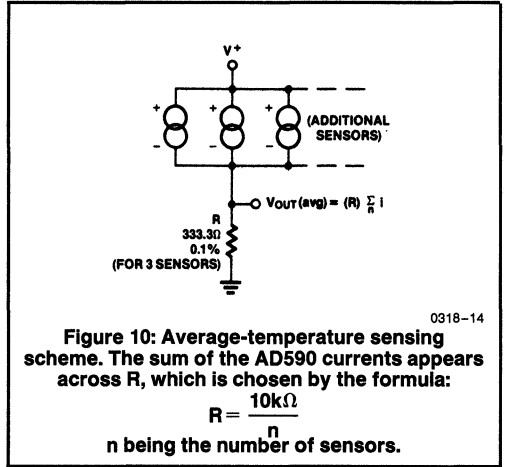


Figure 10: Average-temperature sensing scheme. The sum of the AD590 currents appears across R, which is chosen by the formula:

$$R = \frac{10k\Omega}{n}$$

n being the number of sensors.

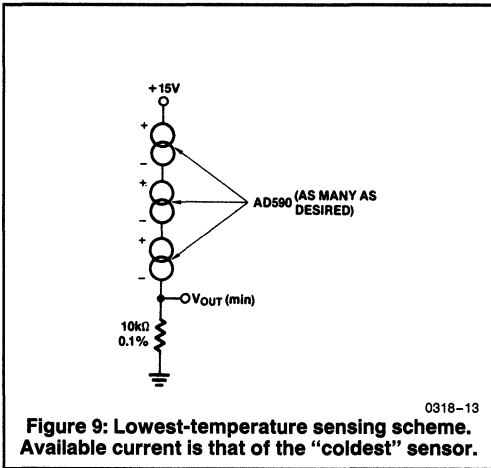
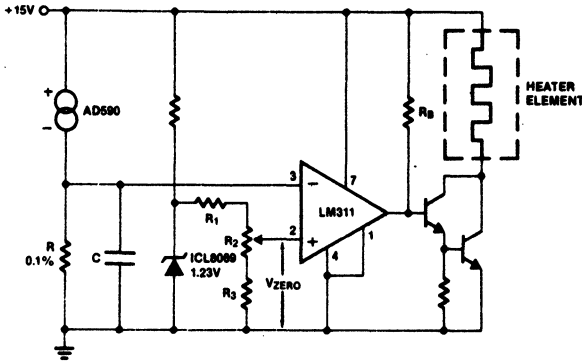


Figure 9: Lowest-temperature sensing scheme. Available current is that of the "coldest" sensor.

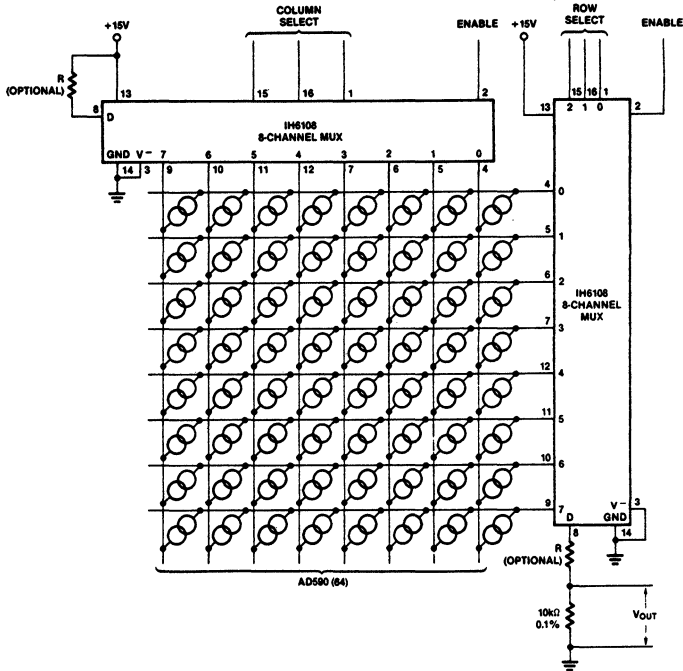
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NOTE: All typical values have been characterized but are not tested.



0318-15

Figure 11: Single-setpoint temperature controller. The AD590 produces a temperature-dependent voltage across R (C is for filtering noise). Setting R_2 produces a scale-zero voltage. For the Celsius scale, make $R = 1k\Omega$ and $V_{ZERO} = 0.273$ volts. For Fahrenheit, $R = 1.8k\Omega$ and $V_{ZERO} = 0.460$ volts.

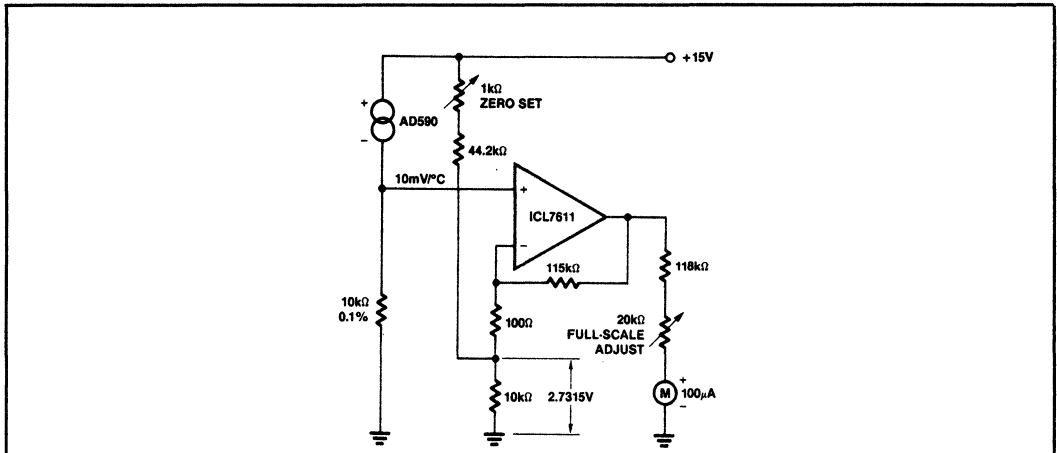


0318-16

Figure 12: Multiplexing sensors. If shorted sensors are possible, a series resistor in series with the D line will limit the current (shown as R, above: only one is needed). A six-bit digital word will select one of 64 sensors.

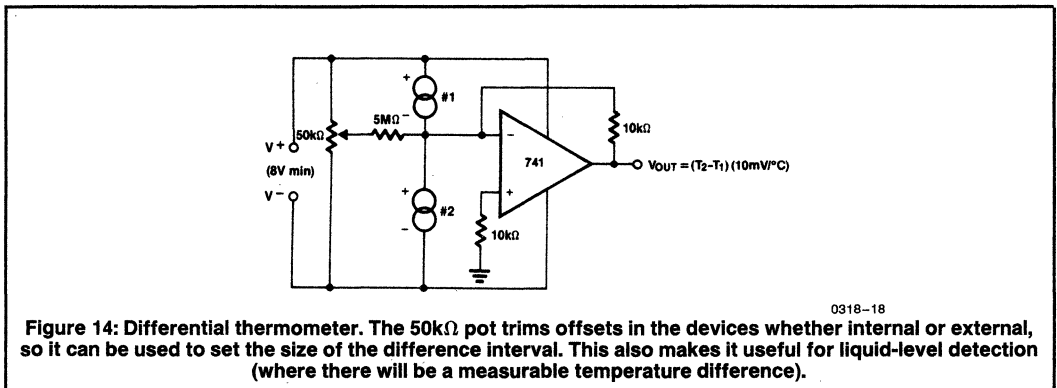
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NOTE: All typical values have been characterized but are not tested.



0318-17

Figure 13: Centigrade thermometer (0°C – 100°C) . the ultra-low bias current of the ICL7611 allows the use of large-value gain-resistors, keeping meter-current error under 1/2%, and therefore saving the expense of an extra meter-driving amplifier.

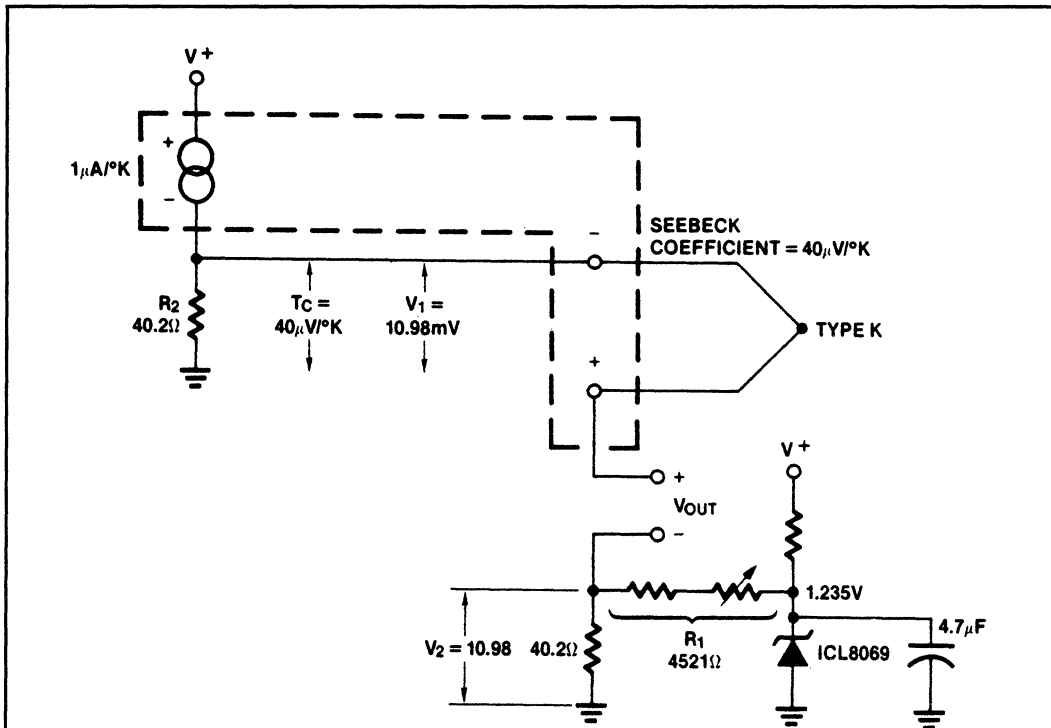


0318-18

Figure 14: Differential thermometer. The 50kΩ pot trims offsets in the devices whether internal or external, so it can be used to set the size of the difference interval. This also makes it useful for liquid-level detection (where there will be a measurable temperature difference).

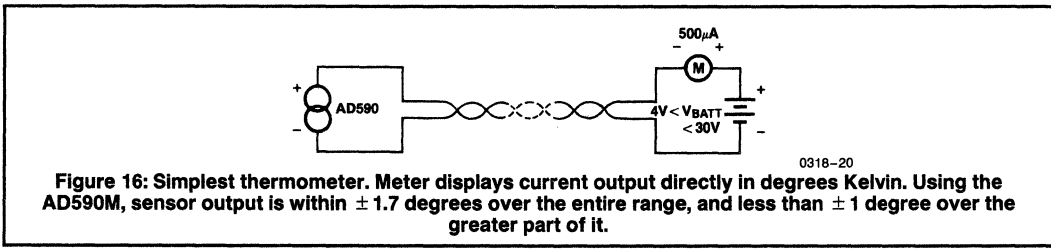
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0318-19

Figure 15: Cold-junction compensation for type K thermocouple. The reference junction(s) should be in close thermal contact with the AD590 case. V^+ must be at least 4V, while ICL8069 current should be set at 1mA – 2mA. Calibration does not require shorting or removal of the thermocouple: set R_1 for $V_2 = 10.98\text{mV}$. If very precise measurements are needed, adjust R_2 to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V_1 , and set R_1 to buck out this voltage (i.e., set $V_2 = V_1$). For other thermocouple types, adjust values to the appropriate Seebeck coefficient.

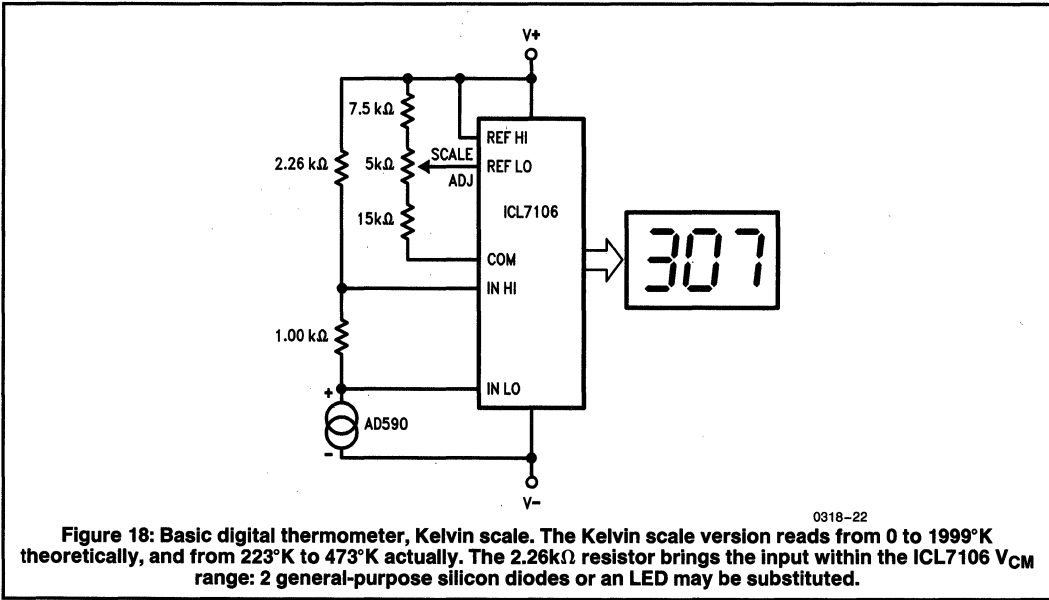
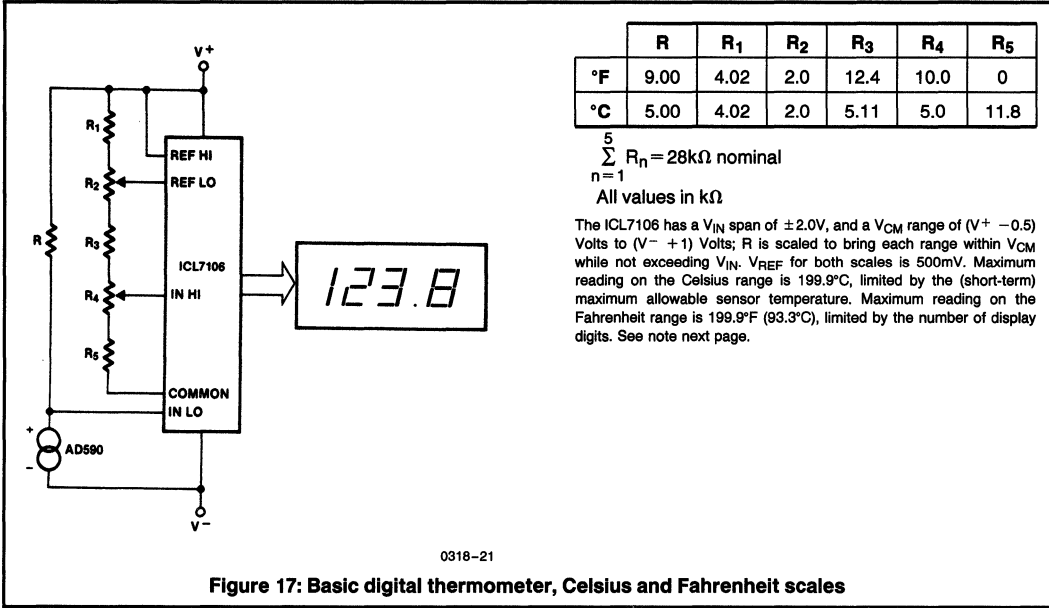


0318-20

Figure 16: Simplest thermometer. Meter displays current output directly in degrees Kelvin. Using the AD590M, sensor output is within ± 1.7 degrees over the entire range, and less than ± 1 degree over the greater part of it.

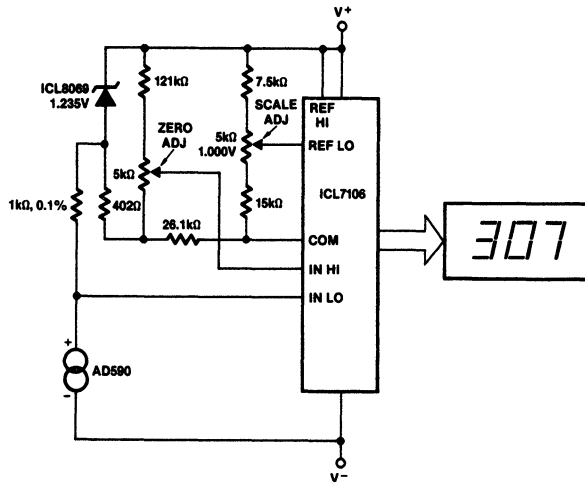
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NOTE: All typical values have been characterized but are not tested.



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0318-23

Figure 19: Basic digital thermometer, Kelvin scale with zero adjust. This circuit allows “zero adjustment” as well as slope adjustment. The ICL8069 brings the input within the common-mode range, while the 5kΩ pots trim any offset at 218°K (−55°C), and set the scale factor.

Note on Figure 17, Figure 18 and Figure 19: Since all 3 scales have narrow V_{IN} spans, some optimization of ICL7106 components can be made to lower noise and preserve CMR. The table below shows the suggested values. Similar scaling can be used with the ICL7126/36.

Scale	V_{IN} Range (V)	$R_{INT}(k\Omega)$	$C_{AZ}(\mu F)$
K	0.223 to 0.473	220	0.47
C	−0.25 to +1.0	220	0.1
F	−0.29 to +0.996	220	0.1

For all:

$C_{REF} = 0.1 \mu F$

$C_{OSC} = 100 pF$

$C_{INT} = 0.22 \mu F$

$R_{OSC} = 100 k\Omega$

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ICL8013

Four Quadrant Analog Multiplier



GENERAL DESCRIPTION

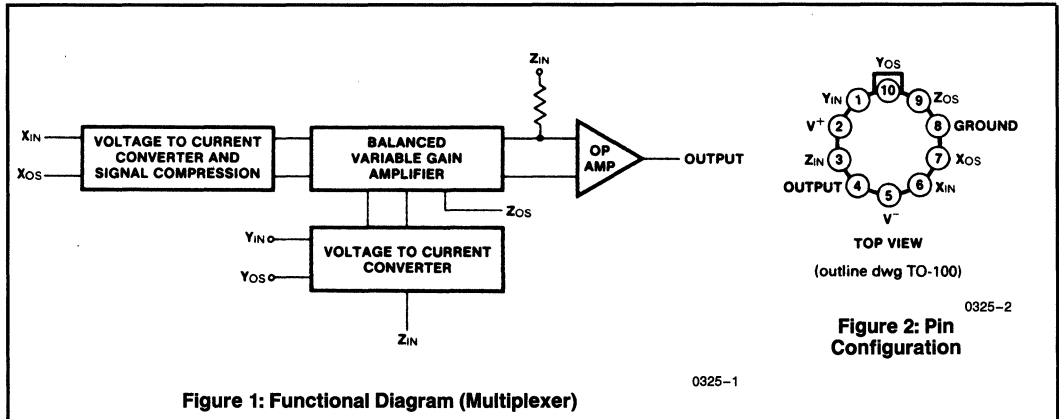
The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feed-through performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

FEATURES

- Accuracy of $\pm 0.5\%$ ("A" Version)
- Full $\pm 10V$ Input Voltage Range
- 1MHz Bandwidth
- Uses Standard $\pm 15V$ Supplies
- Built-in Op Amp Provides Level Shifting, Division and Square Root Functions

ORDERING INFORMATION

Part Number	Multiplication Error	Temperature Range	Package
ICL8013AM TZ	$\pm 0.5\%$	$-55^{\circ}C$ to $+125^{\circ}C$	10-LEAD TO-100
ICL8013BM TZ	$\pm 1\%$	$-55^{\circ}C$ to $+125^{\circ}C$	
ICL8013CM TZ	$\pm 2\%$	$-55^{\circ}C$ to $+125^{\circ}C$	
ICL8013AC TZ	$\pm 5\%$	$0^{\circ}C$ to $+70^{\circ}C$	
ICL8013BC TZ	$\pm 1\%$	$0^{\circ}C$ to $+70^{\circ}C$	
ICL8013CC TZ	$\pm 2\%$	$0^{\circ}C$ to $+70^{\circ}C$	



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 18V$
 Power Dissipation (Note 1) 500mW
 Input Voltages
 (X_{IN} , Y_{IN} , Z_{IN} , X_{OS} , Y_{OS} , Z_{OS}) V_{SUPPLY}

Operating Temperature Range:
 ICL8013XC $0^{\circ}C$ to $+70^{\circ}C$
 ICL8013XM $-55^{\circ}C$ to $+125^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10sec) $300^{\circ}C$

NOTE 1: Derate at 6.8mW/ $^{\circ}C$ for operation at ambient temperature above $75^{\circ}C$.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified $T_A = 25^{\circ}C$, $V_{SUPPLY} = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed)

Parameter	Test Conditions	ICL8013A			ICL8013B			ICL8013C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	$-10 < X < 10$ $-10 < Y < 10$			0.5			1.0			2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	$X = -10$ $X = -1$		0.3 1.5			0.3 1.5			0.3 1.5		% Full Scale % Full Scale
Feedthrough	$X = 0, Y = 20V$ $Y = 0, X = 20V$			50 50			100 100			200 150	mV mV
Non-Linearity	X Input		$X = 20V_{p-p}$ $Y = \pm 10V_{dc}$	± 0.5		± 0.5			± 0.8		%
	Y Input		$Y = 20V_{p-p}$ $X = \pm 10V_{dc}$	± 0.2		± 0.2			± 0.3		%
Frequency Response Small Signal Bandwidth ($-3dB$)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/ μs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Chase Shift)			5			5			5		kHz
Settling Time (to $\pm 2\%$ of Final Value)	$V_{IN} = \pm 10V$		1			1			1		μs
Overload Recovery (to $\pm 2\%$ of Final Value)			1			1			1		μs
Output Noise	5 Hz to 10 kHz 5 Hz to 5 MHz		0.6 3			0.6 3			0.6 3		mV rms mV rms
Input Resistance	X Input		10			10			10		$M\Omega$
	Y Input		6			6			6		$M\Omega$
	Z Input		36			36			36		$k\Omega$
Input Bias Current	X or Y Input		2	5			7.5			10	μA
	Z Input		25			25			25		μA
Power Supply Variation	Multiplication Error		0.2			0.2			0.2		% / %
	Output Offset			50			75			100	mV/V
	Scale Factor		0.1			0.1			0.1		% / %
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, Gain and Offset Potentiometers Externally Trimmed) (Continued)

Parameter	Test Conditions	ICL8013A			ICL8013B			ICL8013C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
The Following Specifications Apply Over the Operating Temperature Ranges											
Multiplication Error	$-10\text{V} < X_{\text{IN}} < 10\text{V}$, $-10\text{V} < Y_{\text{IN}} < 10\text{V}$		1.5			2			3		% Full Scale
Average Temperature Coefficients	Accuracy		0.06			0.06			0.06		%/°C
	Output Offset		0.2			0.2			0.2		mV/°C
	Scale Factor		0.04			0.04			0.04		%/°C
Input Bias Current	X or Y Input			5		5			10		μA
	Z Input			25		25			35		μA
Input Voltage (X, Y, or Z)				± 10		± 10			± 10		V
Output Voltage Swing	$R_L \geq 2\text{k}\Omega$ $C_L < 1000\text{pF}$		± 10			± 10			± 10		V

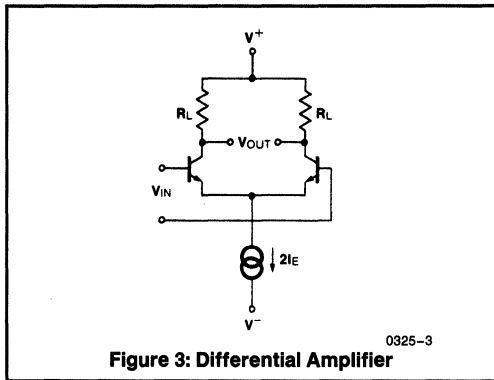


Figure 3: Differential Amplifier

DETAILED DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 3.

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{1}{g_m} = \frac{kT}{qI_E}$

$$V_{\text{OUT}} = V_{\text{IN}} \frac{R_L}{r_e} = V_{\text{IN}} \cdot \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E . In the simple transconductance multiplier of Figure 4, a current source comprising Q_3 , D_1 , and R_Y is used. If V_Y is large compared with the drop across D_1 , then

$$I_D \sim \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{\text{OUT}} = \frac{qR_L}{kTR_Y} (V_X \cdot V_Y)$$

There are several difficulties with this simple modulator:

- 1: V_Y must be positive and greater than V_D .
- 2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.
- 3: V_X must be a small signal for the differential pair to be linear.
- 4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 5, uses another differential pair but with considerable emitter degeneration. In this cir-

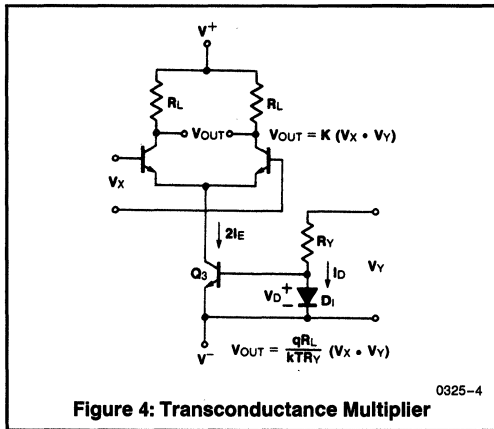


Figure 4: Transconductance Multiplier

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NOTE: All typical values have been characterized but are not tested.

cuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ± 10 volts with excellent linearity.

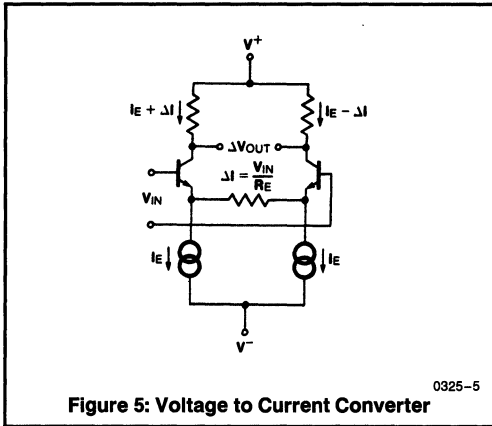


Figure 5: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 6A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 6A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN} , the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

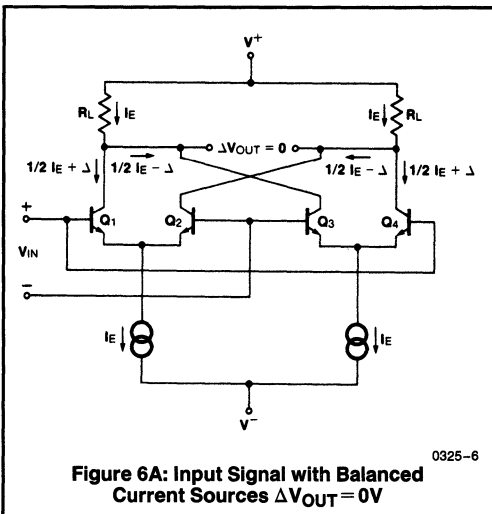


Figure 6A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

In Figure 6B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 6C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2} , the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4 . Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 5 we have a balanced multiplier circuit capable of four quadrant operation (Figure 7).

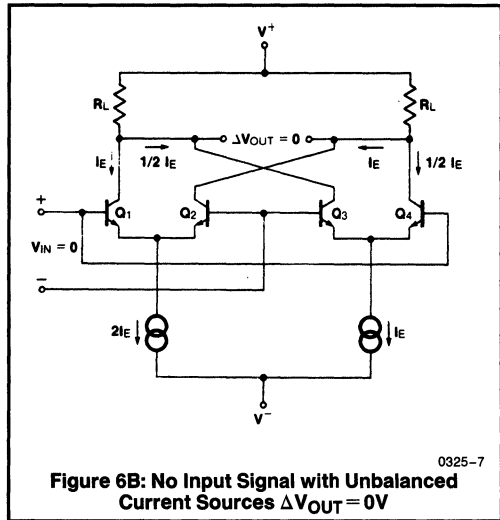


Figure 6B: No Input Signal with Unbalanced Current Sources $\Delta V_{OUT} = 0V$

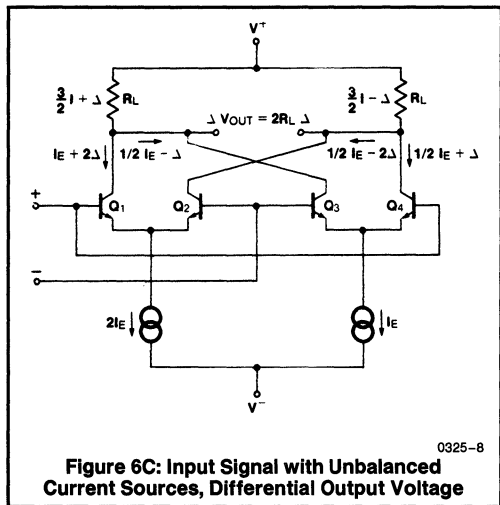


Figure 6C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

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NOTE: All typical values have been characterized but are not tested.

This circuit of Figure 7 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

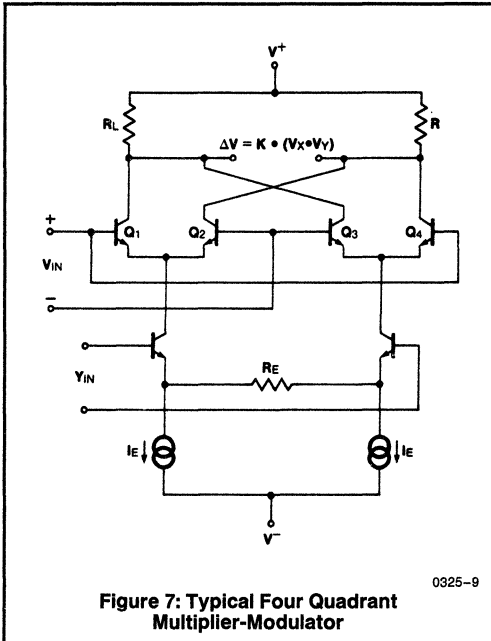


Figure 7: Typical Four Quadrant Multiplier-Modulator

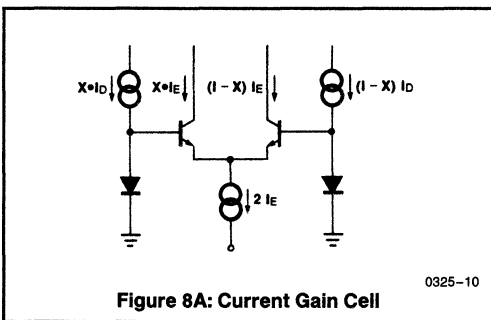


Figure 8A: Current Gain Cell

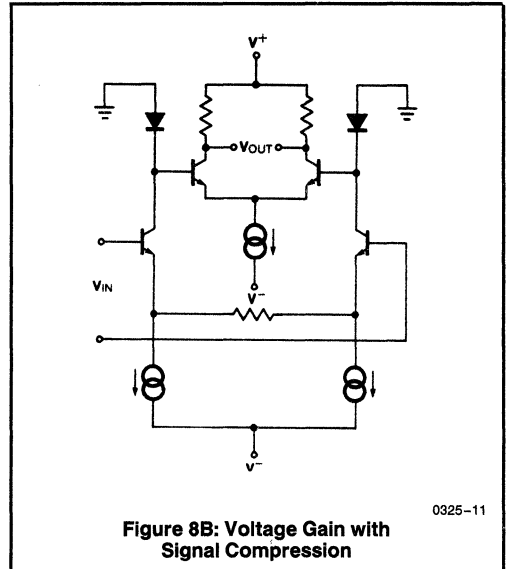


Figure 8B: Voltage Gain with Signal Compression

Figure 5 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 8A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 8A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 5, we have Figure 8B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 9. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2 . These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15} . The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10} . Transistors Q_5 , Q_6 , Q_{11} , and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27} .

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NOTE: All typical values have been characterized but are not tested.

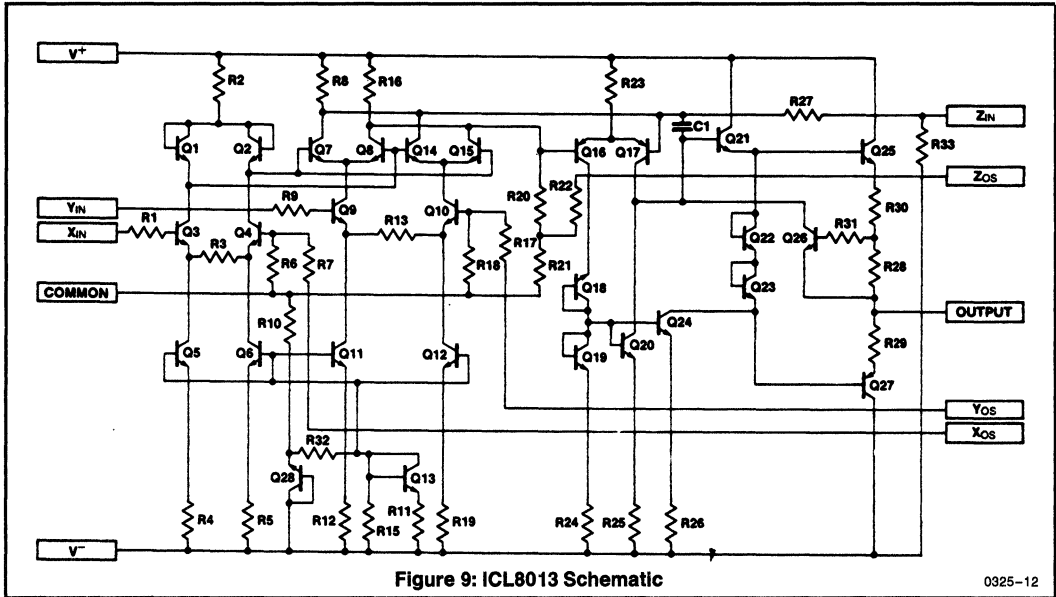


Figure 9: ICL8013 Schematic

0325-12

MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

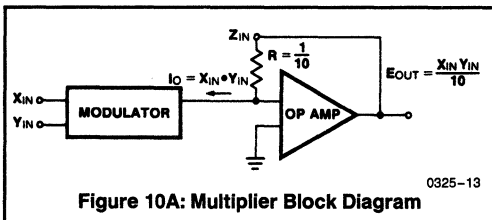


Figure 10A: Multiplier Block Diagram

0325-13

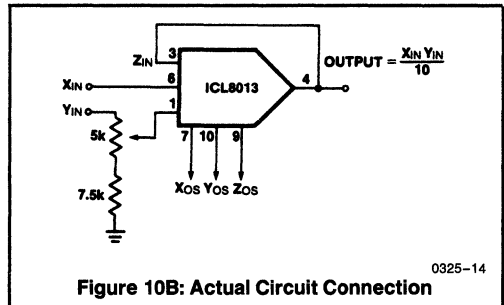


Figure 10B: Actual Circuit Connection

0325-14

6

Multiplier Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a $\pm 10V$ low frequency ($\leq 100Hz$) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With $X_{IN} = 10.0V$ DC and the sweep signal of Step 2 applied to Y_{IN} , adjust the Gain potentiometer for Output = Y_{IN} . This is easily accomplished with a differential scope plug-in (A+B) by inverting one signal and adjusting Gain control for $(Output - Y_{IN}) = Zero$.

DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X_{IN} * Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{IN}$$

$$\text{Since } Y_{IN} = E_{OUT}, E_{OUT} = \frac{10Z_{IN}}{X_{IN}}$$

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NOTE: All typical values have been characterized but are not tested.

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

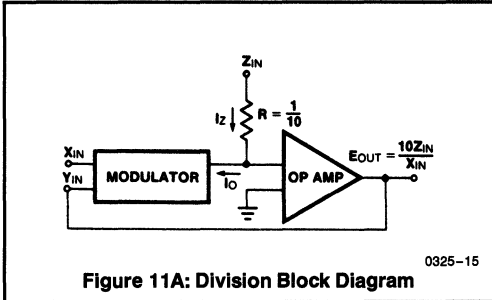


Figure 11A: Division Block Diagram

0325-15

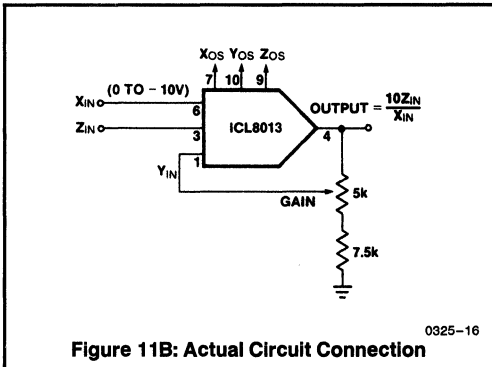


Figure 11B: Actual Circuit Connection

0325-16

Divider Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With Z_{IN} = 0V, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from -10V through -1V.
3. With Z_{IN} = 0V and X_{IN} = -10.0V adjust Y_{OS} for zero Output voltage.
4. With Z_{IN} = X_{IN} (and/or Z_{IN} = -X_{IN}) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from -10V to -1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With Z_{IN} = X_{IN} (and/or Z_{IN} = -X_{IN}) adjust the gain control until the output is the closest average around +10.0V (-10V for Z_{IN} = -X_{IN}) as X_{IN} is varied from -10V to -3V.

SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2 \omega t = \frac{1}{2} (\cos 2\omega t + 1)$.

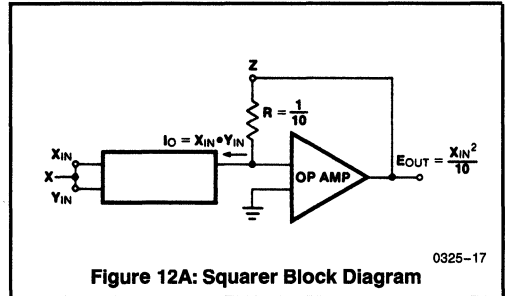


Figure 12A: Squarer Block Diagram

0325-17

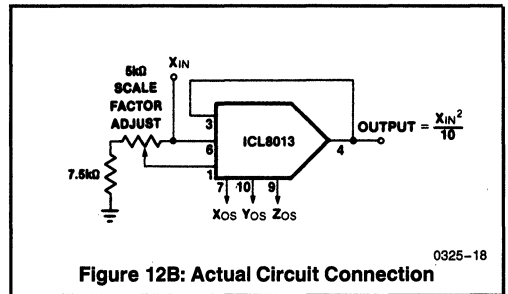


Figure 12B: Actual Circuit Connection

0325-18

SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X_{IN} * Y_{IN} = (-E_{OUT})^2 = 10Z_{IN}$$

$$E_{OUT} = -\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.

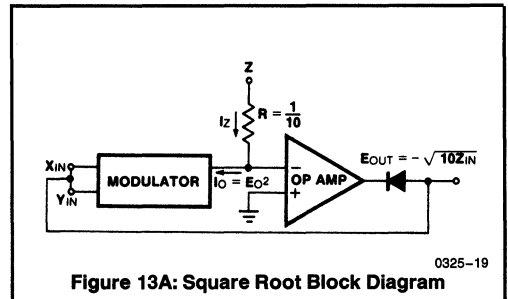
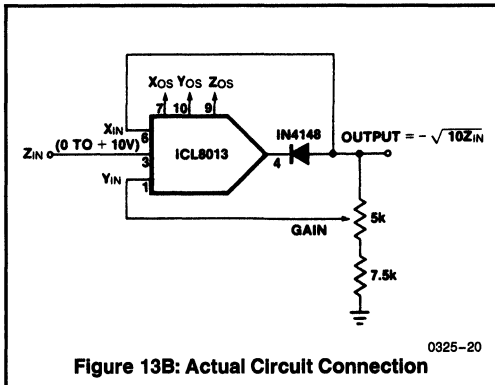


Figure 13A: Square Root Block Diagram

0325-19

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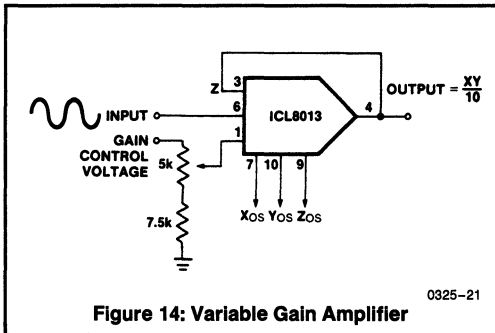


Square Root Trimming Procedure

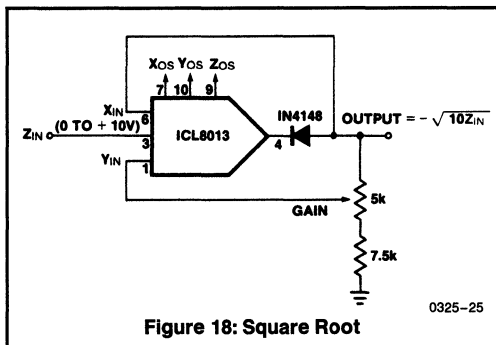
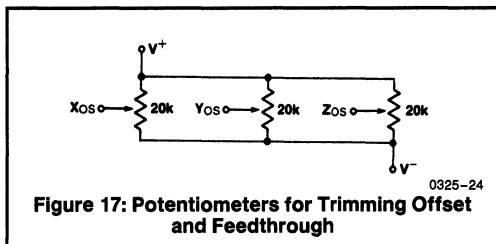
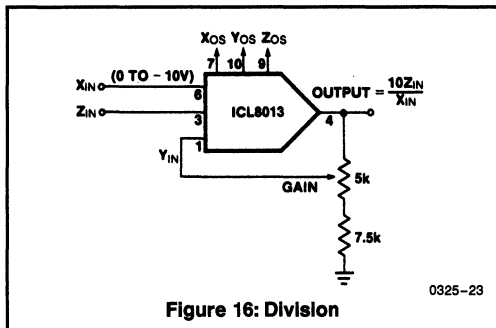
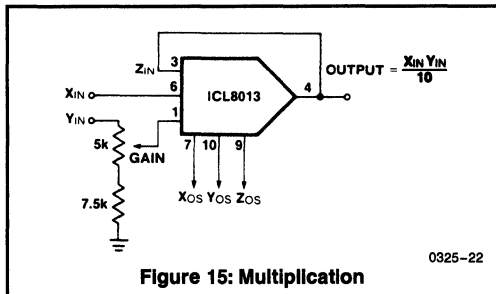
1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.



TYPICAL APPLICATIONS

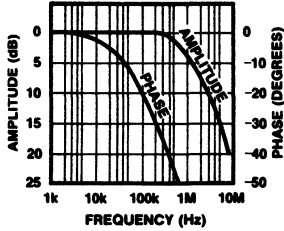


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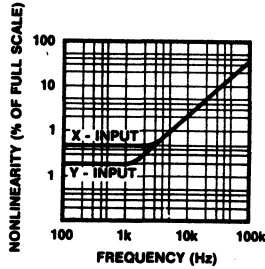
TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



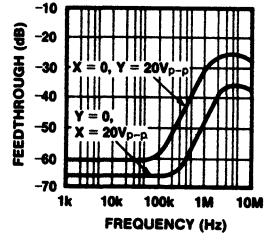
0325-26

NONLINEARITY AS A FUNCTION OF FREQUENCY



0325-27

FEEDTHROUGH AS A FUNCTION OF FREQUENCY



0325-28

DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

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NOTE: All typical values have been characterized but are not tested.

ICL8038

Precision Waveform Generator/Voltage Controlled Oscillator



ICL8038

GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

FEATURES

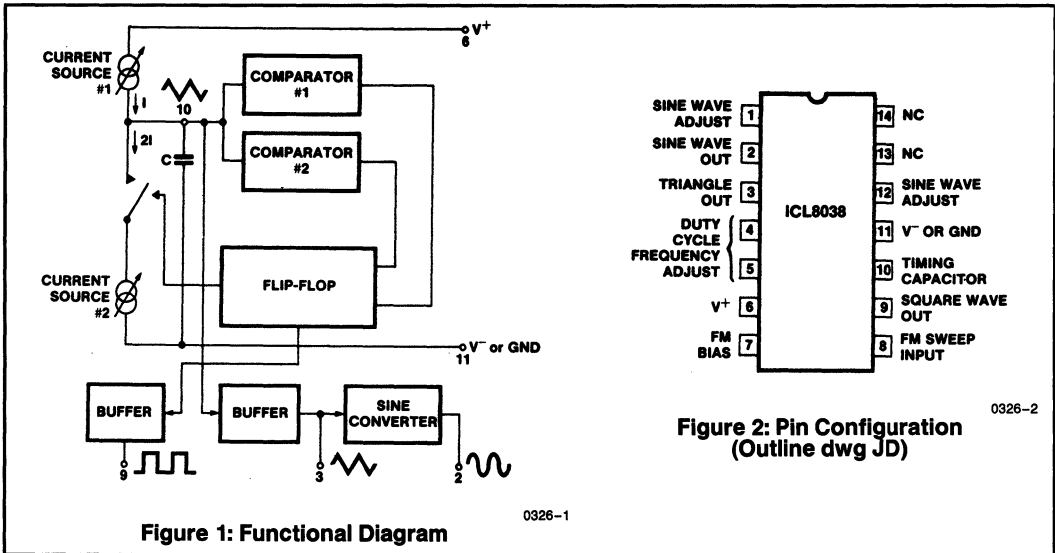
- Low Frequency Drift With Temperature — 250ppm/°C
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Low Distortion — 1% (Sine Wave Output)
- High Linearity — 0.1% (Triangle Wave Output)
- Wide Operating Frequency Range — 0.001Hz to 300kHz
- Variable Duty Cycle — 2% to 98%
- High Level Outputs — TTL to 28V
- Easy to Use — Just A Handful of External Components Required

ORDERING INFORMATION

Part Number	Stability	Temp. Range	Package
ICL8038CCPD	250ppm/°C typ	0°C to +70°C	14 pin MiniDIP
ICL8038CCJD	250ppm/°C typ	0°C to +70°C	CERDIP
ICL8038BCJD	180ppm/°C typ	0°C to +70°C	CERDIP
ICL8038ACJD	120ppm/°C typ 110	0°C to +70°C	CERDIP
ICL8038BMJD*	350ppm/°C max	-55°C to +125°C	CERDIP
ICL8038AMJD*	250ppm/°C max	-55°C to +125°C	CERDIP

*Add /883B to part number if 883 processing is required.

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0326-2

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V⁻ to V⁺) 36V
 Power Dissipation⁽¹⁾ 750mW
 Input Voltage (any pin) V⁻ to V⁺
 Input Current (Pins 4 and 5) 25mA
 Output Sink Current (Pins 3 and 9) 25mA

Storage Temperature Range -65°C to +150°C
 Operating Temperature Range:
 8038AM, 8038BM -55°C to +125°C
 8038AC, 8038BC, 8038CC 0°C to +70°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified)

Symbol	General Characteristics	8038CC			8038BC(BM)			8038AC(AM)			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{SUPPLY}	Supply Voltage Operating Range										
V ⁺	Single Supply	+10		+30	+10		30	+10		30	V
V ⁺ , V ⁻	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I _{SUPPLY}	Supply Current (V _{SUPPLY} = ±10V) ⁽²⁾										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
Frequency Characteristics (all waveforms)											
f _{max}	Maximum Frequency of Oscillation	100			100			100			kHz
f _{sweep}	Sweep Frequency of FM Input		10			10			10		kHz
	Sweep FM Range ⁽³⁾		35:1			35:1			35:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
Δf/ΔT	Frequency Drift With Temperature ⁽⁵⁾ 8038 AC, BC, CC 0°C to 70°C		250			180			120		ppm/°C
	8038 AM, BM, -55°C to 125°C						350		250		
Δf/ΔV	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V
Output Characteristics											
I _{OLK}	Square-Wave Leakage Current (V _g = 30V)			1			1			1	μA
V _{SAT}	Saturation Voltage (I _{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
t _r	Rise Time (R _L = 4.7kΩ)		180			180			180		ns
t _f	Fall Time (R _L = 4.7kΩ)		40			40			40		ns
ΔD	Typical Duty Cycle Adjust (Note 6)	2		98	2		98	2		98	%
V _{TRIANGLE}	Triangle/Sawtooth/Ramp Amplitude (R _{TRI} = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV _{SUPPLY}
	Linearity		0.1			0.05			0.05		%
Z _{OUT}	Output Impedance (I _{OUT} = 5mA)		200			200			200		Ω
V _{SINE}	Sine-Wave Amplitude (R _{SINE} = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV _{SUPPLY}
THD	THD (R _S = 1MΩ) ⁽⁴⁾		2.0	5		1.5	3		1.0	1.5	%
THD	THD Adjusted (Use Figure 6)		1.5			1.0			0.8		%

NOTES: 2. R_A and R_B currents not included.

3. V_{SUPPLY} = 20V; R_A and R_B = 10kΩ, f ≈ 10kHz nominal; can be extended 1000 to 1. See Figures 7a and 7b.

4. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)

5. Figure 3, pins 7 and 8 connected, V_{SUPPLY} = ±10V. See Typical Curves for T.C. vs V_{SUPPLY}.

6. Not tested, typical value for design purposes only.

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NOTE: All typical values have been characterized but are not tested.

TEST CONDITIONS

Parameter	R _A	R _B	R _L	C ₁	SW ₁	Measure	
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6	
Sweep FM Range ⁽¹⁾	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9	
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3	
Frequency Drift with Supply Voltage ⁽²⁾	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9	
Output Amplitude: (Note 4)	Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
	Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off) ⁽³⁾	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9	
Saturation Voltage (on) ⁽³⁾	10kΩ	10kΩ		3.3nF	Closed	Output (low) at Pin 9	
Rise and Fall Times (Note 5)	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9	
Duty Cycle Adjust: (Note 5)	MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
	MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3	
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2	

NOTES: 1. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 ($\frac{2}{3} V_{SUPPLY} + 2V$) $\leq V_{SWEEP} \leq V_{SUPPLY}$ where V_{SUPPLY} is the total supply voltage. In Figure 7b, pin 8 should vary between 5.3V and 10V with respect to ground.

2. $10V \leq V^+ \leq 30V$, or $\pm 5V \leq V_{SUPPLY} \leq \pm 15V$.

3. Oscillation can be halted by forcing pin 10 to +5 volts or -5 volts.

4. Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to -5.0V.

5. Not tested; for design purposes only.

DEFINITION OF TERMS:

Supply Voltage (V_{SUPPLY}). The total supply voltage from V⁺ to V⁻.

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$\left(\frac{2}{3} V_{SUPPLY} + 2V\right) < V_{SWEEP} < V_{SUPPLY}$$

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q₂₃ when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

6

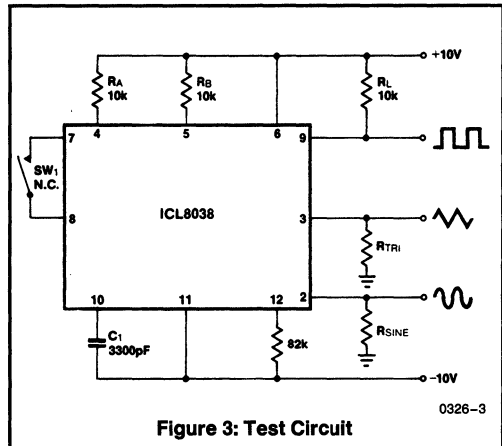


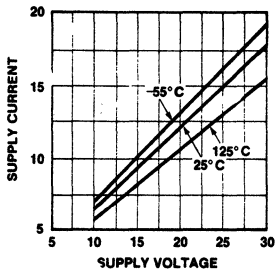
Figure 3: Test Circuit

0326-3

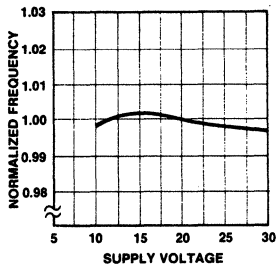
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NOTE: All typical values have been characterized but are not tested.

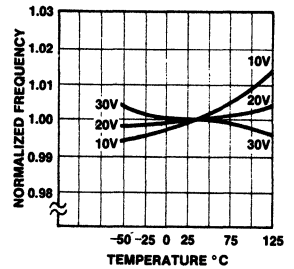
TYPICAL PERFORMANCE CHARACTERISTICS



0326-4

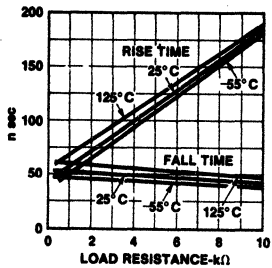


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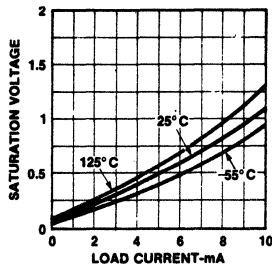


0326-6

Performance of the Square-Wave Output

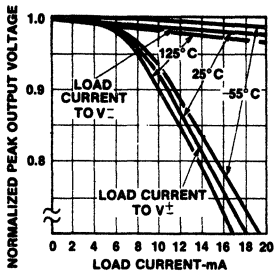


0326-7

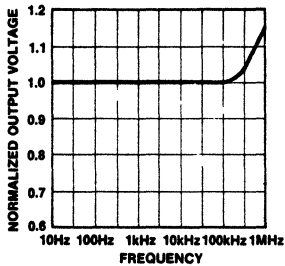


0326-8

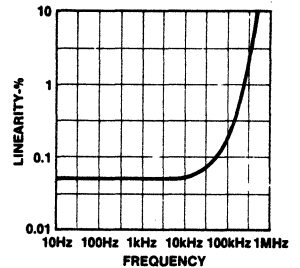
Performance of Triangle-Wave Output



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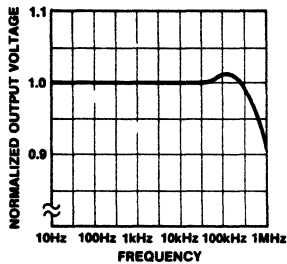


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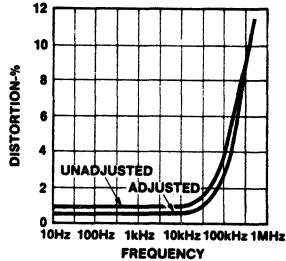


0326-11

Performance of Sine-Wave Output



0326-12



0326-13

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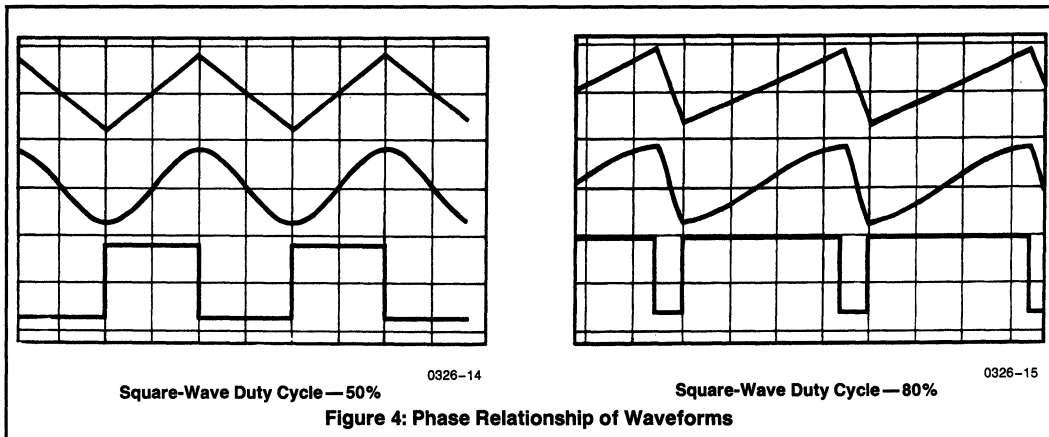


Figure 4: Phase Relationship of Waveforms

DETAILED DESCRIPTION
(See Figure 1)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at 2/3 of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 5. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A

controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{SUPPLY}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times Y}{I} = \frac{C \times \frac{1}{3} V_{SUPPLY}}{2(0.22) \frac{V_{SUPPLY}}{R_B} - 0.22 \frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when R_A = R_B.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 5b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 5c. This connection, however, causes an inherently larger variation of the duty-cycle, frequency, etc.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66} \left(1 + \frac{R_B}{2R_A - R_B} \right)}$$

or, if R_A = R_B = R

$$f = \frac{0.33}{RC} \text{ (for Figure 5a)}$$

If a single timing resistor is used (Figure 5c only), the frequency is

$$f = \frac{0.165}{RC}$$

6

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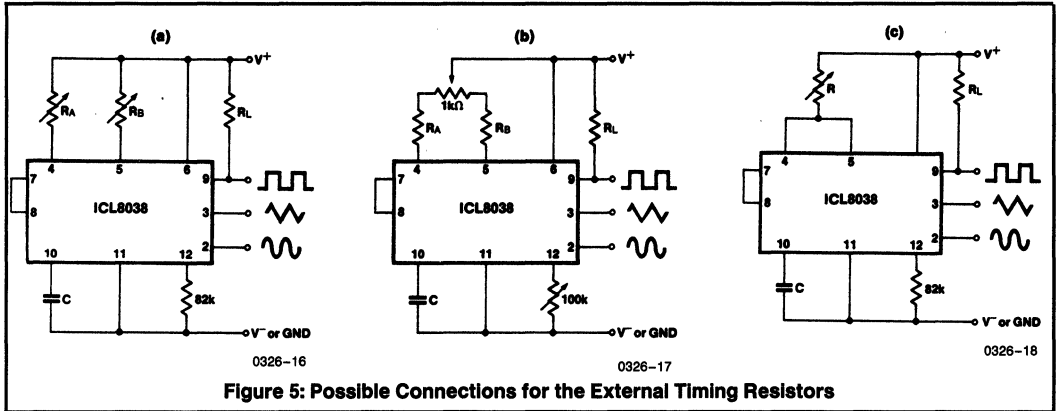


Figure 5: Possible Connections for the External Timing Resistors

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.

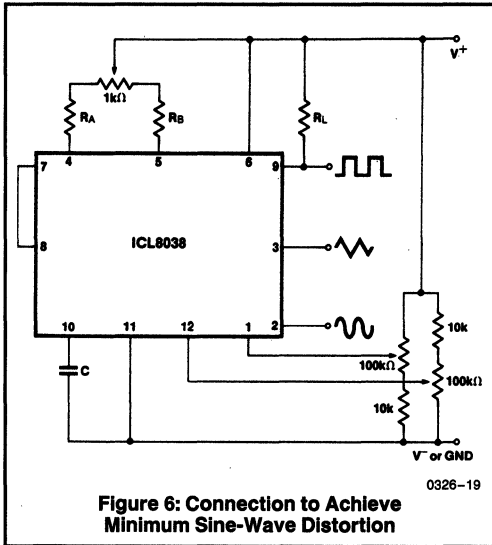


Figure 6: Connection to Achieve Minimum Sine-Wave Distortion

SELECTING RA, RB and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (>5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to RA can be calculated from:

$$I = \frac{R_1 \times (V^+ - V^-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V^+ - V^-)}{R_A}$$

A similar calculation holds for RB.

The capacitor value should be chosen at the upper end of its possible range.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

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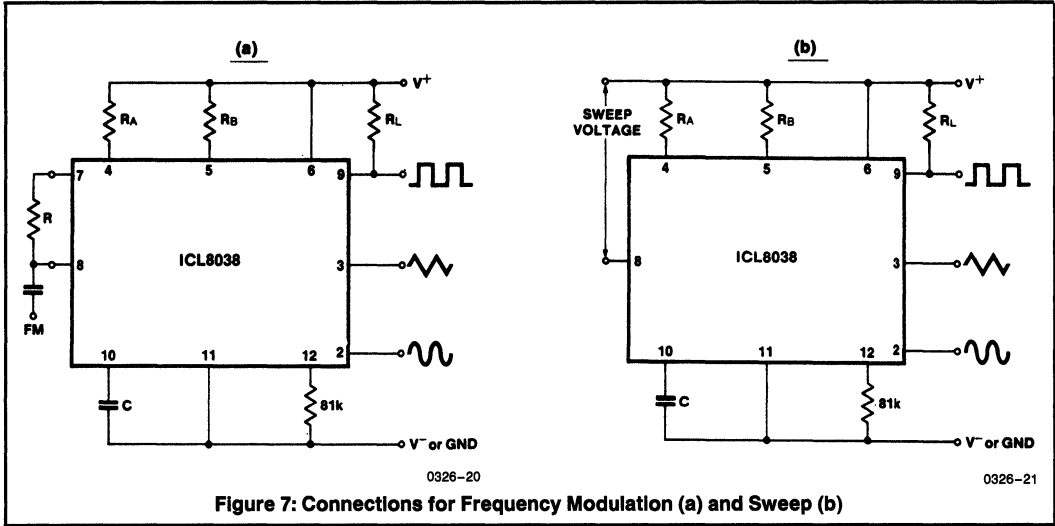


Figure 7: Connections for Frequency Modulation (a) and Sweep (b)

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 7a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 7b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f=0 at V_{sweep}=0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by (1/5 V_{SUPPLY} - 2V).

APPLICATIONS

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 8 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 9 shows a FET switch, diode ANDeD with an input strobe signal to allow the output to always start on the same slope.

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors RA and RB must decrease to nearly zero. This requires that the highest voltage on con-

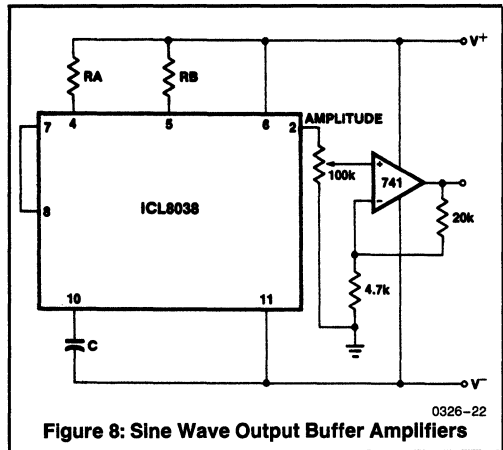


Figure 8: Sine Wave Output Buffer Amplifiers

trol Pin 8 exceed the voltage at the top of RA and RB by a few hundred millivolts. The Circuit of Figure 10 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 11.

USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop as shown in Figure 12. In this application the remaining functional blocks, the

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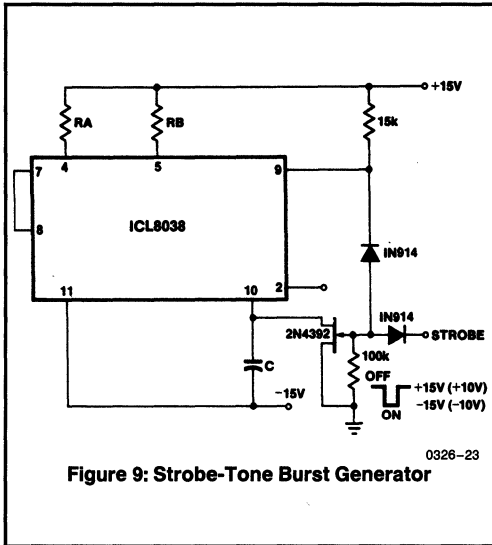


Figure 9: Strobe-Tone Burst Generator

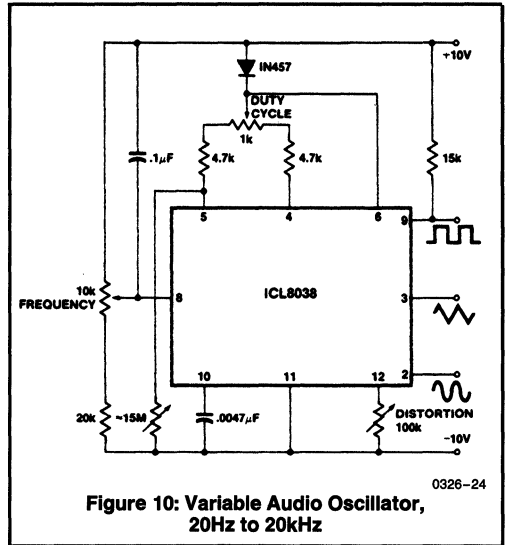


Figure 10: Variable Audio Oscillator, 20Hz to 20kHz

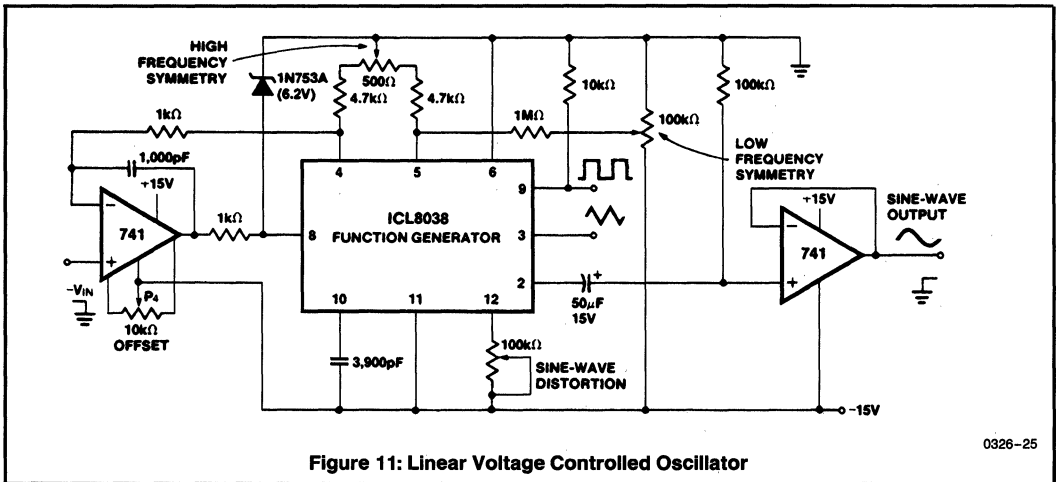


Figure 11: Linear Voltage Controlled Oscillator

phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC4344, NE562, HA2800, HA2820)

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V+ (R1, R2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note A013, "Everything You Always Wanted to Know About The ICL8038."

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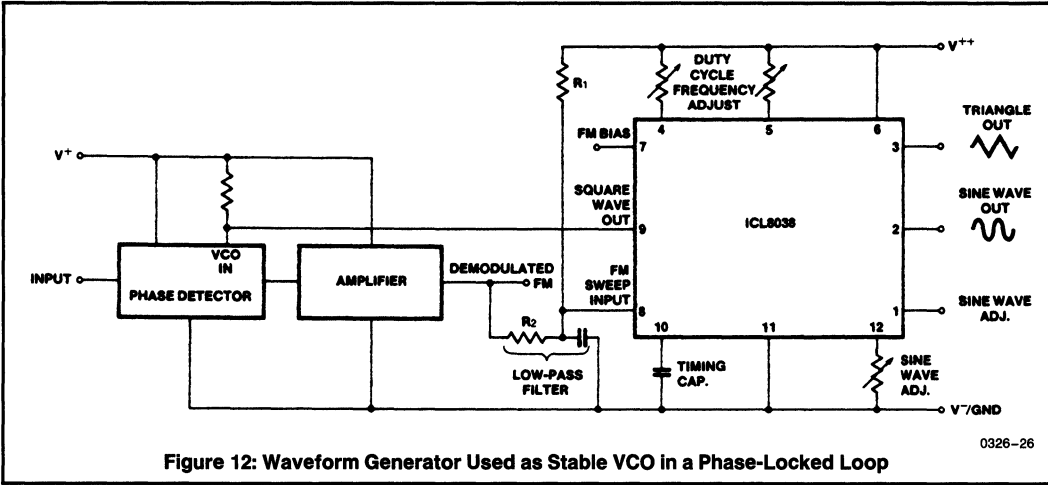


Figure 12: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

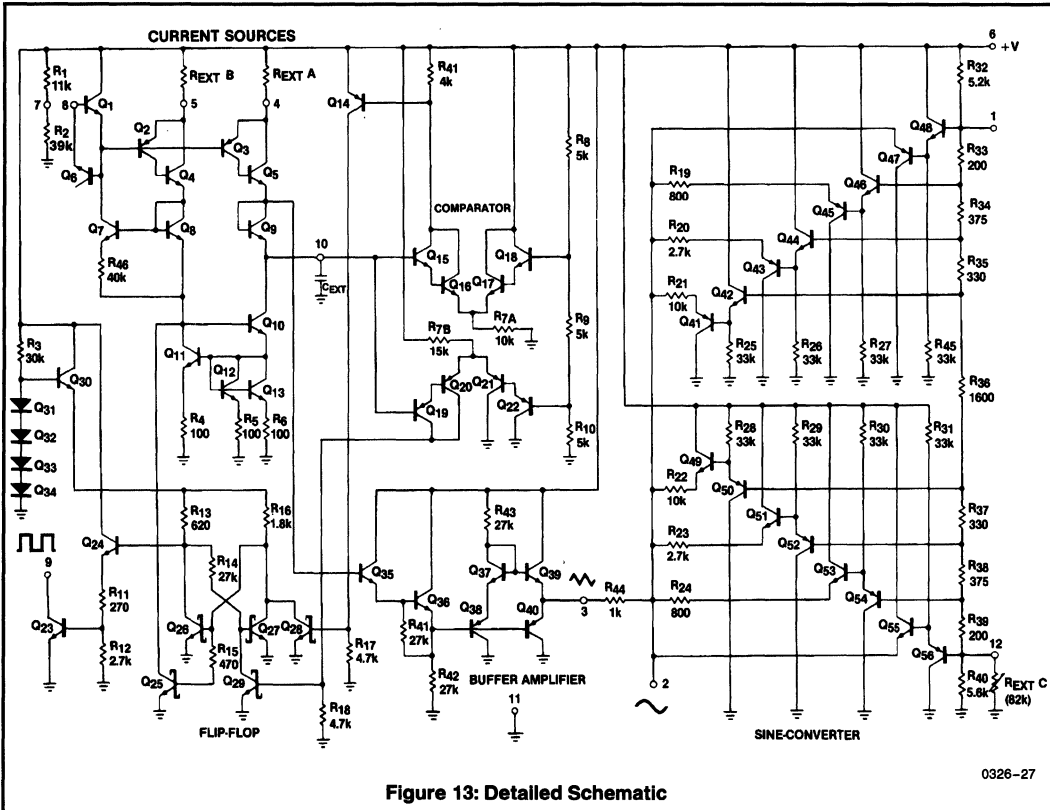


Figure 13: Detailed Schematic

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ICL8048/ICL8049 Log/Antilog Amplifier



GENERAL DESCRIPTION

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

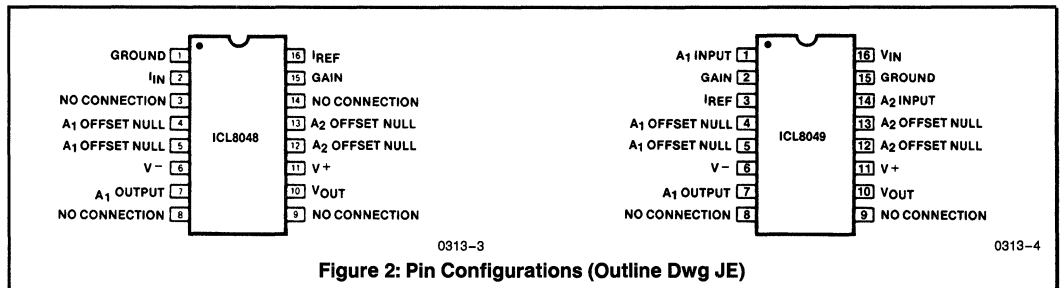
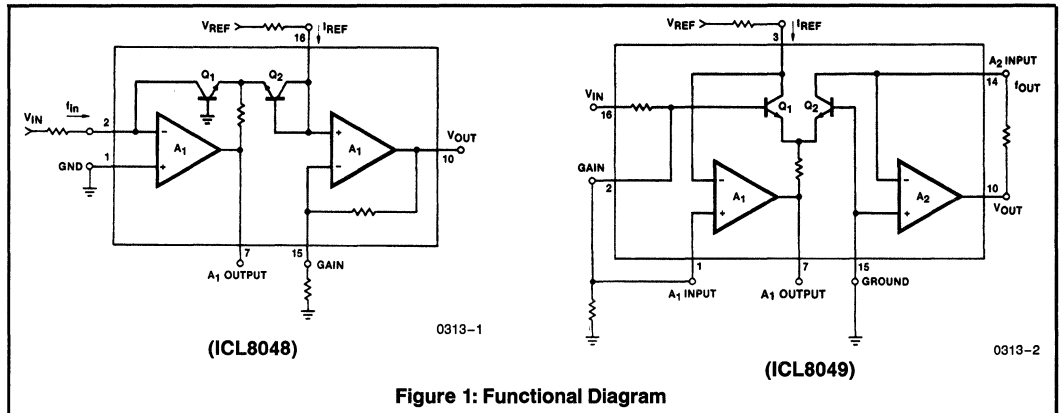
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

FEATURES

- ½% Full Scale Accuracy
- Temperature Compensated for 0°C to +70°C Operation
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual JFET-Input Op-Amps

ORDERING INFORMATION

Part Number	Error (25°C)	Temperature Range	Package
ICL8048BCJE	30mV	0°C to +70°C	16 Pin CERDIP
ICL8048CCJE	60mV	0°C to +70°C	16 Pin CERDIP
ICL8049BCJE	10mV	0°C to +70°C	16 Pin CERDIP
ICL8049CCJE	25mV	0°C to +70°C	16 Pin CERDIP



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (ICL8048)

Supply Voltage	± 18V
I_{IN} (Input Current)	2mA
I_{REF} (Reference Current)	2mA
Voltage between Offset Null and V^+	± 0.5V
Power Dissipation	750mW

Operating Temperature Range	0°C to + 70°C
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to + 150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (ICL8048)

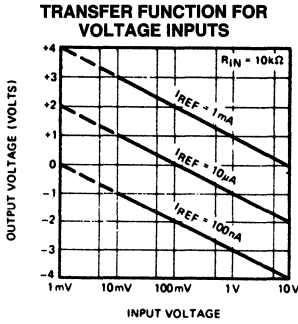
$V_S = \pm 15V$, $T_A = 25^\circ C$, $I_{REF} = 1mA$, scale factor adjusted for 1V/decade unless otherwise specified.

Parameter	Test Conditions	8048BC			8048CC			Units
		Min	Typ	Max	Min	Typ	Max	
Dynamic Range I_{IN} (1nA – 1mA) V_{IN} (10mV – 10V)	$R_{IN} = 10k\Omega$	120			120			dB
		60			60			dB
Error, % of Full Scale	$T_A = 25^\circ C$, $I_{IN} = 1nA$ to 1mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	$T_A = 0^\circ C$ to + 70°C, $I_{IN} = 1nA$ to 1mA		.60	1.25		.80	2.5	%
Error, Absolute Value	$T_A = 25^\circ C$, $I_{IN} = 1nA$ to 1mA		12	30		14	60	mV
Error, Absolute Value	$T_A = 0^\circ C$ to + 70°C $I_{IN} = 1nA$ to 1mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	$I_{IN} = 1nA$ to 1mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for $I_{IN} = 100\mu A$		250			250		μV (RMS)
Output Voltage Swing	$R_L = 10k\Omega$	± 12	± 14		± 12	± 14		V
	$R_L = 2k\Omega$	± 10	± 13		± 10	± 13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

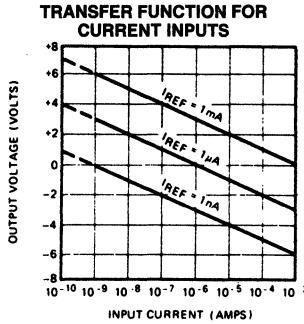
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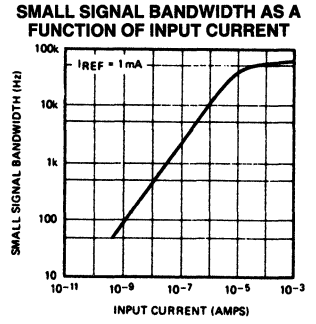
TYPICAL PERFORMANCE CHARACTERISTICS



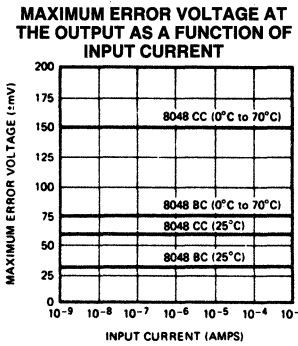
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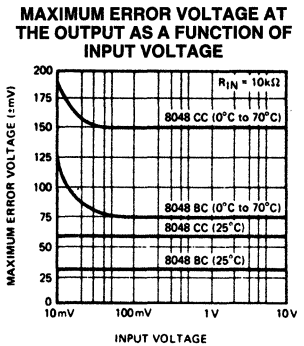
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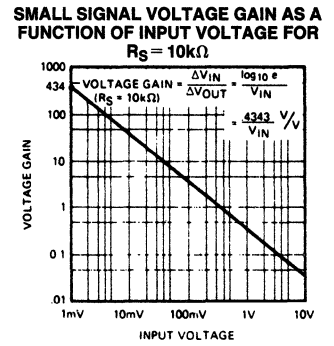
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ABSOLUTE MAXIMUM RATINGS (ICL8049)

Supply Voltage	± 18V
V _{IN} (Input Voltage)	± 15V
I _{REF} (Reference Current)	2mA
Voltage between Offset Null and V ⁺	± 0.5V
Power Dissipation	750mW

Operating Temperature Range	0°C to +70°C
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (ICL8049)

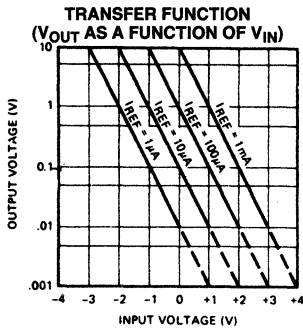
V_S = ± 15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted

for 1 decade (out) per volt (in), unless otherwise specified.

Parameter	Test Conditions	8049BC			8049CC			Units	
		Min	Typ	Max	Min	Typ	Max		
Dynamic Range (V _{OUT})	V _{OUT} = 10mV to 10V	60			60			dB	
Error, Absolute Value	T _A = 25°C, 0V ≤ V _{IN} ≤ 2V	3	15		5	25		mV	
Error, Absolute Value	T _A = 0°C to +70°C, 0V ≤ V _{IN} ≤ 3V	20	75		30	150		mV	
Temperature Coefficient, Referred to V _{IN}	V _{IN} = 3V		0.38			0.55		mV/°C	
Power Supply Rejection Ratio	Referred to Input, for V _N = 0V		2.0			2.0		μV/V	
Offset Voltage (A ₁ & A ₂)	Before Nulling		15	25		15	50	mV	
Wideband Noise	Referred to Input, for V _{IN} = 0V		26			26		μV(RMS)	
Output Voltage Swing	R _L = 10kΩ	± 12	± 14		± 12	± 14		V	
	R _L = 2kΩ	± 10	± 13		± 10	± 13		V	
Power Consumption			150	200		150	200	mW	
Supply Current				5	6.7		5	6.7	mA

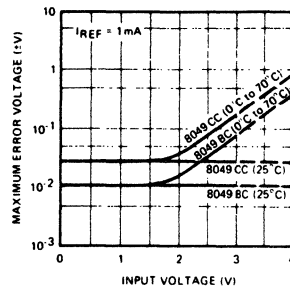
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TYPICAL PERFORMANCE CHARACTERISTICS



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MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF V_{IN}



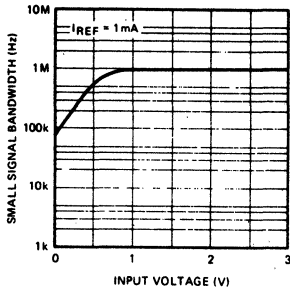
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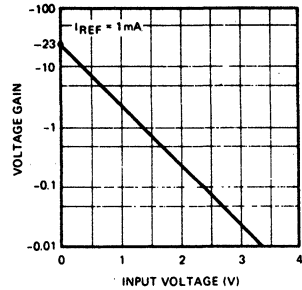
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE



0313-13

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE



0313-14

ICL8048 DETAILED DESCRIPTION

The ICL8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S [e^{qV_{BE}/kT} - 1] \quad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S e^{qV_{BE}/kT} \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10} \left[\frac{I_{C1}}{I_{C2}} \right] \quad (3)$$

Referring to Figure 3, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2 . The output voltage is ΔV_{BE} multiplied by the gain of A_2 :

$$V_{OUT} = -2.303 \left(\frac{R_1 + R_2}{R_2} \right) \left(\frac{kT}{q} \right) \log_{10} \left[\frac{I_{IN}}{I_{REF}} \right] \quad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a $1/T$ characteristic to compensate for kT/q .

In the ICL8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation.

Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of $\pm 20\%$ to allow for production variations in the absolute value of R_1 .

ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT*

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and opens the feedback loop around A_1 . Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Figure 3, this is done as follows:

- 1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0 .
Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.
- 2) Set $I_{IN} = I_{REF} = 1mA$. Adjust R_5 such that the output of A_2 (pin 10) is zero.
- 3) Set $I_{IN} = 1\mu A$, $I_{REF} = 1mA$. Adjust R_2 for $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu A$ in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

*See A053 for an automatic offset nulling circuit.

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NOTE: All typical values have been characterized but are not tested.

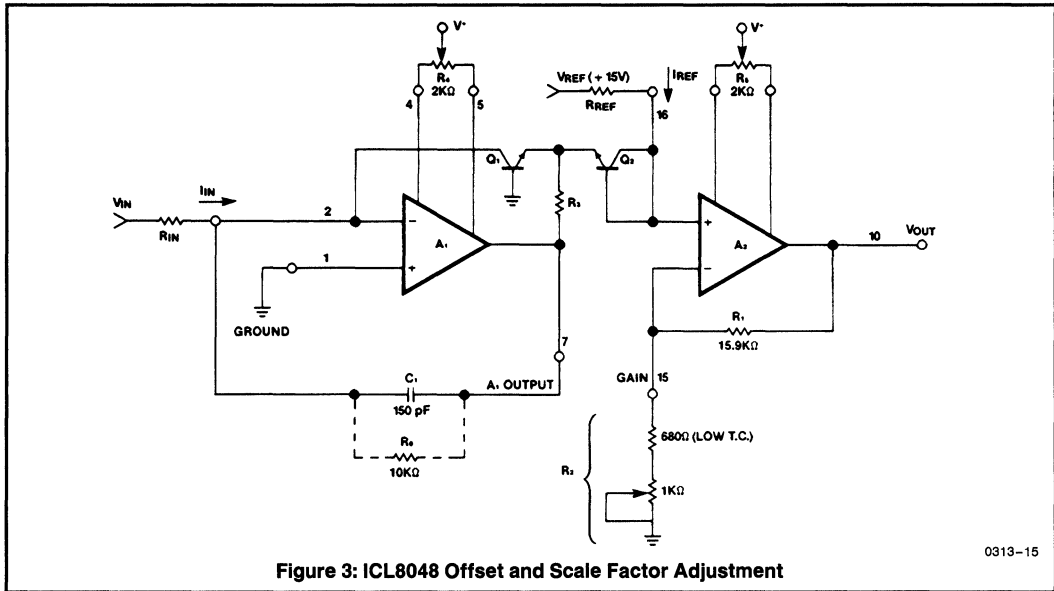


Figure 3: ICL8048 Offset and Scale Factor Adjustment

0313-15

ICL8049 DETAILED DESCRIPTION

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Figure 4). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C1}}{I_{C2}} = \exp \left[\frac{q \Delta V_{BE}}{kT} \right]$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2 . In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable $\pm 20\%$, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp \left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT} I_{REF} \exp \left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp \left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right] \quad (8)$$

ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT*

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2 . This is accomplished by reverse biasing the base-emitter of Q_2 . A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 4, the exact procedure for 1 decade/volt is as follows:

- 1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2 . Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
- 2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
- 3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i.e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.

*See A053 for an automatic offset nulling circuit.

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NOTE: All typical values have been characterized but are not tested.

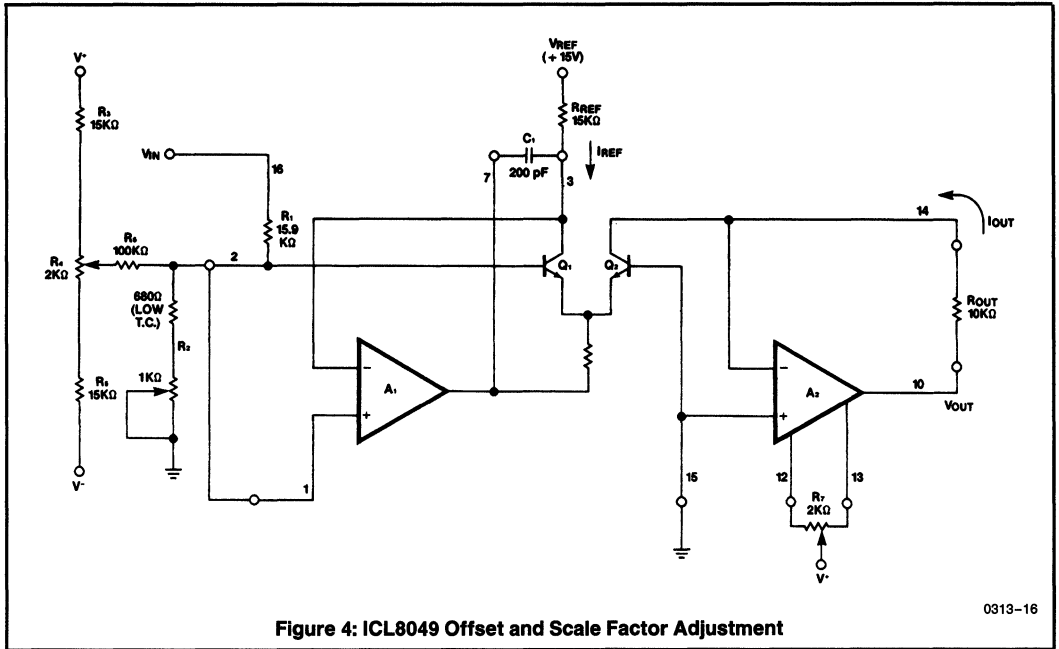


Figure 4: ICL8049 Offset and Scale Factor Adjustment

0313-16

APPLICATIONS INFORMATION

ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048 and ICL8049, are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to $K=1$ in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10} \left[\frac{I_{IN}}{I_{REF}} \right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT} I_{REF} 10^{\frac{-V_{IN}}{K}} \quad (10)$$

By adjusting R_2 (Figure 3 and Figure 4) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Figure 5 for the log amp, and Figure 6 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a $\pm 20\%$ tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by $\pm 20\%$.

$$R_2 = \frac{941}{(K - .059)} \Omega \quad (11)$$

Frequency Compensation

Although the op-amps in both the ICL8048 and the ICL8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150pF should be connected between Pins 2 and 7 (Figure 3). In the 8049, 200pF between Pins 3 and 7 is recommended (Figure 4).

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

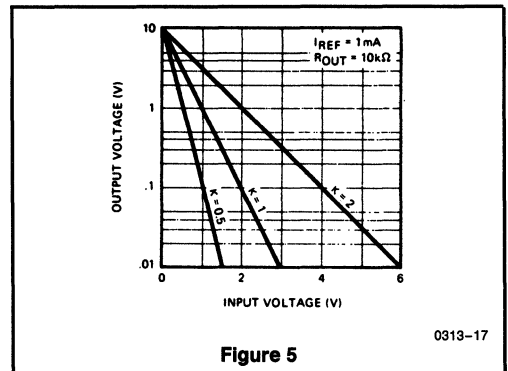


Figure 5

0313-17

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NOTE: All typical values have been characterized but are not tested.

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

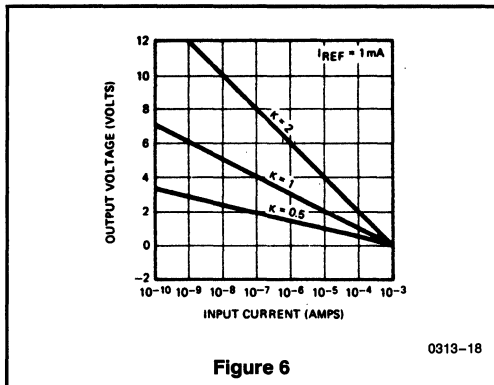


Figure 6

0313-18

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Characteristics section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the ICL8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 7.

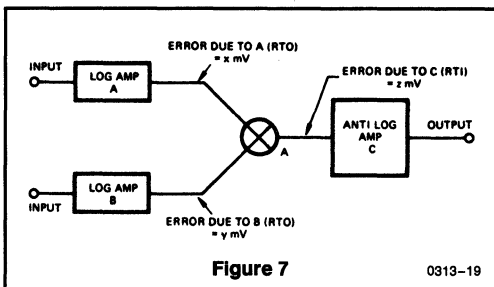


Figure 7

0313-19

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2} \text{ at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 8 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i.e., the horizontal axis. It will be noticed that the maximum error voltage of the ICL8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A₂, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At V_{IN} = 3V, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

TRANSFER FUNCTION FOR CURRENT INPUTS

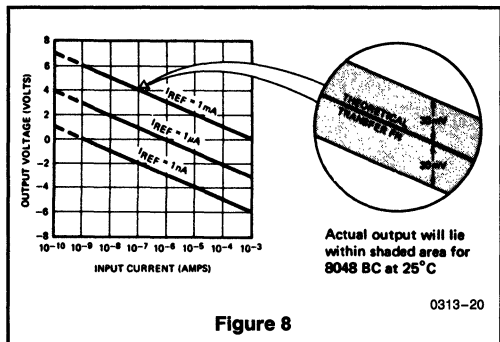


Figure 8

0313-20

6

It is important to note that both the ICL8048 and the ICL8049 require positive values of I_{REF}, and the input (ICL8048) or output (ICL8049) currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the ICL8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the ICL8048 and the ICL8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 3). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the ICL8049, a fraction of the input voltage appears on Pin 3 (Figure 4), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Figure 9.

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NOTE: All typical values have been characterized but are not tested.

ICL8048/ICL8049



LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K \log_{10} \left[\frac{I_{IN}}{I_{REF}} \right] \quad (9)$$

Clearly it is possible to perform division using just one ICL8048, followed by an ICL8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Figure 9 is again recommended if the I_{REF} input is to be modulated.

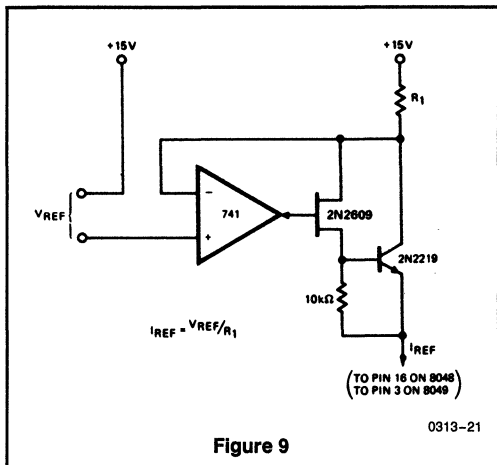


Figure 9

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

DYNAMIC RANGE The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the ICL8049 the dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048) or (ICL8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the ICL8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the ICL8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the ICL8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT} .

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the ICL8048, V_{IN} for the ICL8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the ICL8048, this is the noise occurring at the output under the specified conditions. In the case of the ICL8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

APPLICATION NOTES

For further applications assistance, see

A007 "The ICL8048/8049 Monolithic Log-Antilog Amplifiers"

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NOTE: All typical values have been characterized but are not tested.

ICL8069

Low Voltage Reference



ICL8069

GENERAL DESCRIPTION

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50 μ A. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

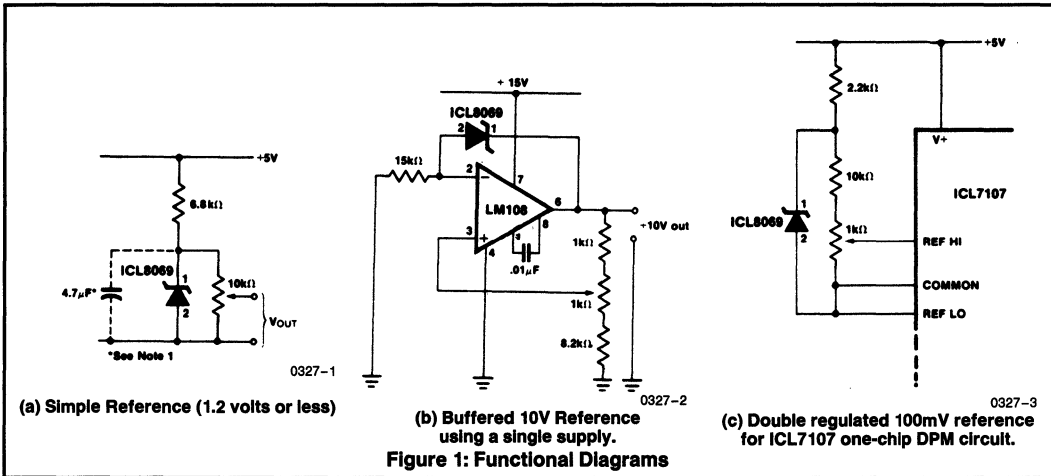
FEATURES

- Low Bias Current — 50 μ A Min
- Low Dynamic Impedance
- Low Reverse Voltage
- Low Cost

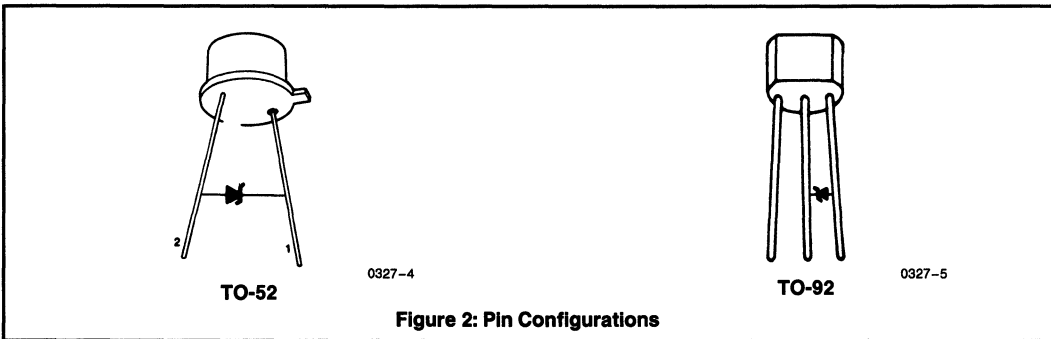
ORDERING INFORMATION

Order P/N TO-92	Order P/N TO-52	Temperature Range	Max. Temp. Coeff. of V_{REF}
ICL8069CCZR	ICL8069CCSQ	0°C to +70°C	0.005%/°C
—	ICL8069CMSQ	-55°C to +125°C	0.005%/°C
ICL8089DCZR	ICL8069DCSQ	0°C to +70°C	0.01%/°C
—	ICL8069DMSQ	-55°C to +125°C	0.01%/°C

**Parameter Min/Max Limits guaranteed at 25°C only for DICE orders.



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NOTE: All typical values have been characterized but are not tested.

ICL8069



ABSOLUTE MAXIMUM RATINGS

Reverse Voltage See Note 2
 Forward Current 10mA
 Reverse Current 10mA
 Power Dissipation Limited by max forward/reverse current

Storage Temperature -65°C to +150°C
 Operating Temperature
 ICL8069C 0°C to +70°C
 ICL8069M -55°C to +125°C
 Lead Temperature (Soldering, 10sec) 300°C

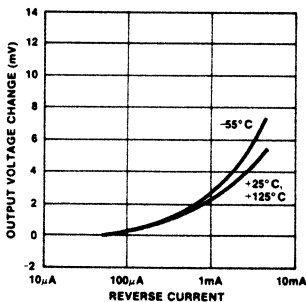
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Test Conditions	Min	Typ	Max	Units
Reverse breakdown Voltage	I _R = 500μA	1.20	1.23	1.25	V
Reverse breakdown Voltage change	50μA ≤ I _R ≤ 5mA		15	20	mV
Reverse dynamic impedance	I _R = 50μA I _R = 500μA		1 1	2 2	Ω
Forward Voltage Drop	I _F = 500μA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I _R = 500μA		5		μV
Long Term Stability	I _R = 4.75mA T _A = 25°C		1		ppm/kHR
Breakdown voltage Temperature coefficient	{ I _R = 500μA T _A = operating Temperature range (Note 3)			.005 .01	%/°C
ICL8069C ICL8069D					
Reverse Current Range		0.050		5	mA

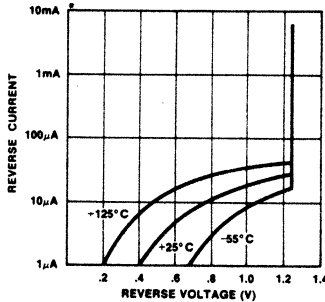
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



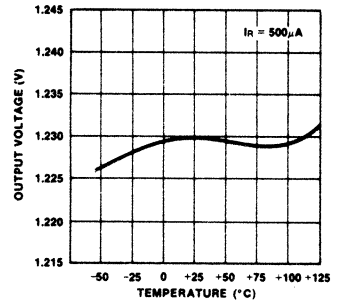
0327-6

REVERSE VOLTAGE AS A FUNCTION OF CURRENT



0327-7

REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



0327-8

- Notes:**
- 1) If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.
 - 2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
 - 3) For the military part, measurements are made at 25°C, -55°C, and +125°C. The unit is then classified as a function of the worst case T.C. from 25°C to -55°C, or 25°C to +125°C.

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NOTE: All typical values have been characterized but are not tested.

Section 7 — Operational Amplifiers

ICH8500/A	7-1
ICL7600	7-7
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ICL7605	7-19
ICL7606	7-19
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ICL7650	7-46
ICL7650S	7-54
ICL7652	7-64
ICL7652S	7-72
ICL8007	7-82
ICL8021	7-86
ICL8023	7-86
ICL8043	7-91
ICL8063	7-99
LM4250	7-108

ICH8500/A

Ultra Low Input-Bias Operational Amplifier



ICH8500/A

GENERAL DESCRIPTION

The ICH8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20kΩ potentiometer. The input bias current for the inverting and noninverting inputs is 0.1pA maximum for the ICH8500, and 0.01pA maximum for the ICH8500A.

Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential. This is the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.

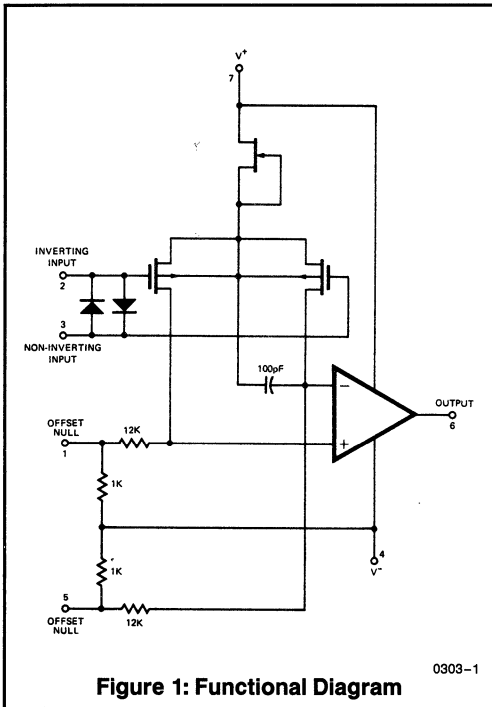


Figure 1: Functional Diagram

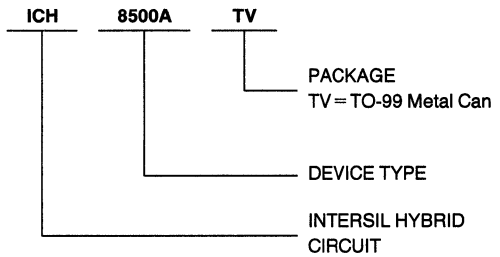
FEATURES

- Input Diode Protection
- Input Bias Current Less Than 0.01pA (8500A)
- No Frequency Compensation Required
- Offset Voltage Null Capability
- Short Circuit Protection
- Low Power Consumption

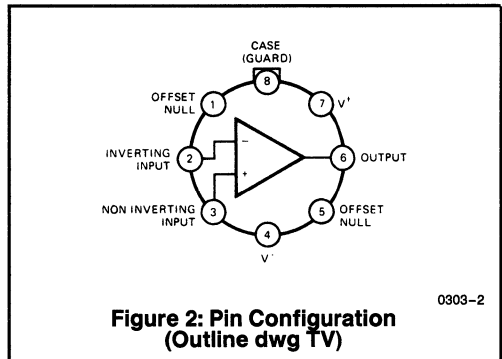
APPLICATIONS

- Femto Ammeter
- Electrometers
- Long Time Integrators
- Flame Detectors
- pH Meters
- Proximity Detector
- Sample and Hold Circuits

ORDERING INFORMATION



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**Figure 2: Pin Configuration
(Outline dwg TV)**

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

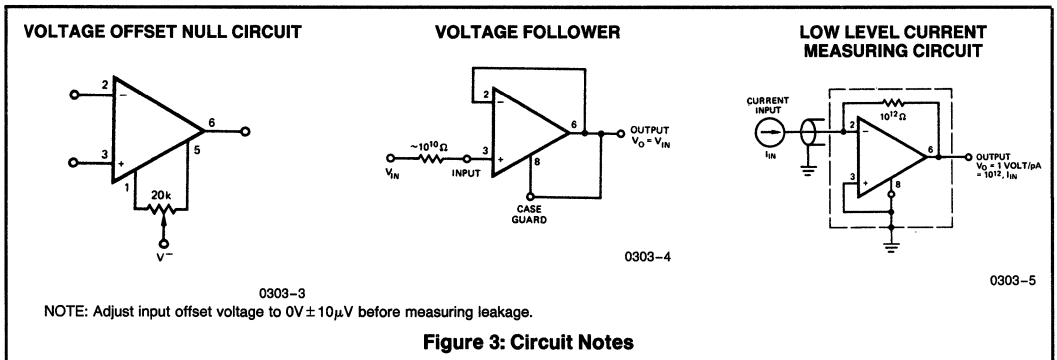
Supply Voltage	± 18V
Internal Power Dissipation (1)	500mW
Differential Voltage	± 0.5V
Storage Temperature	- 65°C to + 150°C
Operating Temperature	- 25°C to + 85°C
Lead Temperature (Soldering, 10sec)	300°C
Output Short Circuit Duration	Indefinite

Note: 1. Rating applies for ambient temperature to +70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_{SUPPLY} = ± 15V)

Symbol	Characteristics	Test Conditions	ICH8500			ICH8500A			Units
			Min	Typ	Max	Min	Typ	Max	
I _{BIAS}	Input Bias Current (Inverting and Non-Inverting)	Case at same potential as inputs			± 0.1			± 0.01	pA
V _{OS}	Input Offset Voltage				± 75			± 50	mV
	Offset Voltage Adjustment Range	20kΩ Potentiometer		± 50			± 50		mV
ΔV _{OS} /ΔT	Change in Input Offset Voltage Over Temperature	+ 25 to + 85°C - 25 to + 25°C		± 200			± 100		mV
ΔV _{OS} /Δt	Long Term Input Offset Voltage Stability	At 25°C		± 3.0			± 3.0		mV
CMRR	Common Mode Rejection Ratio	± 5 volts common mode voltage		75			75		dB
ΔV _O	Output Voltage Swing	R _L ≥ 10kΩ	± 11			± 11			V
CMVR	Common Mode Voltage Range		± 10			± 10			V
A _{VOL}	Large Signal Voltage Gain		20,000	10 ⁵		20,000	10 ⁵		—
C _{fb}	Feedback Capacitance	Case guarded		0.1			0.1		pF
SR	Slew Rate	R _L ≥ 2kΩ		0.5			0.5		V/μs
C _{IN}	Input Capacitance	Case guarded		0.7			0.7		pF
C _{IN}	Input Capacitance	Case grounded		1.5			1.5		pF

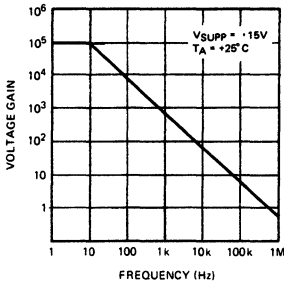


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NOTE: All typical values have been characterized but are not tested.

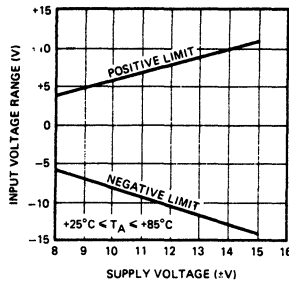
TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



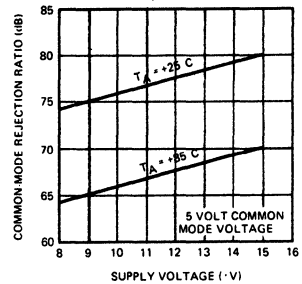
0303-6

INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



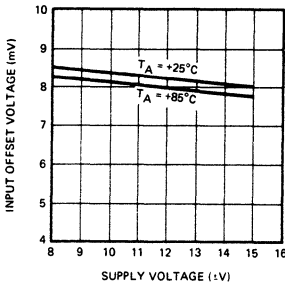
0303-7

COMMON MODE REJECTION RATIO vs. SUPPLY VOLTAGE



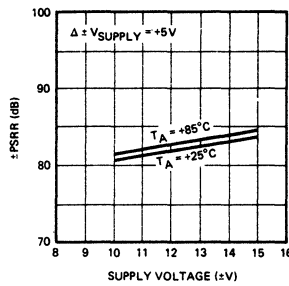
0303-8

INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



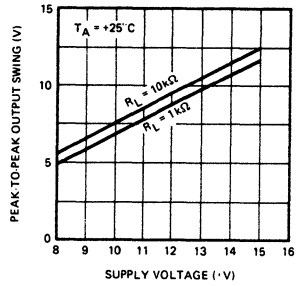
0303-9

± POWER SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



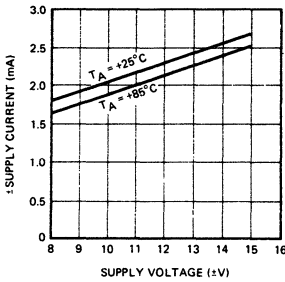
0303-10

OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



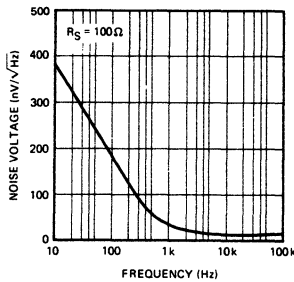
0303-11

± QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



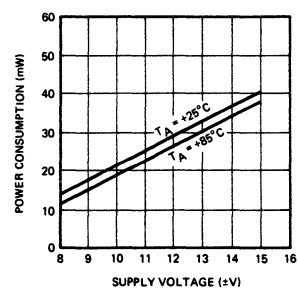
0303-12

INPUT REFERRED NOISE VOLTAGE



0303-13

POWER CONSUMPTION vs. SUPPLY VOLTAGE



0303-14

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

The Pico Ammeter

A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 4) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case the potential of the input is at virtual ground, or 0V. Therefore, the case of the device is grounded to intercept any stray leakage currents

that may otherwise exist between the $\pm 15V$ input terminals and the inverting input summing junctions. Feedback capacitance* should be kept to a minimum in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance C_{fb} times the feedback resistor R_{fb} . For instance, the time constant of the circuit in Figure 4 is 1 sec if $C_{fb} = 1pF$. Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied. C_{fb} of less than 0.2 to 0.3pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 5.

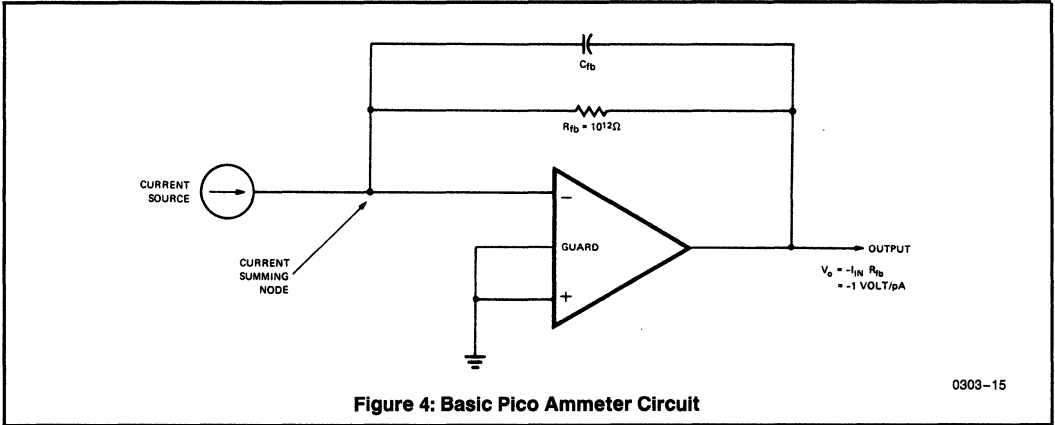


Figure 4: Basic Pico Ammeter Circuit

0303-15

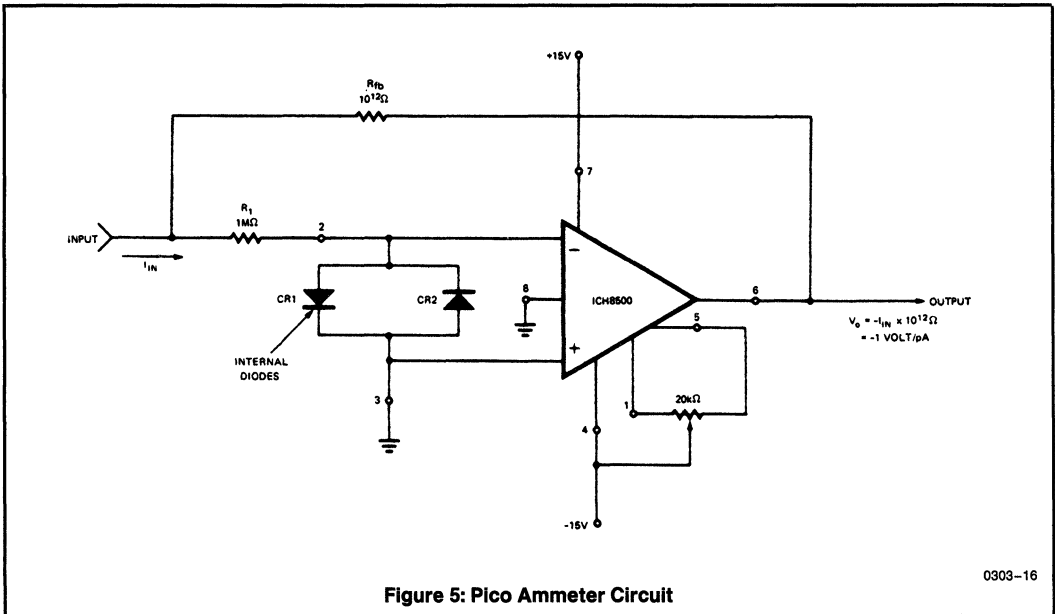


Figure 5: Pico Ammeter Circuit

0303-16

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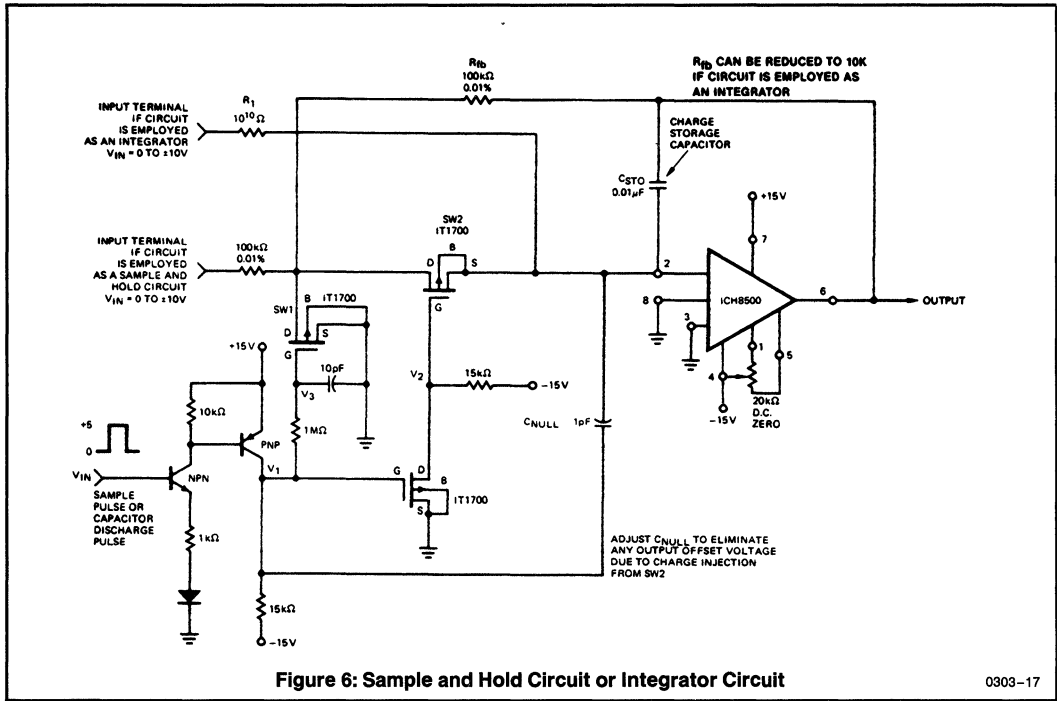


Figure 6: Sample and Hold Circuit or Integrator Circuit

0303-17

The internal diodes CR1 and CR2 together with external resistor R1 protect the input stage of the amplifier from voltage transients. The two diodes contribute no error currents, since under normal operating conditions there is no voltage across them.

*Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.

Sample and Hold Circuit

The basic principle of this circuit (Figure 6) is to rapidly charge a capacitor C_{STO} to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on C_{STO} . Since C_{STO} is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across C_{STO} should remain constant, causing the output of the amplifier to remain constant as well. However, the voltage across C_{STO} will decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of C_{STO} , leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existent ($<0.01\text{pA}$). Note that the voltages on the source, drain and

gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a low drift sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA . The rate of change of the voltage across the $0.01\mu\text{F}$ storage capacitor is then 10mV/sec . In contrast, if an operational amplifier which exhibited an input bias current of 1nA were employed, the rate of change of the voltage across C_{STO} would be 0.1V/sec . An error build up such as this could not be tolerated in most applications.

Waveforms illustrating the operation of the sample and hold circuit are shown in Figure 7.

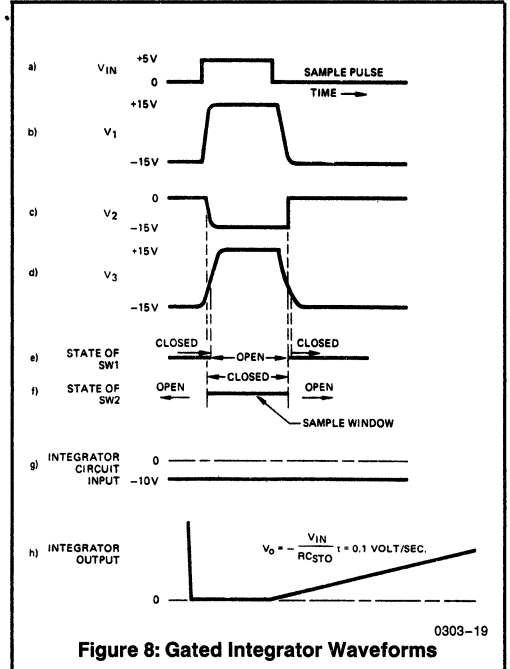
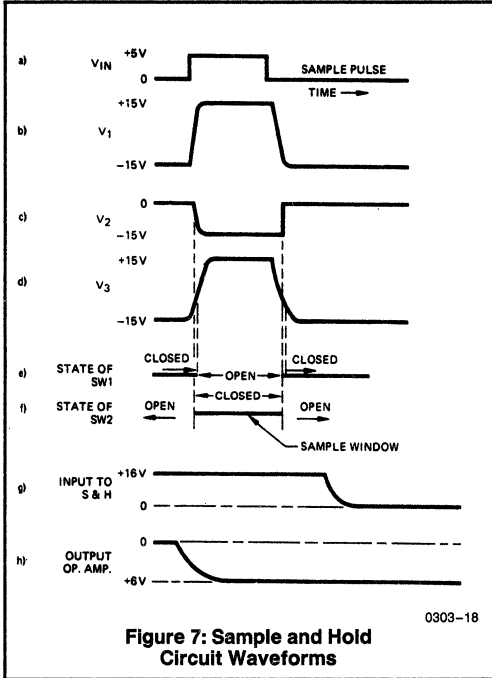
The Gated Integrator

The circuit in Figure 6 can double as an integrator. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of $R1$ and C_{STO} . Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of $R1$ (Up to 10^{12} ohms) can be employed. This permits the use of small values of integrating capacitor (C_{STO}) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 8.

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ICL7600/ICL7601

Commutating Auto-Zero (CAZ) Operational Amplifier



ICL7600/ICL7601

GENERAL DESCRIPTION

The ICL7600/ICL7601 commutating auto-zero (CAZ) operational amplifiers are designed to replace almost any of today's hybrid or monolithic ultra-low offset op amps, and will provide almost three orders of magnitude reduction in input offset voltage compared with conventional device designs. This is achieved through Intersil's CAZ amp principle, an entirely new approach to low-frequency operational amplifier design.

The key feature of the CAZ principle is automatic compensation for long-term drift phenomena and temperature effects. Two internal op amps are connected so that when one amplifier is processing an input signal the other is maintained in an "auto-zero" mode. The ICL7600/ICL7601 contains all of the circuitry required for system operation, including an oscillator, a counter, level translators, analog switches and operational amplifiers. Only two auto-zero capacitors are needed for complete operational amplifier function. Control of the oscillator and counter section is provided through the OSC and DR (division ratio) terminals. Internal biasing of the two on-chip op amps is programmable through a three-voltage-level terminal designated BIAS.

The ICL7600 is internally-compensated and is intended for applications which require voltage gains from unity through 20. The uncompensated ICL7601 is intended for those situations which require voltage gains of greater than 20. Major advantage of the ICL7601 over the ICL7600 at high gain settings is the reduction in commutation noise and subsequent greater accuracy.

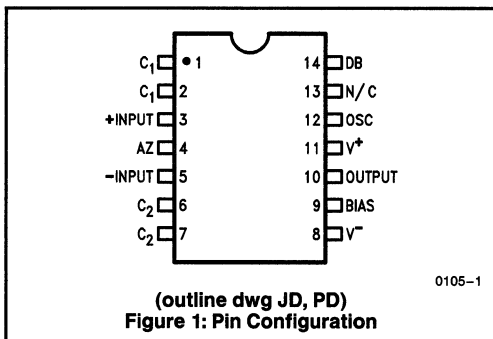
Minimum periodic adjustments and extremely low offset voltage and temperature coefficients make the CAZ operational amplifiers very desirable for operation in adverse environments (temperature, humidity, toxic or radioactive) where equipment service is difficult. Since the device will auto-zero its internal offset errors, no adjustment is required other than that of gain, which is established by the external resistors.

FEATURES

- Exceptionally low input offset voltage— $5 \mu\text{V}$
- Low long-term input offset voltage drift— $0.2 \mu\text{V}/\text{year}$
- Low input offset voltage temperature drift— $0.005 \mu\text{V}/^\circ\text{C}$
- Low DC input bias current— 300 pA
- Low DC input offset bias current— 150 pA
- Wide common mode and differential input voltage ranges
- Excellent low supply voltage operation—Down to $\pm 2\text{V}$
- Static-protected inputs—no special handling required
- Fabricated using proprietary MAXCMOST™ technology
- Compensated (ICL7600) or uncompensated (ICL7601) versions

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7600JJD	-25°C to $+85^\circ\text{C}$	14 Lead Cerdip
ICL7600MJD	-55°C to $+125^\circ\text{C}$	14 Lead Cerdip
ICL7601JJD	-25°C to $+85^\circ\text{C}$	14 Lead Cerdip
ICL7601MJD	-55°C to $+125^\circ\text{C}$	14 Lead Cerdip



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (sum of both positive and negative supply voltages, V^+ and V^-)	18 Volts
DR Input Voltage	$(V^+ + 0.3)$ to $(V^- - 8)$ Volts
Input Voltage (C_1 , C_2 , +INPUT, -INPUT, BIAS, OSC (Note 1))	$(V^+ + 0.3)$ to $(V^- - 0.3)$ Volts
Differential Input Voltage (Note 1)	$\pm(V^+ + 0.3)$ to $(V^- - 0.3)$
Duration of Output Short Circuit (Note 2)	Unlimited
Continuous Total Power Dissipation at or below +25°C free air temperature (Note 3)	
CERDIP Package	500 mW

Operating Temperature Range	
ICL7600XI	-25°C to +85°C
ICL7600XM	-55°C to +125°C
Storage Temperature Range	-55 to +150°C
Lead Temperature (soldering, 60 seconds)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of $(V^+ + 0.3)$ to $(V^- - 0.3)$ volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the ICL7600/ICL7601 supplies are established, and that if multiple supplies are used the ICL7600/ICL7601 supplies be activated first. No restrictions are placed on the differential input voltages on either the inverting or non-inverting inputs, so long as these voltages do not exceed the power supply voltages by more than 0.3V.

- 2: Outputs may be shorted to ground (GND) or to either supply (V^+ , V^-). Temperature and/or supply voltages must be limited to insure that the dissipation rating is not exceeded.
- 3: For operation above 25°C free-air temperature, derate 4mW/°C from 500mW for CERDIP and 3mW/°C from 375mW for plastic.

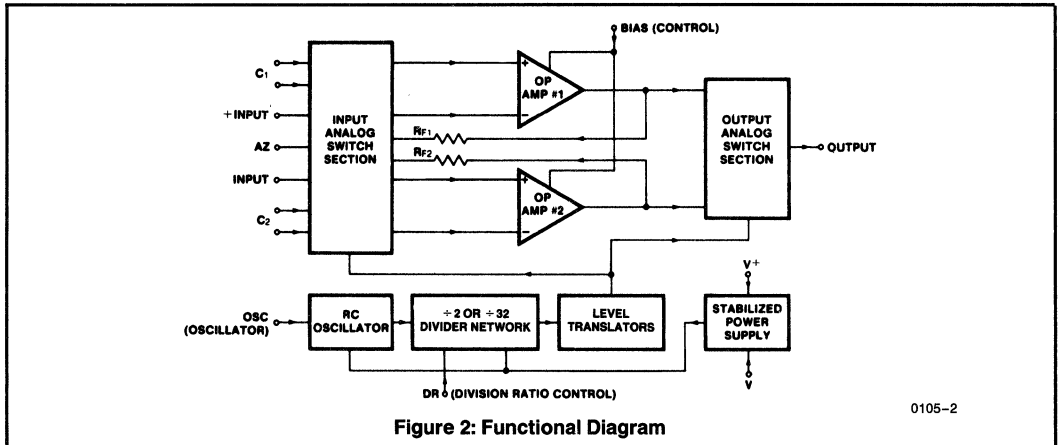


Figure 2: Functional Diagram

0105-2

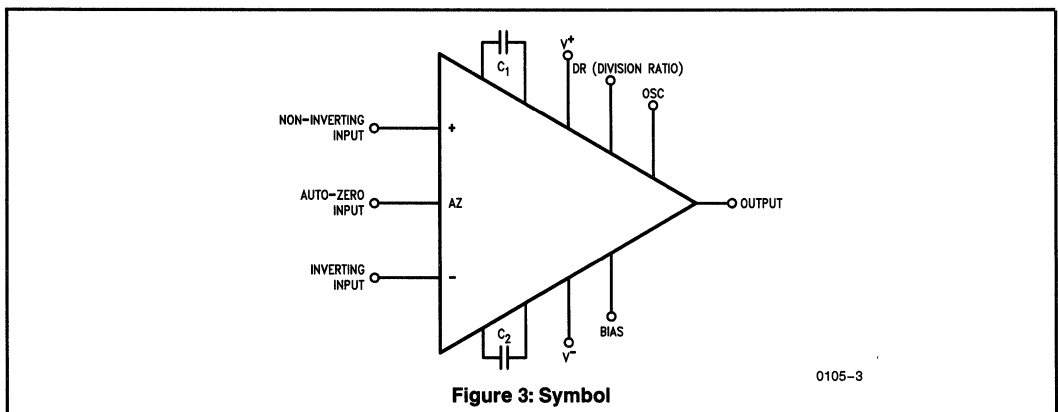


Figure 3: Symbol

0105-3

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25^\circ\text{C}$, DR pin connected to V^+ ($f_{\text{COM}} \approx 160\text{Hz}$), $C_1 = C_2 = 1\mu\text{F}$, Test Circuit 1, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S \leq 1\text{k}\Omega$	Low Bias Setting		± 2		μV
		$C_1 = C_2 = 1\mu\text{F}$	Med Bias Setting		± 5	± 10	μV
			High Bias Setting		± 7		μV
			MIL version over temp. Med Bias Setting			± 40	μV
V_{OS} Time	Long Term Input Offset Voltage Stability	Low or Med Bias Settings			0.2		$\mu\text{V}/\text{year}$
TCV_{OS}	Average Input Offset Voltage Temperature Coefficient (Note 4)	Low or Med Bias Settings $-55^\circ\text{C} > T_A > +25^\circ\text{C}$			0.005	0.2	$\mu\text{V}/^\circ\text{C}$
		$+25^\circ\text{C} > T_A > +85^\circ\text{C}$			0.01	0.2	$\mu\text{V}/^\circ\text{C}$
		$+25^\circ\text{C} > T_A > +125^\circ\text{C}$			0.05	0.2	$\mu\text{V}/^\circ\text{C}$
e_n	Noise Voltage (RMS)	Band Width	Low Bias		0.8		μV
		0.1 to 10Hz	Med Bias		0.8		μV
		$R_S \leq 1\text{k}\Omega$	High Bias		1.0		μV
$e_{\text{np-p}}$	Equivalent Input Noise Voltage Peak-to-peak	Band Width	Low Bias		4.0		μV
		0.1 to 10Hz	Med Bias		4.0		μV
		$R_S \leq 1\text{k}\Omega$	High Bias		5.0		μV
$e_{\text{n}10}$	Spot equivalent Noise voltage	$f = 10\text{Hz}$	Band Width 1Hz			700	$\text{nV}/\sqrt{\text{Hz}}$
$i_{\text{n}10}$	Spot equivalent Noise Current	$f = 10\text{Hz}$	Band Width 1Hz			0.1	$\text{pA}/\sqrt{\text{Hz}}$
DIF V_{IN}	Differential Input Voltage Range			$V^- - 0.3$	to	$V^+ + 0.3$	V
CMVR	Common Mode Input Range	Low Bias		-4.2		+4.2	V
		Med Bias		-4.0		+4.0	V
		High Bias		-3.5		+3.5	V
CMRR	Common Mode Rejection Ratio	Any Bias Setting			88		dB
PSRR	Power Supply Rejection Ratio	Any Bias Setting			110		dB
I_{NIB}	Non Inverting Input Bias Current	Any Bias Setting, (Includes charge injection currents)			0.300	3	nA
I_{IB}	Inverting Input Bias Current	Any Bias Setting, (Includes charge injection currents)			0.150	1.5	nA
A_V	Voltage Gain	$R_L = 100\text{k}\Omega$	Low Bias	90	105		dB
			Med Bias	90	105		dB
			High Bias	80	100		dB
V_{OUT}	Maximum Output Voltage Swing	$R_L = 1\text{M}\Omega$			± 4.9		V
						± 4.8	V
		$R_L = 100\text{k}\Omega$					V
				Positive Swing	+4.4		V
				Negative Swing			V
					-4.5	V	

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NOTE: All typical values have been characterized but are not tested.

ICL7600/ICL7601



ELECTRICAL CHARACTERISTICS (Continued)

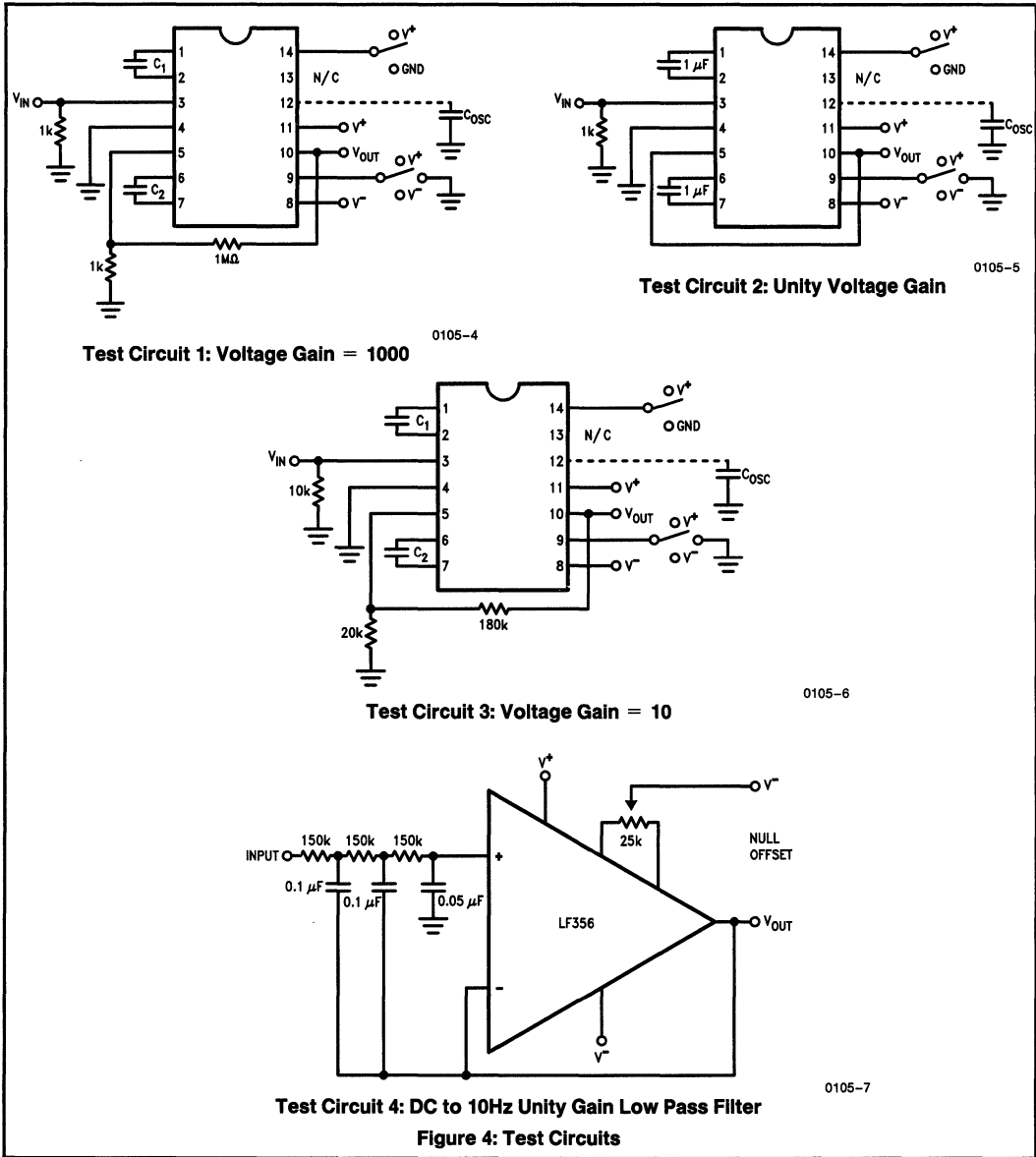
Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25^\circ\text{C}$, DR pin connected to V^+ ($f_{\text{COM}} \cong 160\text{Hz}$), $C_1 = C_2 = 1\mu\text{F}$, Test Circuit 1, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
SR	Large Signal Slew Rate	Unity Gain	High Bias Setting		1.8	$\text{V}/\mu\text{s}$	
		ICL7600	Med Bias Setting		0.5	$\text{V}/\mu\text{s}$	
			Low Bias Setting		0.2	$\text{V}/\mu\text{s}$	
GBW	Unity Gain Band Width	ICL7600	High Bias Setting		1.2	MHz	
			Med Bias Setting		0.3	MHz	
		Test Circuit 2	Low Bias Setting		0.12	MHz	
GBW	Extrapolated Unity Gain Band Width	ICL7601	High Bias Setting		1.8	MHz	
			Med Bias Setting		0.4	MHz	
			Low Bias Setting		0.2	MHz	
I_{BIAS}	BIAS Terminal Input Current	$V^- - 0.3 \leq V_{\text{BIAS}} \leq V^+ + 0.3$ volt		± 30		μA	
V_{BH}	BIAS Voltage to Define Current Modes	Low Bias Setting	$V^+ - 0.3$	V^+	$V^+ + 0.3$	V	
V_{BM}			Med Bias Setting	$V^- + 1.4$	GND	$V^+ - 1.4$	V
V_{BL}				High Bias Setting	$V^- - 0.3$	V^-	$V^- + 0.3$
I_{DR}	DR (Division Ratio) Input Current	$V^+ - 8.0\text{V} \leq V_{\text{DR}} \leq V^+ + 0.3\text{V}$		± 30		μA	
V_{DRH}	DR Voltage to define oscillator division ratio	Internal oscillator division ratio 32	$V^+ - 0.3$		$V^+ + 0.3$	V	
V_{DRL}		Internal oscillator division ratio 2	$V^+ - 8$		$V^+ - 1.4$	V	
f_{COM}	Nominal Commutation Frequency	$C_{\text{OSC}} = 0$ pF	DR Connected to V^+		160	Hz	
			DR Connected to GND		2560	Hz	
I_{S}	Supply Current	High Bias Setting	Medium Bias Setting	Low Bias Setting	7	15	mA
					1.7	5	mA
					0.6	1.5	mA
$V^+ - V^-$	Operating Supply Voltage Range	High Bias Setting	Medium or Low Bias Setting	5	16	V	
				4	16	V	

NOTE 4: For design only, not tested.

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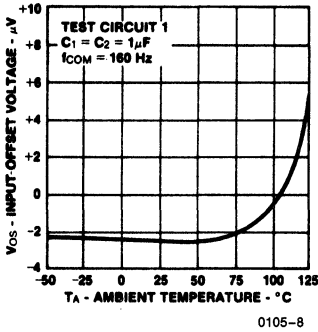
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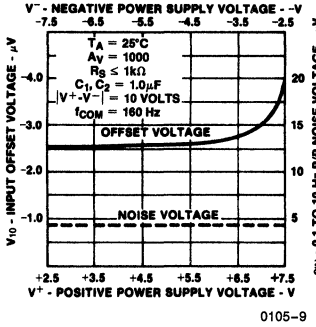
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

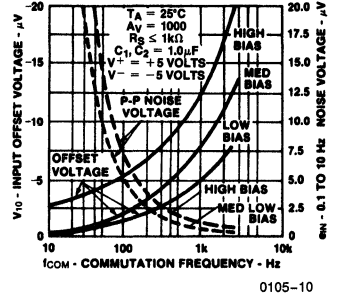
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



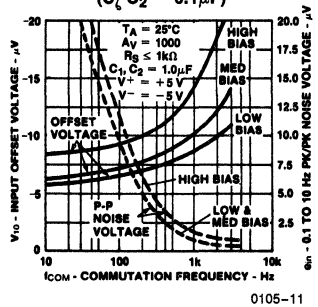
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



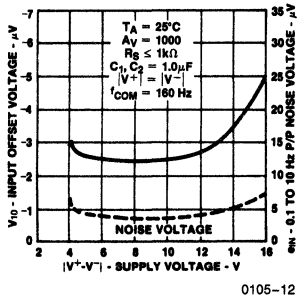
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY ($C_1 C_2 = 1\mu F$)



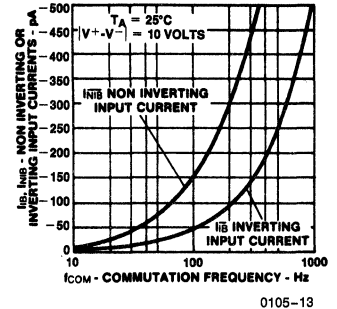
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY ($C_1 C_2 = 0.1\mu F$)



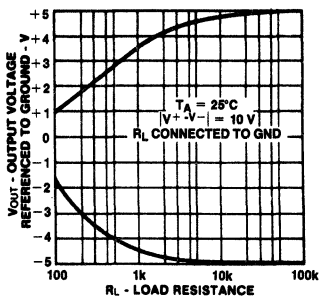
INPUT OFFSET VOLTAGE AND PK TO PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE ($V^+ - V^-$)



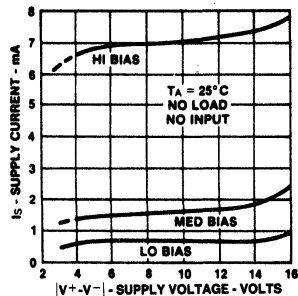
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



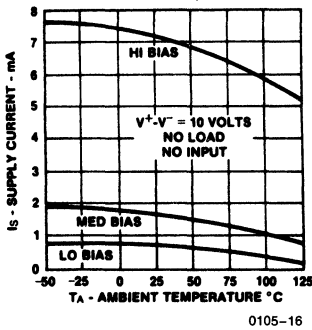
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



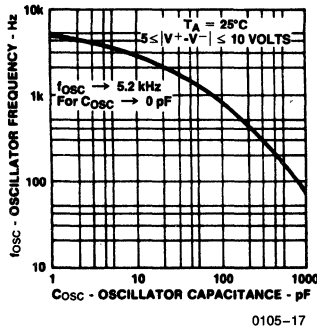
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NOTE: All typical values have been characterized but are not tested.

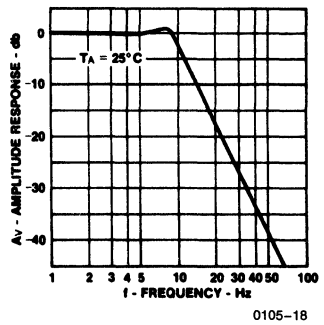
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



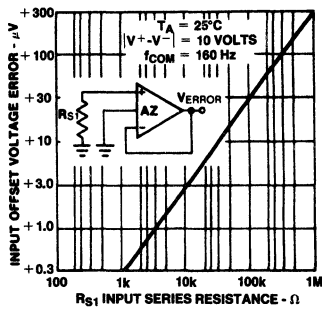
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



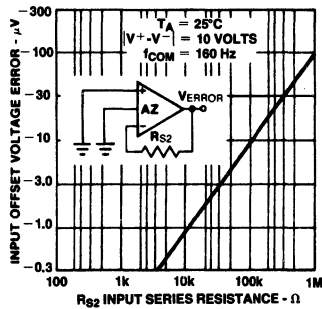
FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 4).



TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE—INPUT



TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE—INPUT



DETAILED DESCRIPTION

CAZ Operational Amplifier Operation

The CAZ operational amplifier functions on principles which are very different from those encountered in conventional op amp types. An important advantage of the ICL7600/ICL7601 devices is the ability to self-compensate for internal error voltages, whether they are steady-state, related to temperature or supply voltage, or variable in nature over a long term.

Operation of the ICL7600/ICL7601 CAZ operational amplifier is demonstrated in Figure 5. The basic amplifier configuration represented by the large triangles has one more input than does a regular op amp—the AZ, or auto-zero input. The voltage at the AZ input is that to which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges the external capacitor C_2 to a

voltage equal to the DC offset voltage of that amplifier and the instantaneous low frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps in the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which was charged to a voltage equal to its offset and noise voltage) connected in series to its non-inverting (+) input and nulls out the input offset and noise voltage of the amplifier. While one of the op amps is processing the input signal, the other is placed in the auto-zero mode and charges its capacitor to a voltage equal to its equivalent DC and low-frequency error voltage. The internal op amps are reconnected at a rate designated as the commutation frequency, f_{COM} .

The CAZ amp concept offers a number of other advantages to the designer, as compared to standard bipolar or FET-input op amps:

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NOTE: All typical values have been characterized but are not tested.

- Effective input offset voltages can be made between 1000x and 10,000x less without trimming.
- Long-term drift phenomena are compensated for and dramatically reduced.
- Temperature effects are compensated for over a wide range. Reductions can be as high as 100 times or higher.
- Supply voltage sensitivity is reduced.

The on-chip op amps are connected internally to the external input and output terminals via CMOS analog switches, as shown in Figure 6. The analog switch structure shown in Figure 6 is arranged so that at any time three switches are open and three switches are conducting. Each analog switch includes a P-channel transistor in parallel with an N-channel transistor.

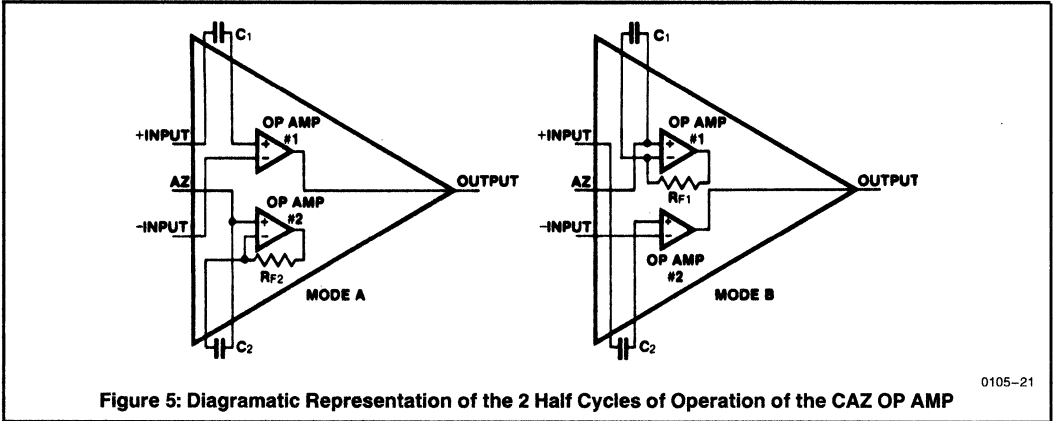


Figure 5: Diagrammatic Representation of the 2 Half Cycles of Operation of the CAZ OP AMP

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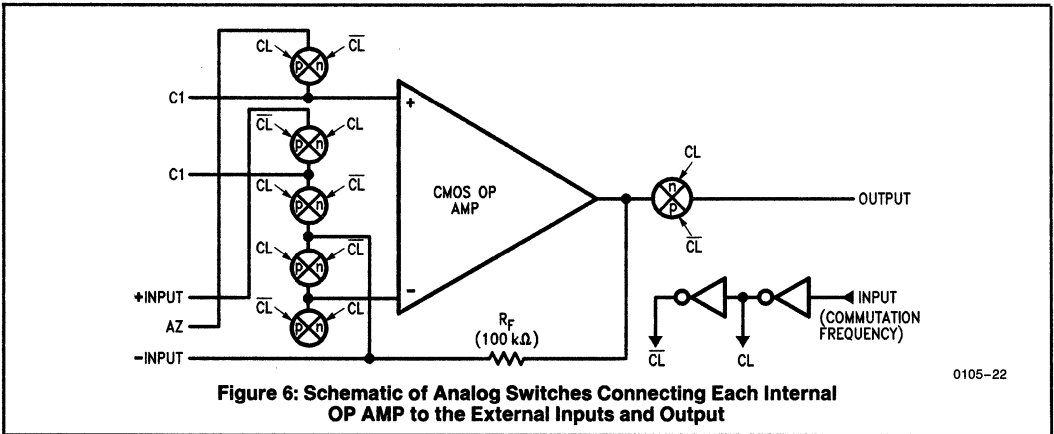


Figure 6: Schematic of Analog Switches Connecting Each Internal OP AMP to the External Inputs and Output

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

The ICL7600/ICL7601 CAZ op amp is ideal for use as a front-end preamplifier for dual-slope A/D converters which require high sensitivity for single-ended input sources such as thermocouples.

A typical high-sensitivity A/D converter system is shown in Figure 7. The system uses an Intersil ICL7109 12-bit monolithic A/D binary converter, and is intended for direct interface with microprocessors. Both the ICL7600/ICL7601 and the ICL7109 use power supply voltages of $\pm 5V$, and the entire system consumes typically 2.5 mA of current.

The input signal is applied through a low-pass filter (150 Hz) to the CAZ op amp, which is connected in a non-inverting gain configuration of either 10 or 100. The internal oscillator of the CAZ amp is allowed to run free at about 5,200 Hz, resulting in a commutation frequency of 160 Hz, with the DR terminal connected to V^+ . The error-storage capacitors C_1 and C_2 are each $1 \mu F$ value, and provide a good compromise between the minimum equivalent input offset voltage and the lowest value of low-frequency noise.

The output signal is then passed through a low-pass filter (1 M Ω and 0.1 μF), with a bandwidth of 1.5 Hz. This results in an equivalent DC offset voltage of $1 \mu V$ to $2 \mu V$, and a peak-to-peak noise voltage of $1.7 \mu V$, referred to the input of the CAZ amp. The output from the low-pass filter feeds directly into the input of the ICL7109.

In a system such as that shown in Figure 7 there is a degree of flexibility possible in assigning various gains to the ICL7600/ICL7601 pre-amplifier, and to various sensitivities for the ICL7109. For optimum performance, the CAZ op amp must amplify the input signal so that the equivalent, $15 \mu V$ input noise voltage of the A/D converter is masked.

This implies a gain of at least 10 for the CAZ op amp preamplifier.

On the other hand, if the gain of the CAZ op amp is increased too much, its output swing will be limited by the $\pm 5V$ supplies. This condition imposes a maximum gain of 200 to produce an output of ± 0.000005 times 4,096 times 200, or $\pm 4,096V$, for a $5 \mu V$ per count sensitivity. Use of an ICL7600 is recommended for low gains (<20) and the ICL7601 for gains of more than 20.

The values of the integrating resistor and the reference voltage must be chosen to suit the overall sensitivity of the system. For example, in a system requiring a sensitivity of $5 \mu V$ per count, use a CAZ amp in a gain configuration of 50 (with ICL7601). Thus for a full scale count of 4096 (12 bits), the input voltage to the ICL7109 would be $5 \mu V$ times 50 times 4096 or 1.024 volts. Since the ratio of input to reference is 2:1, the value of the reference voltage becomes 0.512 and a 50 k Ω integrating resistor is recommended. A system such as that shown in Figure 7 will allow a resolution of $1^\circ C$ for low sensitivity platinum/rhodium junctions. For $0.1^\circ C$ resolution, use high sensitivity thermocouples having copper/constantan junctions.

The low-pass filter between the output of the CAZ op amp and the input of the ICL7109 A/D converter can be used to improve the signal-to-noise ratio of the system by reducing bandwidth. A 10 Hz filter will result in an equivalent peak-to-peak noise voltage figure of $4 \mu V$. If the bandwidth is reduced to 1.5 Hz, the peak-to-peak noise voltage will be reduced to about $1.7 \mu V$, a reduction by a factor of three. The penalty for this reduction will be a longer system response time; however in most cases this will not be a major consideration, because of the large thermal inertia of many thermocouple probes.

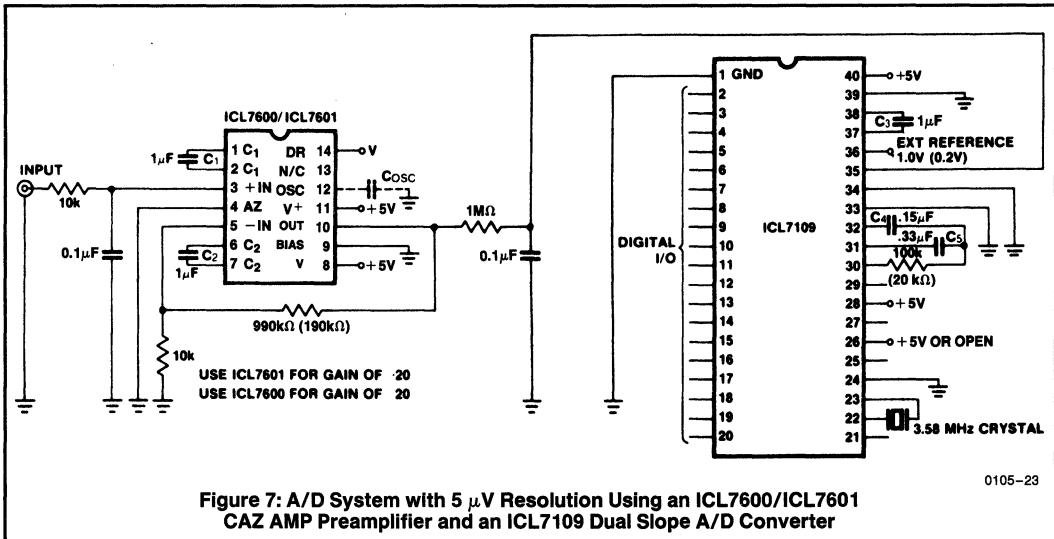


Figure 7: A/D System with $5 \mu V$ Resolution Using an ICL7600/ICL7601 CAZ AMP Preamplifier and an ICL7109 Dual Slope A/D Converter

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SOME HELPFUL HINTS

Testing the ICL7600/ICL7601 CAZ Operational Amplifier

A simple and relatively accurate means of testing the CAZ op amp is to use a Tektronix Type 577 curve tracer, with the CAZ op amp inserted in a special 14-lead socket which plugs into a Tektronix 178, and which contains two soldered-in auto-zero capacitors of 1 μF each. This simple and convenient tester will provide most of the information needed for low-frequency parameters. The test setup will allow resolution of input offset voltages to about 10 μV .

For greater accuracy, it is suggested that a breadboard be built which minimizes thermoelectric effects and which includes an output low-pass filter of the type shown in Test Circuit #4. The output from the CAZ amp can be connected to a dual-slope A/D converter as shown in Figure 7. The low-frequency noise can then be displayed on a storage scope or on a strip chart recorder.

Bias Control

The on-chip op amps consume over 90% of the power required for the ICL7600/ICL7601. Three externally-programmable bias levels are provided. These levels are set by connecting the BIAS terminal to V^+ , GND or V^- , for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is approximately a factor of three, which allows a 9:1 ratio between supply current and the bias setting. The reason for this current programmability is to provide the user with a choice of device power dissipation levels, slew rate values (the higher the slew rate the better the recovery from commutation spikes), and offset errors due to chip "voltage drop" and thermoelectric effects (the higher the power dissipation the higher the input offset error). In most cases, the medium (MED BIAS) setting will be the best choice.

Output Loading (Resistive)

With a 10 k Ω load the output swing can cover nearly the entire supply voltage range, and the device can be used with loads as low as 2 k Ω . However, with loads of less than 50 k Ω , the on-chip op amps become transconductance amplifiers, since their output impedances are about 50 k Ω each. Thus the open-loop gain is 20 dB less with a 2 k Ω load than it would be with a 20 k Ω load. For high gain configurations requiring high accuracy, output loads of 100 k Ω or more are suggested.

Another consideration which must not be overlooked is the additional power dissipation of the chip which results from a large output swing into a low value load. This added variable can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output to reduce high-frequency noise outside the signal passband of interest. With conventional op amps, the obvious solution would be to place a capacitor across the external feedback resistor to provide the low pass filter.

However, with the CAZ op amp, this is not feasible because of the nature of commutation voltage spikes. The voltage spikes show a low impedance characteristic in the direction of the auto-zero voltage, and a high impedance on

the recovery edge, as shown in Figure 8. It can be seen that the effect of the large load capacitor is to produce an area error in the output waveform, and hence an effective gain error. The output low pass filter must be a high impedance type to avoid output voltage area errors. For example, a 1.5 Hz filter should use a 100 k Ω resistor and a 1.0 μF capacitor, or a 1.0 M Ω resistor and an 0.1 μF capacitor. This effect also causes problems with integrator circuits.

Oscillator and Digital Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open-circuited. If the full divider network is used, this will result in a commutation frequency of about 160 Hz nominal. The commutation frequency is the frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents approximately the optimum frequency at which the input offset voltage is close to minimum, where the low-frequency noise is acceptable, and where errors derived from noise spikes will be low. Other commutation frequencies may provide optimization of other parameters, but always to the detriment of major characteristics.

The oscillator is of a high impedance type, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the desired frequency of the oscillation is 5.2 kHz, the terminal should be left unattached and open. In other instances, it may be desirable to lock the oscillator to a clock or to run it at another frequency. The ICL7600/ICL7601 provides two degrees of flexibility. First, the DR (division ratio) terminal permits the user to choose between dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND), to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and V^+ , or system ground terminals. For situations which require the commutation frequency to be locked onto a master clock, the OSC terminal can be driven from TTL logic (with resistive pull-up) or from CMOS logic, provided that the V^+ supply (with respect to ground) is +5V ($\pm 10\%$) and the logic driver also operates from a similar supply voltage. This is because the logic section—including the oscillator—operates from an internal -5V supply referenced to V^+ generated on-chip, and is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-precision DC amplifiers are thermoelectric, Peltier or thermocouple effects in junctions consisting of various metals, alloys, silicon, etc. Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1 $\mu\text{V}/^\circ\text{C}$. However, these voltages can be several tens of microvolts per $^\circ\text{C}$ for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can provide, it is essential to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum. Use the medium bias mode as well as a high impedance load, and keep well away from heat dissipated by surrounding equipment.

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NOTE: All typical values have been characterized but are not tested.

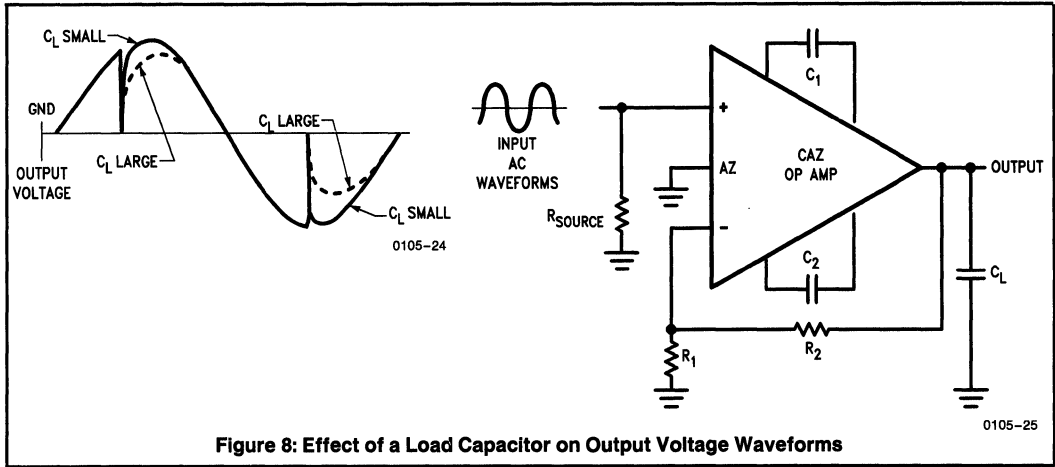


Figure 8: Effect of a Load Capacitor on Output Voltage Waveforms

Component Selection

The two required auto-zero capacitors, C_1 and C_2 , should each be of $1.0 \mu\text{F}$ value. These are large values for non-electrolytic capacitors, but since the voltages impressed on them do not change significantly, problems of dielectric absorption and the like are not important.

Excellent results have been obtained in operation at commercial temperature ranges using several of the smaller-size and more economical capacitors, since the absolute values of the capacitors is not critical. Even polarized electrolytic capacitors rated at $1.0 \mu\text{F}/50\text{V}$, though not recommended, have been used with success.

Commutating Voltage Transient Effects

While in most respects the CAZ op amp behaves like a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 100 Hz. This is because of the finite switching transients which occur in the input and output terminals due to commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and include all of the higher harmonics. If the commutation frequency is higher than the highest in-band frequency, these transients can be effectively blanked with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage equal to the input offset voltage (about 5–10 mV) which occurs during the transition to the signal processing mode from the auto-

zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must be at least $10,000 \times 10 \text{ pF}$, or $0.1 \mu\text{F}$ each.

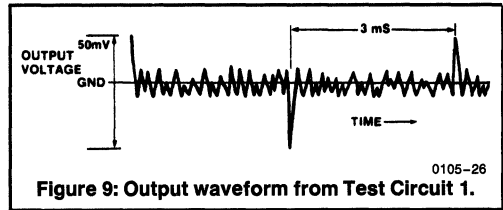


Figure 9: Output waveform from Test Circuit 1.

The charge which is injected into the op amp when it is switched into the signal-processing mode produces a rapidly-decaying voltage spike at the input, in addition to an equivalent DC bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically about 1.0 pA at ambient temperature of 25°C.

The output waveform of Test Circuit #1 (with no input) is shown in Figure 9. Note that the equivalent noise voltage shown is amplified 1000 times, and that because of the finite slew rate of the on-chip op amps the 7 mV input transients are *not* amplified by 1000.

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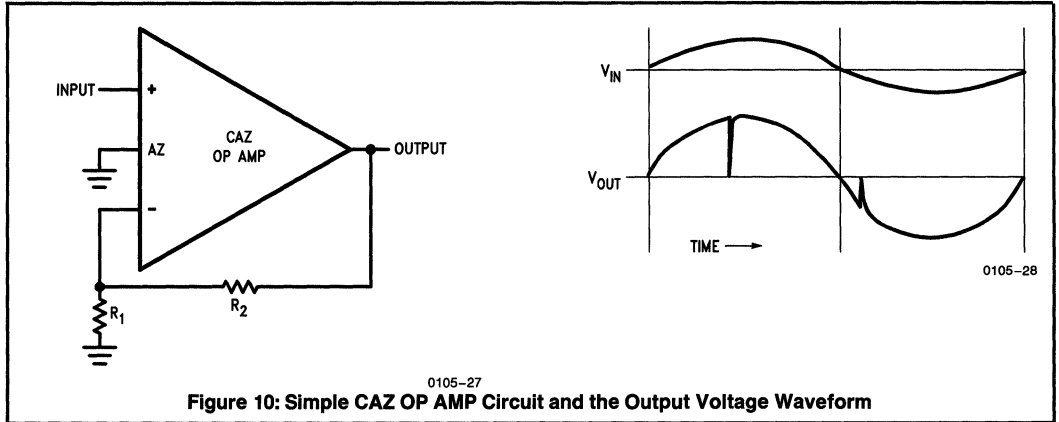
The output transient voltage effects (as distinct from the input effects which are propagated through the on-chip op amps) will occur if there is a difference in the output voltage of the internal op amps between the auto-zero modes and the signal-processing modes. The output stage of the on-chip op amp must slew from its auto-zero output voltage to the desired signal-processing output voltage. This is shown in Figure 10, where the system is auto-zeroed to ground.

The duration of the output transients is greatly affected by the gain configuration and the bias setting, since these two parameters have an effect on system slew rate. At low gains and high bias settings, the output transient durations are very short. For this reason there are two versions of the

CAZ op amp, the ICL7600 which is compensated for unity gain and which can be used for gain configurations up to 20, and the ICL7601, which is uncompensated and recommended for operation in gain configurations greater than 20. Thus, when a signal is being processed in a high gain configuration, the effective output signal error is greater for the ICL7600 than it is for the ICL7601.

Non-Amplifier Applications

In principle, this is one of the few "chopper-stabilized" type amplifiers that could be used as a comparator; the transient effects on the output will normally require careful synchronism of output strobes with oscillator drive.



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NOTE: All typical values have been characterized but are not tested.

ICL7605/ICL7606

Commutating Auto-Zero (CAZ) Instrumentation Amplifier



ICL7605/ICL7606

GENERAL DESCRIPTION

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10Hz. This is made possible by the unique construction of this Intersil device, which takes an entirely new design approach to low frequency amplifiers.

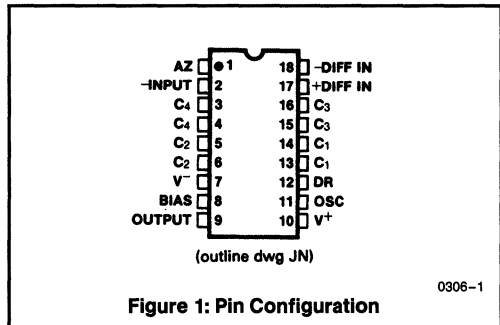
Unlike conventional amplifier designs, which employ three op-amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long-term drift phenomena and temperature effects, and a flying capacitor input.

The ICL7605/ICL7606 consist of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

FEATURES

- Exceptionally Low Input Offset Voltage — $2\mu\text{V}$
- Low Long Term Input Offset Voltage Drift — $0.2\mu\text{V}/\text{Year}$
- Low Input Offset Voltage Temperature Coefficient — $0.05\mu\text{V}/^\circ\text{C}$
- Wide Common Mode Input Voltage Range — 0.3V Above Supply Rail
- High Common Mode Rejection Ratio — 100 dB
- Operates at Supply Voltages As Low As $\pm 2\text{V}$
- Short Circuit Protection On Outputs for $\pm 5\text{V}$ Operation
- Static-Protected Inputs — No Special Handling Required
- Compensated (ICL7605) or Uncompensated (ICL7606) Versions



7

ORDERING INFORMATION

Order parts by the following part numbers:

Part Number	Compensation	Temperature Range	Package
ICL7605CJN	INTERNAL	0°C to $+70^\circ\text{C}$	18-PIN CERDIP
ICL7605IJN	INTERNAL	-25°C to $+85^\circ\text{C}$	18-PIN CERDIP
ICL7605MJN	INTERNAL	-55°C to $+125^\circ\text{C}$	18-PIN CERDIP
ICL7606CJN	EXTERNAL	0°C to $+70^\circ\text{C}$	18-PIN CERDIP
ICL7606IJN	EXTERNAL	-25°C to $+85^\circ\text{C}$	18-PIN CERDIP
ICL7606MJN	EXTERNAL	-55°C to $+125^\circ\text{C}$	18-PIN CERDIP

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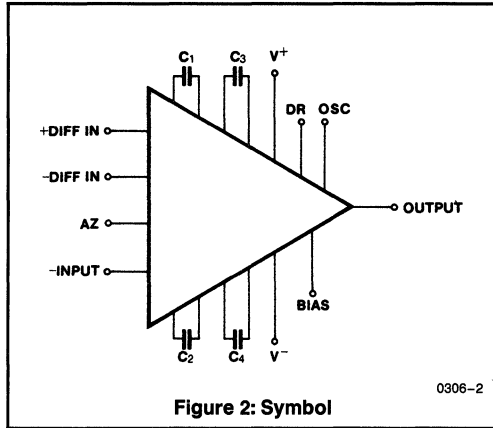


Figure 2: Symbol

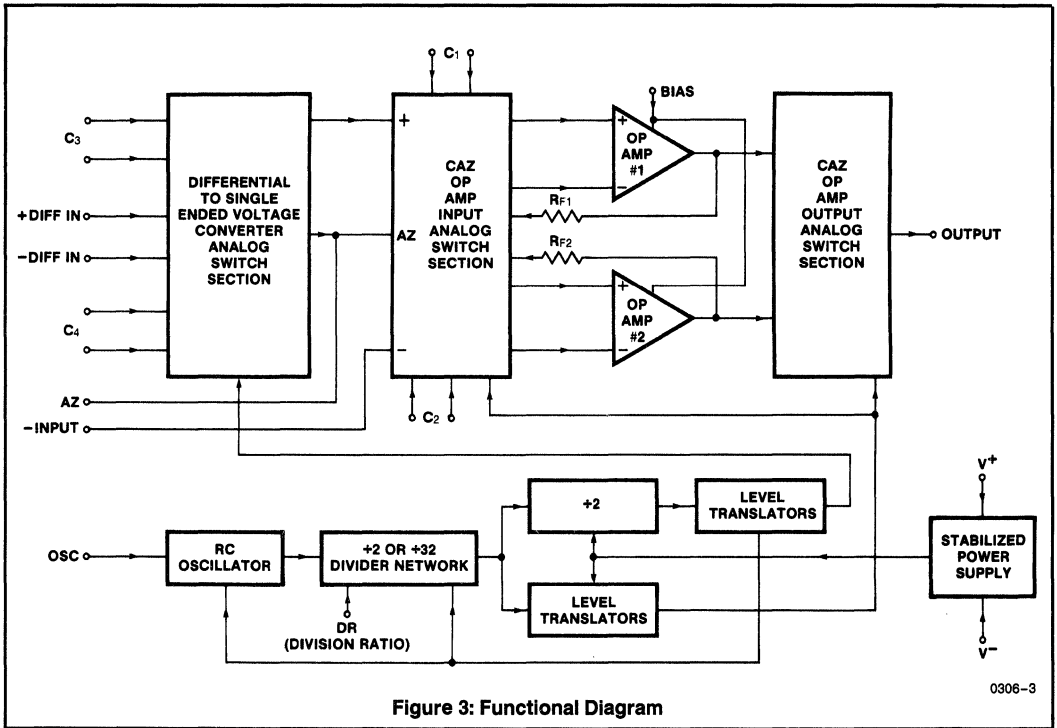


Figure 3: Functional Diagram

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ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
 DR Input Voltage ($V^+ - 8$) to ($V^+ + 0.3$)V
 Input Voltage ($C_1, C_2, C_3, C_4 + \text{DIFF IN}, -\text{DIFF IN},$
 $-\text{INPUT}, \text{BIAS}, \text{OSC}$),
 (Note 1) ($V^- - 0.3$) to ($V^+ + 0.3$)V
 Differential Input Voltage (+DIFF IN to -DIFF IN)
 (Note 2) ($V^- - 0.3$) to ($V^+ + 0.3$)V
 Duration of Output Short Circuit (Note 3) Unlimited

Continuous Total Power Dissipation (Note 4) 500mW
 Operating Temperature Range:
 ICL7605/ICL7606C 0 to +70°C
 ICL7605/ICL7606I -25°C to +85°C
 ICL7605/ICL7606M -55°C to +125°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latch up. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.

Note 2: No restrictions are placed on the differential input voltages on either the +DIFF IN or -DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 3: The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 4: For operation above 25°C ambient temperature, derate 4mW/°C from 500mW above 25°C.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V, V^- = -5V, T_A = +25^\circ\text{C}$, DR pin connected to V^+ ($f_{\text{COM}} \cong 160\text{Hz}, f_{\text{COM}1} \cong 80\text{Hz}$),
 $C_1 = C_2 = C_3 = C_4 = 1\mu\text{F}$, Test Circuit 1 unless otherwise specified.

Symbol	Parameter	Test Conditions	Value			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 1\text{k}\Omega$ Low Bias Setting Med Bias Setting High Bias Setting MIL version over temp. Med Bias Setting		± 2		μV
				± 2	± 5	μV
				± 7		μV
					± 30	μV
$\Delta V_{\text{OS}}/\Delta T$	Average Input Offset Voltage Temperature Coefficient (Note 5)	Low or Med Bias Settings $-55^\circ\text{C} > T_A > +25^\circ\text{C}$ $+25^\circ\text{C} > T_A > +85^\circ\text{C}$ $+25^\circ\text{C} > T_A > +125^\circ\text{C}$		0.01	0.2	$\mu\text{V}/^\circ\text{C}$
				0.01	0.2	$\mu\text{V}/^\circ\text{C}$
				0.05	0.2	$\mu\text{V}/^\circ\text{C}$
$\Delta V_{\text{OS}}/\Delta t$	Long Term Input Offset Voltage Stability	Low or Med Bias Settings		0.5		$\mu\text{V}/\text{Year}$
CMVR	Common Mode Input Range		-5.3		+5.3	V
CMRR	Common Mode Rejection Ratio	$C_{\text{OSC}} = 0$, DR connected to V^+ , $C_3 = C_4 = 1\mu\text{F}$ $C_{\text{OSC}} = 1\mu\text{F}$, DR connected to GND, $C_3 = C_4 = 1\mu\text{F}$ $C_{\text{OSC}} = 1\mu\text{F}$, DR connected to GND, $C_3 = C_4 = 10\mu\text{F}$		94		dB
				100		dB
				104		dB
PSRR	Power Supply Rejection Ratio			110		dB
$-I_{\text{BIAS}}$	-INPUT Bias Current	Any bias setting, $f_c = 160\text{Hz}$ (Includes charge injection currents)		0.15	1.5	nA
$\bar{e}_n(\text{p-p})$	Equivalent Input Noise Voltage peak-to-peak	Band Width 0.1 to 10Hz		4.0		μV
				4.0		μV
				5.0		μV

7

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25^\circ C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified. (Continued)

Symbol	Parameter	Test Conditions	Value			Units
			Min	Typ	Max	
\bar{e}_n	Equivalent Input Noise voltage	Band Width 0.1 to 1.0Hz All Bias Modes		1.7		μV
A_{VOL}	Open Loop Voltage Gain	$R_L = 10k\Omega$ Low Bias Setting Med Bias Setting High Bias Setting	90 90 80	105 105 100		dB dB dB
$\pm V_O$	Maximum Output Voltage Swing	$R_L = 1M\Omega$ $R_L = 100k\Omega$ $R_L = 10k\Omega$ Positive Swing Negative Swing	+ 4.4	± 4.9 ± 4.8		V V V V
GBW	Bandwidth of Input Voltage Translator	$C_3 = C_4 = 1\mu F$ All Bias Modes		10		Hz
f_{COM}	Nominal Commutation Frequency	$C_{OSC} = 0$ DR Connected to V^+ DR Connected to GND		160 2560		Hz Hz
f_{COM1}	Nominal Input Converter Commutation Frequency	$C_{OSC} = 0$ DR Connected to V^+ DR Connected to GND		80 1280		Hz Hz
V_{BH} V_{BM} V_{BL}	Bias Voltage required to set Quiescent Current	Low Bias Setting Med Bias Setting High Bias Setting	$V^+ - 0.3$ $V^- + 1.4$ $V^- - 0.3$	V^+ GND V^-	$V^+ + 0.3$ $V^+ - 1.4$ $V^- + 0.3$	V V V
I_{BIAS}	Bias (Pin 8) Input Current			± 30		μA
I_{DR}	Division Ratio Input Current	$V^+ - 8.0 \leq V_{DR} \leq V^+ + 0.3$ volt		± 30		μA
V_{DRH} V_{DRL}	DR Voltage required to set Oscillator division ratio	Internal oscillator division ratio 32 Internal oscillator division ratio 2	$V^+ - 0.3$ $V^+ - 8$		$V^+ + 0.3$ $V^+ - 1.4$	V V
R_{AS}	Effective Impedance of Voltage Translator Analog Switches			30		$k\Omega$
I_{SUPP}	Supply Current	High Bias Setting Med Bias Setting Low Bias Setting		7 1.7 0.6	15 5 1.5	mA mA mA
$V^+ - V^-$	Operating Supply Voltage Range	High Bias Setting Med or Low Bias Setting	5 4		10 10	V V

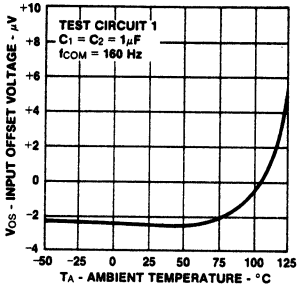
Note 5: For Design only, not tested.

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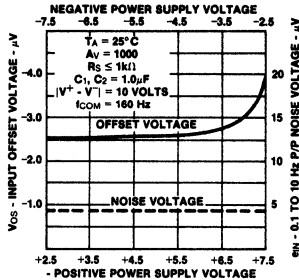
TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



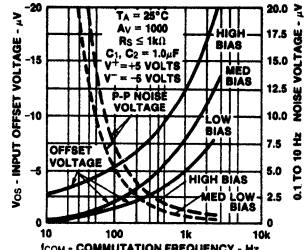
0306-4

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



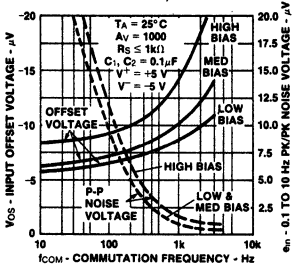
0306-5

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY ($C_1, C_2 = 1 \mu\text{F}$)



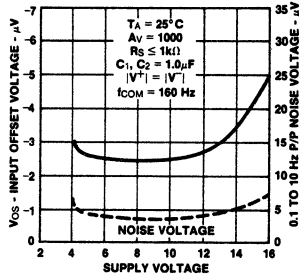
0306-6

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY ($C_1, C_2 = 0.1 \mu\text{F}$)



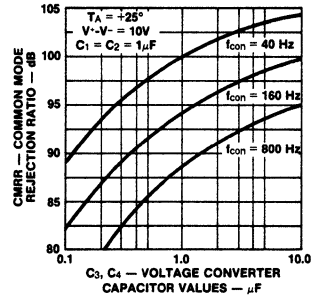
0306-7

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE ($V^+ - V^-$)



0306-8

COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



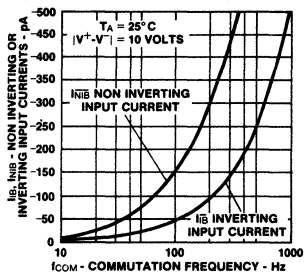
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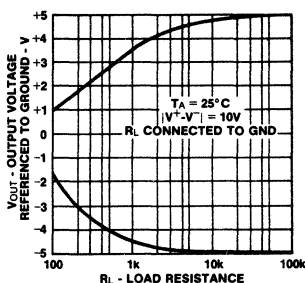
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



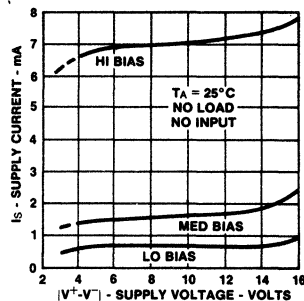
0306-10

MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



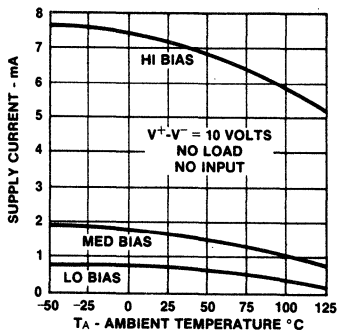
0306-11

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



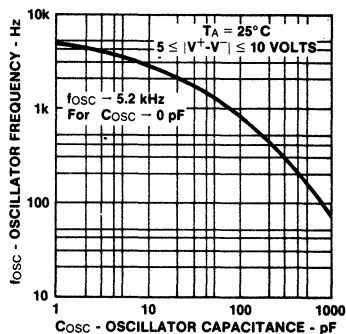
0306-12

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



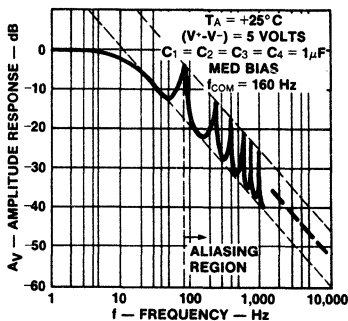
0306-13

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



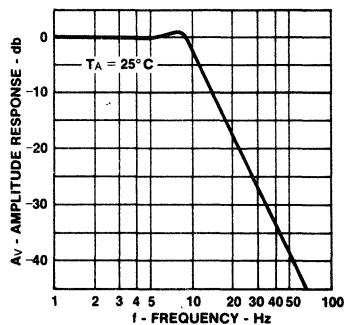
0306-14

AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



0306-15

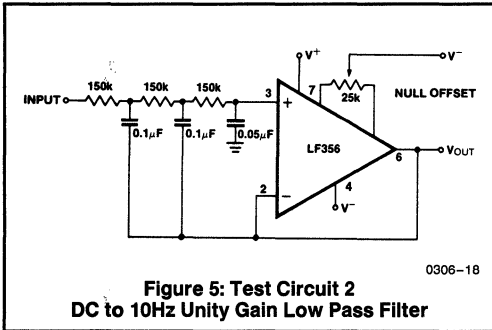
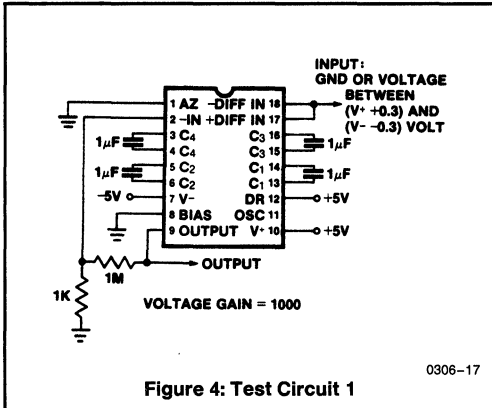
FREQUENCY RESPONSE OF THE 10Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).



0306-16

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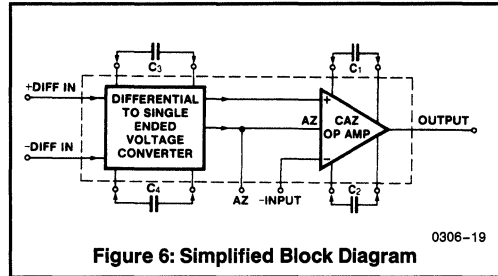


DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op-amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation of internal error voltages, whether they are derived from steady-state conditions, such as temperature and supply voltage fluctuations, or are due to long term drift.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 6.



The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20Hz maximum). However in many applications bandwidth is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ op-amp section of the ICL7605/ICL7606 is best illustrated by referring to Figure 7. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

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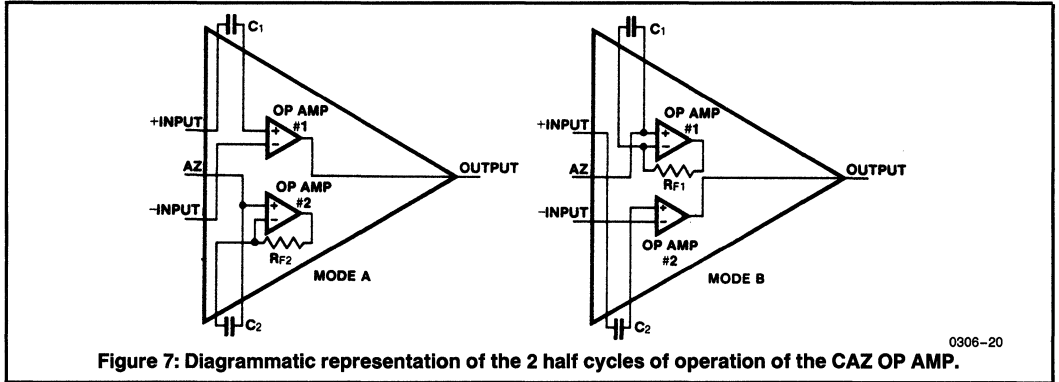


Figure 7: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

0306-20

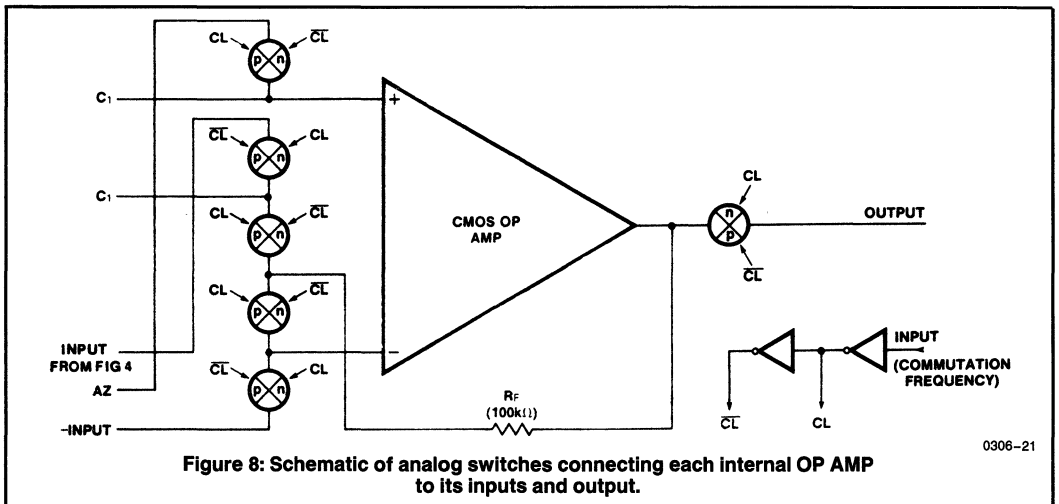


Figure 8: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

0306-21

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

- * Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
- * Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
- * Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
- * Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge

injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. The CMOS structure provides the CAZ op-amp with open-loop gains of greater than 100dB, typical input offset voltages of $\pm 5mV$, and ultra-low leakage currents, typically 1pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 8. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

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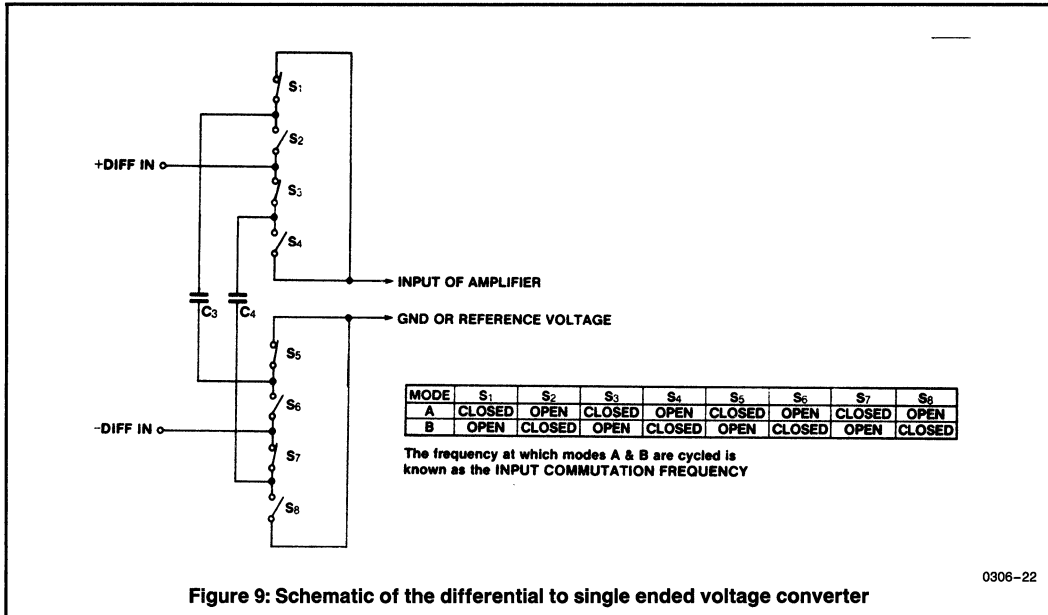


Figure 9: Schematic of the differential to single ended voltage converter

0306-22

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of the voltage converter block is shown in Figure 9. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 10, where the voltage steps equal the differential voltage ($V_A - V_B$) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, including commutation and noise voltages. Sampling theory states that to preserve the information to be processed, at least two samples must be taken within a period ($1/f$) of the highest frequency being sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is translated to a lower frequency. This phenomenon is known as aliasing. Although the output responds to inputs above the commutation frequency, the frequencies of the output responses will be below the commutation frequency.

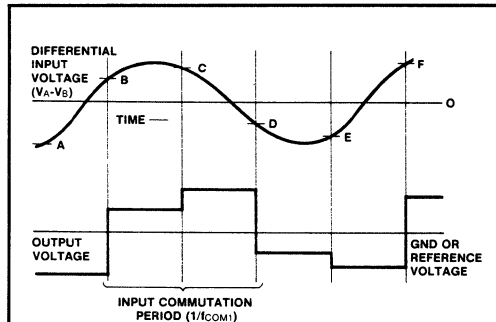


Figure 10: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

0306-23

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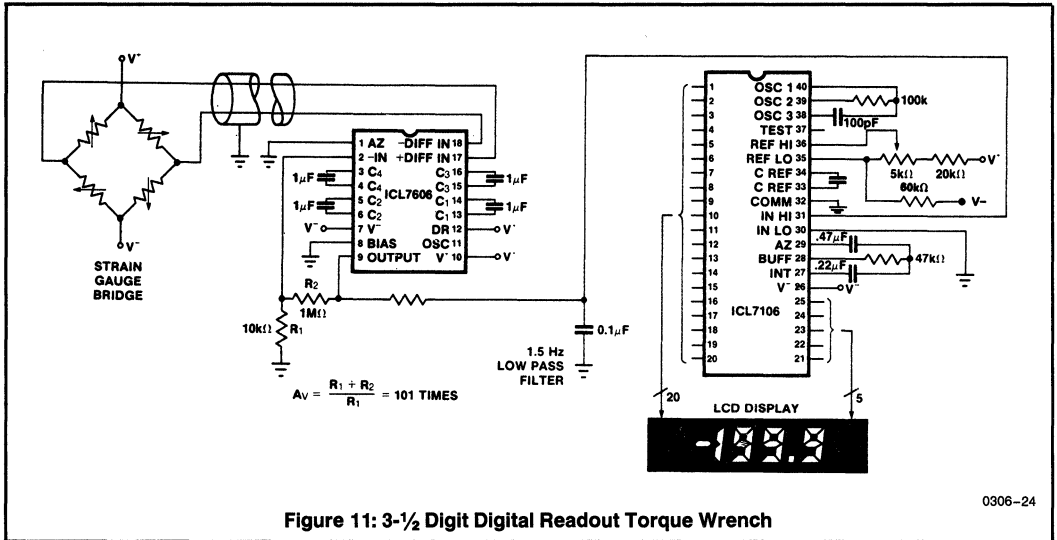


Figure 11: 3-1/2 Digit Digital Readout Torque Wrench

0306-24

The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have a finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C₃ and C₄ must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is down approximately 3dB at 10Hz.

APPLICATIONS

Using the ICL7605/ICL7606 to Build a Digital Readout Torque Wrench

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting it to a single-ended voltage referenced to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter which drives the LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of

the A/D. In order to set the full-scale reading, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp must be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale, the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2mA. The accuracy is limited only by resistor ratios and the transducer.

SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Figure 4 and 5 (Test Circuits) provide a convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be a high-input impedance RC type — not simply a capacitor across the feedback resistor R₂. Resistor and capacitor values of about 100kΩ and 1.0μF are necessary so that the output load impedance on the CAZ op-amp is greater than 100kΩ.

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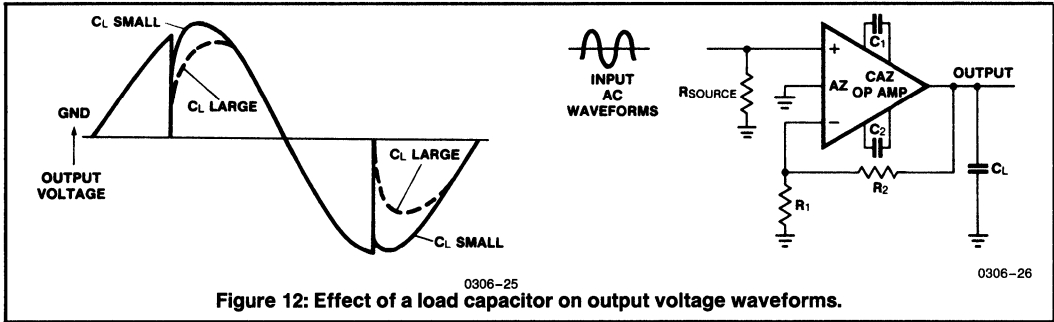


Figure 12: Effect of a load capacitor on output voltage waveforms.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606. For this reason, the internal op amps have externally programmable bias levels. These levels are set by connecting the BIAS terminal to either V+, GND, or V-, for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of quiescent supply current versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output load of 100kΩ or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked. This is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteris-

tic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 12. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1MΩ resistor and a 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 13) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V+ supply is +5V (±10%) and the logic driver also operates from a similar voltage supply. The reason for this requirement is that the logic section (including the oscillator) operates from an internal -5V supply, referenced to V+ supply, which is not accessible externally.

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NOTE: All typical values have been characterized but are not tested.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about $0.1\mu\text{V}/^\circ\text{C}$. However, these voltages can be several tens of microvolts per $^\circ\text{C}$ for certain thermocouple materials.

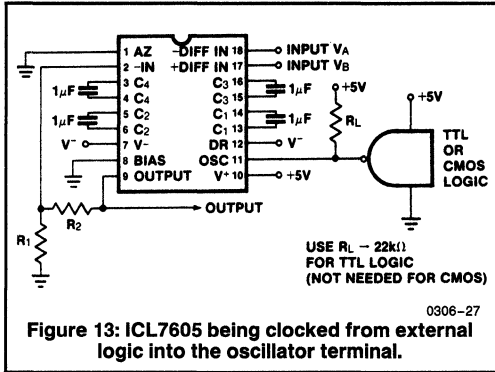


Figure 13: ICL7605 being clocked from external logic into the oscillator terminal.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep the ICL7605/ICL7606 away from equipment which dissipates heat.

Component Selection

The four capacitors (C_1 thru C_4) should each be about $1.0\mu\text{F}$. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene types are the best for C_3 and C_4 , although Mylar may be adequate for C_1 and C_2 .

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at $1.0\mu\text{F}$ and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op-amps are typically in the 10pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least $10,000 \times 10\text{pF}$, or $0.1\mu\text{F}$ each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0pA at an ambient temperature of 25°C .

The output waveform in Figure 4 (with no input signal) is shown in Figure 14. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7mV are amplified by a factor of less than 1000.

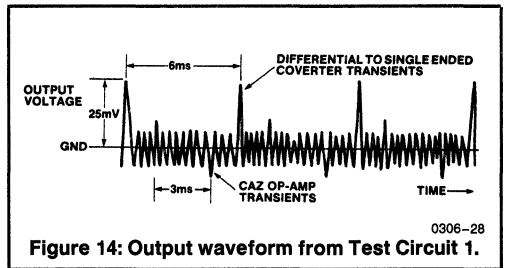


Figure 14: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board particularly the capacitors C_1 , C_2 , C_3 and C_4 , which must all be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

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NOTE: All typical values have been characterized but are not tested.

ICL76XX

ICL76XX Series Low Power CMOS Operational Amplifiers



ICL76XX

GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from $\pm 1V$ to $\pm 8V$, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100 μA , or 10 μA , with no external components. This results in power consumption as low as 20 μW . Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of .01pA/ \sqrt{Hz} , and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

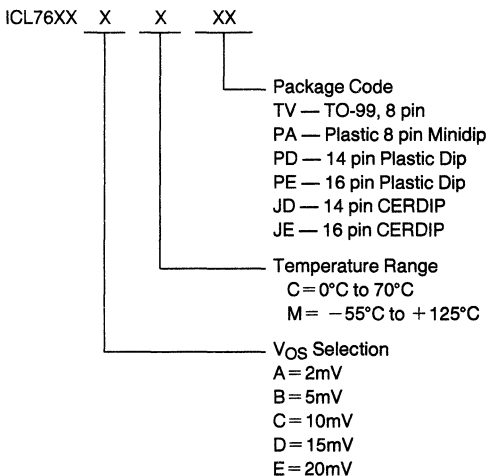
The inputs are internally protected and require no special handling procedures. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/ μs , and unity gain bandwidth of 1MHz at $I_Q = 1mA$.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

SELECTION GUIDE

DEVICE NOMENCLATURE



FEATURES

- Wide Operating Voltage Range $\pm 1V$ to $\pm 8V$
- High Input Impedance — $10^{12}\Omega$
- Programmable Power Consumption — Low As 20 μW
- Input Current Lower Than BIFETs — Typ 1pA
- Available As Singles, Duals, Triples, and Quads
- Output Voltage Swings to Within Millivolts Of V^- and V^+
- Low Power Replacement for Many Standard Op Amps
- Compensated and Uncompensated Versions
- Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)

APPLICATIONS

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers

SPECIAL FEATURE CODES

- C = INTERNALLY COMPENSATED
- H = HIGH QUIESCENT CURRENT (1mA)
- L = LOW QUIESCENT CURRENT (10 μA)
- M = MEDIUM QUIESCENT CURRENT (100 μA)
- O = OFFSET NULL CAPABILITY
- P = PROGRAMMABLE QUIESCENT CURRENT
- V = EXTENDED CMVR

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NOTE: All typical values have been characterized but are not tested.

ORDERING INFORMATION

Basic Part Number	Number of OP-AMPS in Package, and Special Features (SEE CODES)	Package Type and Suffix						
		8-Lead TO-99		8-Pin MINIDIP	8-Pin SOIC	Plastic DIP (1)	Ceramic DIP (1)	
		0°C to +70°C	-55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	-55°C to +125°C
ICL7611 ICL7612	SINGLE OP-AMP: C, O, P C, O, P, V	ACTV BCTV	AMTV BMTV	ACPA BCPA	DCPA DCBA			
ICL7621	DUAL OP-AMP: C, M	ACTV BCTV DCTV	AMTV BMTV	ACPA BCPA DCPA				
ICL7631	TRIPLE OP-AMP: C, P					ECPE	ECJE	
ICL7641 ICL7642	QUAD OP-AMP: C, H C, L					CCPD ECPD	CCJD ECJD	CMJD

NOTES: 1. Duals and quads are available in 14 pin DIP package, triples in 16 pin only.
2. Ordering code must consist of basic part number and package suffix, e.g., ICL7611BCPA.

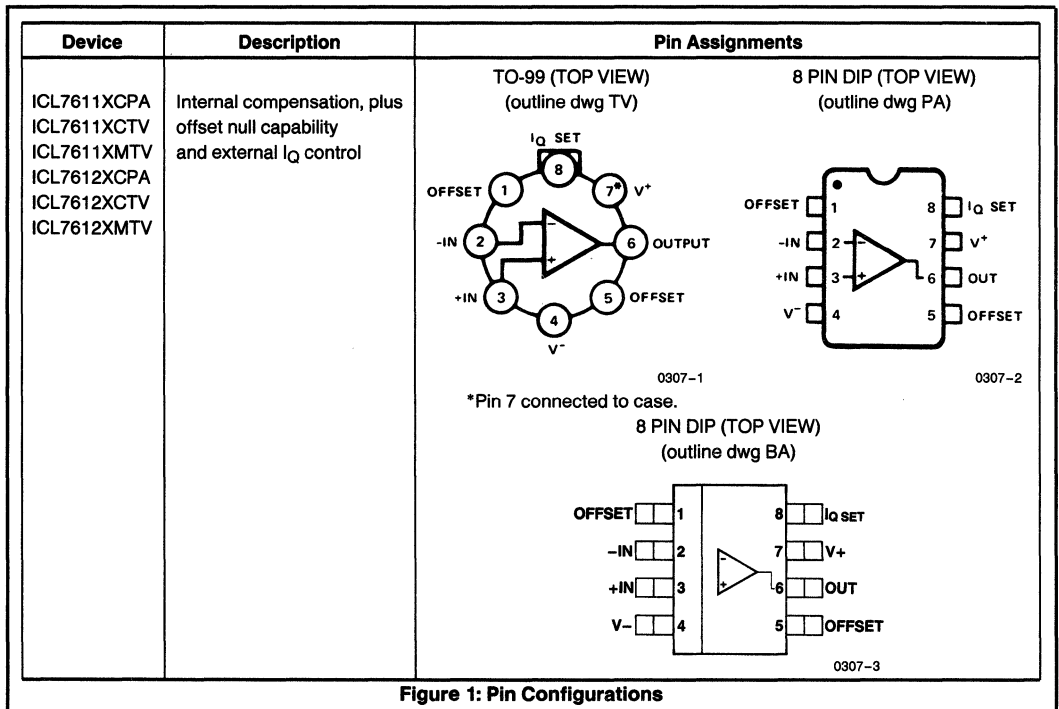


Figure 1: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

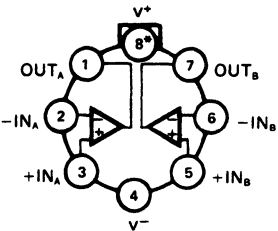
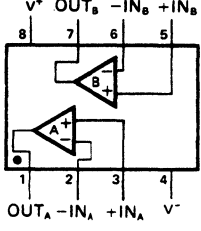
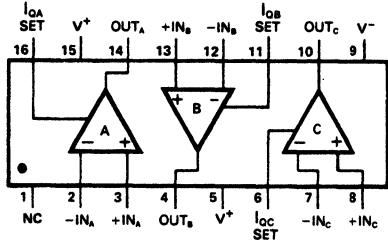
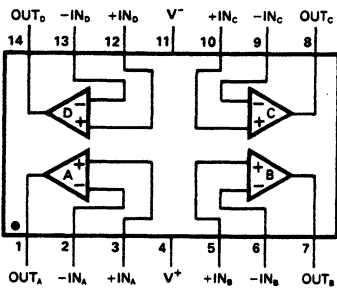
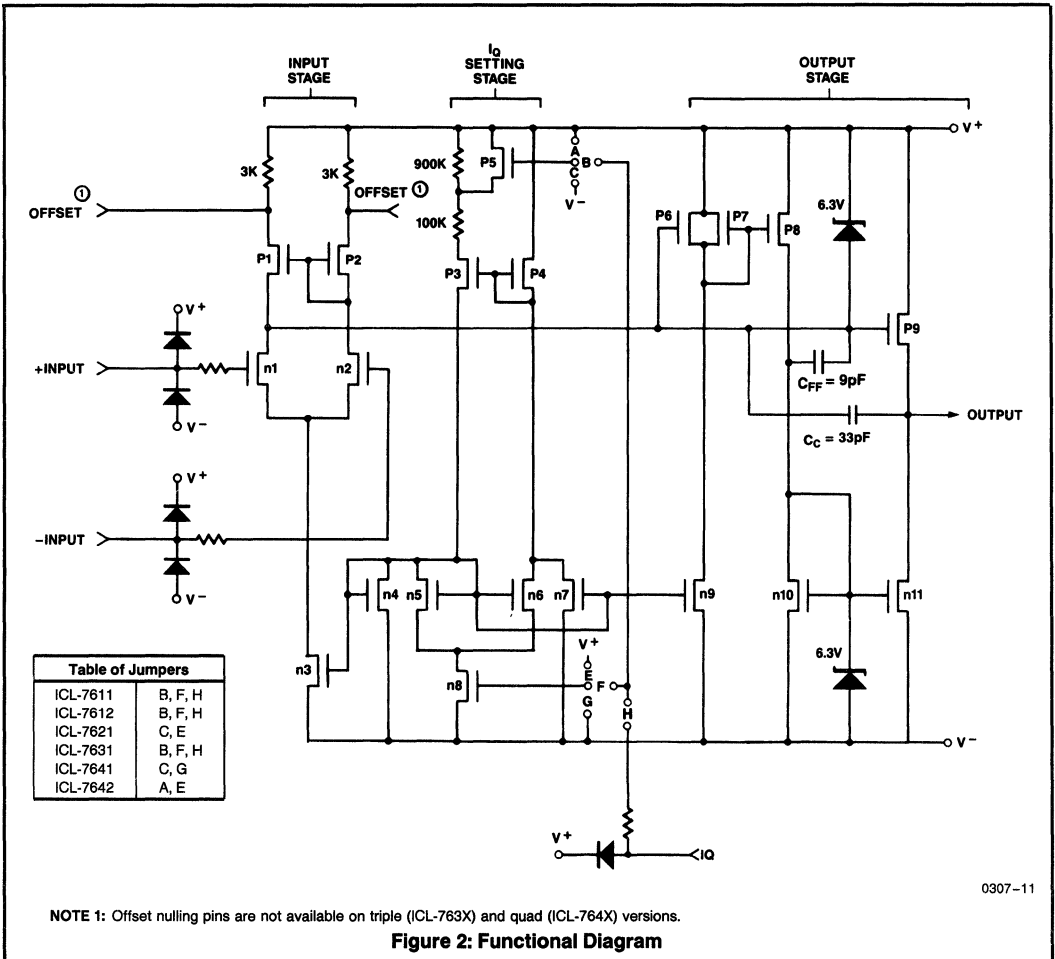
Device	Description	Pin Assignments	
ICL7621XCPA ICL7621XCTV ICL7621XMTV	Dual op amps with internal compensation; I_Q fixed at $100\mu A$ Pin compatible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	<p>TO-99 (TOP VIEW) (outline dwg TV)</p>  <p>0307-6 *Pin 8 connected to case.</p>	<p>* PIN DIP (TOP VIEW) (outline dwg PA)</p>  <p>0307-7</p>
ICL7631XCPE	Triple op amps with internal compensation. Adjustable I_Q Same pin configuration as ICL8023.	<p>16 PIN DIP (TOP VIEW) (outline dwgs JE, PE)</p>  <p>0307-9 Note: pins 5 and 15 are internally connected.</p>	
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at $10\mu A$ (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	<p>14 PIN DIP (TOP VIEW) (outline dwg JD, PD)</p>  <p>0307-10</p>	

Figure 1: Pin Configurations (Cont.)

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NOTE: All typical values have been characterized but are not tested.



0307-11

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage V^+ to V^-	18V
Input Voltage	$V^- - 0.3$ to $V^+ + 0.3$ V
Differential Input Voltage ^[1] . . . ±[($V^+ + 0.3$) - ($V^- - 0.3$)]V	
Duration of Output Short Circuit ^[2]	Unlimited

Continuous Power Dissipation

	@25°C	Above 25°C
		derate as below:
TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C
Storage Temperature Range	-65°C to +150°C	
Operating Temperature Range		
ICL76XXM	-55°C to +125°C	
ICL76XXC	0°C to +70°C	
Lead Temperature (Soldering, 10sec)	300°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.

2. The outputs may be shorted to ground or to either supply. for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS (7611/12 and 7621 ONLY)

($V_{SUPPLY} = \pm 5.0V$, $T_A = 25^\circ C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXA			76XXB			76XXD			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25^\circ C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7			15 20	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		10			15		25			$\mu V/^\circ C$
I_{OS}	Input Offset Current	$T_A = 25^\circ C$ $\Delta T_A = C_{(2)}$ $\Delta T_A = M_{(2)}$		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
I_{BIAS}	Input Bias Current	$T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
V_{CMR}	Common Mode Voltage Range (Except ICL7612)	$I_Q = 10\mu A^{(1)}$ $I_Q = 100\mu A$ $I_Q = 1mA^{(1)}$	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
V_{CMR}	Extended Common Mode Voltage Range (ICL7612 Only)	$I_Q = 10\mu A$ $I_Q = 100\mu A$ $I_Q = 1mA$	±5.3 +5.3 -5.1			±5.3 +5.3 -5.1			±5.3 +5.3 -5.1			V
V_{OUT}	Output Voltage Swing	(1) $I_Q = 10\mu A$, $R_L = 1M\Omega$ $T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$	±4.9 ±4.8 ±4.7			±4.9 ±4.8 ±4.7			±4.9 ±4.8 ±4.7			V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$ $T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$	±4.9 ±4.8 ±4.5			±4.9 ±4.8 ±4.5			±4.9 ±4.8 ±4.5			V
		(1) $I_Q = 1mA$, $R_L = 10k\Omega$ $T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$	±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			V

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7611/12 and 7621 ONLY) (Continued)

 $(V_{SUPPLY} = \pm 5.0V, T_A = 25^\circ C, \text{ unless otherwise specified.})$

Symbol	Parameter	Test Conditions	76XXA			76XXB			76XXD			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 4.0V, R_L = 1M\Omega$ $I_Q = 10\mu A^{(1)}, T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$	86 80 74	104		80 75 68	104		80 75 68	104		dB
		$V_O = \pm 4.0V, R_L = 100k\Omega$ $I_Q = 100\mu A, T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$	86 80 74	102		80 75 68	102		80 75 68	102		
		$V_O = \pm 4.0V, R_L = 10k\Omega$ $I_Q = 1mA^{(1)}, T_A = 25^\circ C$ $\Delta T_A = C$ $\Delta T_A = M$	80 76 72	83		76 72 68	83		76 72 68	83		
GBW	Unity Gain Bandwidth	$I_Q = 10\mu A^{(1)}$ $I_Q = 100\mu A$ $I_Q = 1mA^{(1)}$		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz
R_{IN}	Input Resistance			1012			1012			1012		Ω
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega, I_Q = 10\mu A^{(1)}$	76	96		70	96		70	96		dB
		$R_S \leq 100k\Omega, I_Q = 100\mu A$	76	91		70	91		70	91		
		$R_S \leq 100k\Omega, I_Q = 1mA^{(1)}$	66	87		60	87		60	87		
PSRR	Power Supply Rejection Ratio	$R_S \leq 100k\Omega, I_Q = 10\mu A^{(1)}$	80	94		80	94		80	94		dB
		$R_S \leq 100k\Omega, I_Q = 100\mu A$	80	86		80	86		80	86		
		$R_S \leq 100k\Omega, I_Q = 1mA^{(1)}$	70	77		70	77		70	77		
e_n	Input Referred Noise Voltage	$R_S = 100\Omega, f = 1kHz$		100			100			100		nV/ \sqrt{Hz}
i_n	Input Referred Noise Current	$R_S = 100\Omega, f = 1kHz$		0.01			0.01			0.01		pA/ \sqrt{Hz}
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load $I_Q \text{ SET} = +5V^{(1)}$ $I_Q \text{ SET} = 0V$ $I_Q \text{ SET} = -5V^{(1)}$		0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5	mA
V_{O1}/V_{O2}	Channel Separation	$A_{VOL} = 100$		120			120			120		dB
SR	Slew Rate ⁽³⁾	$A_{VOL} = 1, C_L = 100pF$ $V_{IN} = 8V_{pp}$ $I_Q = 10\mu A^{(1)}, R_L = 1M\Omega$		0.016			0.016			0.016		V/ μs
		$I_Q = 100\mu A, R_L = 100k\Omega$		0.16			0.16			0.16		
		$I_Q = 1mA^{(1)}, R_L = 10k\Omega$		1.6			1.6			1.6		
t_r	Rise Time ⁽³⁾	$V_{IN} = 50mV, C_L = 100pF$ $I_Q = 10\mu A^{(1)}, R_L = 1M\Omega$		20			20			20		μs
		$I_Q = 100\mu A, R_L = 100k\Omega$		2			2			2		
		$I_Q = 1mA^{(1)}, R_L = 10k\Omega$		0.9			0.9			0.9		
	Overshoot Factor ⁽³⁾	$V_{IN} = 50mV, C_L = 100pF$ $I_Q = 10\mu A^1, R_L = 1M\Omega$		5			5			5		%
		$I_Q = 100\mu A, R_L = 100k\Omega$		10			10			10		
		$I_Q = 1mA^1, R_L = 10k\Omega$		40			40			40		

NOTES: 1. ICL7611, 7612 only.

2. C = Commercial Temperature Range: $0^\circ C$ to $+70^\circ C$
M = Military Temperature Range: $-55^\circ C$ to $+125^\circ C$

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7611/12 AND 7621 ONLY)

($V_{SUPPLY} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25^\circ C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXA			76XXB			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25^\circ C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		10			15		$\mu V/^\circ C$
I_{OS}	Input Offset Current	$T_A = 25^\circ C$ $\Delta T_A = C$		0.5	30 300		0.5	30 300	pA
I_{BIAS}	Input Bias Current	$T_A = 25^\circ C$ $\Delta T_A = C$		1.0	50 500		1.0	50 500	pA
V_{CMR}	Common Mode Voltage Range (Except ICL7612)		± 0.6			± 0.6			V
V_{CMR}	Extended Common Mode Voltage Range (ICL7612 Only)		+0.6 to -1.1			+0.6 to -1.1			V
V_{OUT}	Output Voltage Swing	$R_L = 1M\Omega$, $T_A = 25^\circ C$ $\Delta T_A = C$		± 0.98 ± 0.96			± 0.98 ± 0.96		V
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25^\circ C$ $\Delta T_A = C$		90 80			90 80		dB
GBW	Unity Gain Bandwidth			0.044					MHz
R_{IN}	Input Resistance			10^{12}			10^{12}		
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$		80			80		
PSRR	Power Supply Rejection Ratio	$R_S \leq 100k\Omega$		80			80		dB
e_n	Input Referred Noise Voltage	$R_S = 100\Omega$, $f = 1kHz$		100			100		nV/\sqrt{Hz}
i_n	Input Referred Noise Current	$R_S = 100\Omega$, $f = 1kHz$		0.01			0.01		pA/\sqrt{Hz}
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		6	15		6	15	μA
SR	Slew Rate	$A_{VOL} = 1$, $C_L = 100pF$ $V_{IN} = 0.2V_{pp}$ $R_L = 1M\Omega$		0.016			0.016		$V/\mu s$
t_r	Rise Time	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
	Overshoot Factor	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

NOTE: C=Commercial Temperature Range (0°C to +70°C) M=Military Temperature Range (-55°C to +125°C).

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7631, 7641/42 ONLY)

(V_{SUPPLY} = ±5.0V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC (6)			76XXE (6)			Units
			Min	Typ	Max	Min	Typ	Max	
V _{OS}	Input Offset Voltage	R _S ≤ 100kΩ, T _A = 25°C T _{MIN} ≤ T _A ≤ T _{MAX}			10 15			20 25	mV
ΔV _{OS} /ΔT	Temperature Coefficient of V _{OS}	R _S ≤ 100kΩ (Note 5)		20			30		
I _{OS}	Input Offset Current	T _A = 25°C ΔT _A = C ΔT _A = M		0.5	30 300 800		0.5	30 300 800	pA
I _{BIAS}	Input Bias Current	T _A = 25°C ΔT _A = C ΔT _A = M		1.0	50 500 4000		1.0	50 500 4000	pA
V _{CMR}	Common Mode Voltage Range	I _Q = 10μA ⁽¹⁾ I _Q = 100μA ⁽³⁾ I _Q = 1mA ⁽²⁾	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
V _{OUT}	Output Voltage Swing	(1) I _Q = 10μA, R _L = 1MΩ T _A = 25°C ΔT _A = C ΔT _A = M	±4.9 ±4.8 ±4.7			±4.9 ±4.8 ±4.7			V
		I _Q = 100μA, R _L = 100kΩ (3) T _A = 25°C ΔT _A = C ΔT _A = M	±4.9 ±4.8 ±4.5			±4.9 ±4.8 ±4.5			
		(2) I _Q = 1mA, R _L = 10kΩ T _A = 25°C ΔT _A = C ΔT _A = M	±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			
A _{VOL}	Large Signal Voltage Gain	V _O = ±4.0V, R _L = 1MΩ ⁽¹⁾ I _Q = 10μA ⁽¹⁾ , T _A = 25°C ΔT _A = C ΔT _A = M	80 75 68	104		80 75 68	104		dB
		V _O = ±4.0V, R _L = 100kΩ ⁽³⁾ I _Q = 100μA, T _A = 25°C ΔT _A = C ΔT _A = M	80 75 68	102		80 75 68	102		
		V _O = ±4.0V, R _L = 10kΩ ⁽²⁾ I _Q = 1mA ⁽¹⁾ , T _A = 25°C ΔT _A = C ΔT _A = M	80 75 68	98		80 75 68	98		
GBW	Unity Gain Bandwidth	I _Q = 10μA ⁽¹⁾ I _Q = 100μA ⁽³⁾ I _Q = 1mA ⁽²⁾		0.044 0.48 1.4			0.044 0.48 1.4		MHz
R _{IN}	Input Resistance			10 ¹²			10 ¹²		Ω
CMRR	Common Mode Rejection Ratio	R _S ≤ 100kΩ, I _Q = 10μA ⁽¹⁾	70	96		70	96		dB
		R _S ≤ 100kΩ, I _Q = 100μA	70	91		70	91		
		R _S ≤ 100kΩ, I _Q = 1mA ⁽²⁾	60	87		60	87		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7631, 7641/42 ONLY) (Continued)

(V_{SUPPLY} = ± 5.0V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC (6)			76XXE (6)			Units
			Min	Typ	Max	Min	Typ	Max	
PSRR	Power Supply Rejection Ratio	R _S ≤ 100kΩ, I _Q = 10μA ⁽¹⁾	80	94		80	94		dB
		R _S ≤ 100kΩ, I _Q = 100μA	80	86		80	86		
		R _S ≤ 100kΩ, I _Q = 1mA ⁽²⁾	70	77		70	77		
e _n	Input Referred Noise Voltage	R _S = 100Ω, f = 1kHz		100			100		nV/√Hz
I _n	Input Referred Noise Current	R _S = 100Ω, f = 1kHz		0.01			0.01		pA/√Hz
I _{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load 7642 ONLY		0.01	0.03		0.01	0.03	mA
		I _Q = 10μA ⁽¹⁾		0.01	0.022		0.01	0.022	
		I _Q = 100μA		0.1	0.25		0.1	0.25	
		I _Q = 1mA ⁽²⁾		1.0	2.5		1.0	2.5	
V _{O1} /V _{O2}	Channel Separation	A _{VOL} = 100		120			120		dB
SR	Slew Rate	A _{VOL} = 1, C _L = 100pF							V/μs
		V _{IN} = 8Vp-p							
		I _Q = 10μA ⁽¹⁾ , R _L = 1MΩ		0.016			0.016		
		I _Q = 100μA, R _L = 100kΩ		0.16			0.16		
		I _Q = 1mA ⁽¹⁾ , R _L = 10kΩ ⁽²⁾		1.6			1.6		
t _r	Rise Time	V _{IN} = 50mV, C _L = 100pF							μs
		I _Q = 10μA ⁽¹⁾ , R _L = 1MΩ		20			20		
		I _Q = 100μA, R _L = 100kΩ		2			2		
		I _Q = 1mA ⁽²⁾ , R _L = 10kΩ		0.9			0.9		
	Overshoot Factor	V _{IN} = 50mV, C _L = 100pF							%
		I _Q = 10μA ⁽¹⁾ , R _L = 1MΩ		5			5		
		I _Q = 100μA, R _L = 100kΩ		10			10		
		I _Q = 1mA ⁽²⁾ , R _L = 10kΩ		40			40		

- NOTES: 1. Does not apply to 7641.
- 2. Does not apply to 7642.
- 3. ICL7631 only.

For Test Conditions:
 C = Commercial Temperature Range: 0°C to +70°C
 M = Military Temperature Range: -55°C to +125°C

ELECTRICAL CHARACTERISTICS (7631 AND 7642 ONLY)

(V_{SUPPLY} = ± 1.0V, I_Q = 10μA, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC			Units
			Min	Typ	Max	
V _{OS}	Input Offset Voltage	R _S ≤ 100kΩ, T _A = 25°C T _{MIN} ≤ T _A ≤ T _{MAX}			10 12	mV
ΔV _{OS} /ΔT	Temperature Coefficient of V _{OS}	R _S ≤ 100kΩ		20		μV/°C
I _{OS}	Input Offset Current	T _A = 25°C ΔT _A = C		0.5	30 300	pA
I _{BIAS}	Input Bias Current	T _A = 25°C ΔT _A = C		1.0	50 500	pA
V _{CMR}	Common Mode Voltage Range		± 0.6			V

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7631 AND 7642 ONLY) (Continued)

(V_{SUPPLY} = ±1.0V, I_Q = 10μA, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC			Units
			Min	Typ	Max	
V _{OUT}	Output Voltage Swing	R _L = 1MΩ, T _A = 25°C ΔT _A = C		±0.98 ±0.96		V
A _{VOL}	Large Signal Voltage Gain	V _O = ±0.1V, R _L = 1MΩ T _A = 25°C ΔT _A = C		90 80		dB
GBW	Unity Gain Bandwidth			0.044		MHz
R _{IN}	Input Resistance			1012		Ω
CMRR	Common Mode Rejection Ratio	R _S ≤ 100kΩ		80		dB
PSRR	Power Supply Rejection Ratio			80		dB
e _n	Input Referred Noise Voltage	R _S = 100Ω, f = 1kHz		100		nV/√Hz
i _n	Input Referred Noise Current	R _S = 100Ω, f = 1kHz		0.01		pA/√Hz
I _{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		6	15	μA
V _{O1} /V _{O2}	Channel Separation	A _{VOL} = 100		120		dB
SR	Slew Rate	A _{VOL} = 1, C _L = 100pF V _{IN} = 0.2Vp-p R _L = 1MΩ		0.016		V/μs
t _r	Rise Time	V _{IN} = 50mV, C _L = 100pF R _L = 1MΩ		20		μs
	Overshoot Factor	V _{IN} = 50mV, C _L = 100pF R _L = 1MΩ		5		%

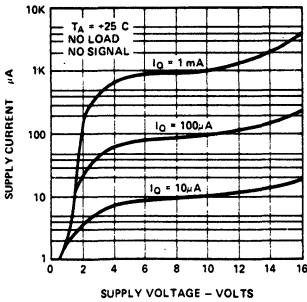
NOTE: C = Commercial Temperature Range (0°C to +70°C)

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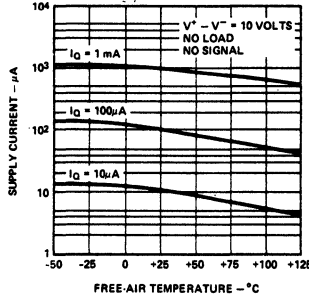
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE



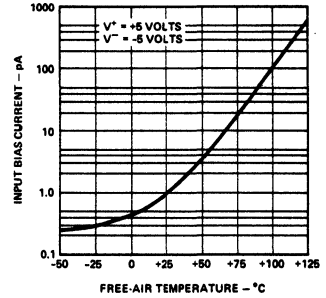
0307-12

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE



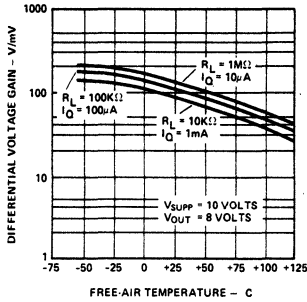
0307-13

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



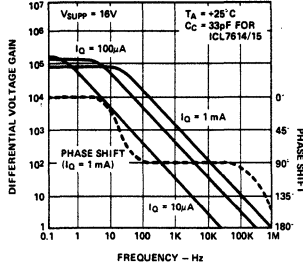
0307-14

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE



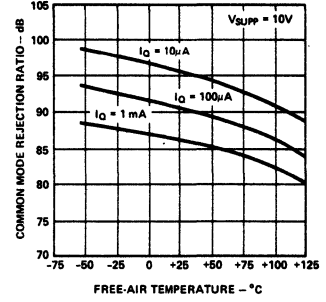
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LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY



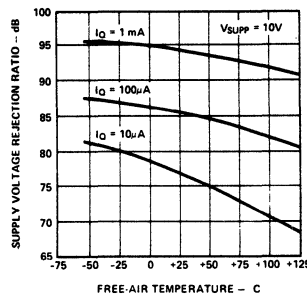
0307-16

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



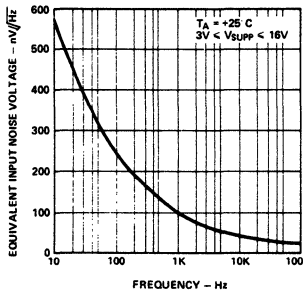
0307-17

POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



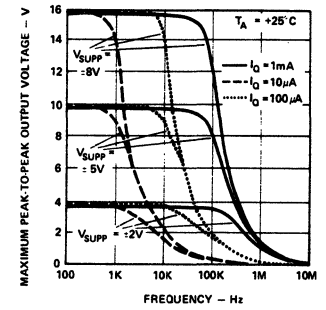
0307-18

EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



0307-19

PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



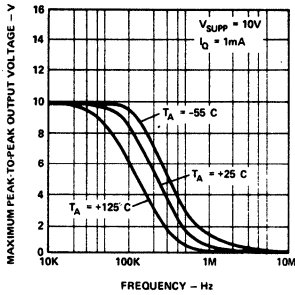
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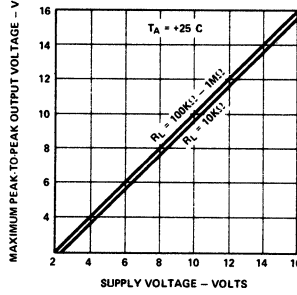
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



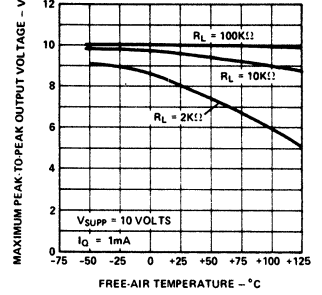
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MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



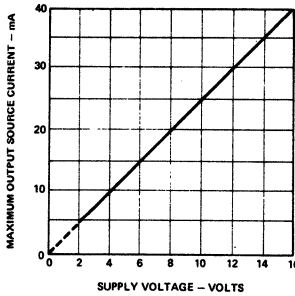
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MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



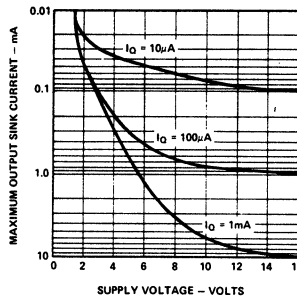
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MAXIMUM OUTPUT SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



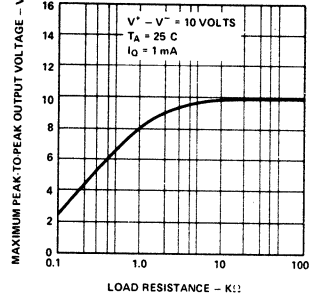
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MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



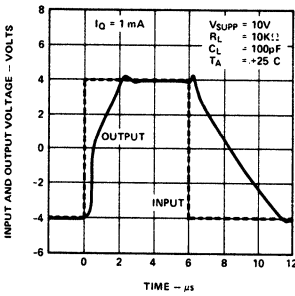
0307-25

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



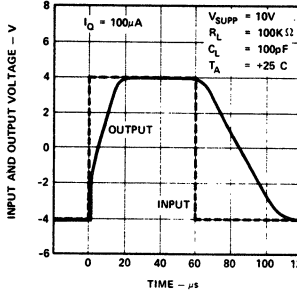
0307-26

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



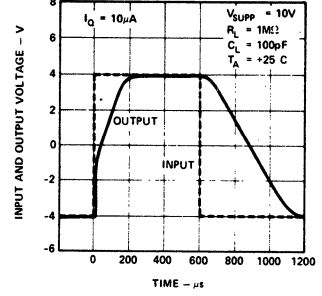
0307-27

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



0307-28

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



0307-29

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10 μ A, 100 μ A or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 and ICL7631 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The 7621 and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

$I_Q = 10\mu\text{A}$ — I_Q pin to V^+

$I_Q = 100\mu\text{A}$ — I_Q pin to ground. If this is not possible, any voltage from $V^+ - 0.8$ to $V^- + 0.8$ can be used.

$I_Q = 1\text{mA}$ — I_Q pin to V^-

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1M Ω , 100k Ω , and 10k Ω , using the output stage

in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10k Ω , 100k Ω , and 1M Ω are used.

Input Offset Nulling

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+ . At quiescent currents of 1mA and 100 μ A, the nulling range provided is adequate for all V_{OS} selections; however with $I_Q = 10\mu\text{A}$, nulling may not be possible with higher values of V_{OS} .

Frequency Compensation

The ICL76XX are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF

Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$, the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for $V_{SUPP} = \pm 1.0V$, the input CMVR would be +0.6 volts to -1.1 volts).

OPERATION AT $V_{SUPP} = \pm 1.0$ VOLTS

Operation at $V_{SUPP} = \pm 1.0V$ is guaranteed at $I_Q = 10\mu\text{A}$ only. This applies to those devices with selectable I_Q , and devices that are set internally to $I_Q = 10\mu\text{A}$ (i.e., ICL7611, 7612, 7631, 7642).

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is $\pm 0.6V$ minimum and typically +0.9V to -0.7V at $V_{SUPP} = \pm 1.0V$. For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

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The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

APPLICATIONS

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

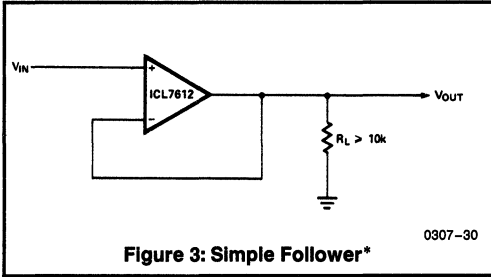
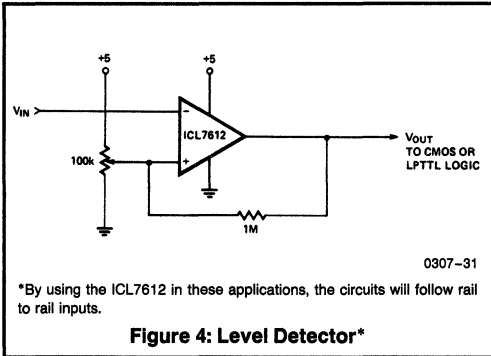
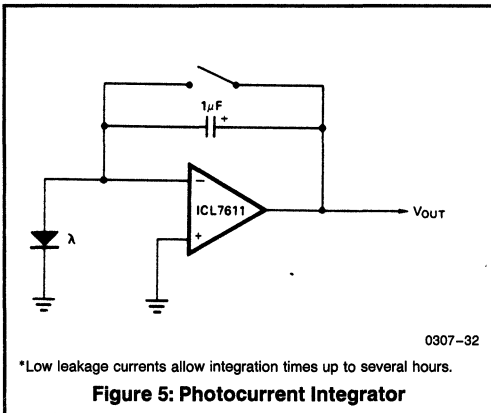


Figure 3: Simple Follower*



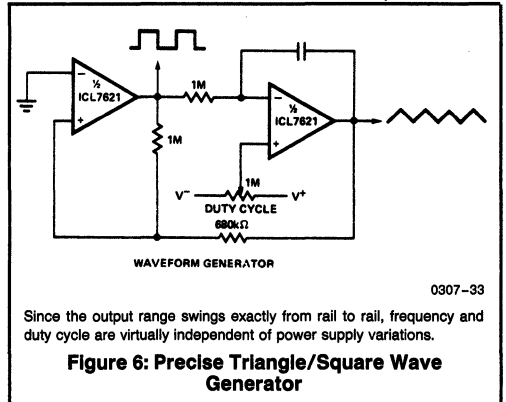
*By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

Figure 4: Level Detector*



*Low leakage currents allow integration times up to several hours.

Figure 5: Photocurrent Integrator



Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

Figure 6: Precise Triangle/Square Wave Generator

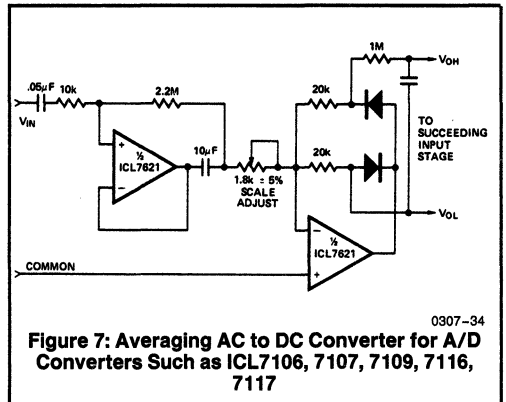
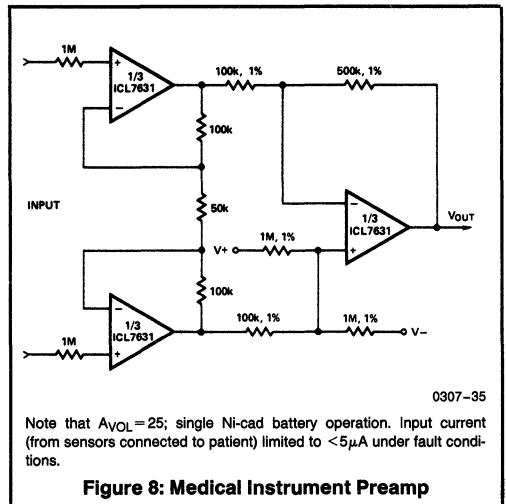


Figure 7: Averaging AC to DC Converter for A/D Converters Such as ICL7106, 7107, 7109, 7116, 7117

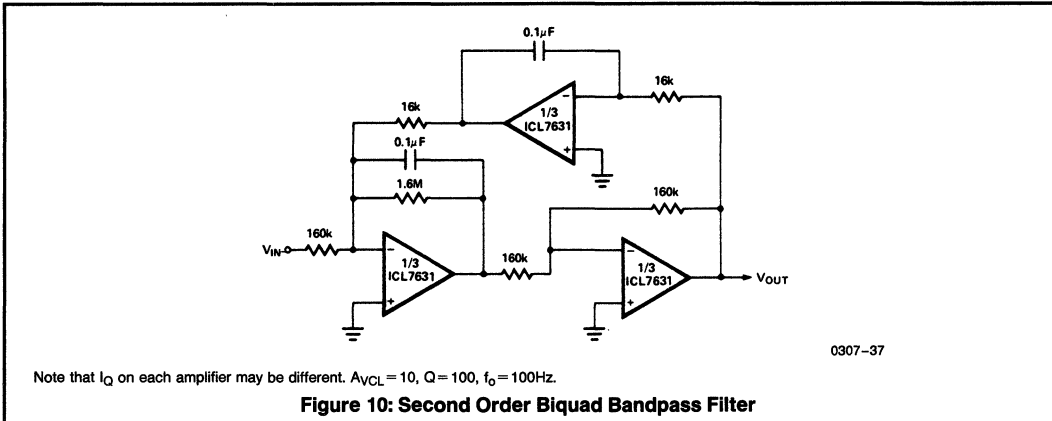
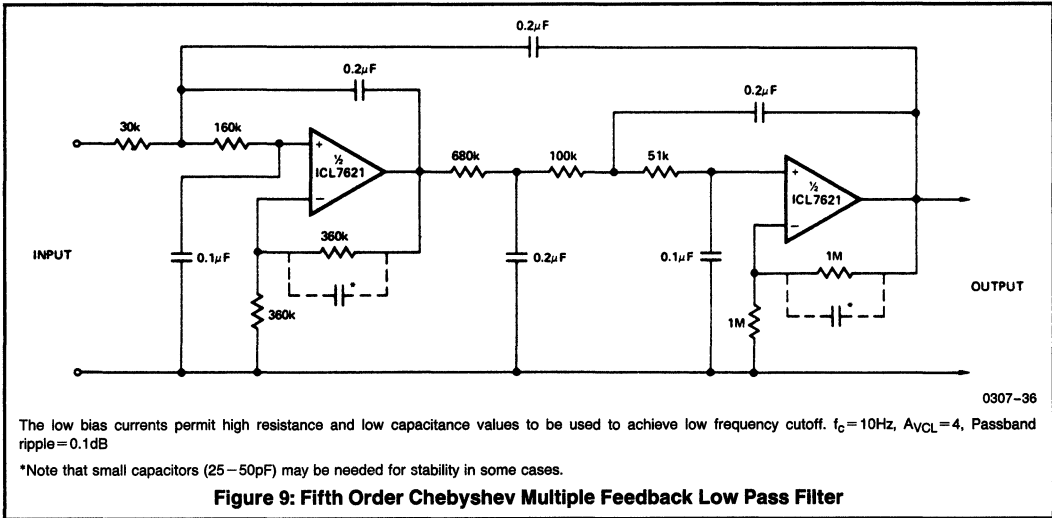


Note that $A_{VOL} = 25$; single Ni-cad battery operation. Input current (from sensors connected to patient) limited to $< 5\mu A$ under fault conditions.

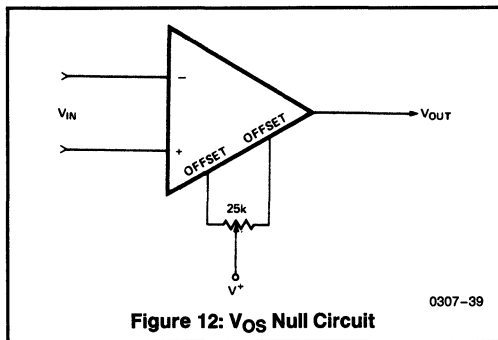
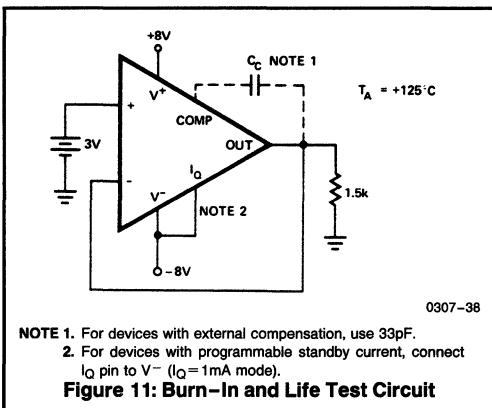
Figure 8: Medical Instrument Preamp

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

ICL7650

Chopper-Stabilized Operational Amplifier



GENERAL DESCRIPTION

The ICL7650 chopper-stabilized amplifier is a high-performance device which offers exceptionally low offset voltage and input-bias parameters, combined with excellent bandwidth and speed characteristics. Intersil's unique CMOS approach to chopper-stabilized amplifier design yields a versatile precision component that can replace more expensive hybrid or monolithic devices.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650 is internally compensated for unity-gain operation.

An enhanced direct replacement for this part called ICL7650S will become available shortly and will be more appropriate for new designs.

FEATURES

- **Extremely Low Input Offset Voltage** — $2\mu V$
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- **Low DC Input Bias Current** — 10pA (20pA 7650B)
- **Extremely High Gain, CMRR and PSRR** — Min 120dB
- **High Slew Rate** — $2.5V/\mu s$
- **Wide Bandwidth** — 2MHz
- **Unity-Gain Compensated**
- **Very Low Intermodulation Effects (Open Loop Phase Shift $< 10^\circ C$ @ Chopper Frequency)**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**

ORDERING INFORMATION

Part	Temperature Range	Package
ICL7650CPA-1	0°C to +70°C	8-PIN Plastic
ICL7650BCPA-1	0°C to +70°C	8-PIN Plastic
ICL7650CPD	0°C to +70°C	14-PIN Plastic
ICL7650BCPD	0°C to +70°C	14-PIN Plastic
ICL7650CTV-1	0°C to +70°C	8-PIN TO-99
ICL7650BCTV-1	0°C to +70°C	8-PIN TO-99
ICL7650IJA-1	-25°C to +85°C	8-PIN CERDIP
ICL7650BIJA-1	-25°C to +85°C	8-PIN CERDIP
ICL7650IJD	-25°C to +85°C	14-PIN CERDIP
ICL7650BIJD	-25°C to +85°C	14-PIN CERDIP
ICL7650ITV-1	-25°C to +85°C	8-PIN TO-99
ICL7650BITV-1	-25°C to +85°C	8-PIN TO-99
ICL7650MJD	-55°C to +125°C	14-PIN CERDIP
ICL7650BMJD	-55°C to +125°C	14-PIN CERDIP
ICL7650MTV-1	-55°C to +125°C	8-PIN TO-99
ICL7650BMTV-1	-55°C to +125°C	8-PIN TO-99

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NOTE: All typical values have been characterized but are not tested.

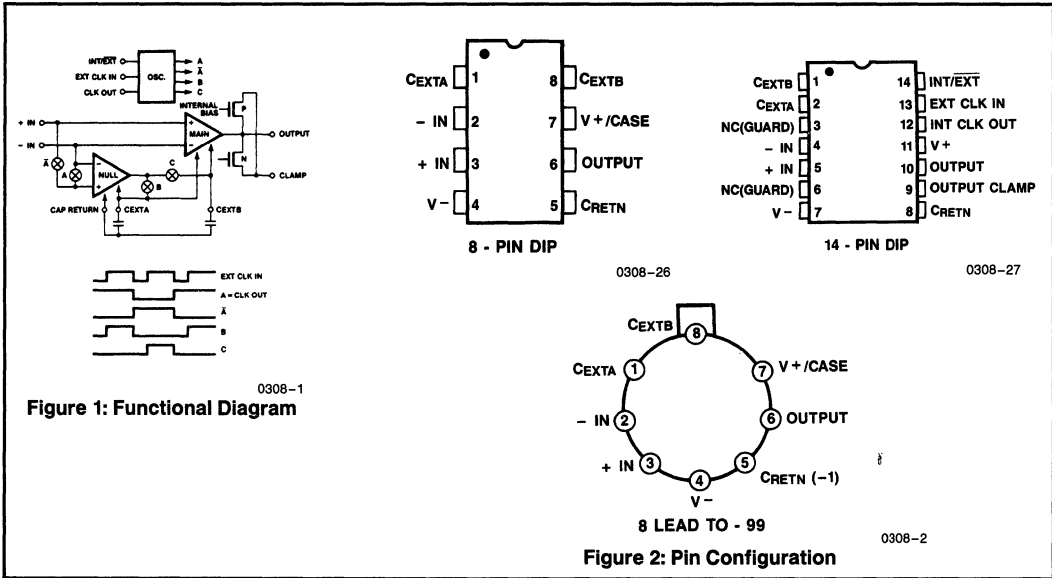
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18 Volts
 Input Voltage ($V^+ + 0.3$) to ($V^- - 0.3$) Volts
 Voltage on oscillator control pins V^+ to V^-
 except EXT CLOCK IN: ($V^+ + 0.3$) to ($V^+ - 6.0$) Volts
 Duration of Output short circuit Indefinite
 Current into any pin 10mA
 — while operating (Note 4) 100 μ A

Cont. Total Power Dissipn ($T_A = 25^\circ\text{C}$)

CERDIP Package 500mW
 Plastic Package 375mW
 TO-99 250mW
 Storage Temp. Range -65°C to 150°C
 Operating Temp. Range See Note 1
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25^\circ C$, (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits 7650			Limits 7650B			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$T_A = +25^\circ C$ $-25^\circ C < T_A < +85^\circ C$ $-55^\circ C < T_A < +125^\circ C$		± 2 ± 5	± 5		± 2 ± 5	± 10.0 ± 75	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temp. Coefficient of Input Offset Voltage	$-25^\circ C < T_A < +85^\circ C$		0.1			0.1		$\mu V/^\circ C$
$\frac{\Delta V_{OS}}{\Delta t}$	Change in Input Offset Voltage With Time			100			100		nV/month
I_{BIAS}	Input Bias Current (doubles every $10^\circ C$) Polarity is + or - (Note 6)	$T_A = +25^\circ C$ $0^\circ C < T_A < +70^\circ C$ $-25^\circ C < T_A < +85^\circ C$		± 1.5 ± 35 ± 100	± 10		± 1.5 ± 35 ± 100	± 20	pA
I_{OS}	Input Offset Current (Note 5)	$T_A = 25^\circ C$		5.0			5.0		pA
R_{IN}	Input Resistance			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k\Omega$	1×10^6	5×10^6		1×10^6	5×10^6		V/V
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10k\Omega$ $R_L = 100k\Omega$	± 4.7	± 4.85 ± 4.95		± 4.7	± 4.85 ± 4.95		V
CMVR	Common Mode Voltage Range		-5.0	-5.2 to +2.0	1.5 +2.0	-5.0	-5.2 to 1.5		V
CMRR	Common Mode Rejection Ratio	CMVR = -5V to +1.5	110	120		110	120		dB
PSRR	Power Supply Rejection Ratio	$\pm 3V$ to $\pm 8V$	120	130		120	130		dB
e_n	Input Noise Voltage	$R_S = 100\Omega$ $f = 0$ to $10Hz$		2			2		μV_{p-p}
i_n	Input Noise Current	$f = 10Hz$		0.01			0.01		pA/\sqrt{Hz}
GBW	Unity Gain Bandwidth			2.0			2.0		MHz
SR	Slew Rate	$C_L = 50pF$, $R_L = 10k\Omega$		2.5			2.5		V/ μs
t_r	Rise Time			0.2			0.2		μs
	Overshoot			20			20		%
V^+ to V^-	Operating Supply Range		4.5		16	4.5		16	V
I_{SUPP}	Supply Current	no load		2.0	3.5		2.0	3.5	mA
f_{ch}	Internal Chopping Frequency	pins 12-14 open (DIP)	120	200	375	120	200	375	Hz
	Clamp ON Current (note 2)	$R_L = 100k\Omega$	25	70	150	25	70	150	μA
	Clamp OFF Current (note 2)	$-4.0V < V_{OUT} < +4.0V$		1			1		pA

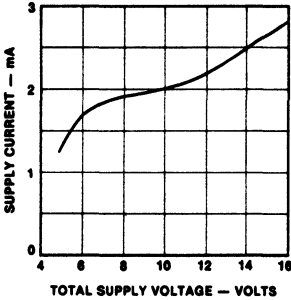
- NOTES: 1. Operating temperature range for M series parts is $-55^\circ C$ to $+125^\circ C$, for I series is $-25^\circ C$ to $+85^\circ C$, for C series is $0^\circ C$ to $+70^\circ C$
2. See OUTPUT CLAMP under detailed description.
3. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
4. Limiting input current to $100\mu A$ is recommended to avoid latchup problems. Typically $1mA$ is safe, however this is not guaranteed.
5. $I_{OS} = 2 \cdot I_{BIAS}$
6. I_{BIAS} tested with clock disabled.

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NOTE: All typical values have been characterized but are not tested.

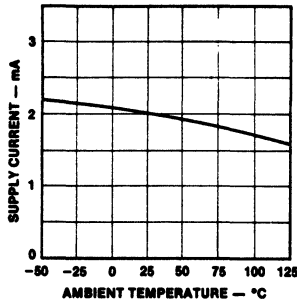
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT vs. SUPPLY VOLTAGE



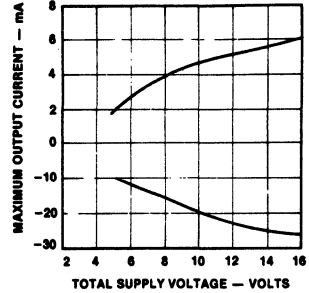
0308-3

SUPPLY CURRENT vs. AMBIENT TEMPERATURE



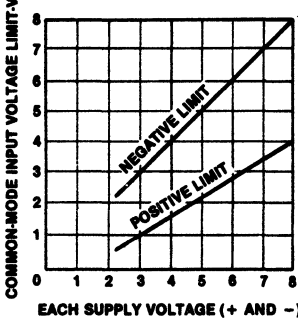
0308-4

MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



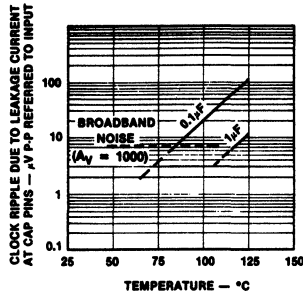
0308-5

COMMON-MODE INPUT-VOLTAGE RANGE vs SUPPLY VOLTAGE



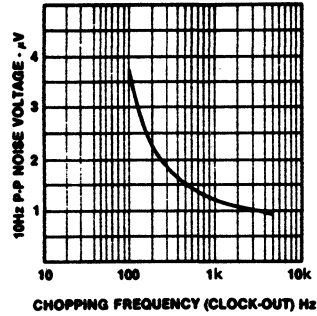
0308-6

CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



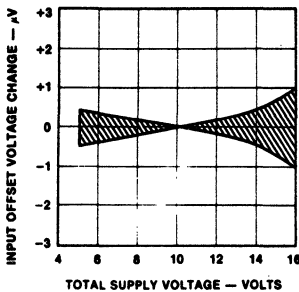
0308-7

10Hz P-P NOISE VOLTAGE vs. CHOPPING FREQUENCY



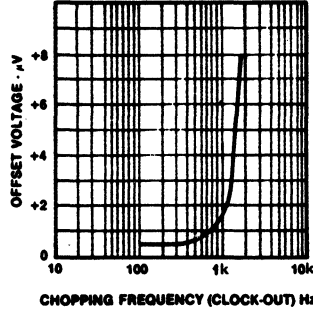
0308-8

INPUT OFFSET VOLTAGE CHANGE vs. SUPPLY VOLTAGE



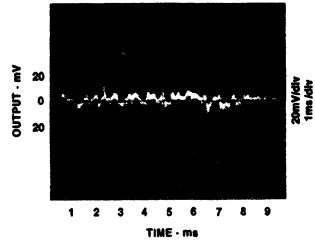
0308-9

INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



0308-10

OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10KΩ



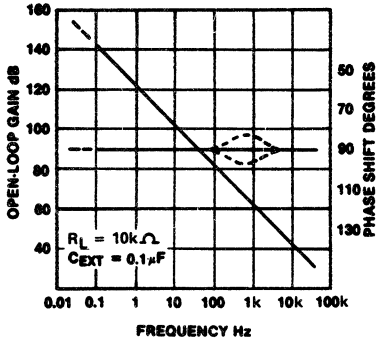
0308-11

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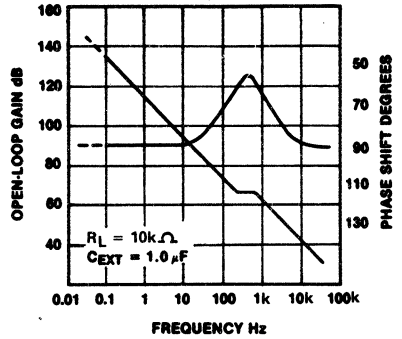
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



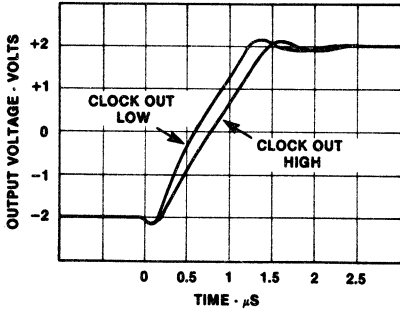
0308-12

OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



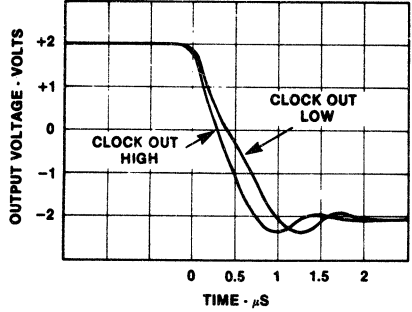
0308-13

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE*



0308-14

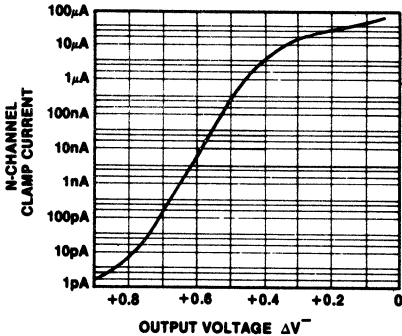
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE*



0308-15

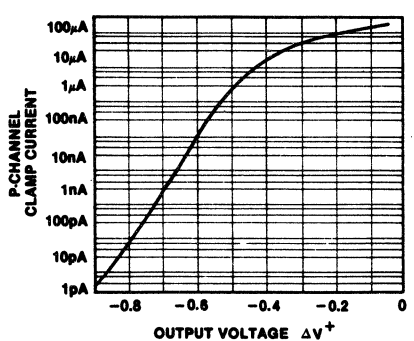
* THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-CHANNEL CLAMP CURRENT vs. OUTPUT VOLTAGE



0308-16

P-CHANNEL CLAMP CURRENT vs. OUTPUT VOLTAGE



0308-17

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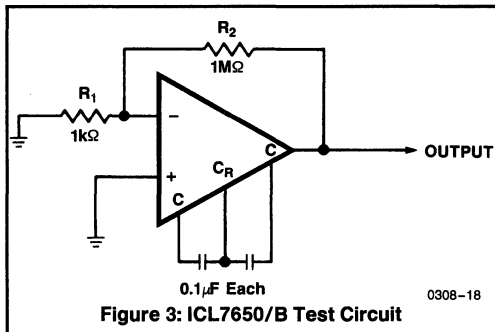


Figure 3: ICL7650/B Test Circuit

DETAILED DESCRIPTION

Amplifier

The functional diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL} .

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null/storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} .

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled differential input voltages are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650 has an internal oscillator giving a chopping frequency of 200Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies, the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50-80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V^+ and GROUND for power supplies up to $\pm 6V$, and between V^+ and $V^+ - 6V$ for higher supply voltages. Note that a signal of about 400Hz will be present at the EXT CLK IN pin with INT/EXT high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than $10\mu V/sec$, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

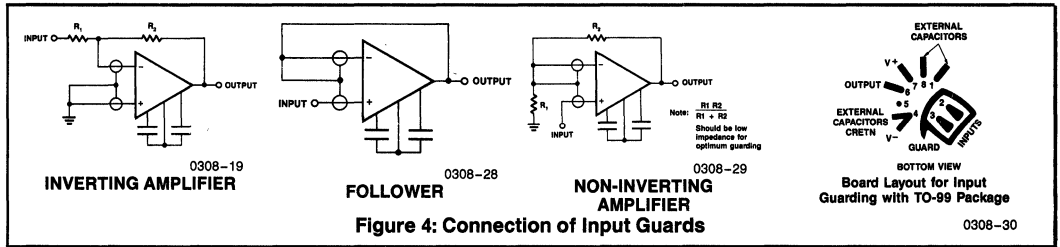
The two required capacitors, C_{EXTA} and C_{EXTB} , have optimum values depending on the clock or chopping frequency. For the present internal clock, the correct value is $0.1\mu F$, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to $1\mu V$.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

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NOTE: All typical values have been characterized but are not tested.



Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18k Ω), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1k Ω load than with a 10k Ω load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1k Ω load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10k Ω or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μ V/°C, but up to tens of μ V/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V⁺, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μ A748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650.

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NOTE: All typical values have been characterized but are not tested.

TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op. amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650 are the supply voltage ($\pm 8V$ max.) and the output drive capability (10k Ω load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

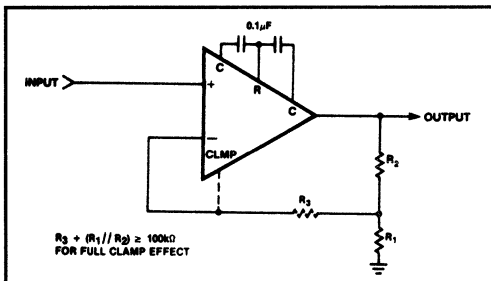


Figure 5: Non Inverting Amplifier With (Optional Clamp)

NOTE: R₁ R₂ INDICATES THE PARALLEL COMBINATION OF R₁ AND R₂

0308-20

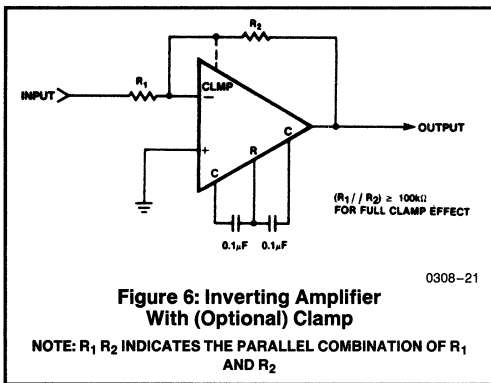


Figure 6: Inverting Amplifier With (Optional Clamp)

NOTE: R₁ R₂ INDICATES THE PARALLEL COMBINATION OF R₁ AND R₂

0308-21

Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.

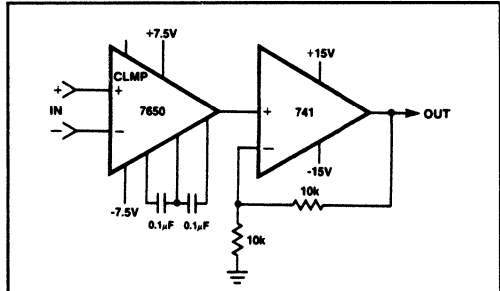


Figure 7: Using 741 to Boost Output Drive Capacity

0308-22

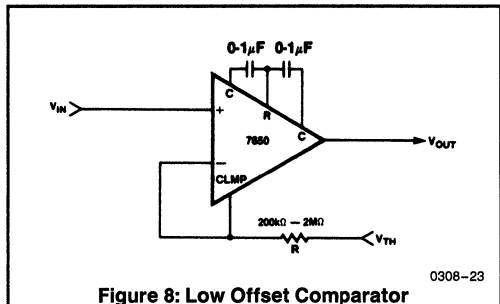


Figure 8: Low Offset Comparator

0308-23

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Figure 9. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

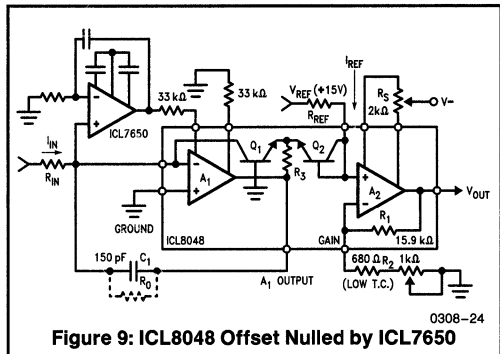


Figure 9: ICL8048 Offset Nulled by ICL7650

0308-24

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

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NOTE: All typical values have been characterized but are not tested.

ICL7650S

Super Chopper-Stabilized Operational Amplifier



GENERAL DESCRIPTION

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering *improved* input offset voltage, *lower* input offset voltage temperature coefficient, *reduced* input bias current, *wider* common mode voltage range and *ESD protection* greater than 2000 volts. All improvements are highlighted in *bold italics* in the Electrical Characteristics section. *Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.*

Intersil's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained. However the 14-lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

FEATURES

- **Guaranteed Max Input Offset Voltage for All Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- **Guaranteed Max Input Bias Current—10 pA**
- **Enhanced ESD Protection > 2000V**
- **Extremely Wide Common Mode Voltage Range—+3.5 to -5V**
- **Reduced Supply Current—2 mA**
- **Guaranteed Minimum Output Source/Sink Current**
- **Extremely High Gain—150 dB**
- **Extremely High CMRR and PSRR—140 dB**
- **High Slew Rate—2.5V/μs**
- **Wide Bandwidth—2 MHz**
- **Unity-gain Compensated**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully Over All Temperature Ranges**
- **Improved, Direct Replacement for Industry-Standard ICL7650 and other Second-Source Parts**

ORDERING INFORMATION

Part	Temperature Range	Package
ICL7650SCPA-1	0°C to +70°C	8-Pin Plastic
ICL7650SCPD		14-Pin Plastic
ICL7650SCTV-1		8-Pin TO-99
ICL7650SIJA-1	-25°C to +85°C	8-Pin CERDIP
ICL7650SIPA-1		8-Pin Plastic
ICL7650SIPD		14-Pin Plastic
ICL7650SIJD		14-Pin CERDIP
ICL7650SITV-1		8-Pin TO-99
ICL7650SMJD	-55°C to +125°C	14-Pin CERDIP
ICL7650SMTV-1		8-Pin TO-99

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	($V^+ + 0.3$) to ($V^- - 0.3$)
Voltage on Oscillator Control Pins	V^+ to V^-
Duration of Output Short Circuit	Indefinite
Current into Any Pin	10 mA
—while operating (Note 1)	100 μ A
Continuous Total Power Dissipation ($T_A = 25^\circ\text{C}$)	
CERDIP Package	500 mW
Plastic Package	375 mW
TO-99	250 mW

Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$
Operating Temperature Range	
ICL7650SC	0°C to $+70^\circ\text{C}$
ICL7650SI	-25°C to $+85^\circ\text{C}$
ICL7650SM	-55°C to $+125^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Conditions: ($V^+ = +5\text{V}$, $V^- = -5\text{V}$, $T_A = +25^\circ\text{C}$, Test Circuit as in Fig. 3 (unless otherwise specified))

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage (Note 2)	$T_A = +25^\circ\text{C}$		± 0.7	+5	μV
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		± 1	± 8	
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 2	± 10	
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 4	± 20	
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage (Note 2)	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		0.02		$\mu\text{V}/^\circ\text{C}$
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.02		
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.03	0.1	
$\Delta V_{OS}/\Delta t$	Change in Input Offset with Time			100		$\text{nV}/\sqrt{\text{month}}$
I_{bias}	Input Bias Current $ I(+) , I(-) $	$T_A = 25^\circ\text{C}$		4	10	pA
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		5	20	
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		20	50	
		$-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		20	50	
		$+85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		100	500	
I_{OS}	Input Offset Current $ I(-) - I(+) $	$T_A = 25^\circ\text{C}$		8	20	pA
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		10	40	
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		20	40	
		$-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		20	40	
		$+85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	50	
R_{IN}	Input Resistance			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain (Note 2)	$R_L = 10 \text{ k}\Omega, V_O = \pm 4\text{V}, T_A = 25^\circ\text{C}$	135	150		dB
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	130			
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	130			
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120			
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10 \text{ k}\Omega$	± 4.7	± 4.85		V
		$R_L = 100 \text{ k}\Omega$		± 4.95		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: ($V^+ = +5V$, $V^- = -5V$, $T_A = +25^\circ C$, Test Circuit as in Fig. 3 (unless otherwise specified))

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
CMVR	Common Mode Voltage Range (Note 2)	$T_A = 25^\circ C$	-5	-5.2 to +4	+3.5	V
		$0^\circ C \leq T_A \leq +70^\circ C$	-5		+3.5	
		$-25^\circ C \leq T_A \leq +85^\circ C$	-5		+3.5	
		$-55^\circ C \leq T_A \leq +125^\circ C$	-5		+3.5	
CMRR	Common Mode Rejection Ratio (Note 2)	$CMVR = -5V$ to $+3.5V$, $T_A = 25^\circ C$	120	140		dB
		$0^\circ C \leq T_A \leq +70^\circ C$	120			
		$25^\circ C \leq T_A \leq +85^\circ C$	115			
		$-55^\circ C \leq T_A \leq +125^\circ C$	110			
PSRR	Power Supply Rejection Ratio	$V^+, V^- = \pm 3V$ to $\pm 8V$	120	140		dB
en	Input Noise Voltage	$R_S = 100\Omega$, $f = DC$ to 10 Hz		2		μV_{p-p}
in	Input Noise Current	$f = 10$ Hz		0.01		pA/\sqrt{Hz}
GBW	Gain Bandwidth Product			2		MHz
SR	Slew Rate	$C_L = 50$ pF, $R_L = 10$ k Ω		2.5		V/ μs
t_r	Rise Time			0.2		μs
	Overshoot			20		%
V^+ to V^-	Operating Supply Range		4.5		16	V
I_{supp}	Supply Current	No Load, $T_A = 25^\circ C$		2	3	mA
		$0^\circ C \leq T_A \leq +70^\circ C$			3.2	
		$-25^\circ C \leq T_A \leq +85^\circ C$			3.5	
		$-55^\circ C \leq T_A \leq +125^\circ C$			4	
$I_{O\ source}$	Output Source Current	$T_A = 25^\circ C$	2.9	4.5		mA
		$0^\circ C \leq T_A \leq +70^\circ C$	2.3			
		$-25^\circ C \leq T_A \leq +85^\circ C$	2.2			
		$-55^\circ C \leq T_A \leq +125^\circ C$	2			
$I_{O\ sink}$	Output Sink Current	$T_A = 25^\circ C$	25	30		mA
		$0^\circ C \leq T_A \leq +70^\circ C$	20			
		$-25^\circ C \leq T_A \leq +85^\circ C$	19			
		$-55^\circ C \leq T_A \leq +125^\circ C$	17			
f_{ch}	Internal Chopping Frequency	Pins 12 & 14 Open	120	250	375	Hz
	Clamp ON Current (Note 4)	$R_L = 100$ k Ω , $T_A = 25^\circ C$	25	70		μA
	Clamp OFF Current (Note 4)	$-4V \leq V_{out} \leq +4V$, $T_A = 25^\circ C$		0.001	5	nA
		$0^\circ C \leq T_A \leq +70^\circ C$			10	
		$-25^\circ C \leq T_A \leq +85^\circ C$			10	
		$-55^\circ C \leq T_A \leq +125^\circ C$			15	

NOTE 1: Limiting input current to 100 μA is recommended to avoid latchup problems. Typically 1 mA is safe, however this is not guaranteed.

2: These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.

3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs. clamp current characteristics.

4: See OUTPUT CLAMP under detailed description.

5: All significant improvements over the industry-standard ICL7650 are highlighted in **bold italics**.

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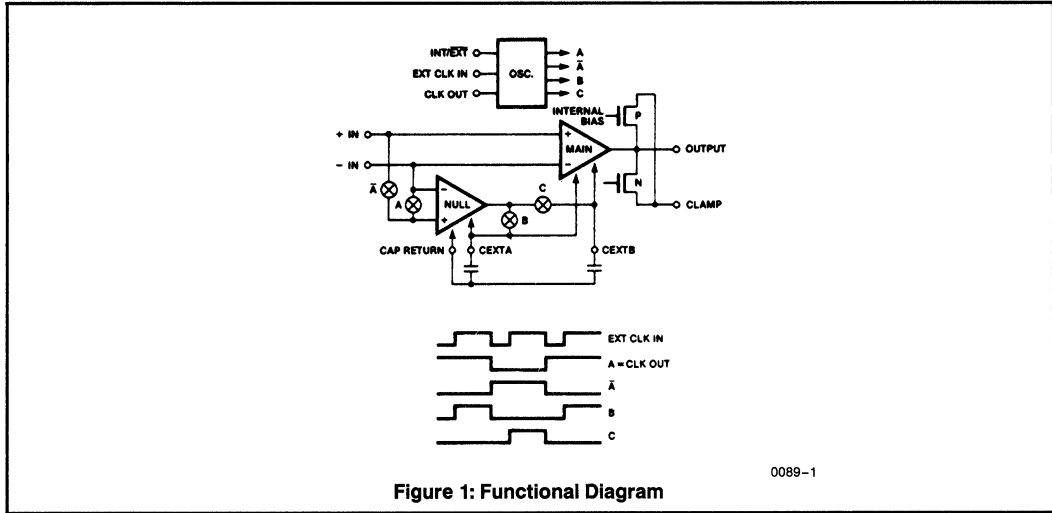


Figure 1: Functional Diagram

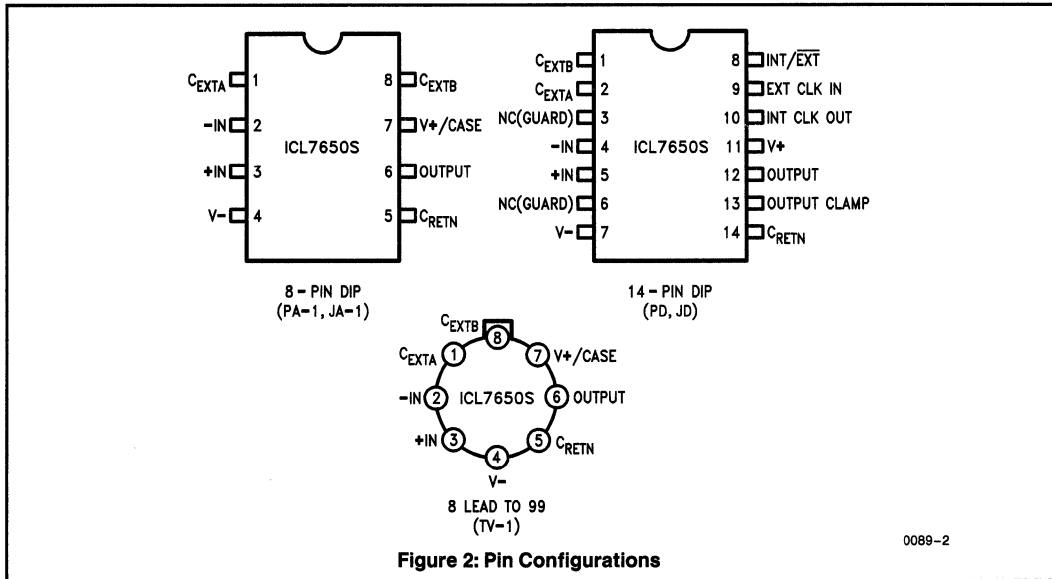
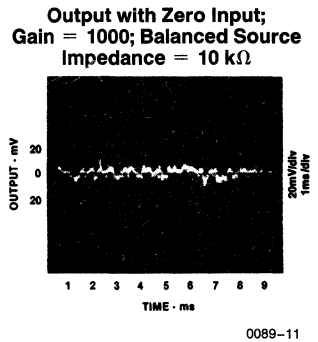
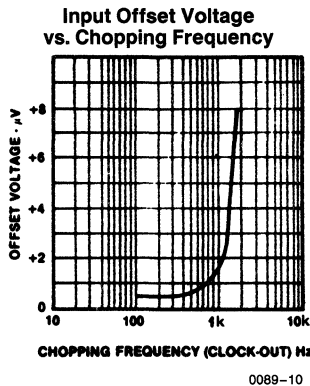
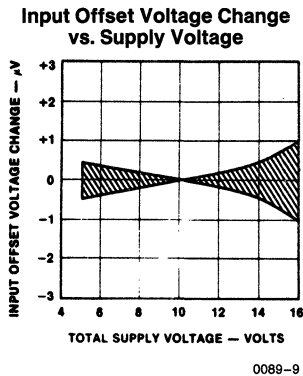
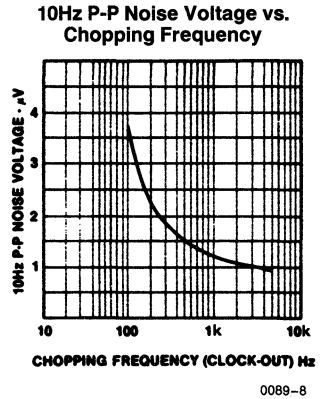
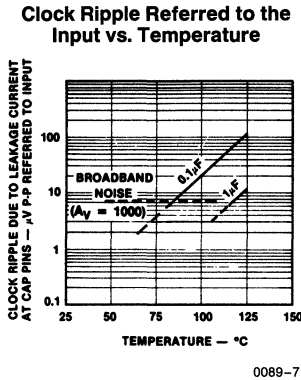
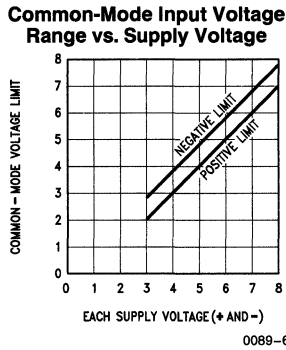
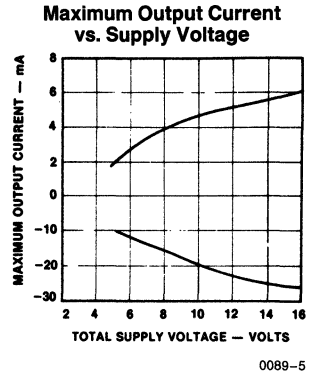
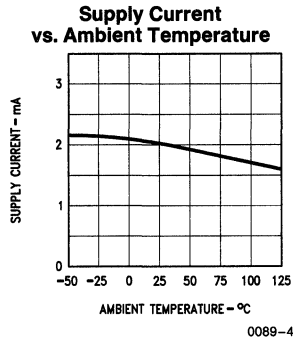
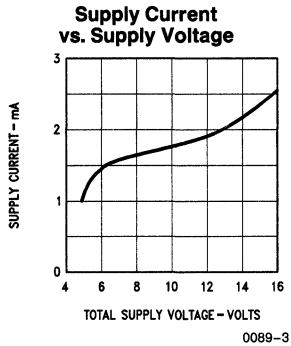


Figure 2: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

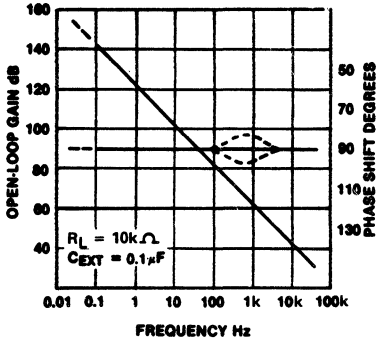


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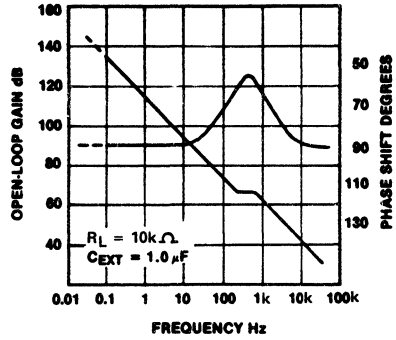
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Open Loop Gain and Phase Shift vs. Frequency



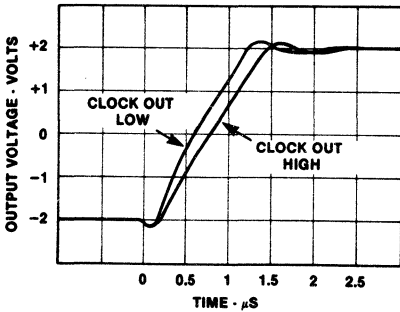
0089-12

Open Loop Gain and Phase Shift vs. Frequency



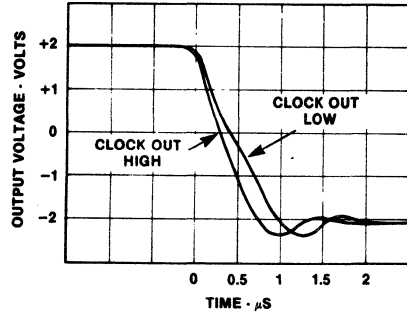
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Voltage Follower Large Signal Pulse Response*



0089-14

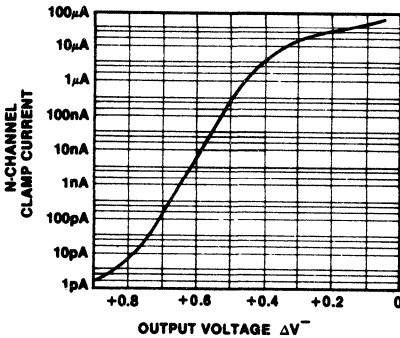
Voltage Follower Large Signal Pulse Response*



0089-15

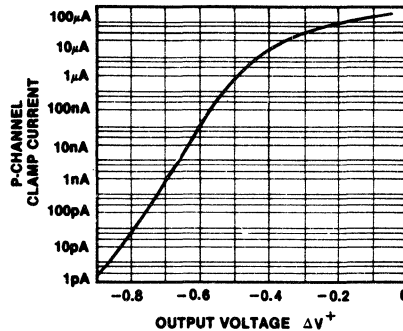
*THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-Channel Clamp Current vs. Output Voltage



0089-16

P-Channel Clamp Current vs. Output Voltage



0089-17

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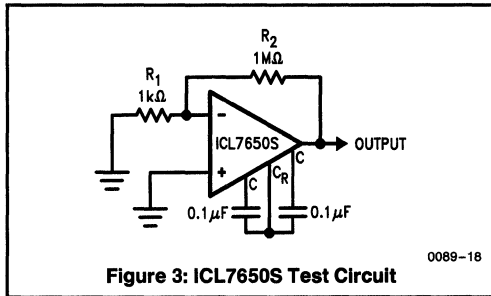


Figure 3: ICL7650S Test Circuit

DETAILED DESCRIPTION

Amplifier

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL} .

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null/storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} .

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650S has an internal oscillator, giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%–80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^- . The logic threshold will be at about 2.5V below V^+ . Note also that a signal of about 400 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10 μ V/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The two required capacitors, C_{EXTA} and C_{EXTB} , have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μ F, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest setting on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μ V.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

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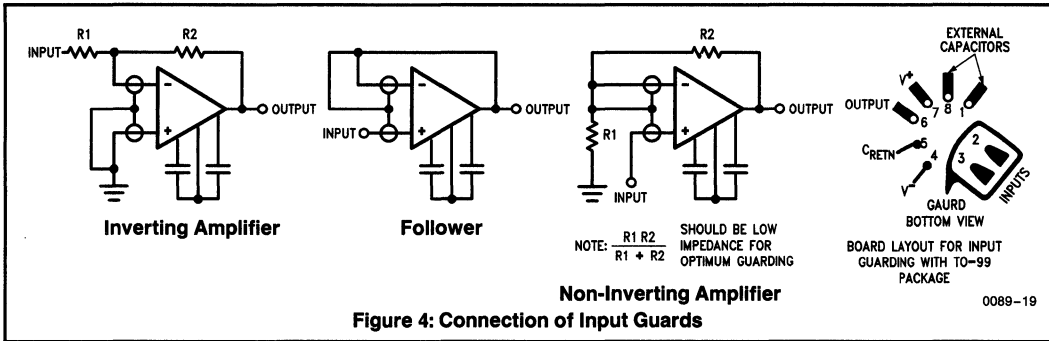


Figure 4: Connection of Input Guards

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18 kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120 dB even with a 1 kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to

realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

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Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and $V+$, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μ A748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650S.

TYPICAL APPLICATIONS

Clearly the applications of the ICL7650S will mirror those of other op amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650S are the supply voltage ($\pm 8V$ max.) and the output drive capability (10 k Ω load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

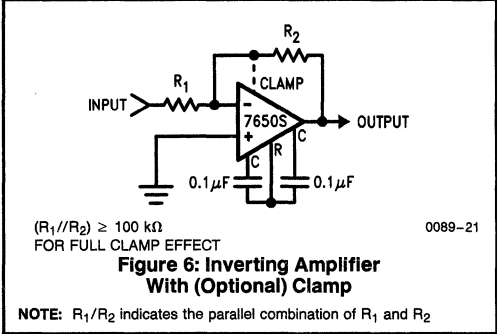
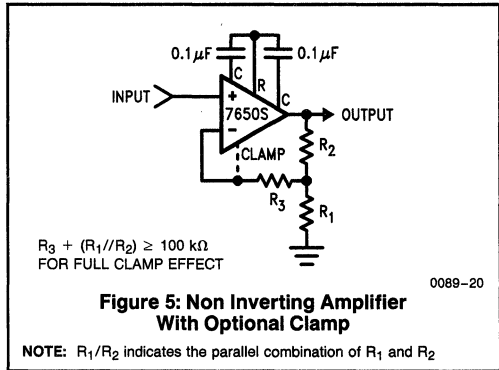


Figure 6: Inverting Amplifier With (Optional) Clamp
 Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.

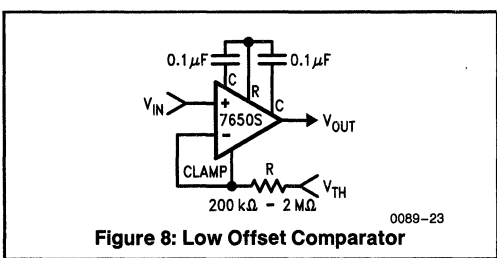
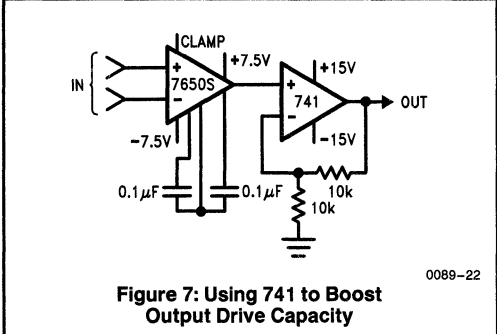
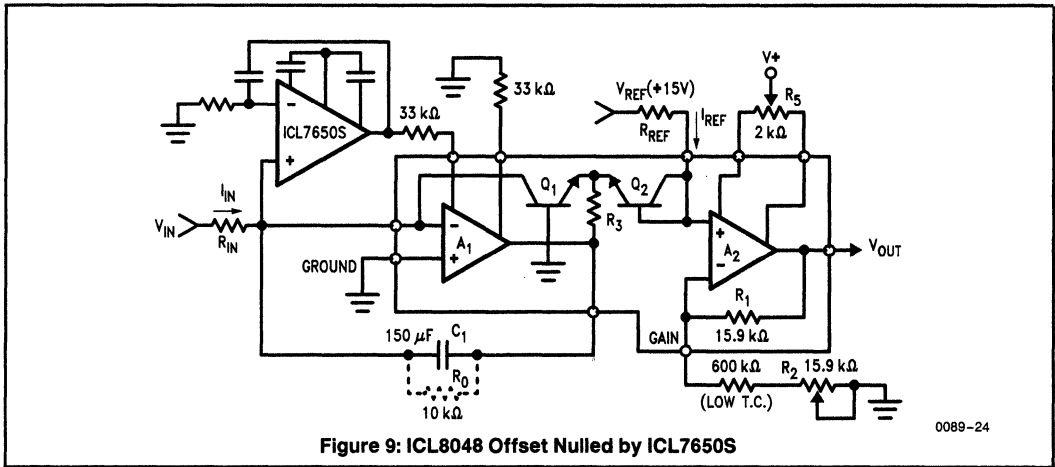


Figure 7: Using 741 to Boost Output Drive Capacity
Figure 8: Low Offset Comparator
 Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650S to offset-null the ICL8048, as shown in Figure 9. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

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NOTE: All typical values have been characterized but are not tested.



FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

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NOTE: All typical values have been characterized but are not tested.

ICL7652

Chopper-Stabilized Low-Noise Operational Amplifier



GENERAL DESCRIPTION

The ICL7652 chopper-stabilized amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is similar to INTERSIL's ICL7650 but offers improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are reduced slightly.

INTERSIL's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652 is internally compensated for unity-gain operation.

An enhanced direct replacement for this part called ICL7652S will become available shortly and will be more appropriate for new designs.

FEATURES

- Extremely Low Input Offset Voltage — $10\mu\text{V}$ Over Temperature Range
- Ultra Low Long-Term and Temperature Drifts of Input Offset Voltage ($150\text{nV}/\text{Month}$, $100\text{nV}/^\circ\text{C}$)
- Low DC Input Bias Current — 15pA
- Extremely High Gain, CMRR and PSRR — Min 110dB
- Low Input Noise Voltage — $0.2\mu\text{Vp-p}$ (DC — 1Hz)
- Internally Compensated for Unity-Gain Operation
- Very Low Intermodulation Effects (Open-Loop Phase Shift $<2^\circ$ @ Chopper Frequency)
- Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use
- Extremely Low Chopping Spikes at Input and Output

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7652CPD	0°C to $+70^\circ\text{C}$	14-pin plastic
ICL7652JJD	-25°C to $+85^\circ\text{C}$	14-pin Cerdip
ICL7652CTV	0°C to $+70^\circ\text{C}$	8-pin TO-99
ICL7652ITV	-25°C to $+85^\circ\text{C}$	8-pin TO-99

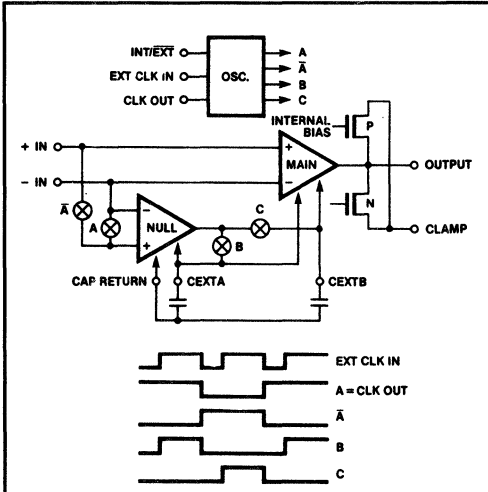


Figure 1: Functional Diagram

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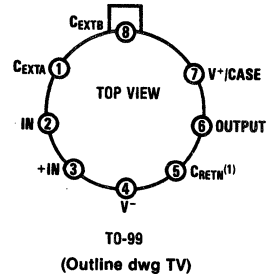
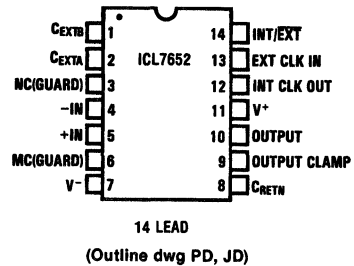


Figure 2: Pin Configuration

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
 Input Voltage ($V^+ + 0.3$) to ($V^- - 0.3$)V
 Voltage on Oscillator Control Pins V^+ to V^-
 Duration of Output Short Circuit Indefinite
 Current into Any Pin 10mA
 — while operating (Note 4) 100 μ A

Continuous Total Power Dissipation ($T_A = 25^\circ\text{C}$)
 CERDIP Package 500mW
 Plastic Package 375mW
 TO-99 250mW
 Storage Temperature Range -55°C to 150°C
 Operating Temperature Range
 ICL7652C 0°C to $+70^\circ\text{C}$
 ICL7652I -25°C to $+85^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $T_A = +25^\circ\text{C}$, Test Circuit (unless otherwise specified)

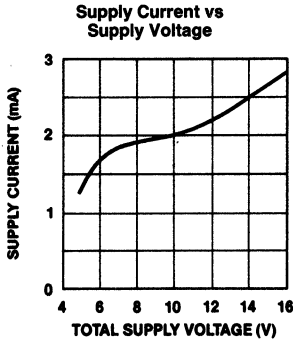
Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$T_A = +25^\circ\text{C}$		± 2	± 5	μV
		Over Operating Temperature Range (Note 1)		± 10		
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temperature Coefficient of Input Offset Voltage	Operating Temperature Range (Note 1)		0.1		$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage vs Time			150		nV/month
I_{BIAS}	Input Bias Current (Doubles every 10°C) (Note 5)	$T_A = +25^\circ\text{C}$		15	30	pA
		$0^\circ\text{C} < T_A < +70^\circ\text{C}$		35		
		$-25^\circ\text{C} < T_A < +85^\circ\text{C}$		100		
I_{OS}	Input Offset Current	$T_A = +25^\circ\text{C}$		25		pA
R_{IN}	Input Resistance			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 10\text{k}\Omega$, $V_{OUT} = \pm 4\text{V}$	120	150		dB
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10\text{k}\Omega$	± 4.7	± 4.85		V
		$R_L = 100\text{k}\Omega$		± 4.95		
CMVR	Common-Mode Voltage Range		-4.3	-4.8 to +4.0	3.5	V
CMRR	Common-Mode Rejection Ratio	CMVR = -4.3V to +3.5V	110	130		dB
PSRR	Power Supply Rejection Ratio	$\pm 3\text{V}$ to $\pm 8\text{V}$	110	130		dB
e_n	Input Noise Voltage	$R_S = 100\Omega$, DC to 1Hz		0.2		$\mu\text{Vp-p}$
		DC to 10Hz		0.7		
i_n	Input Noise Current	$f = 10\text{Hz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
GBW	Unity-Gain Bandwidth			0.4		MHz
SR	Slew Rate	$C_L = 50\text{pF}$, $R_L = 10\text{k}\Omega$		0.5		$\text{V}/\mu\text{s}$
		Overshoot		15		
V^+ to V^-	Operating Supply Range		5.0		16	V
I_{SUPPLY}	Supply Current	No Load		2.0	3.5	mA
f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	200	400	600	Hz
	Clamp ON Current (Note 2)	$R_L = 100\text{k}\Omega$	25	100	150	μA
	Clamp OFF Current (Note 2)	$-4.0\text{V} < V_{OUT} < +4.0\text{V}$		1		pA

- NOTES:** 1. -25°C to $+85^\circ\text{C}$, or 0°C to $+70^\circ\text{C}$.
 2. See OUTPUT CLAMP under detailed description.
 3. OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs clamp current characteristics.
 4. Limiting input current to 100 μA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
 5. I_{BIAS} tested with clock disabled.

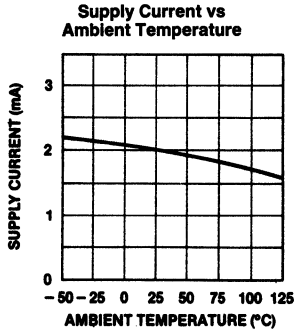
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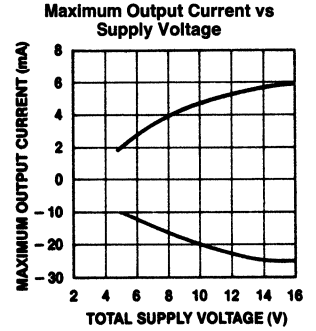
TYPICAL PERFORMANCE CHARACTERISTICS



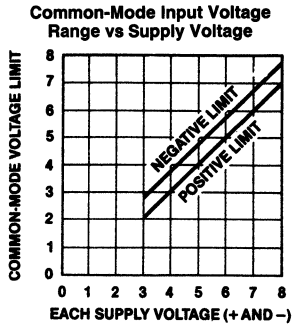
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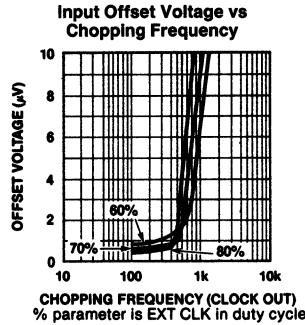
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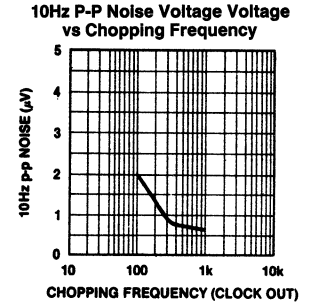
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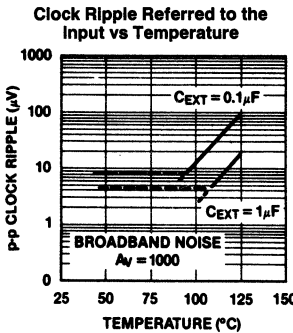
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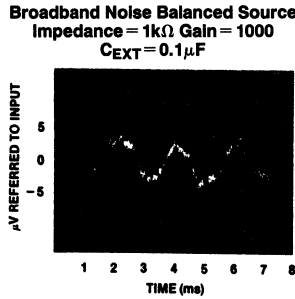
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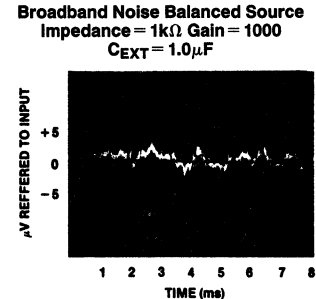
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0309-10



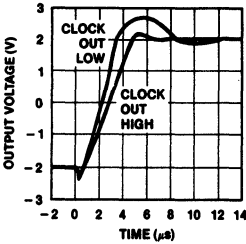
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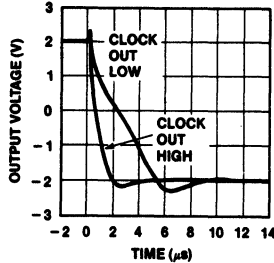
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Follower Large Signal Pulse Response*



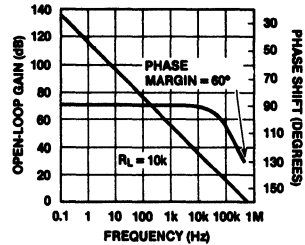
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Voltage Follower Large Signal Pulse Response*



0309-13

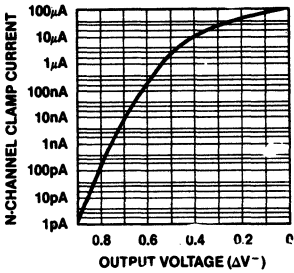
Open-Loop Gain and Phase Shift vs Frequency



0309-14

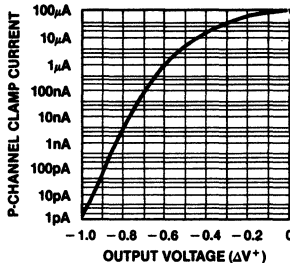
*The two different responses correspond to the two phases of the clock.

N-Channel Clamp Current vs Output Voltage



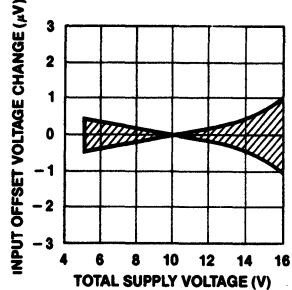
0309-15

P-Channel Clamp Current vs Output Voltage



0309-16

Input Offset Voltage Change vs Supply Voltage



0309-17

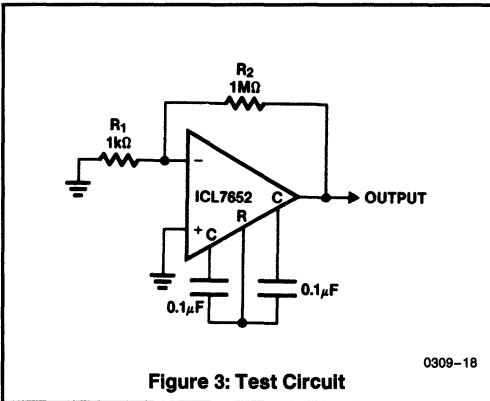


Figure 3: Test Circuit

0309-18

DETAILED DESCRIPTION

The Functional Diagram (Figure 1) shows the major elements of the ICL7652. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from

the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high-impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL} .

Careful balancing of the input switches, together with the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals. Feedforward-type injection into the compensation capacitor is also minimized, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and

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NOTE: All typical values have been characterized but are not tested.

phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7652, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} .

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled differential input voltages are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7652 has an internal oscillator, giving a chopping frequency of 400Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50% – 80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^- . The logic threshold will be at about 2.5V below V^+ . Note also that a signal of about 800Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than $10\mu\text{V}/\text{sec}$, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The required capacitors, C_{EXTA} and C_{EXTB} , are normally in the range of $0.1\mu\text{F}$ to $1.0\mu\text{F}$. A $1.0\mu\text{F}$ capacitor should be used in broad bandwidth circuits if minimum clock ripple

noise is desired. For limited bandwidth applications where clock ripple is filtered out, using a $0.1\mu\text{F}$ capacitor results in slightly lower offset voltage. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to $1\mu\text{V}$.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics which may result in increased input-leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately $18\text{k}\Omega$), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a $1\text{k}\Omega$ load than with a $10\text{k}\Omega$ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a $1\text{k}\Omega$ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of $10\text{k}\Omega$ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermo-couple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around $0.1\mu\text{V}/^\circ\text{C}$, but up to tens of $\mu\text{V}/^\circ\text{C}$ for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

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Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7652. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 lead TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, which are usually used for offset-null or compensation capacitors. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, $\mu A748$, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7652.

7

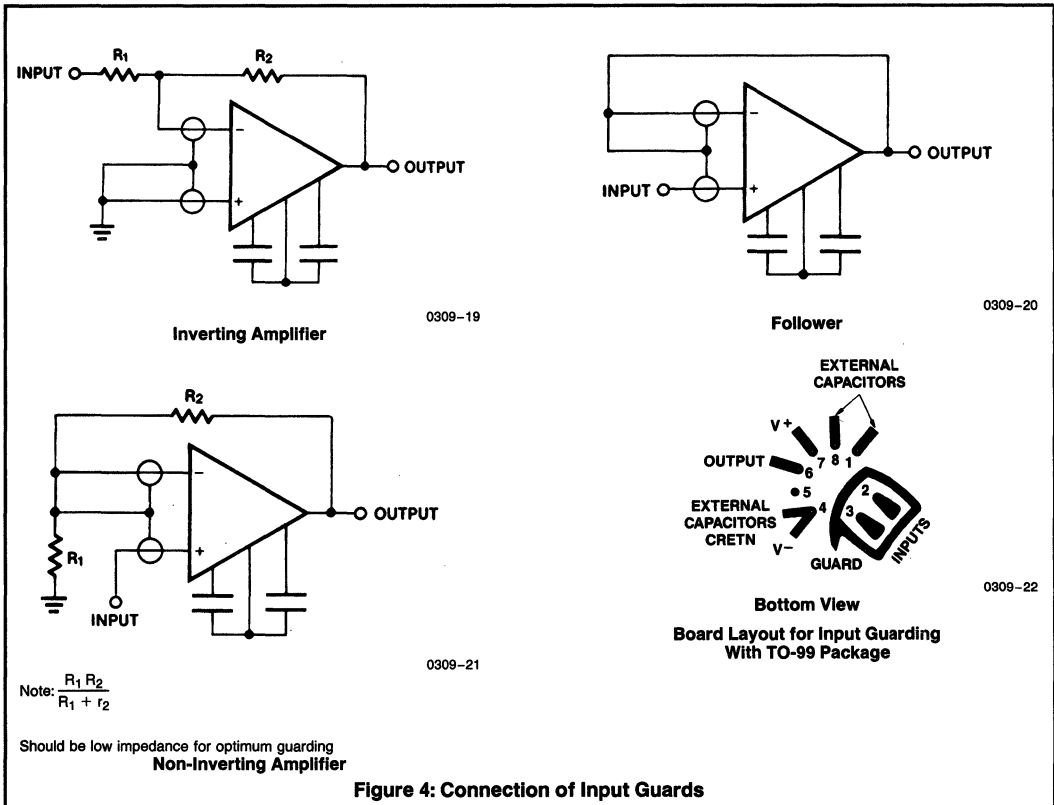


Figure 4: Connection of Input Guards

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TYPICAL APPLICATIONS

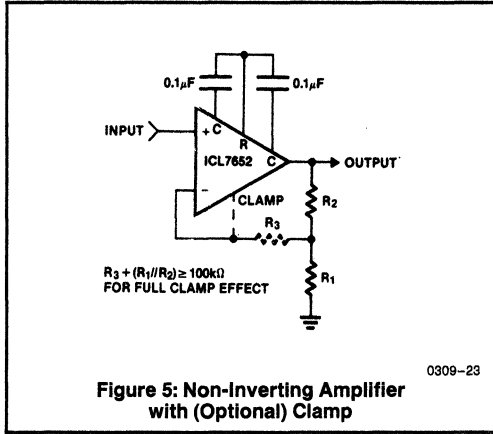


Figure 5: Non-Inverting Amplifier with (Optional) Clamp

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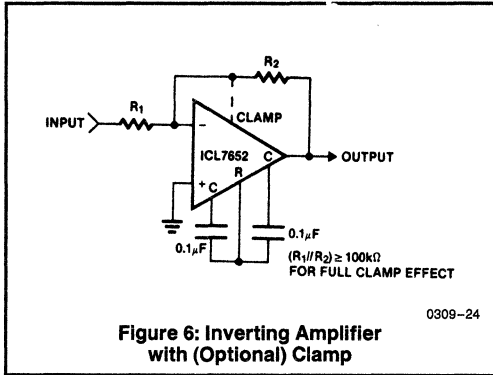


Figure 6: Inverting Amplifier with (Optional) Clamp

0309-24

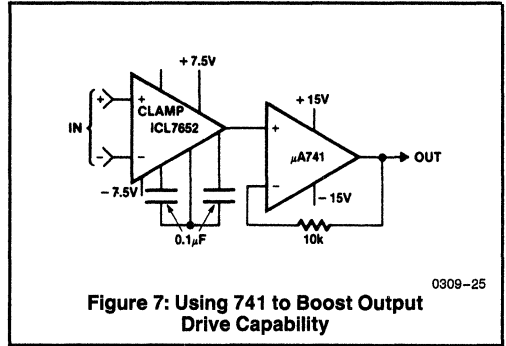


Figure 7: Using 741 to Boost Output Drive Capability

0309-25

Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper-stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.

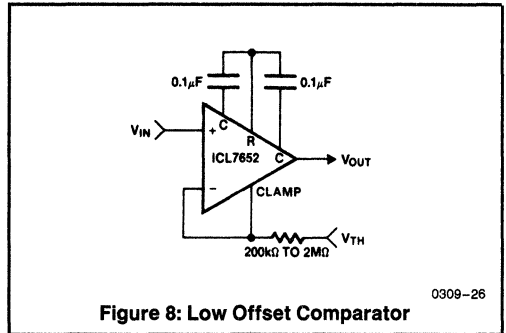


Figure 8: Low Offset Comparator

0309-26

Clearly the applications of the ICL7652 will mirror those of other op-amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7652 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op-amps by the ICL7652 are the supply voltage ($\pm 8V$ max) and the output drive capability ($10k\Omega$ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7652. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

It is possible to use the ICL7652 to offset-null such high slew rate and bandwidth amplifiers as the HA2500 and HA2600 series, as shown in Figure 9. The same basic idea can be used with low-noise bipolar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced. More details on these and other ideas are explained in application note A053.

Mixing the ICL7652 with circuits operating at $\pm 15V$ supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit "backwards". A suitable connection is shown in Figure 10.

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TYPICAL APPLICATIONS (Continued)

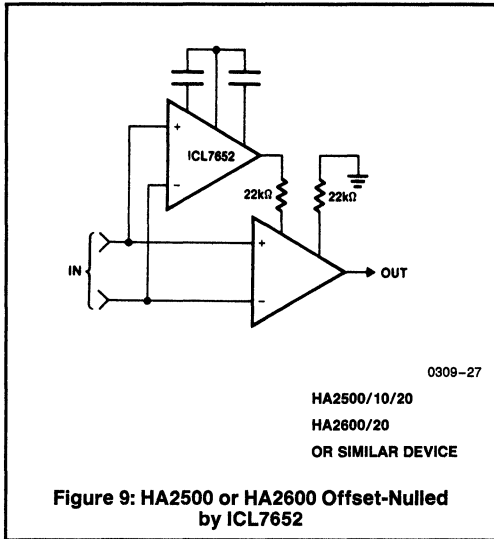


Figure 9: HA2500 or HA2600 Offset-Nullled by ICL7652

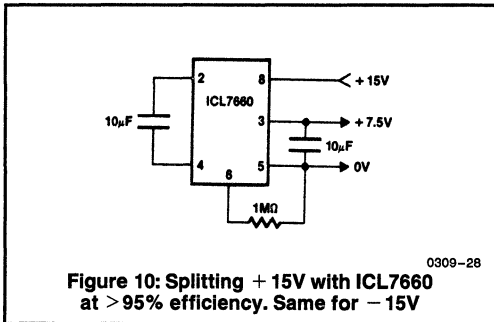


Figure 10: Splitting +15V with ICL7660 at >95% efficiency. Same for -15V

For further applications assistance, see A053 and R017

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NOTE: All typical values have been characterized but are not tested.

ICL7652S

Super Chopper-Stabilized Low-Noise Operational Amplifier



GENERAL DESCRIPTION

The ICL7652S Super Chopper-Stabilized Low-Noise Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7652 offering **Improved** input offset voltage, **lower** input offset voltage temperature coefficient, **reduced** input bias current, **wide** common mode voltage range, and **ESD protection** greater than 2000 volts. All improvements are highlighted in **bold italics** in the Electrical Characteristics Section. **Critical parameters are guaranteed over the entire commercial, industrial, and military temperature range.**

Intersil's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652S is internally compensated for unity-gain operation.

FEATURES

- **Guaranteed Max Input Offset Voltage for All Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- **Reduced Input Bias Current—3 pA Typ; 30 pA Max over Temperature**
- **Enhanced ESD Protection > 2000V**
- **Extremely Wide Common Mode Voltage Range—+3.5 to -4.3 Volts**
- **Reduced Supply Current—1.7 mA; 3.5 mA Max over mil Temperature**
- **Guaranteed Minimum Output Source/Sink Current**
- **Extremely High Gain -150 dB**
- **Low Input Noise Voltage—0.2 μ Vp-p (DC-1 Hz)**
- **Unity-Gain Compensated**
- **Very Low Intermodulation Effects (Open-Loop Phase Shift < 2 μ @ Chopper Frequency)**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use (14-Lead only)**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully Over Military Temperature Range**
- **Improved Direct Replacement for Industry-Standard IC7652 and other Second-Source Parts**

ORDERING INFORMATION

Part	Temperature Range	Package
ICL7652SCPD	0°C to +70°C	14-Pin Plastic
ICL7652SCJD		14-Pin CERDIP
ICL7652SCTV		8-Pin TO-99
ICL7652SIJD	-25°C to +85°C	14-Pin CERDIP
ICL7652SITV		8-Pin TO-99
ICL7652SIPD		14-Pin Plastic
ICL7652SMJD	-55°C to +125°C	14-Pin CERDIP
ICL7652SMTV		8-Pin TO-99

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	$(V^+ + 0.3)$ to $(V^- - 0.3)$
Voltage on Oscillator Control Pins	V^+ to V^-
Duration of Output Short Circuit	Indefinite
Current into Any Pin	10 mA
—While Operating (Note 1)	100 μ A
Continuous Total Power Dissipation ($T_A = 25^\circ\text{C}$)	
CERDIP Package	500 mW
Plastic Package	375 mW
TO-99	250 mW

Storage Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$
Operating Temperature Range	
ICL7652SC	0°C to $+70^\circ\text{C}$
ICL7652SI	-25°C to $+85^\circ\text{C}$
ICL7652SM	-55°C to $+125^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $T_A = +25^\circ\text{C}$, Test Circuit as in Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$T_A = +25^\circ\text{C}$		± 0.7	± 5	μV
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		± 2	± 7	
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 3	± 10	
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 15	± 50	
$\Delta V_{OS}/\Delta T$	Average Temp. Coefficient of Input Offset Voltage (Note 2)	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		0.01	0.06	$\mu\text{V}/^\circ\text{C}$
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.02	0.07	
		$-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.02	0.07	
		$-85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.4	1.0	
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.1	0.4	
$\Delta V_{OS}/\Delta t$	Change in Input Offset with Time			150		$\text{nV}/\sqrt{\text{month}}$
I_{bias}	Input Bias Current $ I(+) , I(-) $	$T_A = 25^\circ\text{C}$		3	30	pA
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$			30	
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			30	
		$-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			30	
		$+85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			500	
I_{os}	Input Offset Current $ I(-) - I(+) $	$T_A = 25^\circ\text{C}$		15	40	pA
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$			40	
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			40	
		$-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			40	
		$+85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			75	
R_{iN}	Input Resistance			10 ¹²		Ω
A_{VOL}	Large Signal Voltage Gain (Note 2)	$R_L = 10\text{K}\Omega, V_O = \pm 4\text{V}, T_A = 25^\circ\text{C}$	135	150		dB
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	130			
		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	130			
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120			
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10\text{K}\Omega$	± 4.7	± 4.85		V
		$R_L = 100\text{K}\Omega$		± 4.95		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

 Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25^\circ C$, Test Circuit (unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
CMRR	Common Mode Rejection Ratio (Note 2)	$CMVR = -4.3V$ to $+3.5$, $T_A = 25^\circ C$	120	130		dB
		$0^\circ C \leq T_A \leq +70^\circ C$	110			
		$-25^\circ C \leq T_A \leq +85^\circ C$	110			
		$-55^\circ C \leq T_A \leq +125^\circ C$	100			
PSRR	Power Supply Rejection Ratio (Note 2)	$V^+, V^- = \pm 3V$ to $\pm 8V$	120	130		dB
		$0^\circ C \leq T_A \leq +70^\circ C$	110			
		$-25^\circ C \leq T_A \leq +85^\circ C$	110			
		$-55^\circ C \leq T_A \leq +125^\circ C$	100			
en	Input Noise Voltage	$R_s = 100\Omega$, $f = DC$ to 1 Hz		0.2		μV_{p-p}
		$f = DC$ to 10 Hz		0.7		
in	Input Noise Current	$f = 10$ Hz		0.01		pA/\sqrt{Hz}
GBW	Gain Bandwidth			500		kHz
SR	Slew Rate	$CL = 50$ pF, $RL = 10$ K Ω		1.0		V/ μs
	Overshoot			15		%
V^+ to V^-	Operating Supply Range		5.0		16	V
I_{SUPP}	Supply Current	No Load $T_A = 25^\circ C$		1.7	2.5	mA
		$0^\circ C < T_A < 70^\circ C$			3.0	
		$-25^\circ C < T_A < 85^\circ C$			3.0	
		$-55^\circ C < T_A < 125^\circ C$			3.5	
I _{O source}	Output Source Current	$T_A = 25^\circ C$	2.4	4.4		mA
		$0^\circ C < T_A < 70^\circ C$	2.0			
		$-25^\circ C < T_A < 85^\circ C$	1.9			
		$-55^\circ C < T_A < 125^\circ C$	1.7			
I _{O sink}	Output Sink Current	$T_A = 25^\circ C$	15.0	20.0		mA
		$0^\circ C < T_A < 70^\circ C$	12.0			
		$-25^\circ C < T_A < 85^\circ C$	12.0			
		$-55^\circ C < T_A < 125^\circ C$	11.0			
f_{ch}	Internal Chopping Frequency	Pins 12 & 14 Open (dip)	250	450	650	Hz
	Clamp ON Current (Note 4)	$RL = 100$ K Ω , $T_A = 25^\circ C$	30	100		μA
	Clamp OFF Current (Note 4)	$-4.0V < V_{OUT} < +4.0V$, $T_A = 25^\circ C$		0.001	10	nA
		$0^\circ C \leq T_A \leq +70^\circ C$			10	
		$-25^\circ C \leq T_A \leq +85^\circ C$			10	
		$-55^\circ C \leq T_A \leq +125^\circ C$			10	

NOTE 1: Limiting input current to 100 μA is recommended to avoid latchup problems. Typically 1 mA is safe, however this is not guaranteed.

2: These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.

3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.

4: See OUTPUT CLAMP under detailed description.

5: All significant improvements over the industry-standard ICL7652 are highlighted in **bold italics**.

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NOTE: All typical values have been characterized but are not tested.

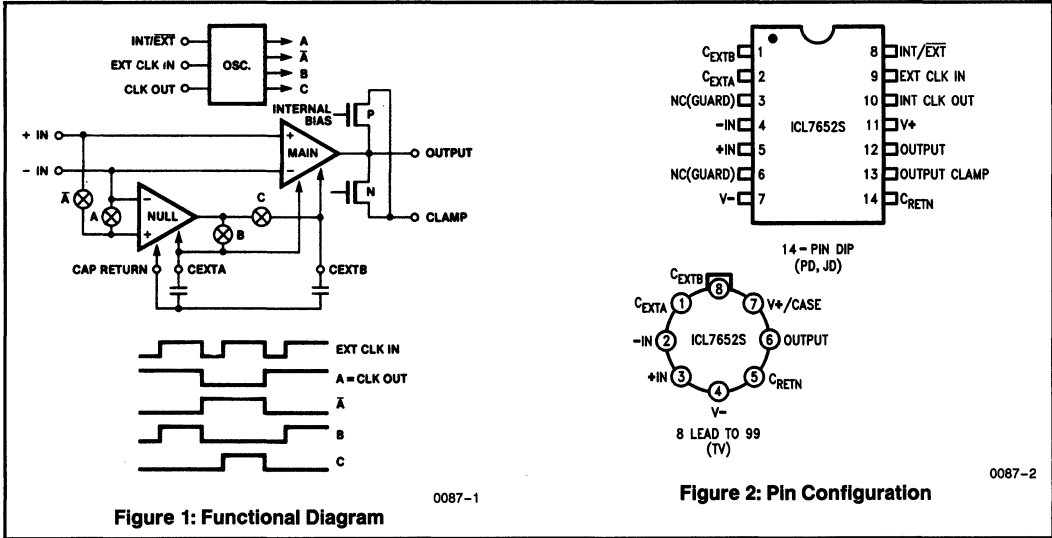
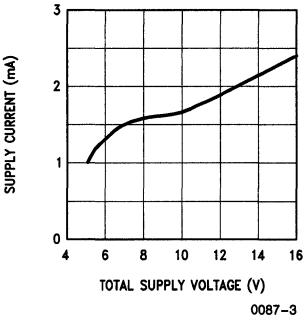


Figure 1: Functional Diagram

Figure 2: Pin Configuration

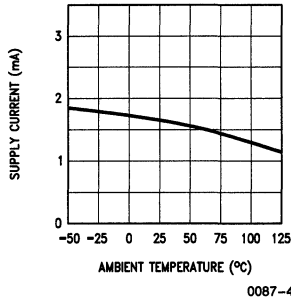
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



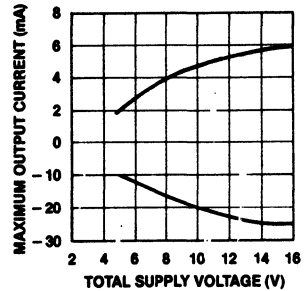
0087-3

Supply Current vs Ambient Temperature



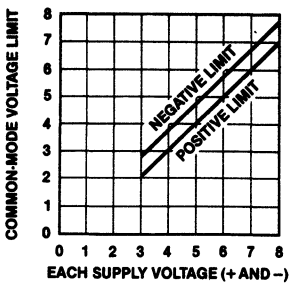
0087-4

Maximum Output Current vs Supply Voltage



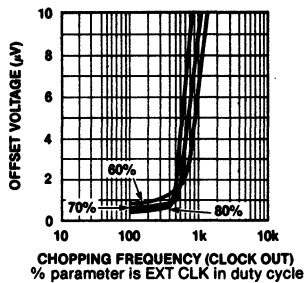
0087-5

Common-Mode Input Voltage Range vs Supply Voltage



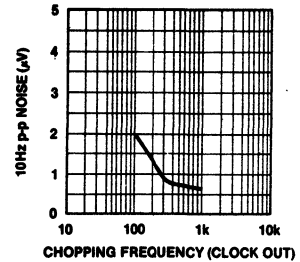
0087-6

Input Offset Voltage vs Chopping Frequency



0087-7

10 Hz P-P Noise Voltage vs Chopping Frequency



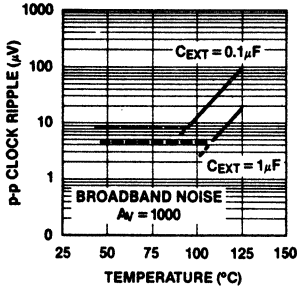
0087-8

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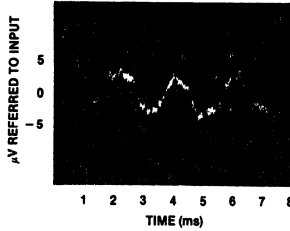
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Clock Ripple Referred to the Input vs Temperature



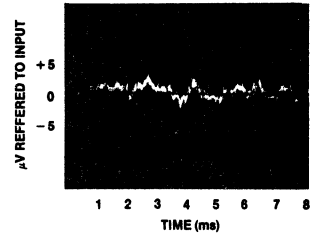
0087-9

Broadband Noise Balanced Source Impedance = 1 kΩ Gain = 1000 C_{EXT} = 0.1 µF



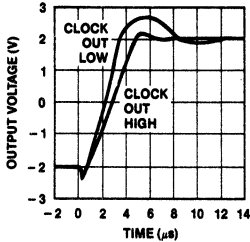
0087-10

Broadband Noise Balanced Source Impedance = 1 kΩ Gain = 1000 C_{EXT} = 1.0 µF



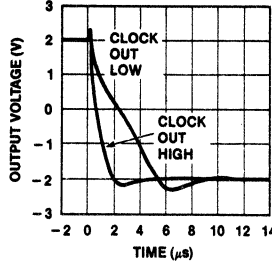
0087-11

Voltage Follower Large Signal Pulse Response*



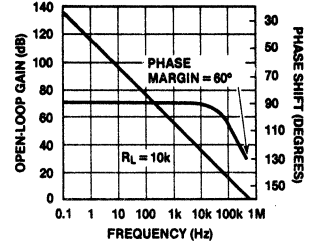
0087-12

Voltage Follower Large Signal Pulse Response*



0087-13

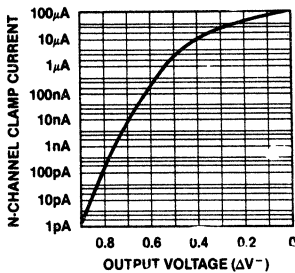
Open-Loop Gain and Phase Shift vs Frequency



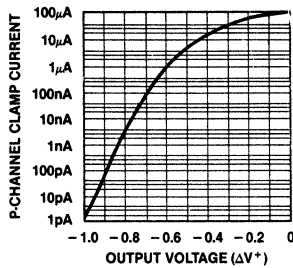
0087-14

*THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-Channel Clamp Current vs Output Voltage

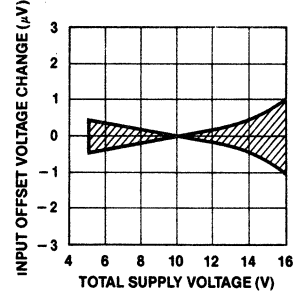


P-Channel Clamp Current vs Output Voltage



0087-16

Input Offset Voltage Change vs Supply Voltage



0087-17

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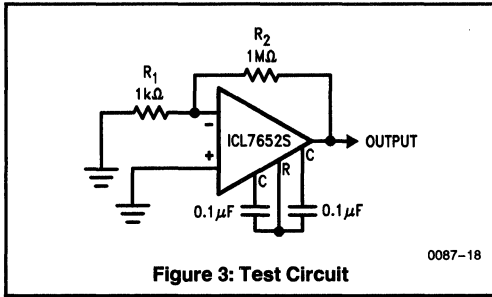


Figure 3: Test Circuit

DETAILED DESCRIPTION

The Functional Diagram (Figure 1) shows the major elements of the ICL7652S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high-impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL} .

Careful balancing of the input switches, together with the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals. Feedforward-type injection into the compensation capacitor is also minimized, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7652S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} .

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled differential input voltages are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7652S has an internal oscillator, giving a chopping frequency of 400 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%-80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^- . The logic threshold will be at about 2.5V below V^+ . Note also that a signal of about 800 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than $10 \mu V/sec$, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The required capacitors, C_{EXTA} and C_{EXTB} , are normally in the range of $0.1 \mu F$ to $1.0 \mu F$. A $1.0 \mu F$ capacitor should be used in broad bandwidth circuits if minimum clock ripple noise is desired. For limited bandwidth applications where clock ripple is filtered out, using a $0.1 \mu F$ capacitor results in slightly lower offset voltage. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest setting on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to $1 \mu V$.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics which may result in increased input-leakage currents.

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Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18 kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120 dB even with a 1 kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7652S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 lead TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, which are usually used for offset-null or compensation capacitors. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA 748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7652S.

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NOTE: All typical values have been characterized but are not tested.

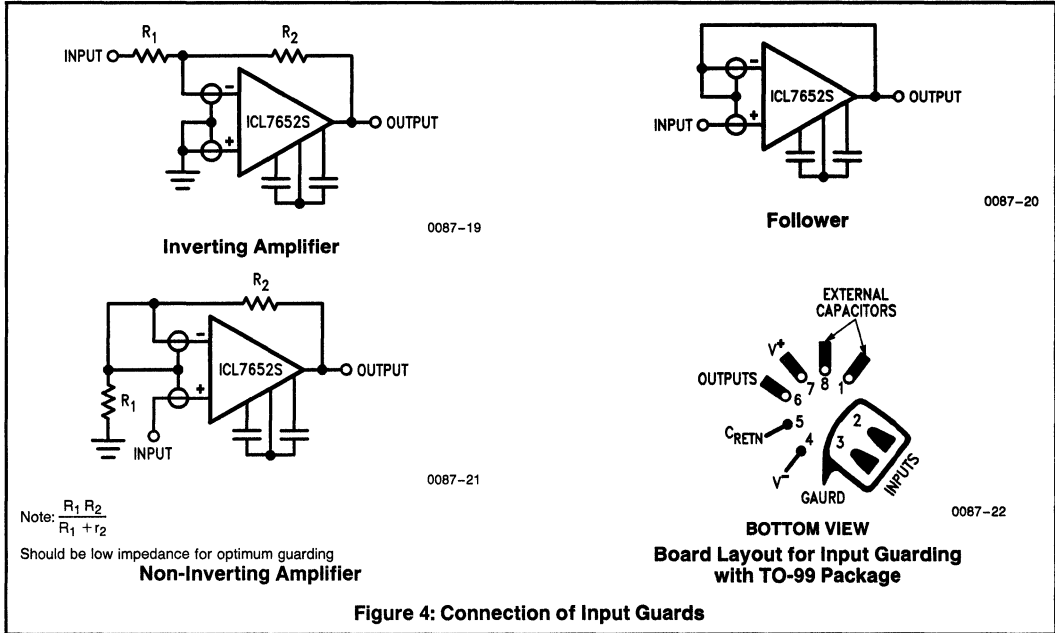
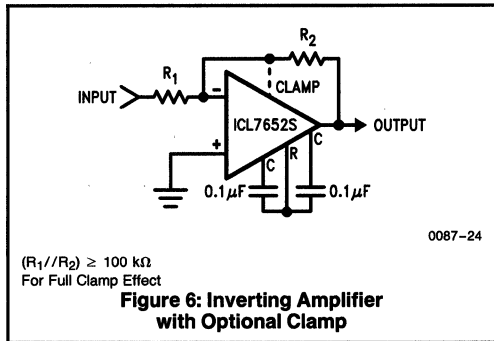
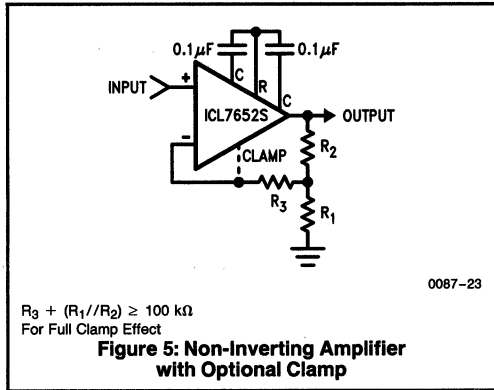


Figure 4: Connection of Input Guards

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NOTE: All typical values have been characterized but are not tested.

TYPICAL APPLICATIONS



Clearly the applications of the ICL7652S will mirror those of other op-amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7652S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op-amps by the ICL7652S are the supply voltage ($\pm 8\text{V}$ max) and the output drive capability (10 k Ω load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7652S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

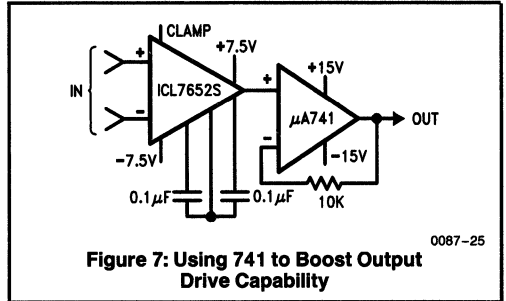
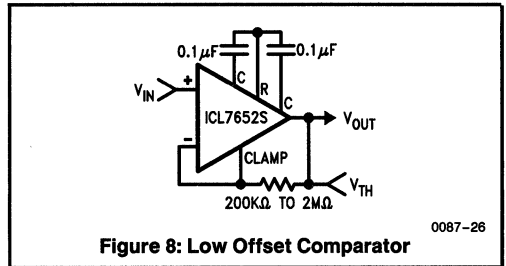


Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper-stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.



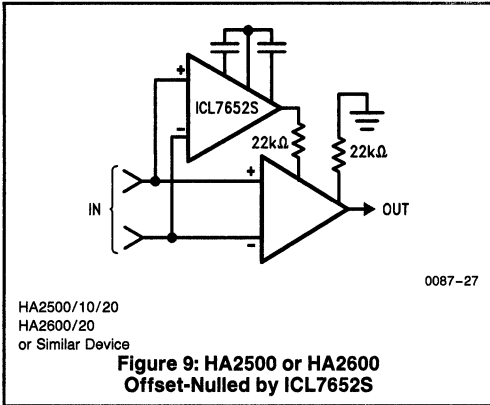
It is possible to use the ICL7652S to offset-null such high slew rate and bandwidth amplifiers as the HA2500 and HA2600 series, as shown in Figure 9. The same basic idea can be used with low-noise bipolar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced. More details on these and other ideas are explained in application note A053.

Mixing the ICL7652S with circuits operating at $\pm 15\text{V}$ supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the ICL7660S voltage converter circuit "backwards". A suitable connection is shown in Figure 10.

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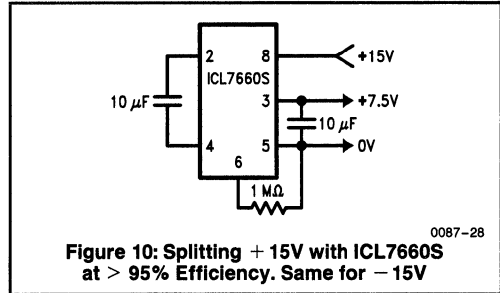
NOTE: All typical values have been characterized but are not tested.

TYPICAL APPLICATIONS (Continued)



**Figure 9: HA2500 or HA2600
Offset-Nullified by ICL7652S**

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017.



**Figure 10: Splitting +15V with ICL7660S
at > 95% Efficiency. Same for -15V**

ICL8007 JFET Input Operational Amplifier



GENERAL DESCRIPTION

The Intersil ICL8007 is a low input current JFET input operational amplifier. The ICL8007A is selected for 4 pA max input current.

The devices are designed for use in very high input impedance applications. Because of their high slew rate, high common mode voltage range and absence of "latch-up", they are ideal for use as a voltage follower.

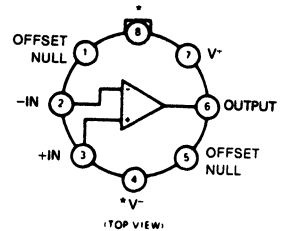
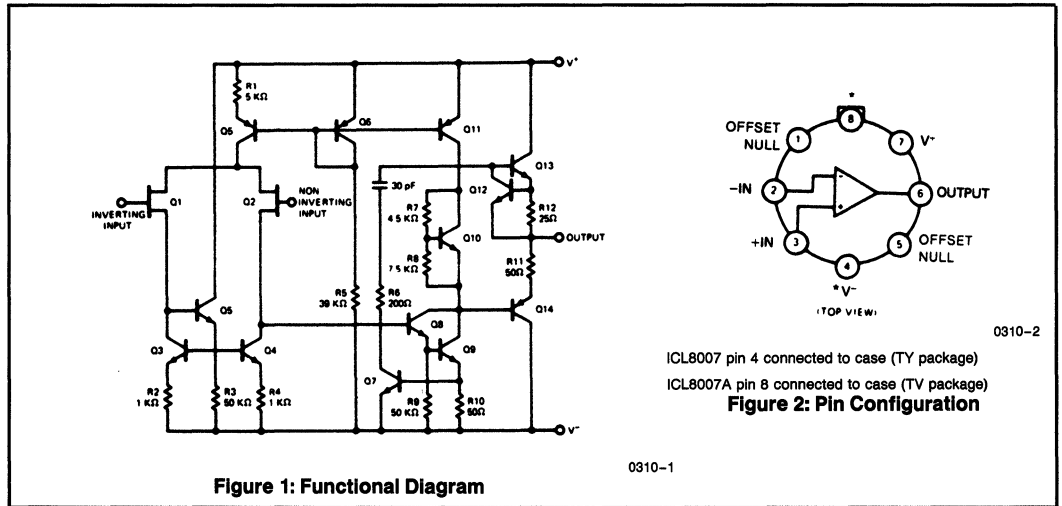
The Intersil 8007 and 8007A are short circuit protected. They require no external components for frequency compensation because the internal 6 dB/roll-off insures stability in closed loop applications. A unique bootstrap circuit insures unusually good common mode rejection for a JFET input op-amp and prevents large input currents as seen in some amplifiers at high common mode voltage.

FEATURES

- Ultra Low Input Current
- High Slew Rate — $6V/\mu s$
- Wide Input Common Mode Voltage
- 1MHz Band Width
- Excellent Stability
- Ideal for Unity Gain Applications

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8007CTY ICL8007ACTV	0°C to +70°C	8 LEAD TO-99 METAL CAN
ICL8007MTY ICL8007AMTV	-55°C to +125°C	



ICL8007 pin 4 connected to case (TY package)
ICL8007A pin 8 connected to case (TV package)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	± 30V
Input Voltage (Note 2)	± 15V
Storage Temperature Range	-65°C to +150°C

Operating Temperature Range	
8007M, 8007AM	-55°C to +125°C
8007C, 8007AC	0°C to +70°C
Lead Temperature (Soldering, 10sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

NOTES:

- Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
- For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- For Design only, not 100% tested.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

Characteristics	Test Conditions	8007M			8007C			8007AM & 8007AC			Units	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
The following specifications apply for T_A = 25°C:												
Input Offset Voltage	R _S ≤ 100kΩ		10	20		20	50		15	30	mV	
Input Offset Current			0.5			0.5			0.2		pA	
Input Bias Current (either input)			2.0	20		3.0	50		0.5	4.0	pA	
Input Resistance			10 ⁶			10 ⁶			10 ⁶		MΩ	
Input Capacitance			2.0			2.0			2.0		pF	
Large Signal Voltage Gain	R _L ≥ 2kΩ, V _{OUT} = ±10V	50,000			20,000			20,000			V/V	
Output Resistance			75			75			75		Ω	
Output Short-Circuit Current			25			25			25		mA	
Supply Current			3.4	5.2		3.4	6.0		3.4	6.0	mA	
Power Consumption			102	156		102	180		102	180	mW	
Slew Rate			6.0			6.0		2.5	6.0		V/μs	
Unity Gain Bandwidth			1.0			1.0			1.0		MHz	
Risetime	C _L ≤ 100pF, R _L = 2kΩ		300			300			300		ns	
Overshoot	C _L ≤ 100pF, R _L = 2kΩ		10			10			10		%	
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8007C and 8007AC), and -55°C ≤ T_A ≤ +125°C (8007M and 8007AM):												
Input Voltage Range			±10	±12		±10	±12		±10	±12	V	
Common Mode Rejection Ratio			70	90		70	90		86	95	dB	
Supply Voltage Rejection Ratio				70	300		70	600		70	200	μV/V
Large Signal Voltage Gain			25,000			15,000			15,000		V/V	
Output Voltage Swing	R _L ≥ 10kΩ R _L ≥ 2kΩ		±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13	V V	
Input Bias Current (either input)	T _A = +125°C T _A = +70°C			2.0			50		1.0 30		nA pA	
Average Temperature Coefficient of Input Offset Voltage	(Note 4)			75			75			50	μV/°C	

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NOTE: All typical values have been characterized but are not tested.

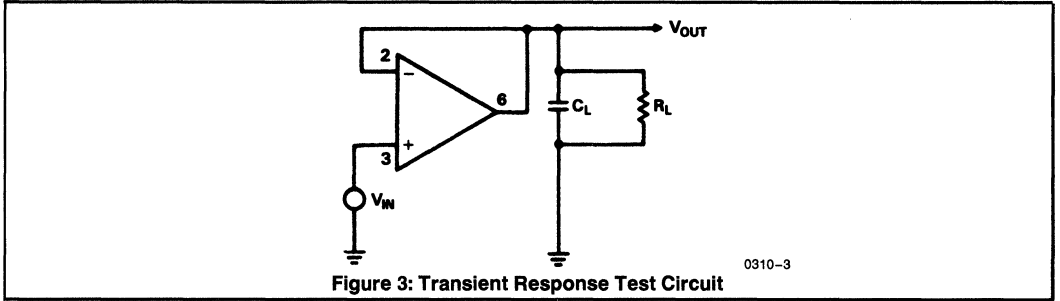
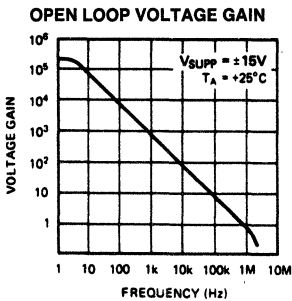
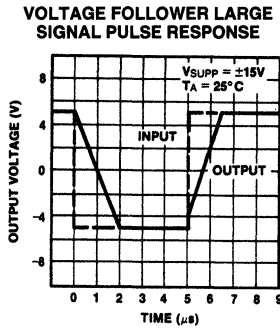


Figure 3: Transient Response Test Circuit

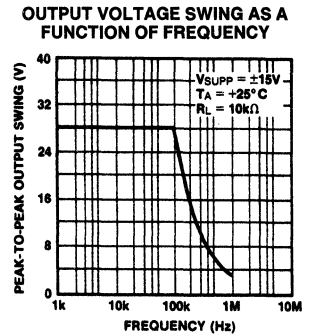
TYPICAL PERFORMANCE CHARACTERISTICS



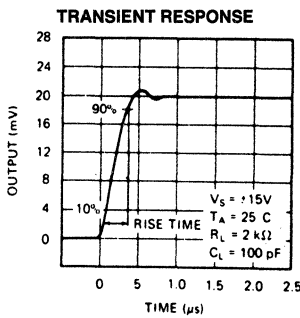
0310-4



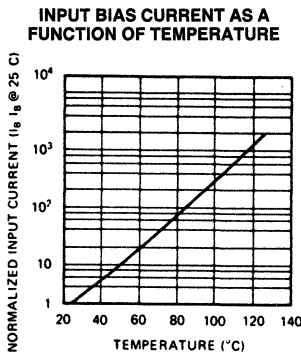
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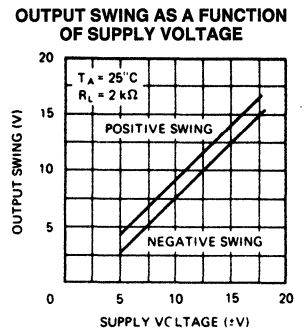
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0310-7



0310-8



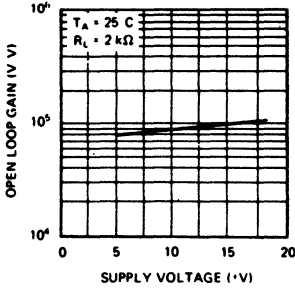
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NOTE: All typical values have been characterized but are not tested.

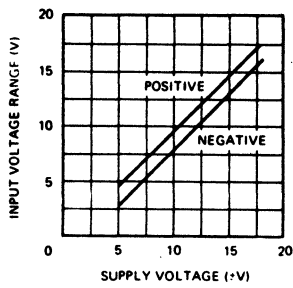
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



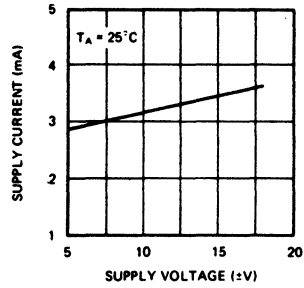
0310-10

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



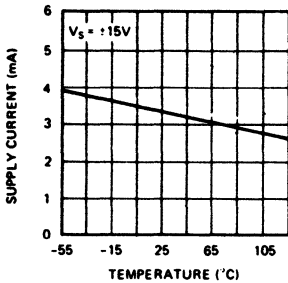
0310-11

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



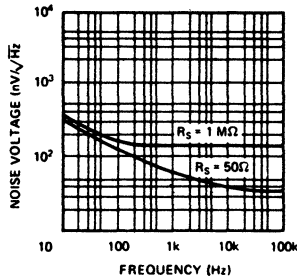
0310-12

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



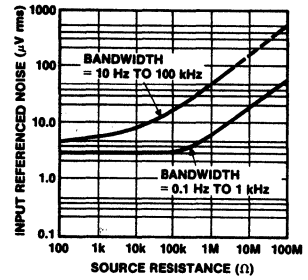
0310-13

INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



0310-14

WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



0310-15

For additional information, see Application Note A005.

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NOTE: All typical values have been characterized but are not tested.

ICL8021/ICL8023

Low Power Bipolar Operational Amplifier



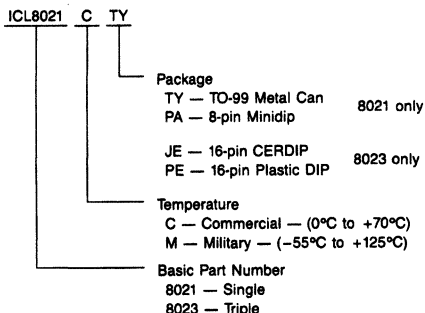
GENERAL DESCRIPTION

The Intersil ICL8021 series are low power operational amplifiers specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 series can be tailored to a particular application by adjusting an external resistor, R_{SET} , which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

Other features of the 8021 series include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

The Intersil 8023 consists of three low power operational amplifiers in a single 16-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET} , which controls the quiescent current of that amplifier.

ORDERING INFORMATION



0311-20

FEATURES

- $V_{OS} = 3mV$ Max (Adjustable to Zero)
- $\pm 1.5V$ to $\pm 18V$ Power Supply Operation
- Power Consumption — $20\mu W$ @ $\pm 1V$
- Input Bias Current — $30nA$ Max
- Internal Compensation
- Pin-For-Pin Compatible With 741
- Short Circuit Protected

Part Number	Temperature Range	Package
ICL8021CJA	0°C to 70°C	8 Lead CERDIP
ICL8021CBA	0°C to 70°C	8 Lead S.O.I.C
ICL8021CPA	0°C to 70°C	8 Lead MINIDIP
ICL8021CTY	0°C to 70°C	8 Lead Metal Can
ICL8021MJA	-55°C to +125°C	8 Lead CERDIP
ICL8021MTY*	-55°C to +125°C	8 Lead Metal Can
ICL8023CJE	0°C to 70°C	16 Lead CERDIP
ICL8023CPE	0°C to 70°C	16 Lead MINIDIP
ICL8023MJE*	-55°C to +125°C	16 Lead CERDIP

*Add /88313 to Part Number if 883B processing is required.

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

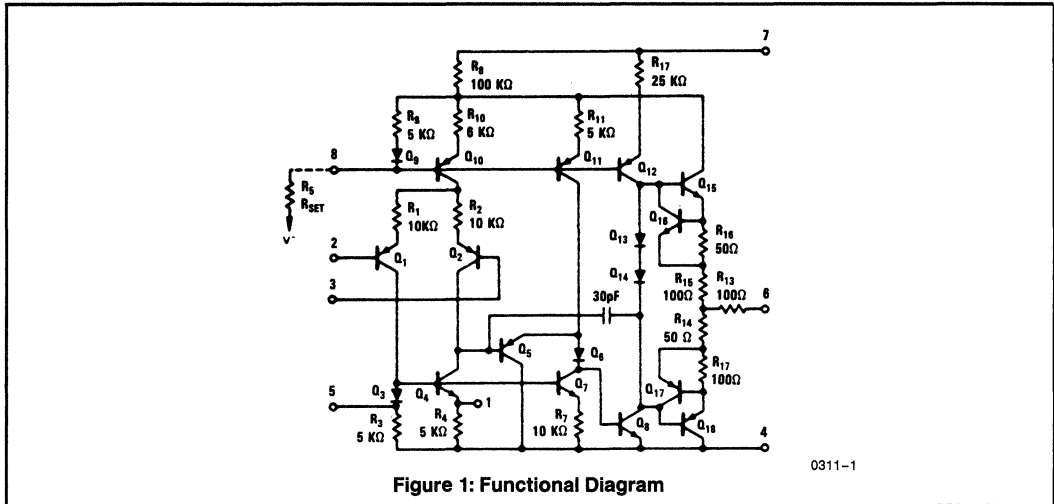
Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Indefinite
Power Dissipation (Note 2)	300mW

Operating Temperature Range	
8021M/8023M	-55°C to +125°C
8021C/8023C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

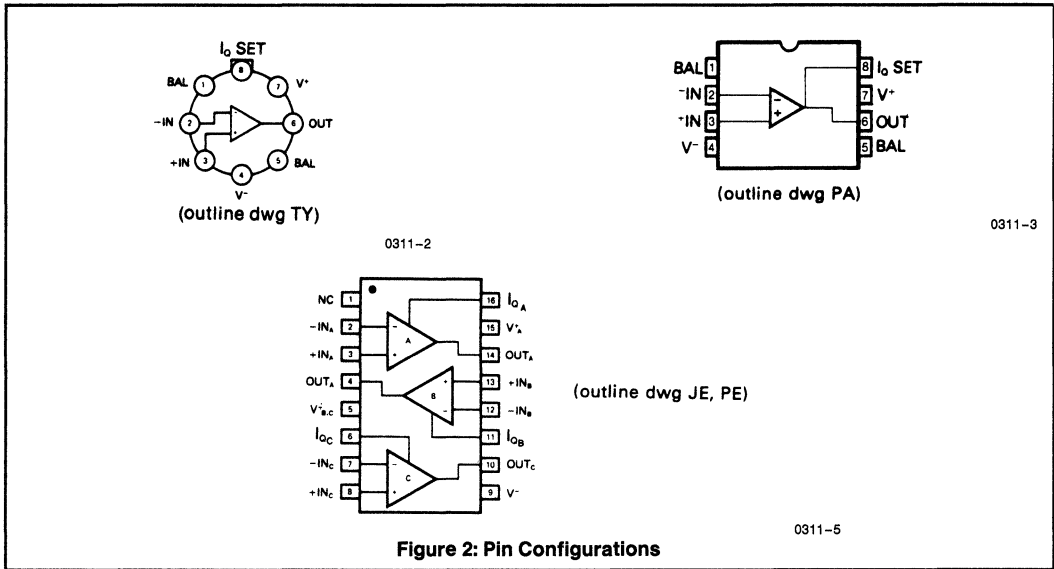
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

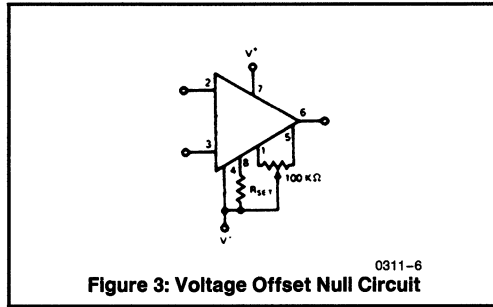


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NOTE: All typical values have been characterized but are not tested.



ELECTRICAL CHARACTERISTICS ($V_{SUPPLY} = \pm 6V$, $I_Q = 30\mu A$, unless otherwise specified.)

Characteristics	Test Conditions	8021M			8021C			Units
		Min	Typ	Max	Min	Typ	Max	
The following specifications apply for $T_A = 25^\circ C$:								
Input Offset Voltage	$R_S \leq 100k\Omega$		2	3		2	6	mV
Input Offset Current			0.5	7.5		0.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance		3	10		3	10		MΩ
Input Voltage Range	$V_{SUPPLY} = \pm 15V$	± 12	± 13		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	$\mu V/V$
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20k\Omega$, $V_{SUPPLY} = \pm 15V$	± 12	± 14		± 12	± 14		V
	$R_L \geq 10k\Omega$, $V_{SUPPLY} = \pm 15V$	± 11	± 13		± 11	± 13		V
Output Short-Circuit Current			± 13			± 13		mA
Power Consumption	$V_{OUT} = 0$		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/ μs
Unity Gain Bandwidth	$R_L = 20k\Omega$, $V_{IN} = 20mV$		270			270		kHz
Transient Response (Unity Gain)	$R_L = 20k\Omega$, $V_{IN} = 20mV$	Risetime		1.3			1.3	μs
		Overshoot		10			10	%
Specifications Applicable over Temperature		$-55^\circ C \leq T_A \leq +125^\circ C$			$0^\circ C \leq T_A \leq +70^\circ C$			
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	7.5	mV
Input Offset Current			1.0	11		1.5	15	nA
Input Bias Current			10	32		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10k\Omega$		5			5		$\mu V/^\circ C$
Average Temperature Coefficient of Input Offset Current			1.7			0.8		$pA/^\circ C$
Large Signal Voltage Gain	$R_L = 10k\Omega$	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	± 10	± 13		± 10	± 13		V

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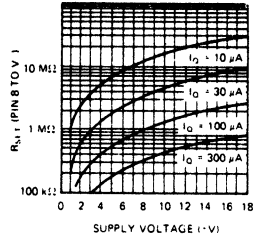
NOTE: All typical values have been characterized but are not tested.

QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 to V⁻)

V _S	I _Q			
	10 μA	30 μA	100 μA	300 μA
± 1.5	1.5MΩ	470kΩ	150kΩ	—
± 3	3.3MΩ	1.1MΩ	330kΩ	100kΩ
± 6	7.5MΩ	2.7MΩ	750kΩ	220kΩ
± 9	13MΩ	4MΩ	1.3MΩ	350kΩ
± 12	18MΩ	5.6MΩ	1.5MΩ	510kΩ
± 15	22MΩ	7.5MΩ	2.2MΩ	620kΩ

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 to V⁻)

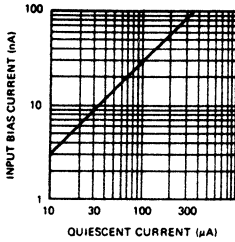


0311-7

TYPICAL PERFORMANCE CHARACTERISTICS*

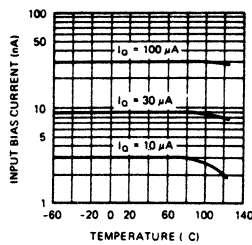
(T_A = +25°C, V_S = ±6V, I_Q = 30 μA unless otherwise specified.)

INPUT BIAS CURRENT VS QUIESCENT CURRENT



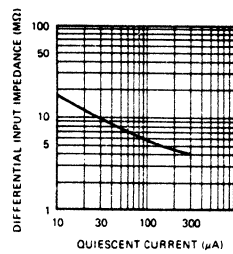
0311-8

INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



0311-9

DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT



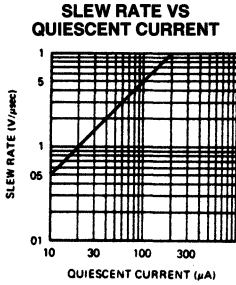
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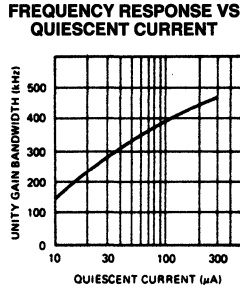
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS*

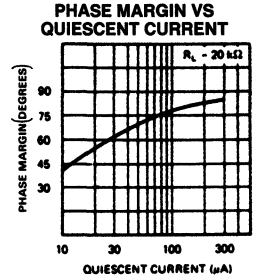
($T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $I_Q = 30\mu\text{A}$ unless otherwise specified.) (Continued)



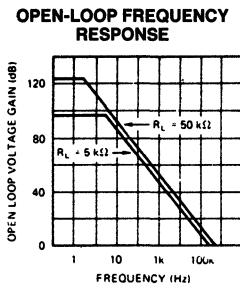
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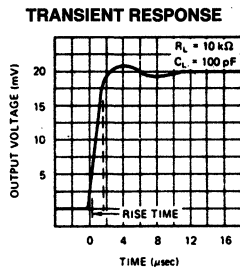
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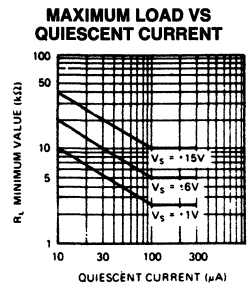
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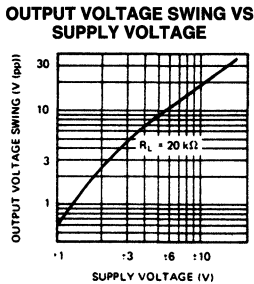
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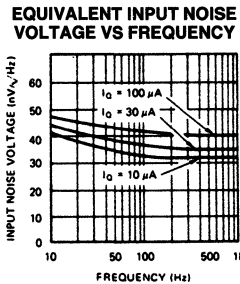
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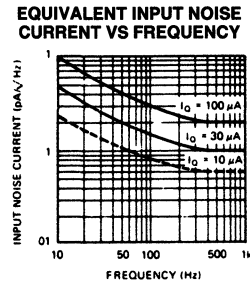
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0311-17



0311-18



0311-19

*ICL8021C guaranteed only for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$

NOTE: All typical values have been characterized but are not tested.

ICL8043

Dual JFET Input Operational Amplifier



ICL8043

GENERAL DESCRIPTION

The ICL8043 contains two FET input op amps, each similar in performance to the ICL8007. The inputs and outputs are fully short circuit protected, and no latch-up problems exist. Offset nulling is accomplished by using a single pot (for each amplifier) connected to the positive supply voltage. The devices have excellent common mode rejection.

FEATURES

- Very Low Input Current — 2pA Typical
- High Slew Rate — 6V/μs
- Internal Frequency Compensation
- Low Power Dissipation — 135mW Typical
- Monolithic Construction

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8043MJE	-55°C to 125°C	CERAMIC 16 Pin DIP
ICL8043CJE	0°C to 70°C	CERAMIC 16 Pin DIP

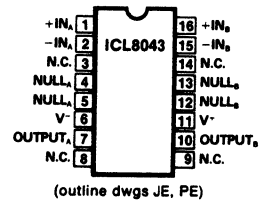
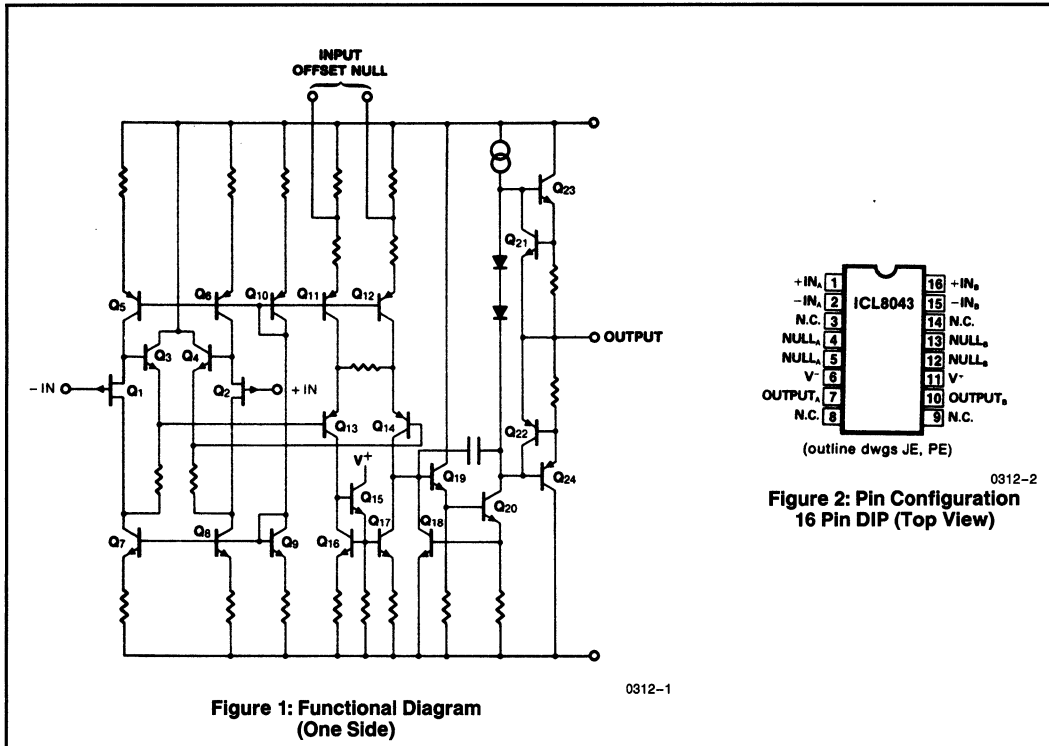


Figure 2: Pin Configuration 16 Pin DIP (Top View)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	± 30V
Input Voltage (Note 2)	± 15V
Voltage between Offset Null and V ⁺	± 0.5V
Storage Temperature Range	-65°C to +150°C

Operating Temperature Range	
8043M	-55°C to +125°C
8043C	0°C to +70°C
Lead Temperature (Soldering, 10sec)	300°C
Output Short-Circuit Duration	Indefinite

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- NOTES:** 1. Rating applies for case temperatures to 125°C; derate linearly at 9mW/°C for ambient temperatures above +95°C.
 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

Symbol	Characteristic	Test Conditions	8043M			8043C			Units	
			Min	Typ	Max	Min	Typ	Max		
The following specifications apply for T_A = 25°C:										
V _{OS}	Input Offset Voltage	R _S < 100kΩ		10	20		20	50	mV	
I _{OS}	Input Offset Current			0.5			0.5		pA	
I _{IN}	Input Current (either input)			2.0	20		3.0	50	pA	
R _{IN}	Input Resistance			10 ⁶			10 ⁶		MΩ	
C _{IN}	Input Capacitance			2.0			2.0		pF	
A _V	Large Signal Voltage Gain	R _L > 2kΩ, V _{out} = ±10V	50,000				20,000		V/V	
R _O	Output Resistance			75			75		Ω	
I _{SC}	Output Short-Circuit Current			25			25		mA	
I _{SUPPLY}	Supply Current (Total)			4.5	6		4.5	6.8	mA	
P _{DISS}	Power Consumption			135	180		135	204	mW	
SR	Slew Rate			6.0			6.0		V/μs	
GBW	Unity Gain Bandwidth			1.0			1.0		MHz	
t _r	Transient Response (Unity Gain)	C _L < 100pF, R _L = 2kΩ								
	Risetime			300			300		ns	
	Overshoot			10			10		%	
The following specifications apply for 0°C < T_A < +70°C (8043C), -55°C < T_A < +125°C (8043M):										
ΔV _{IN}	Input Voltage Range			± 10	± 12		± 10	± 12	V	
CMRR	Common Mode Rejection Ratio			70	90		70	90	dB	
PSRR	Supply Voltage Rejection Ratio				70	300		70	600	μV/V
A _V	Large Signal Voltage Gain			25,000			15,000		V/V	
ΔV _O	Output Voltage Swing	R _L > 10kΩ		± 12	± 14		± 12	± 14	V	
		R _L > 2kΩ		± 10	± 13		± 10	± 13	V	
V _{OS}	Input Offset Voltage			15	30		30	60	mV	
I _{IN}	Input Current (either input)	T _A = +125°C		2.0	15				nA	
		T _A = +70°C					50	175	pA	
ΔV _{OS} /ΔT	Average Temperature Coefficient of Input Offset Voltage	(Note 3)		75			75		μV/°C	

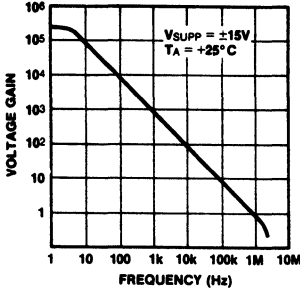
NOTE: 3. For Design only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

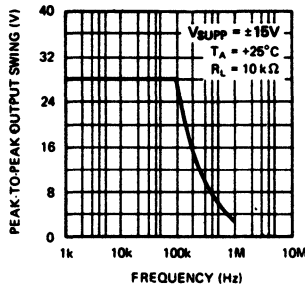
TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



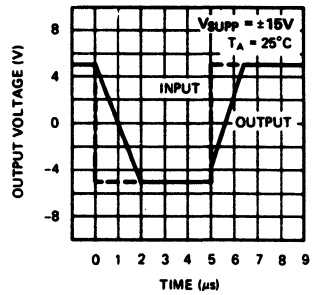
0312-3

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



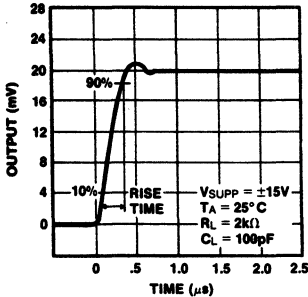
0312-4

VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



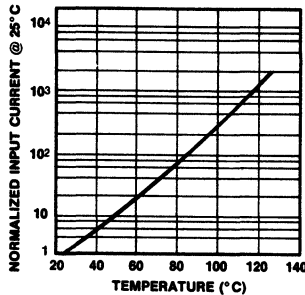
0312-5

TRANSIENT RESPONSE



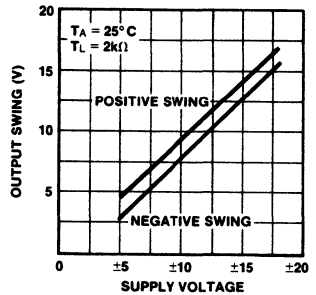
0312-6

INPUT CURRENT AS A FUNCTION OF TEMPERATURE



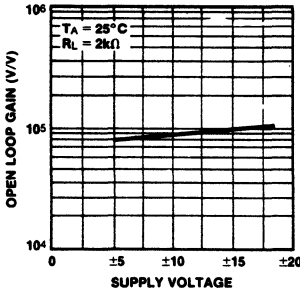
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OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE



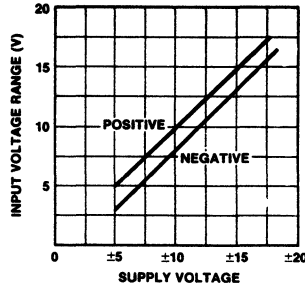
0312-8

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



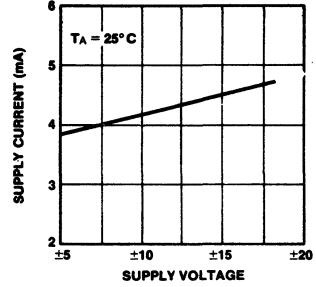
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INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



0312-10

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

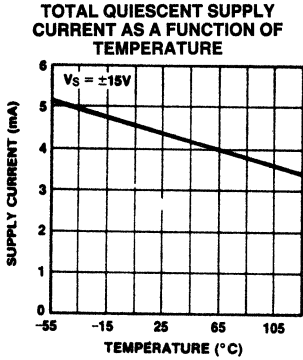


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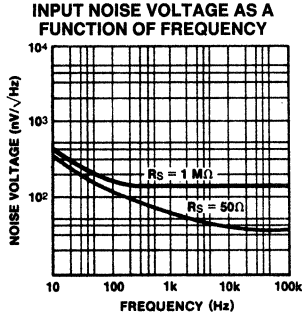
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NOTE: All typical values have been characterized but are not tested.

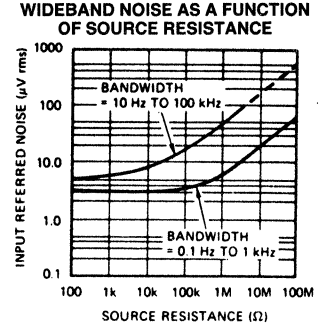
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



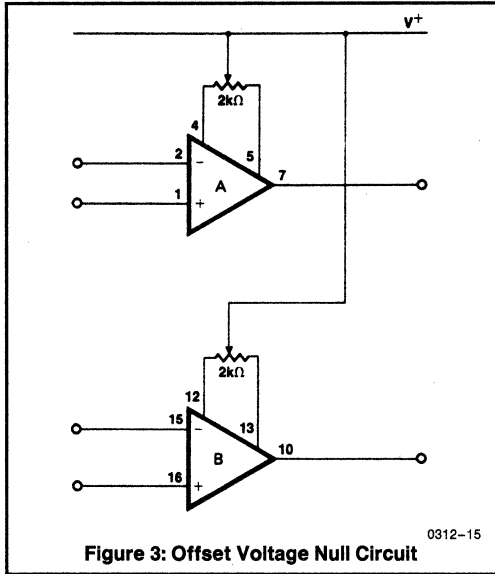
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0312-13



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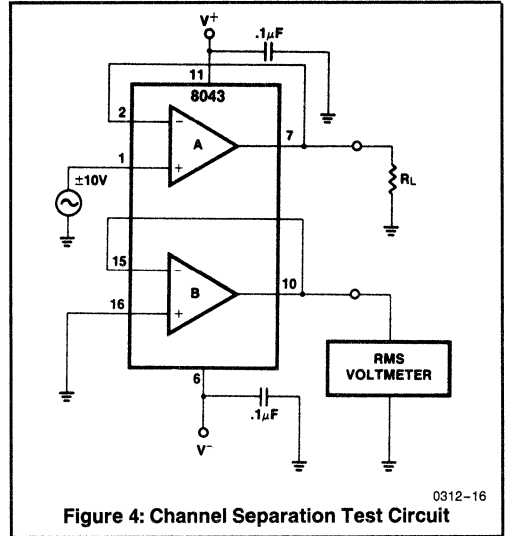


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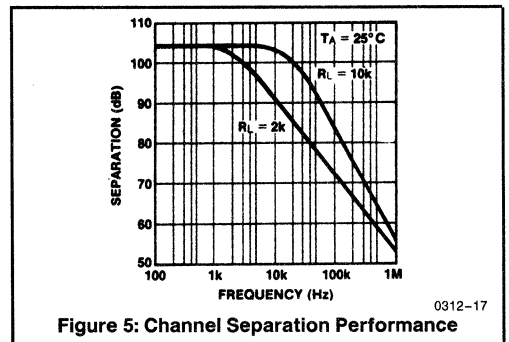
CHANNEL SEPARATION

Channel separation or crosstalk is measured using the circuit of Figure 4. One amplifier is driven so that its output swings ±10V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Figure 5.

$$\text{Channel Separation} = 20 \log \left(\frac{V_{\text{OUT}}(A)}{V_{\text{IN}}(B)} \right)$$



0312-16



0312-17

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

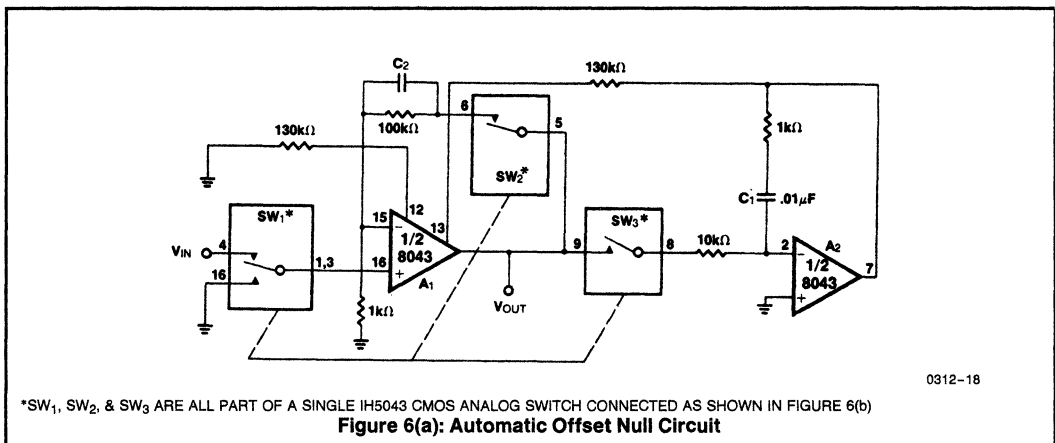
Applications for any dual amplifier fall into two categories. There are those which use the two-in-one package concept simply to save circuit-board space and cost, but more interesting are those circuits where the two sides of the dual are used to complement one another in a subsystem application. The circuits which follow have been selected on this basis.

AUTOMATIC OFFSET SUPPRESSION CIRCUIT

The circuit shown in Figure 6 uses one amplifier (A_1) as a normal gain stage, while the other (A_2) forms part of an offset voltage zeroing loop. There are two modes of operation which occur sequentially. First, an offset null correction mode occurs during which the offset voltage of A_1 is nulled

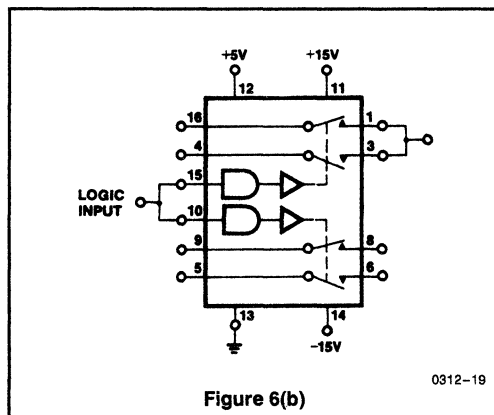
out. Following this nulling operation, A_1 is used as a normal amplifier while the voltage necessary to zero its offset voltage is stored on the integrator comprised of A_2 and C_1 .

The advantage of this circuit is that it allows chopper amplifier performance to be achieved at one-tenth the cost. The only limitation is that during the offset nulling mode, A_1 is disconnected from the input. However, in most data acquisition systems, many inputs are scanned sequentially. It is fairly simple to synchronize the offset nulling operation so that it does not occur when that particular amplifier is being "looked at". For the component values shown in Figure 3, and assuming a total leakage of 50pA at the inverting input of A_2 , the offset voltage referred to the input of A_1 will drift away from zero at only $40\mu\text{V}/\text{sec}$. Thus, the offset nulling information stored on C_1 can be "refreshed" relatively infrequently. The measured offset voltage of A_1 during the amplification mode was $11\mu\text{V}$; offset voltage drift with temperature was less than $0.1\mu\text{V}/^\circ\text{C}$.



0312-18

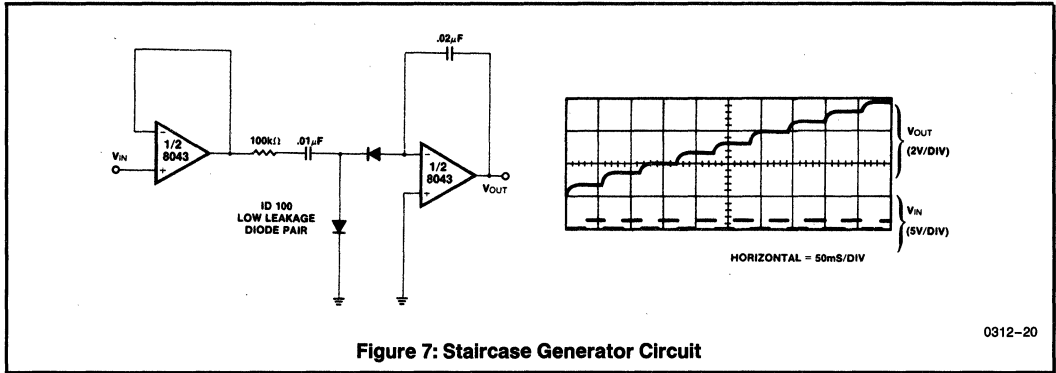
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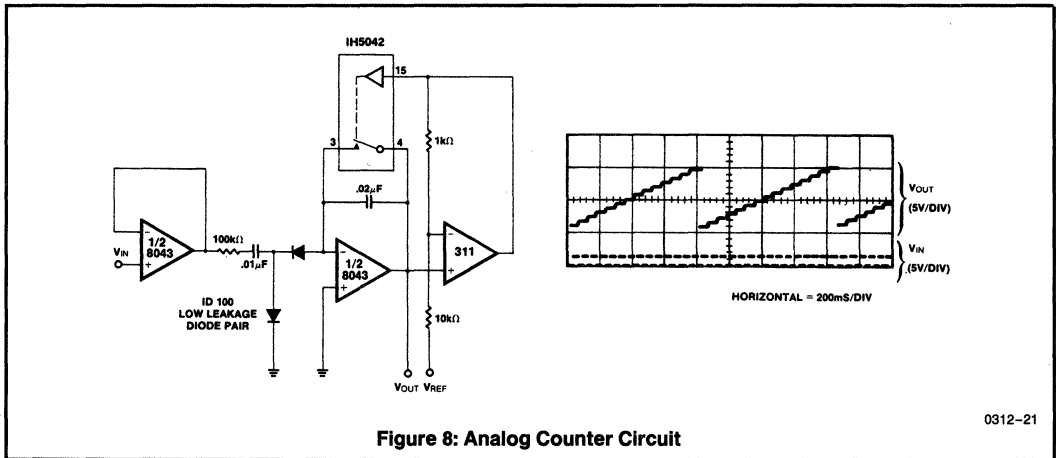
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NOTE: All typical values have been characterized but are not tested.



0312-20



0312-21

STAIRCASE GENERATOR

The circuit shown in Figure 7 is a high input impedance version of the so-called "diode pump" or staircase generator. Note that charge transfer takes place at the negative-going edge of the input-signal.

The most common application for staircase generators is in low cost counters. By resetting the capacitor when the output reaches a predetermined level, the circuit may be made to count reliably up to a maximum of about 10. A straightforward circuit using a LM311 for the level detector, and a CMOS analog gate to discharge the capacitor, is shown in Figure 8. An important property of this type of counter is the ease with which the count can be changed; it is only necessary to change the voltage at which the comparator trips. A low cost A-D converter can also be designed using the same principle since the digital count between reset periods is directly proportional to the analog voltage used as a reference for the comparator.

A considerable amount of hysteresis is used in the comparator shown in Figure 8. This ensures that the capacitor is completely discharged during the reset period. In a more sophisticated circuit, a dual comparator "window detector" could be used, the lower trip point set close to ground to

assure complete discharge. The upper trip point could then be adjusted independently to determine the pulse count.

SAMPLE & HOLD CIRCUIT

Two important properties of the 8043 are used to advantage in this circuit. The low input bias currents give rise to slow output decay rates ("droop") in the hold mode, while the high slew rate ($6V/\mu s$) improves the tracking speed and the response time of the circuit. See Figure 6.

The ability of the circuit to track fast moving inputs is shown in Figure 10A. The upper waveform is the input (10V/div), the lower waveform the output (5V/div). The logic input is high.

Actual sample and hold waveforms are shown in Figure 10B. The center waveform is the analog input, a ramp moving at about $67V/ms$, the lower waveform is the logic input to the sample & hold; a logic "1" initiates the sample mode. The upper waveform is the output, displaced by about 1 scope division (2V) from the input to avoid superimposing traces. The hold mode, during which the output remains constant, is clearly visible. At the beginning of a sample period, the output takes about $8\mu s$ to catch up with the input, after which it tracks until the next hold period.

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NOTE: All typical values have been characterized but are not tested.

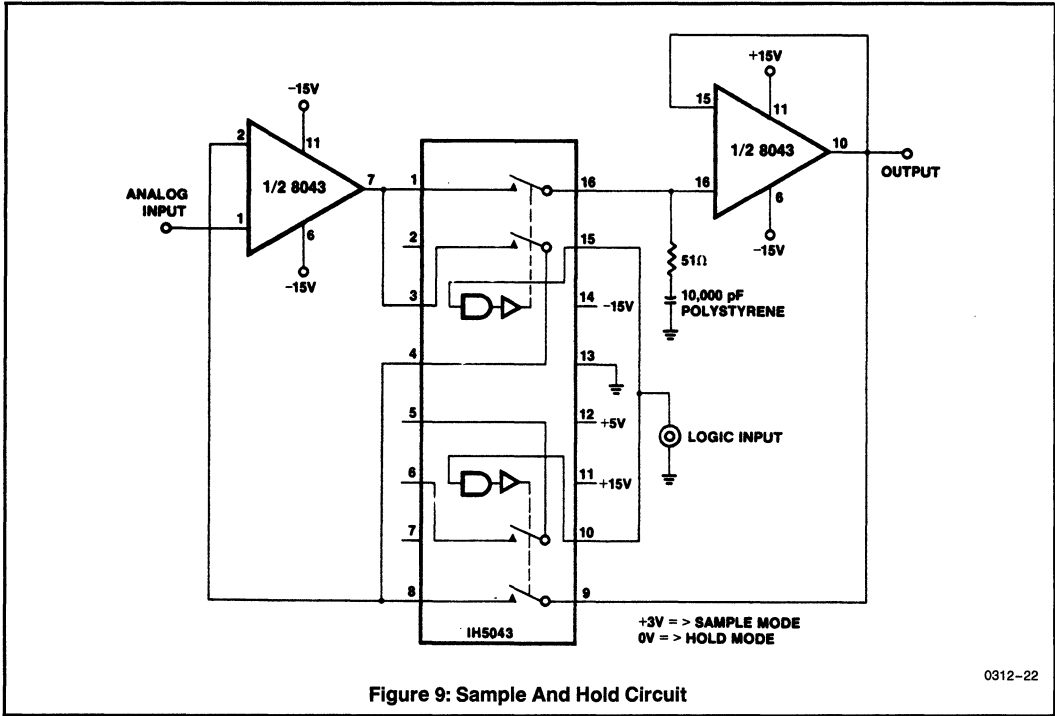
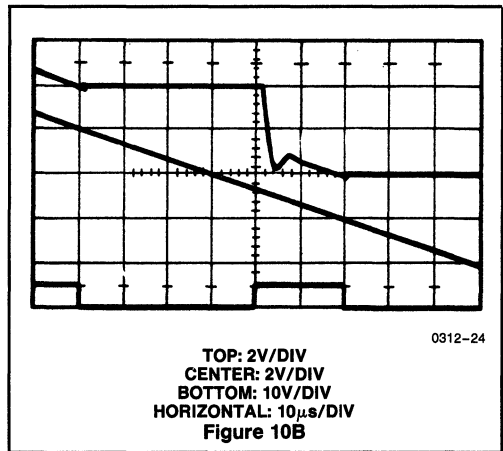
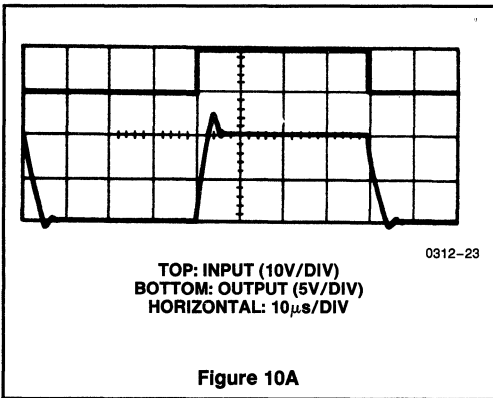


Figure 9: Sample And Hold Circuit



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NOTE: All typical values have been characterized but are not tested.

INSTRUMENTATION AMPLIFIER

A dual JFET-input operational amplifier is an attractive component around which to build an instrumentation amplifier because of the high input resistance. The circuit shown in Figure 11 uses the popular triple op-amp approach. The output amplifier is a High Speed 741 (741 HS, slew rate guaranteed $\geq 0.7V/\mu s$) so that the high slew rate of the 8043 is utilized to the full extent. Input resistance of the circuit (either input, regardless of gain configuration) is in excess of 10^{12} ohms.

For the component values shown, the overall amplifier gain is 200 (front end gain = $\frac{2R_1 + R_2}{R_2}$, back end gain, = R_6/R_4).

Common mode rejection is largely determined by the matching between R_4 and R_5 , and R_6 and R_7 . In applications where offset nulling is required, a single potentiometer can be connected as shown in Figure 12.

Another popular circuit is given in Figure 13. In this case the gain is $1 + R_1/R_2$, and the CMRR determined by the match between R_1 and R_4 , R_2 and R_3 .

For more information on FET input operational amplifiers, see Intersil Application Bulletin A005 "The 8007: A High Performance FET-input Operational Amplifier."

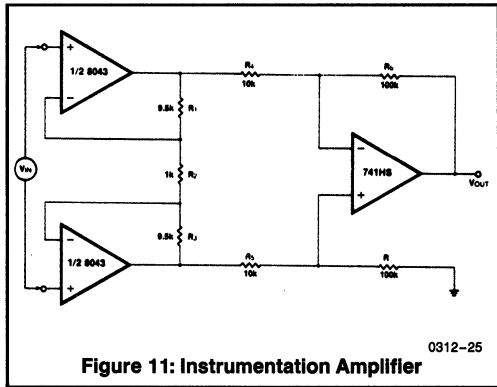


Figure 11: Instrumentation Amplifier

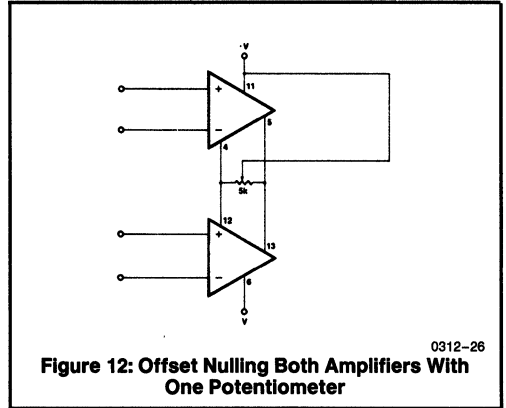


Figure 12: Offset Nulling Both Amplifiers With One Potentiometer

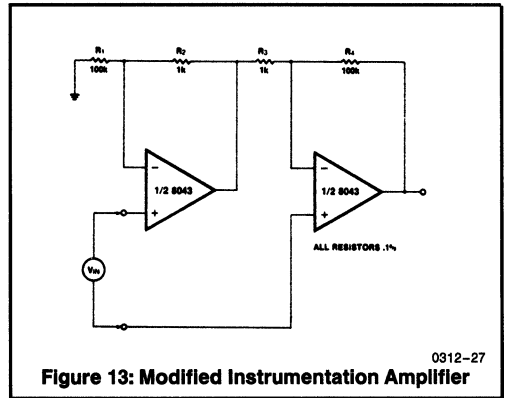


Figure 13: Modified Instrumentation Amplifier

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NOTE: All typical values have been characterized but are not tested.

ICL8063

Power Transistor Driver/Amplifier



ICL8063

GENERAL DESCRIPTION

The ICL8063 is a unique monolithic power transistor driver and amplifier that allows construction of minimum chip power amplifier systems. It includes built in safe operating area circuitry, short circuit protection and voltage regulators, and is primarily intended for driving complementary output stages.

Designed to operate with all varieties of operational amplifiers and other functions, two external power transistors, and 8 to 10 passive components, the ICL8063 is ideal for use in such applications as linear and rotary actuator drivers, stepper motor drivers, servo motor drivers, power supplies, power DACs and electronically controlled orifices.

The ICL8063 takes the output levels (typically $\pm 11V$) from an op amp and boosts them to $\pm 30V$ to drive power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 supply up to 100mA to the base leads of the external power transistors.

The amplifier-driver contains internal positive and negative regulators, to power an op amp or other device; thus, only $\pm 30V$ supplies are needed for a complete power amp.

FEATURES

- Converts $\pm 12V$ Outputs From Op Amps and Other Linear Devices to $\pm 30V$ Levels
- When Used In Conjunction With General-Purpose Op Amps and External Complementary Power Transistors, System Can Deliver > 50 Watts to External Loads
- Built-in Safe Area Protection and Short-Circuit Protection
- Produces 25mA Quiescent Current in Power Output Stage
- Built-in $\pm 13V$ Regulators to Power Op Amps or Other External Functions
- $500k\Omega$ Input Impedance With $R_{BIAS} = 1M\Omega$

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8063MJE	$-55^{\circ}C$ to $+125^{\circ}C$	CERDIP
ICL8063CJE	$0^{\circ}C$ to $+70^{\circ}C$	CERDIP
ICL8063CPE	$0^{\circ}C$ to $+70^{\circ}C$	PLASTIC DIP

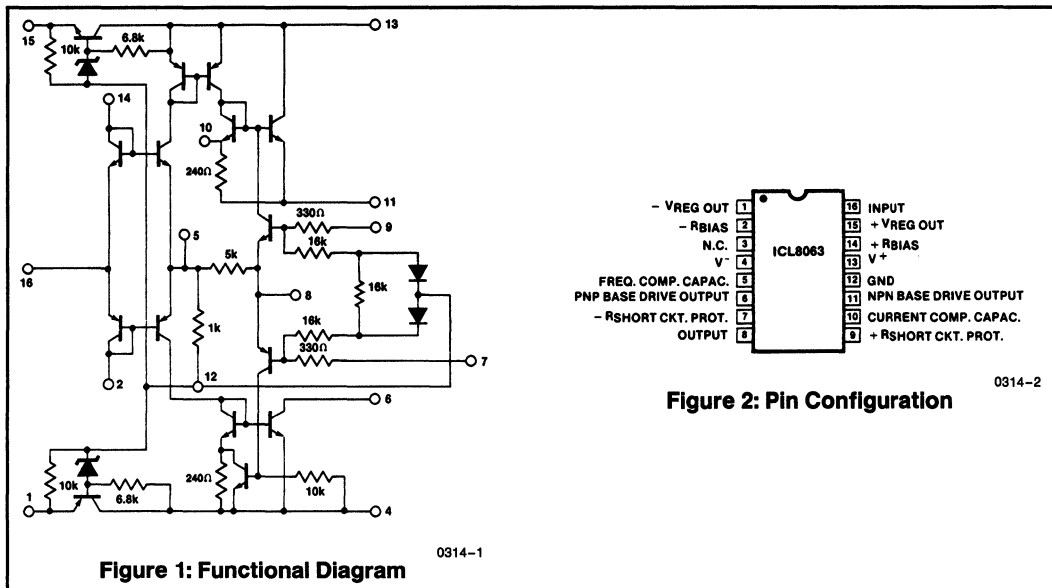


Figure 1: Functional Diagram

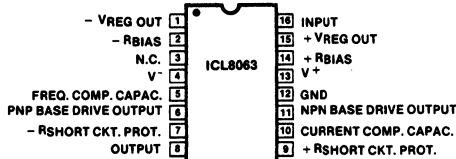


Figure 2: Pin Configuration

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 35V
Power Dissipation	500mW
Input Voltage (Note 1)	± 30V
Regulator Output Currents	10mA
Operating Temperature Range	
ICL8063MJE	-55°C to +125°C
ICL8063CPE	0°C to +70°C
ICL8063CJE	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{SUPPLY} = ±30V)

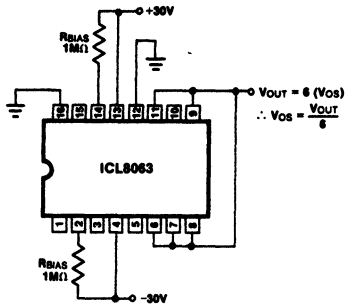
Symbol	Characteristic	Test Conditions	Min/Max Limits						Units
			ICL8063M			ICL8063C			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
V _{OS}	Max. Offset Voltage	See Figure 3	150	50	50		75		mV
I _{OH}	Min. Positive Drive Current	See Figure 4	50	50	50		40		mA
I _{OQ}	Max. Positive Output Quiescent Current	See Figure 5	500	250	250		300		μA
I _{OL}	Min. Negative Drive Current	See Figure 4	25	25	25		20		mA
I _{QL}	Max. Negative Output Quiescent Current	See Figure 6	500	250	250		300		μA
V _{REG}	Regulator Output Voltages Range		±13.7 ±1.2V	±13.7 ±1.0V	±13.7 ±1.5V	±13.7 ±1.0V	±13.7 ±1.0V	±13.7 ±1.0V	V
I _{REG}	Regulator Output Current	(See Note 2)	10	10			10		mA
Z _{IN}	A.C. Input Impedance	See Figure 8		400 (Typ)			400 (Typ)		kΩ
V _{SUPPLY}	Power Supply Range		±5 to ±35V						V
I _Q	Power Supply Quiescent Currents		10	6	6		7		mA
A _V	Range of Voltage Gain	See Figure 9 V _{IN} = 8Vp-p	6 ± 2	6 ± 2	6 ± 2		6 ± 2		V/V
V _{OUT(MIN)}	Minimum Output Swing	See Figure 9; Increase V _{IN} until V _{OUT} flattens	±27	±27	±27		±27		V
I _{BIAS}	Input Bias Current	See Figure 10	100	100	100		100		μA

NOTES: 1. For supply voltages less than ±30V the absolute maximum input voltage is equal to the supply voltage.
 2. Care should be taken to ensure that maximum power dissipation is not exceeded.

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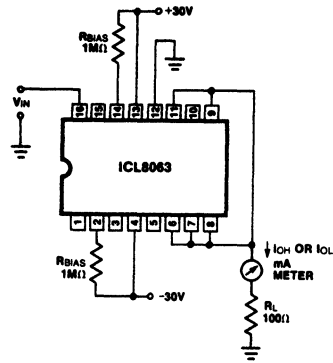
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



0314-3

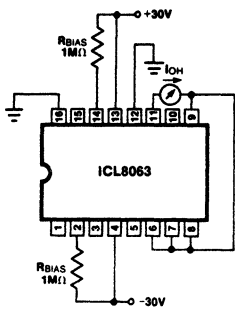
Figure 3: Offset Voltage Measurement



0314-4

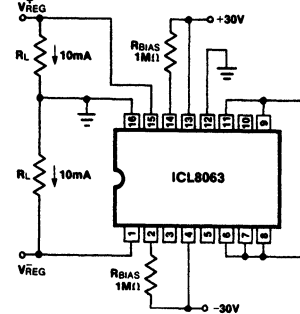
Figure 4: Output Current Measurement

FOR I_{OUT}: V_{IN} IS POSITIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS
 FOR I_{OUT}: V_{IN} IS NEGATIVE: INCREASE V_{IN} UNTIL I_{OUT} LIMITS



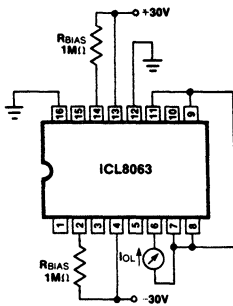
0314-5

Figure 5: Positive Output Quiescent Current



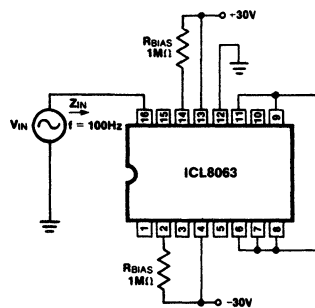
0314-7

Figure 7: On Chip Regulator Measurement



0314-6

Figure 6: Negative Output Quiescent Current



0314-8

Figure 8: A.C. Input Impedance Measurement

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NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS (Continued)

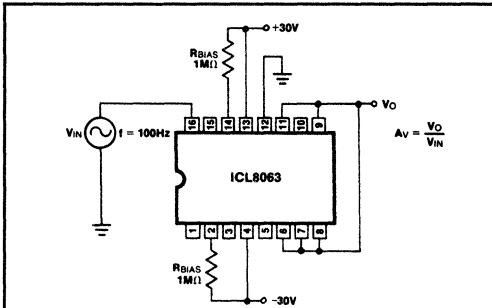


Figure 9: Gain and Output Voltage Swing Measurement

0314-9

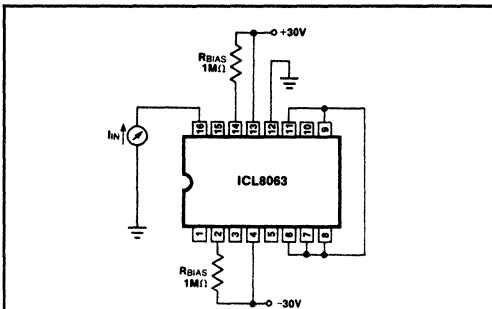


Figure 10: Input Bias Current Measurement

0314-10

APPLICATIONS INFORMATION

One problem faced almost every day by circuit designers is how to interface the low voltage, low current outputs of linear and digital devices to that of power transistors and darlingtonts.

For example, a low level op amp has a typical output voltage range of ± 6 to ± 12 V, and output current usually on the order of about 5 milliamperes. A power transistor with a ± 35 volt supply, a collector current of 5 amperes, and a beta, or gain of 100 needs at least 50 milliamperes of drive.

In the past, connecting two transistors with widely dissimilar requirements meant that a rather ornate discrete circuit had to be built to convert the weak output signals from the first into levels large enough to drive the second. However, in addition to converting voltage and current, it was also necessary to include a number of protection circuits to guard against damage from shorts, for example, and all this design work was both tedious and expensive.

The ICL8063 provides a solution to these problems. It's a monolithic power transistor driver and power transistor amplifier circuit on the same chip, has all the necessary safe operating area circuitry and short circuit protection, and has on-chip ± 13 V voltage regulators to eliminate the need for extra external power supplies.

Using the ICL8063 to make a complete Power Amplifier

As Figure 11 shows, using the ICL8063 allows the circuit designer to build a power amplifier block capable of delivering ± 2 amperes at ± 25 volts (50 watts) to any load, with only three additional discrete devices and 8 passive components. Moreover, the circuit draws only about ± 30 milliamperes of quiescent current from either of the ± 30 V power supplies. A similar design using discrete components would require anywhere from 50 to 100 components.

Slew rate is about the same as that of a 741 op amp, approximately $1V/\mu s$. Input current, voltage offset, CMRR and PSRR are also the same. Use of 1,000 picofarad compensation capacitors (three in this configuration) allows good stability down to unity gain non-inverting (the worst case). This circuit will drive a 1000pF C_L to Gnd, or in other words, the circuit can drive 30 feet of RG-58 coaxial cable for line driver applications with no problems.

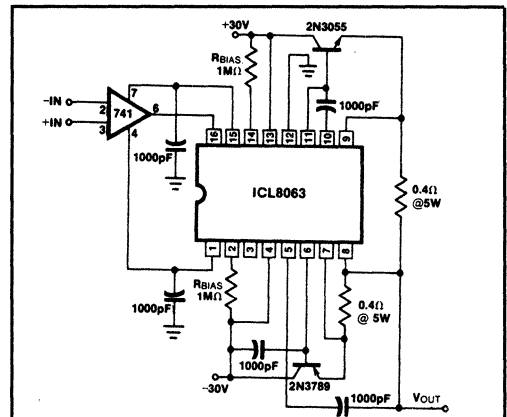


Figure 11: Standard Circuit Diagram

0314-11

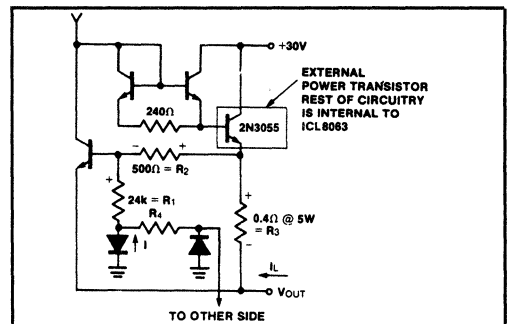


Figure 12: Current Limiting (Safe Area) Protection Circuit (one side shown)

0314-12

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NOTE: All typical values have been characterized but are not tested.

As Figure 12 indicates, setting up a current limiting (safe area) protection circuit is straightforward. The 0.4 ohm, 5 watt resistors set the maximum current one can get out of the output. The equation this SOA circuit follows is: for V_{OUT} positive,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2} (V_{OUT} + I_L R_3 - 0.7V)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2} (V_{OUT})$$

for V_{OUT} negative,

$$V_{be} = I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4} (V_{OUT} + I_2 R_3 + 0.7)$$

$$\approx I_L R_3 - \frac{R_2}{R_1 + R_2 + R_4} (V_{OUT})$$

Solving these equations we get the following:

V_{OUT}	I	I_L @ 25°C	I_L @ 125°C
24V	1mA	3 amps	2.4 amps
20V	830 μ A	2.8 amps	
16V	670 μ A	2.6 amps	
12V	500 μ A	2.4 amps	1.8 amps
8V	333 μ A	2.1 amps	
4V	167 μ A	1.9 amps	
0V	0 μ A	1.7 amps	1.1 amps

As this table indicates, maximum power delivered to a load is obtained when $V_{OUT} \geq 24V$.

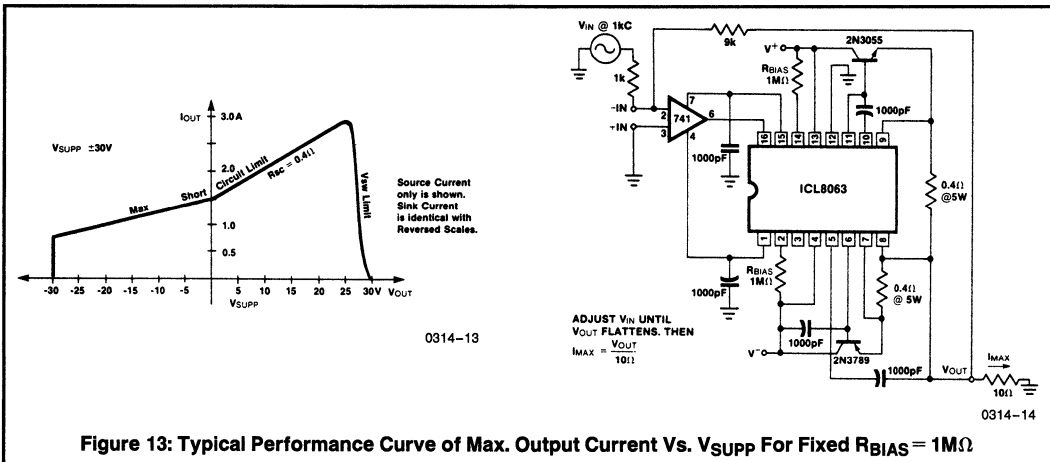
Often design requirements necessitate an unsymmetrical output current capability. In that case, instead of the 0.4 ohm resistors protecting the npn and pnp output stages, as shown in Figure 11, simply substitute any other value. For example, if up to 3 amps are required when $V_{OUT} \geq +24V$ and only 1 amp out when $V_{OUT} \geq -24V$, use a 0.4 ohm resistor between pin 8 and pin 9 on the ICL8063 and a 1 ohm, 2 watt resistor between pin 7 and pin 8. Maximum output current versus V_{OUT} for varying values of protection resistors are as follows:

V_{OUT}	0.4 Ω @ 25°C	0.68 Ω @ 25°C	1 Ω @ 25°C
24V	3 amps	1.7 amps	1.2 amps
12V	2.4 amps	1.4 amps	0.9 amps
0V	1.7 amps	1.0 amps	0.7 amps

The biasing resistors located between pin 13 and pin 14 and between pin 2 and pin 4 are typically 1m Ω for $V_{SUPPLY} = \pm 30V$, which guarantees adequate performance in such applications as DC motor drivers, power DACs, programmable power supplies and line drivers (with ± 30 volt supplies). The table that follows shows the proper value for R_{BIAS} for optimum output current capability with supply voltages between $\pm 5V$ and $\pm 30V$.

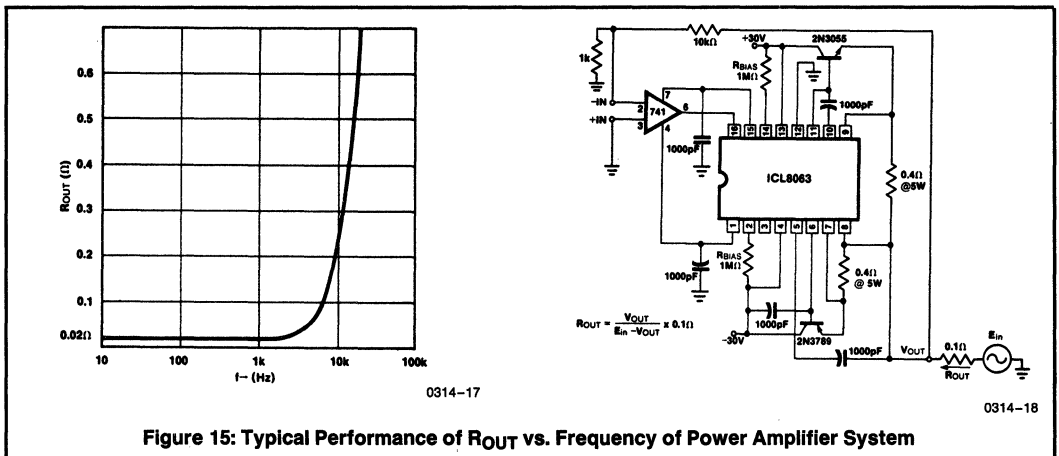
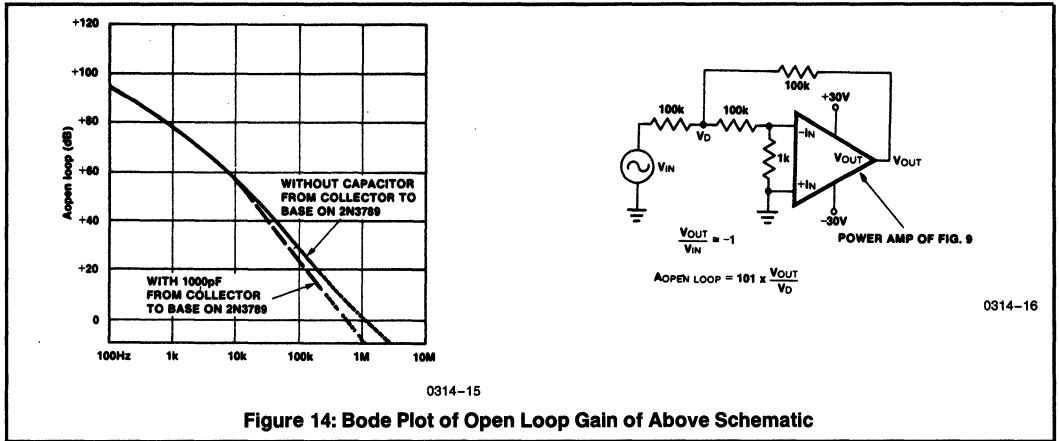
$\pm V_{CC}$	R_{BIAS}
30V	1 M Ω
25V	680k Ω
20V	500k Ω
15V	300k Ω
10V	150k Ω
5V	62k Ω

If 30V and 1M Ω are used, performance curves appear as shown in Figure 13.



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When buying external power transistors, careful attention should be paid to beta values. For 2N3055 and 2N3789 transistors used in this circuit, beta should be no more than 150 max at $I_C = 20\text{mA}$ and $V_{CE} = 30\text{V}$. This beta value sets the quiescent current at less than 30mA when not delivering power to a load.

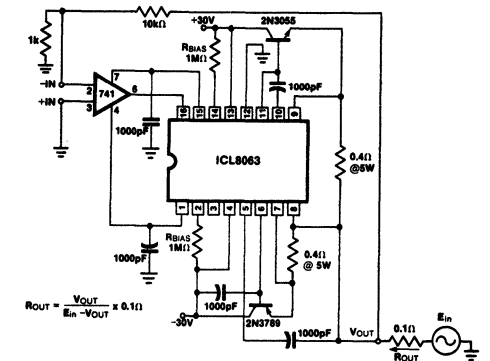
The design in Figure 11 will tolerate a short circuit to ground indefinitely, provided adequate heat sinking is used.

However if V_{OUT} is shunted to $\pm 30\text{V}$ the output transistors (2N3055 and 2N3789) will be destroyed, but since the safe operating area for these devices is 4 amps at 30 volts, the problem does not occur for $V_{SUPP} = \pm 15\text{V}$.

A typical bode plot of the power amplifier system open-loop frequency-response is shown in Figure 14. Referring to Figure 8, the schematic for this bode plot is shown in Figure 14.

Designing A Simple Function Generator

Using a variation of the fundamental power amplifier building block described in the previous section, the



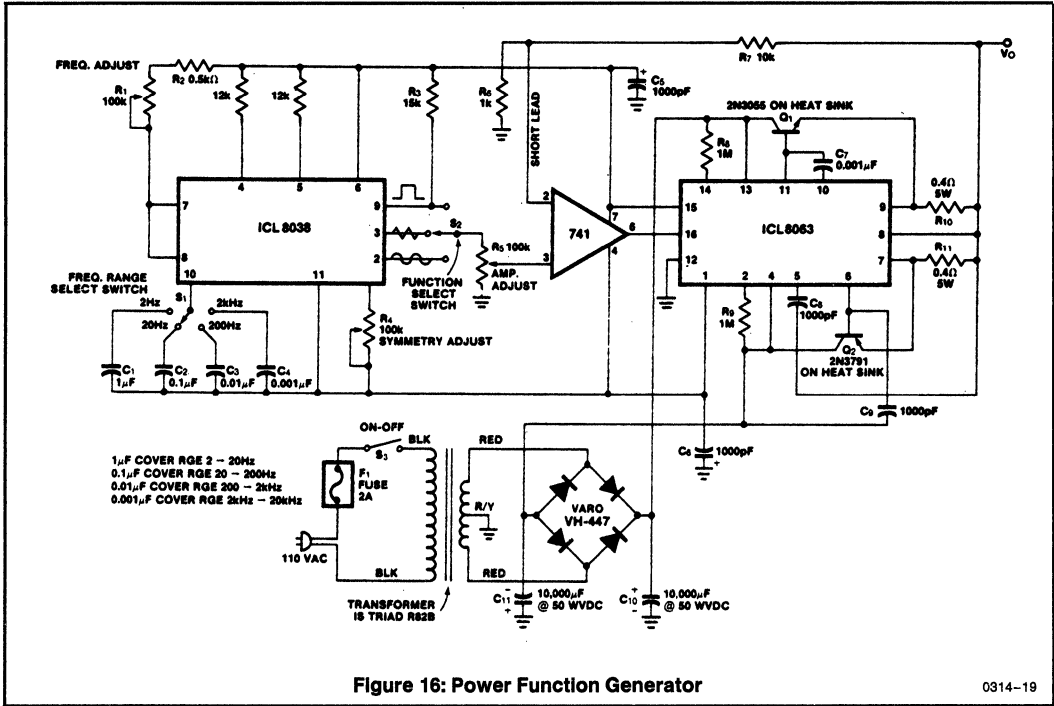
ICL8063 can be used in the design of a simple, low cost function generator (Figure 16). It will supply sine waves, triangular waves and square waves from 2 hertz to 20 kilohertz. This complete test instrument can be plugged into a standard 110VAC line for power. V_{OUT} will be up to $\pm 25\text{V}$ (50V p-p) across loads as small as 10 ohms (about 2.5 amps maximum output current).

Capacitor working voltages should be greater than 50V DC and all resistors should be $\frac{1}{2}\text{W}$, unless otherwise indicated. The interconnecting leads from the 741 pins 2 and 3 to their respective resistors should be kept short, less than 2 inches if possible; longer leads may result in oscillation.

Full output swing is possible to about 5kHz; after that the output begins to taper off due to the slew rate of the 741, until at 20kHz the output swing will be about $20V_{pp}$ ($\pm 10\text{V}$). This problem can be remedied by simply using an op amp with a higher slew rate, such as the LF356.

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NOTE: All typical values have been characterized but are not tested.



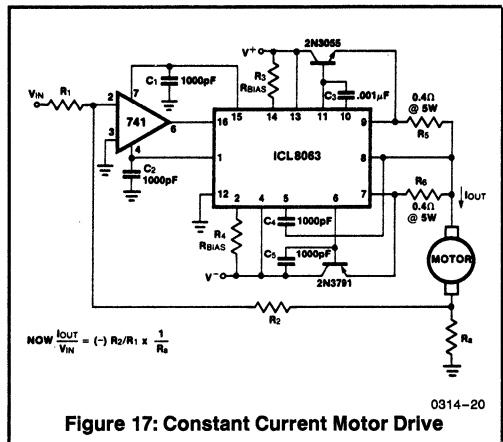
Building a Constant Current Motor Drive Circuit

The constant current motor drive configuration shown in Figure 17 is an extremely simple circuit to construct using the ICL8063. This minimum device circuit can be used to drive DC motors where there is some likelihood of stalling or lock up; if the motor locks, the current drive remains constant and the system does not destroy itself. Using this approach two 6V batteries are sufficient for good performance. A 10 volt input will produce one amp of output current to drive the motor, and if the motor is stalled, I_{OUT} remains at 1 amp.

For example, suppose it is necessary to drive a 24V DC motor with 1 amp of drive current. First make V_{SUPPLY} at least 6 volts more than the motor being driven (in this case 30 volts). Next select R_{BIAS} according to V_{SUPPLY} from the data sheet, which indicates $R_{BIAS} = 1M\Omega$. Then choose R_1 , R_2 , and R_a for optimum sensitivity. That means making $R_a = 1\Omega$ to minimize the voltage drop across R_a (the drop will be $1\text{ amp} \times 1\text{ ohm} = 1\text{ volt}$). If 1 amp/volt sensitivity is desirable let $R_2 = R_1 = 10k\Omega$ to minimize feedback current error. Then a $\pm 1V$ input voltage will produce a ± 1 amp current through the motor.

Capacitors should be at least 50 volts working voltage and all resistors $\frac{1}{2}W$, except for those valued at 0.4 ohms. Power across $R_a = I \times V = 1\text{ amp} \times 1\text{ volt} = 1\text{ watt}$, so at least a 2 watt value should be used. Use large heat sinks for the 2N3055 and 2N3791 power transistors. A Delta NC-641 or the equivalent is appropriate. Use a thermal compound when mounting the transistor to the heat sink. (See Intersil ICH8510 data sheet for further information).

7



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NOTE: All typical values have been characterized but are not tested.

Building A Low Cost 50 Watt per Channel Audio Amplifier

For about \$20 per channel, it is possible to build a high fidelity amplifier using the ICL8063 to drive 8 ohm speakers. A channel is defined here as all amplification between turntable or tape output and power output. (Figure 18)

The input 741 stage is a preamplifier with R.I.A.A. equalization for records. Following the first 741 stage is a 10kΩ control pot, whose wiper arm feeds into the power amplifier stage consisting of a second 741, the ICL8063 and the power transistors. To achieve good listening results, selection of proper resistance values in the power amplifier stage is important. Best listening is to be found at a gain value of 6 [(5kΩ + 1kΩ)/1kΩ = 6]. 3 is a practical minimum, since the first stage 741 preamp puts out only ±10 volt maximum signals, and if maximum power is necessary this value must be multiplied by 3 to get ±30 volt levels at the output of the power amp stage.

Each channel delivers about 56 volts p-p across an 8 ohm speaker and this converts to 50 watts RMS power. This is derived as follows:

$$\text{Power} = \frac{V_{\text{rms}}^2}{8 \text{ ohms}} \quad V_{\text{rms}} = \frac{56V_{\text{p-p}}}{2.82} = 20V, (20V)^2 = 400V^2$$

$$\therefore \text{Power} = \frac{400V^2}{8 \text{ ohms}} = 50 \text{ watts RMS Power.}$$

Distortion will be <0.1% up to about 100Hz, and then it increases as the frequency increases, reaching about 1% at 20kHz.

The ganged switch at the input is for either disc playing or FM, either from an FM tuner or a tape amplifier. Assuming DC coupling on the outputs, there is no need for a DC reference to ground (resistor) for FM position. To clear the signal in the FM position, place a 51kΩ resistor to ground as shown in Figure 18 (from FM input position to ground).

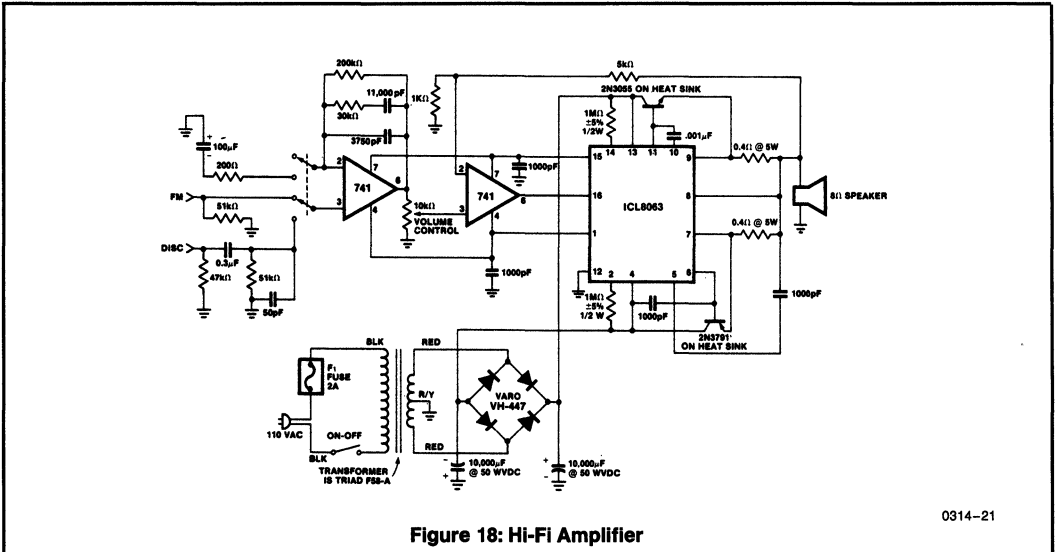
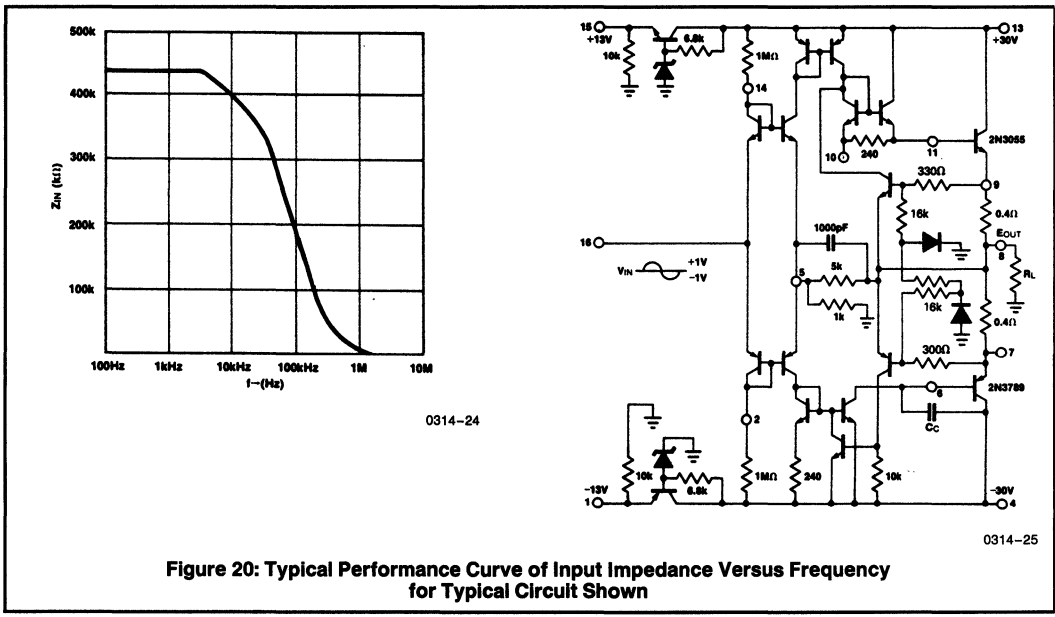
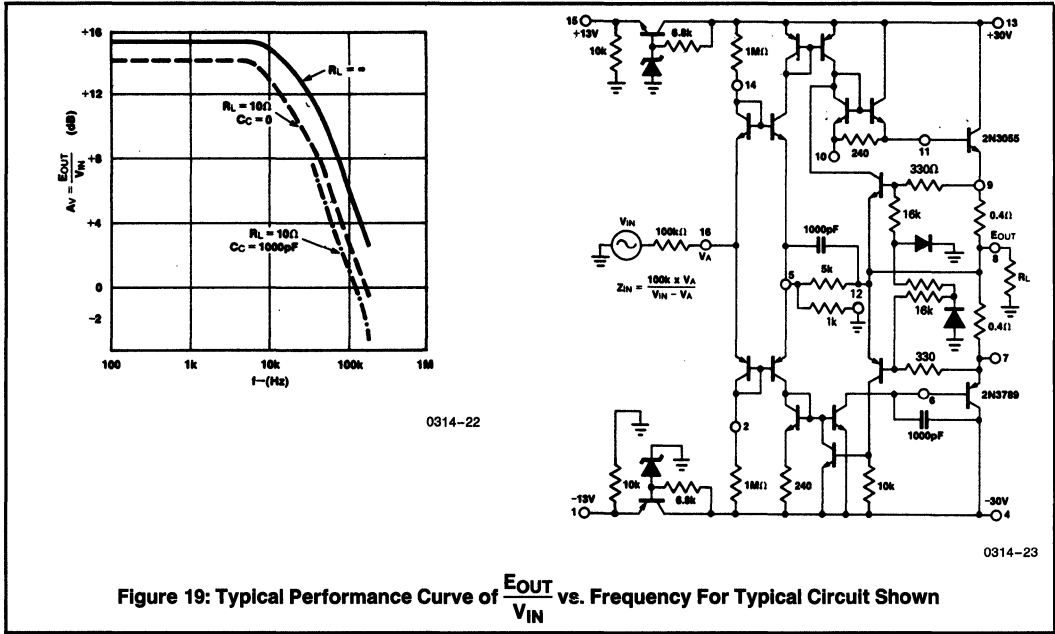


Figure 18: Hi-Fi Amplifier

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NOTE: All typical values have been characterized but are not tested.



Note: Intersil offers a hybrid power amplifier similar to that shown in Figure 11. See ICH8510/8520/8530 data sheet for details.

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NOTE: All typical values have been characterized but are not tested.

LM4250

Programmable Operational Amplifier



GENERAL DESCRIPTION

The 4250 is an extremely versatile programmable monolithic operational amplifier. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product.

The 4250C is guaranteed over a 0°C to 70°C temperature range.

RESISTOR BIASING

Set Current Setting Resistor to V^-

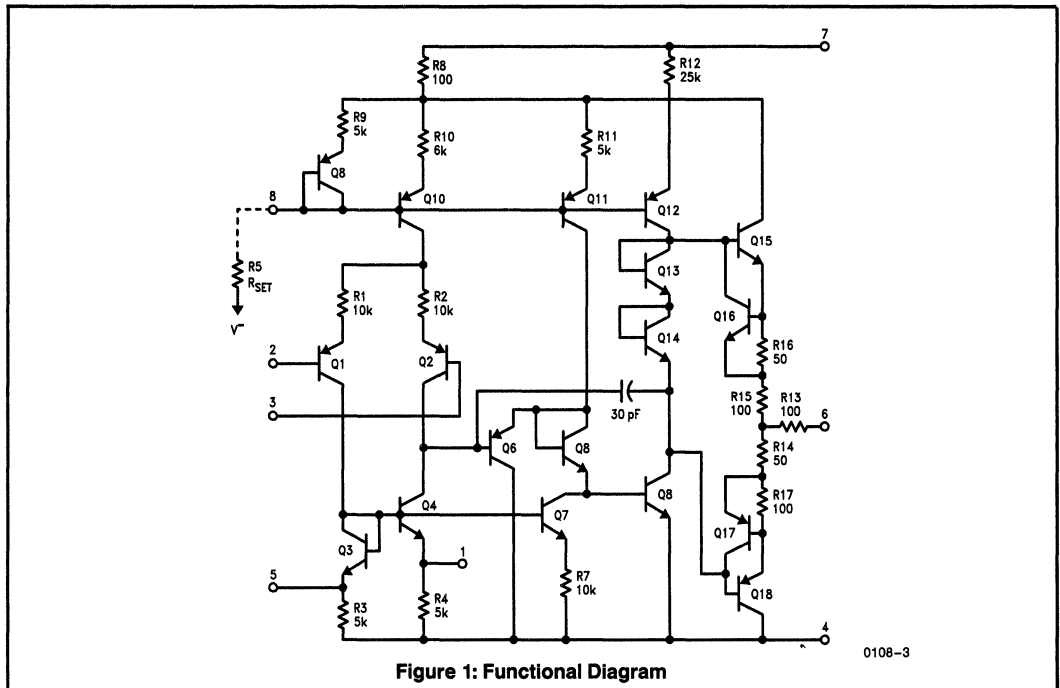
V_S	I_{SET}				
	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
$\pm 1.5V$	25.6 M Ω	5.04 M Ω	2.5 M Ω	492 k Ω	244 k Ω
$\pm 3.0V$	55.6 M Ω	11.0 M Ω	5.5 M Ω	1.09 M Ω	544 k Ω
$\pm 6.0V$	116 M Ω	23.0 M Ω	11.5 M Ω	2.29 M Ω	1.14 M Ω
$\pm 9.0V$	176 M Ω	35.0 M Ω	17.5 M Ω	3.49 M Ω	1.74 M Ω
$\pm 12.0V$	236 M Ω	47.0 M Ω	23.5 M Ω	4.69 M Ω	2.34 M Ω
$\pm 1.50V$	296 M Ω	59.0 M Ω	29.5 M Ω	5.89 M Ω	2.94 M Ω

FEATURES

- $\pm 1V$ to $\pm 18V$ Power Supply Operation
- 3 nA Input Offset Current
- Standby Power Consumption as Low as 500 nW
- No Frequency Compensation Required
- Programmable Electrical Characteristics
- Offset Voltage Nulling Capability
- Can be Powered by Two Flashlight Batteries
- Short Circuit Protection

ORDERING INFORMATION

Part Number	Temperature Range	Package
LM4250 CN	0°C to +70°C	8 Lead MINIDIP
LM4250 CJ	0°C to +70°C	8 Lead CERDIP
LM4250 CH	0°C to +70°C	TO-99 CAN
LM4250 J	-55°C to +125°C	8 Lead CERDIP
LM4250 H	-55°C to +125°C	TO-99 CAN



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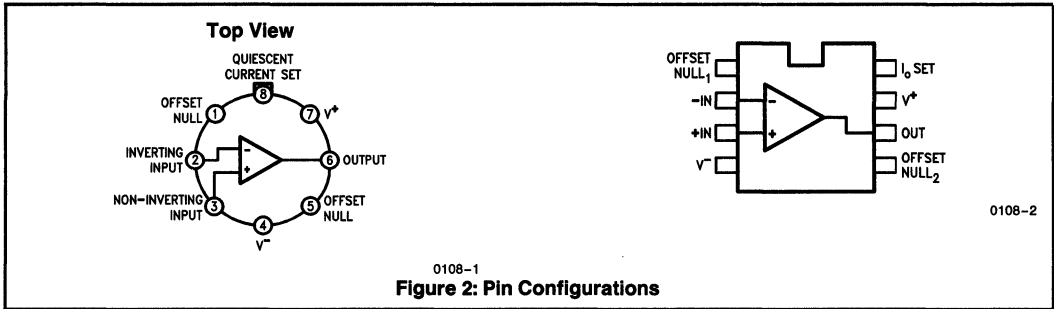
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
I _{SET} Current	150 μA
Operating Temperature Range	
LM4250C	0°C to +70°C
LM4250	-55°C to +125°C

Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C unless otherwise specified)

Parameters	Conditions	V _S = ±1.5V			
		I _{SET} = 1 μA		I _{SET} = 10 μA	
		Min	Max	Min	Max
V _{OS}	T _A = 25°C, R _S ≤ 100 kΩ		5 mV		6 mV
I _{OS}	T _A = 25°C		6 nA		20 nA
I _{bias}	T _A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	T _A = 25°C, R _L = 100 kΩ V _O = ±0.6V, R _L = 10 kΩ	25k		25k	
Supply Current	T _A = 25°C		8 μA		90 μA
Power Consumption	T _A = 25°C		24 μW		270 μW
V _{OS}	R _S ≤ 10 kΩ		6.5 mV		7.5 mV
I _{OS}			8 nA		25 nA
I _{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	V _O = ±0.6V, R _L = 100 kΩ R _L = 10 kΩ	25k		25k	
Output Voltage Swing	R _L = 100 kΩ R _L = 10 kΩ	±0.6V		±0.6V	
Common Mode Rejection Ratio	R _S ≤ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	R _S ≤ 10 kΩ	74 dB		74 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ unless otherwise specified) (Continued)

Parameters	Conditions	$V_S = \pm 15\text{V}$			
		$I_{SET} = 1\ \mu\text{A}$		$I_{SET} = 10\ \mu\text{A}$	
		Min	Max	Min	Max
V_{OS}	$T_A = 25^{\circ}\text{C}, R_S \leq 100\ \text{k}\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25^{\circ}\text{C}$		6 nA		20 nA
I_{bias}	$T_A = 25^{\circ}\text{C}$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25^{\circ}\text{C}, R_L = 100\ \text{k}\Omega$ $V_O = \pm 0.6\text{V}, R_L = 10\ \text{k}\Omega$	60k		60k	
Supply Current	$T_A = 25^{\circ}\text{C}$		11 μA		100 μA
Power Consumption	$T_A = 25^{\circ}\text{C}$		330 μW		3 mW
V_{OS}	$R_S \leq 10\ \text{k}\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 13.5\text{V}$		$\pm 13.5\text{V}$	
Large Signal Voltage Gain	$V_O = \pm 10\text{V}, R_L = 100\ \text{k}\Omega$ $R_L = 10\ \text{k}\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ \text{k}\Omega$ $R_L = 10\ \text{k}\Omega$	$\pm 12\text{V}$		$\pm 12\text{V}$	
Common Mode Rejection Ratio	$R_S \leq 10\ \text{k}\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ \text{k}\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			300 μW		3 mW

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified)

Parameters	Conditions	$V_S = \pm 1.5\text{V}$			
		$I_{SET} = 1 \mu\text{A}$		$I_{SET} = 10 \mu\text{A}$	
		Min	Max	Min	Max
V_{OS}	$T_A = 25^{\circ}\text{C}, R_S \leq 100 \text{ k}\Omega$		6 mV		6 mV
I_{OS}	$T_A = 25^{\circ}\text{C}$		6 nA		20 nA
I_{bias}	$T_A = 25^{\circ}\text{C}$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25^{\circ}\text{C}, R_L = 100 \text{ k}\Omega$ $V_O = \pm 0.6\text{V}, R_L = 10 \text{ k}\Omega$	25k		25k	
Supply Current	$T_A = 25^{\circ}\text{C}$		8 μA		90 μA
Power Consumption	$T_A = 25^{\circ}\text{C}$		24 μW		270 mW
V_{OS}	$R_S \leq 10 \text{ k}\Omega$		7.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 0.6\text{V}$		$\pm 0.6\text{V}$	
Large Signal Voltage Gain	$V_O = \pm 0.5\text{V}, R_L = 100 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$	25k		25k	
Output Voltage Swing	$R_L = 100 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$	$\pm 0.6\text{V}$		$\pm 0.6\text{V}$	
Common Mode Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	65 dB		65 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified) (Continued)

Parameters	Conditions	$V_S = \pm 15\text{V}$			
		$I_{SET} = 1\ \mu\text{A}$		$I_{SET} = 10\ \mu\text{A}$	
		Min	Max	Min	Max
V_{OS}	$T_A = 25^{\circ}\text{C}, R_S \leq 100\ \text{k}\Omega$		6 mV		6 mV
I_{OS}	$T_A = 25^{\circ}\text{C}$		6 nA		20 nA
I_{bias}	$T_A = 25^{\circ}\text{C}$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25^{\circ}\text{C}, R_L = 100\ \text{k}\Omega$ $V_O = \pm 0.6\text{V}, R_L = 10\ \text{k}\Omega$	60k		60k	
Supply Current	$T_A = 25^{\circ}\text{C}$		11 μA		100 μA
Power Consumption	$T_A = 25^{\circ}\text{C}$		330 μW		3 mW
V_{OS}	$R_S \leq 10\ \text{k}\Omega$		7.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 13.5\text{V}$		$\pm 13.5\text{V}$	
Large Signal Voltage Gain	$V_O = \pm 10\text{V}, R_L = 100\ \text{k}\Omega$ $R_L = 10\ \text{k}\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ \text{k}\Omega$ $R_L = 10\ \text{k}\Omega$	$\pm 12\text{V}$		$\pm 12\text{V}$	
Common Mode Rejection Ratio	$R_S \leq 10\ \text{k}\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ \text{k}\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			300 μW		3 mW

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NOTE: All typical values have been characterized but are not tested.

Section 8 — Analog Switches

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DG153.....	8-11	DGM184.....	8-49	IH5052.....	8-86
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DG143.....	8-17	IH311.....	8-54	IH5142.....	8-92
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DG189.....	8-22	IH5022.....	8-65	MM555.....	8-122
DG190.....	8-22	IH5023.....	8-65		

D123/D125

SPST 6-Channel JFET Switch Driver

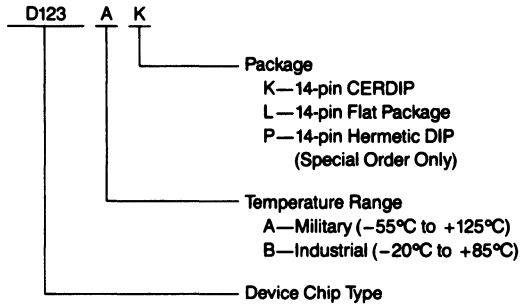


D123/D125

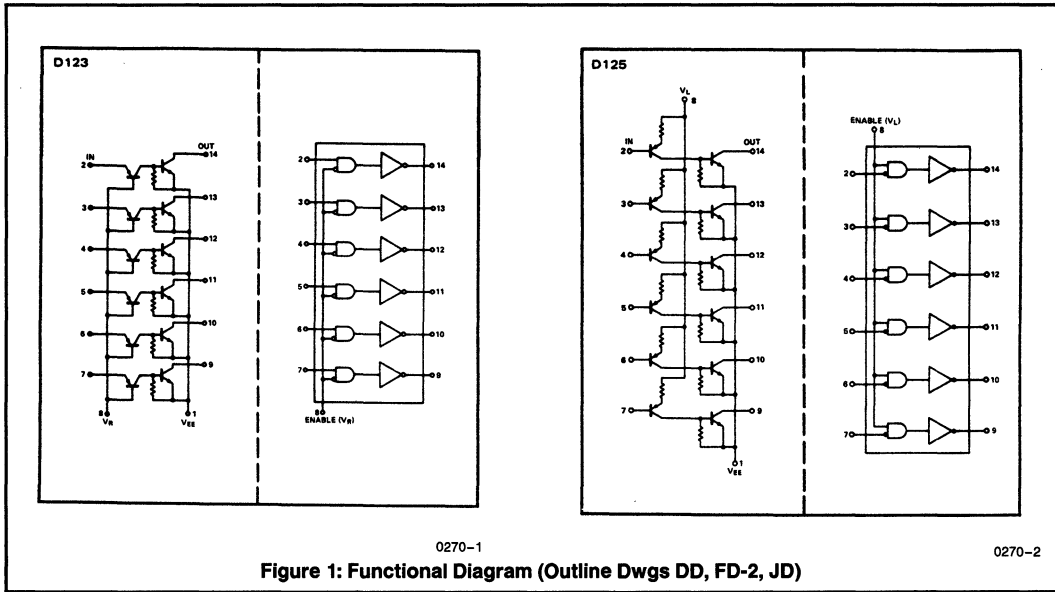
GENERAL DESCRIPTION

The D123 and D125 monolithic bipolar drivers convert low-level positive logic signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

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0270-1

0270-2

Figure 1: Functional Diagram (Outline Dwgs DD, FD-2, JD)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Input-to-Emitter Voltage ($V_{IN} - V_{EE}$)	33V
Output-to-Emitter Voltage ($V_O - V_{EE}$)	33V
Logic Supply-to-Emitter Voltage ($V_L - V_{EE}$)	27V
Input-to-Reference Voltage ($V_{IN} - V_R$)	2V
Input-to-Logic Supply Voltage ($V_{IN} - V_L$)	+6V
Reference-to-Emitter Voltage ($V_R - V_{EE}$)	31V

Maximum Dissipation (Note)	750mW
Current (any pin)	30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified are as follows: $V_{EE} = -20V$, $V_L = 4.5V$, $I_{OUT} = 0$, $V_R = 0$. Output and power supply measurements based on specified input conditions.

Device No.	Parameter	Test Conditions	Max Limit			Units
			-55°C	25°C	125°C	
INPUT						
D123	$I_{IN(OFF)}$	$V_{IN} = 0.4V$	1	1	100	μA
	$V_{IN(ON)}$	$I_{IN} = 1mA$	1.3	1	0.8	V
D125	$I_{IN(OFF)}$	$V_{IN} = 4.1V$	1	1	20	μA
	$I_{IN(ON)}$	$V_{IN} = 0.5V$	-0.7	-0.7	-0.7	mA
OUTPUT						
D125 & D123	$I_{OUT(OFF)}$	$V_{OUT} = +10V$	0.1	0.1	10	μA
	$V_{OUT(ON)}$	$I_{OUT} = 1mA$	-19.7	-19.7	-19.5	V
	$V_{OUT(ON)}$	$I_{OUT} = 4mA$	-19.2	-19.2	-19.0	V
POWER SUPPLY						
D123	$I_{R(ON)}^{(1)}$	$I_{OUT} = 0$ for ON measurements. $V_{OUT} = +10V$ for OFF measurements.	0.5	0.5	0.5	mA
	$I_{R(OFF)}^{(2)}$		1	1	150	μA
	$I_{EE(ON)}^{(1)}$		1	1	1	mA
	$I_{EE(OFF)}^{(2)}$		2	2	200	μA
D125	$I_{L(ON)}^{(1)}$		2	2	1.9	mA
	$I_{L(OFF)}^{(1)}$		1	1	100	μA
	$I_{EE(ON)}^{(1)}$		2	2	1.9	mA
	$I_{EE(OFF)}^{(2)}$		2	2	200	μA
SWITCHING TIMES						
D125 & D123	$t_{(ON)}$	$I_{OUT} = 1mA$, $C_{OUT}^{(3)} = 10pF$ (See Switching Times) (4)		250		ns
	$t_{(OFF)}^{(4)}$			800		ns
	$t_{(on)}$	$I_{OUT} = 4mA$, $C_{OUT}^{(3)} = 10pF$ (See Switching Times)		250		ns
	$t_{(off)}^{(5)}$			600		ns

- NOTES:**
- One channel ON, 5 channels OFF.
 - All channels OFF.
 - Add 30ns per pF for 1mA and add 8ns per pF for 4mA for additional capacitive loading.
 - For Dual-In-Line package add 120ns to $t_{(off)}$.
 - For Dual-In-Line package add 30ns to $t_{(off)}$.

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NOTE: All typical values have been characterized but are not tested.

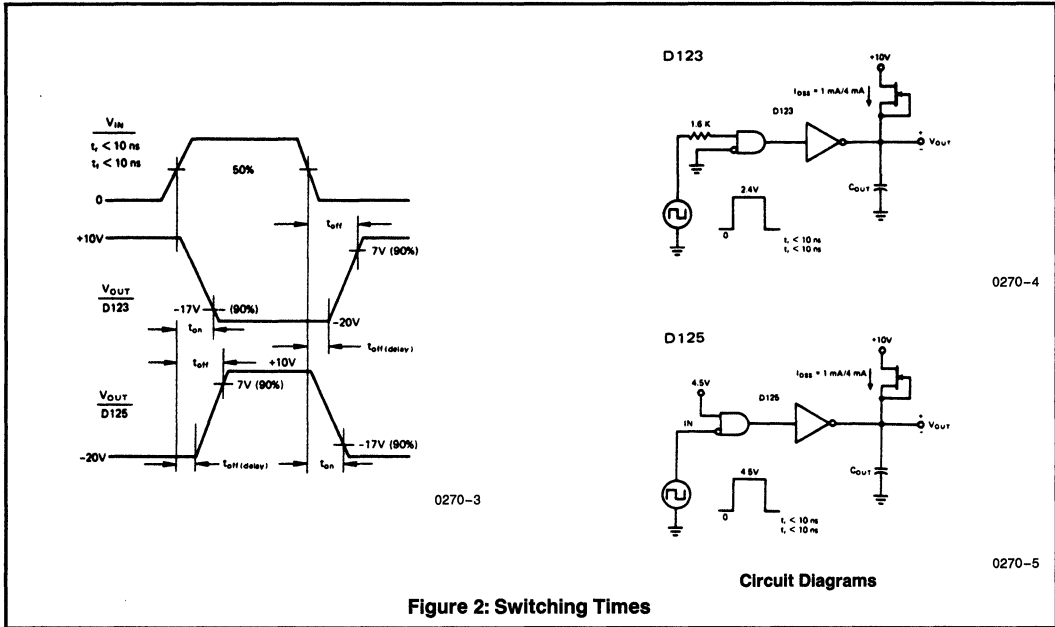
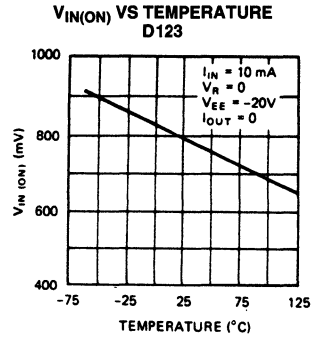
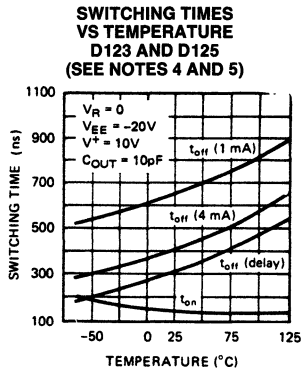
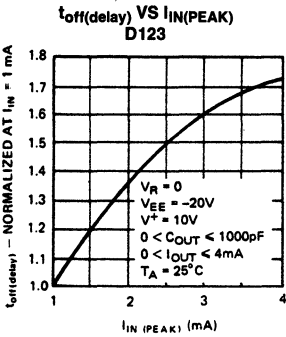


Figure 2: Switching Times

TYPICAL PERFORMANCE CHARACTERISTICS

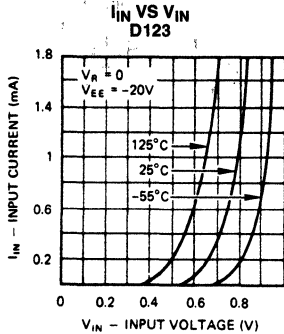


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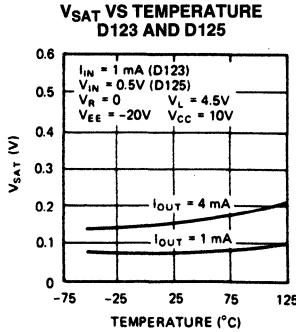
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NOTE: All typical values have been characterized but are not tested.

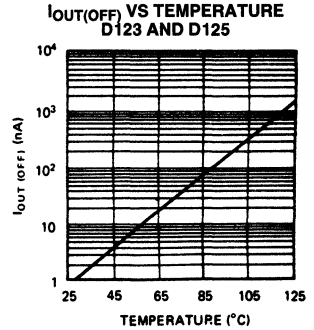
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



0270-9



0270-10



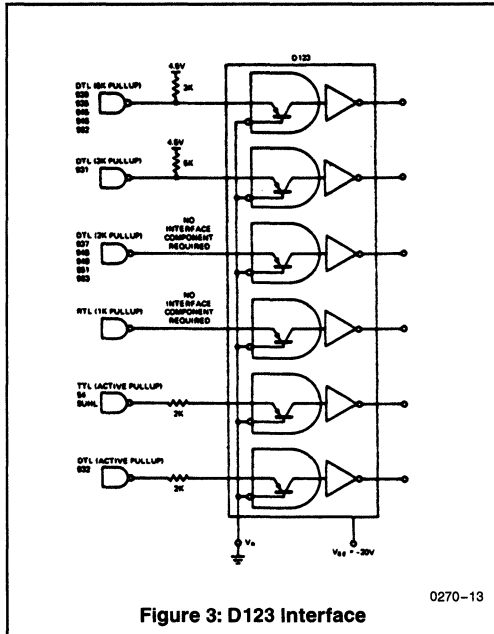
0270-11

APPLICATION TIPS

Interfacing the D123 and D125

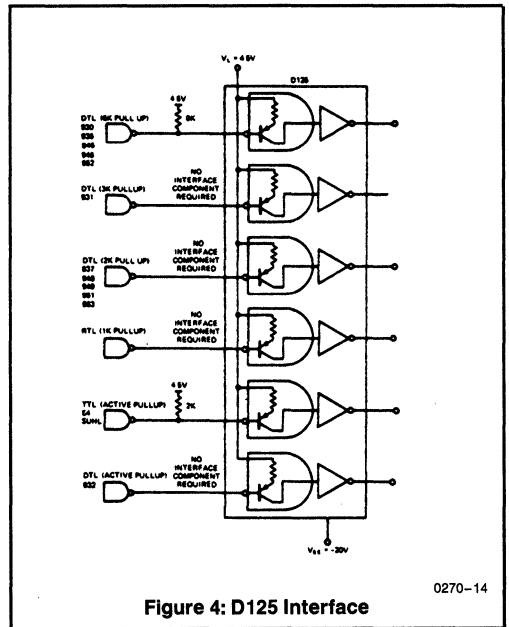
In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping $V_L - V_{IN} \leq 0.4V$ is a must to insure turn-off. To accomplish this, a shunt resistor must be added to supply the leakage current (I_{CES}) for DTL devices. Since $I_{CES} = 50\mu A$, a $0.4V/0.05mA = 8k\Omega$ or less resistor should be used. For TTL devices using a $2k\Omega$ resistor will insure turn-off with up to $200\mu A$ of leakage current.



0270-13

Figure 3: D123 Interface



0270-14

Figure 4: D125 Interface

Using the ENABLE Control

Device pins V_R or V_L can be used to enable the D123 or D125 drivers. For the D123, the enabling driver must sink $I_{R(ON)} \times \text{no. of channels used}$. For the D125, $I_{L(ON)} \times \text{no. of channels used}$ must be sourced with a voltage at least +4V greater than V_{IN} .

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NOTE: All typical values have been characterized but are not tested.

D129

4-Channel Decoded JFET Switch Driver



D129

GENERAL DESCRIPTION

The D129 is a 4-channel driver with binary decode input. It was designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V^- terminal can be set at any voltage between $-5V$ and $-30V$. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V^- in the off-state.

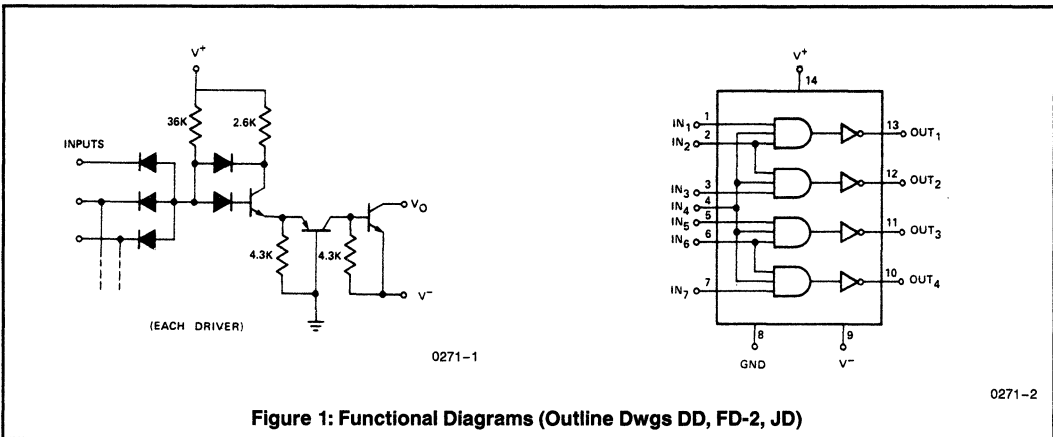
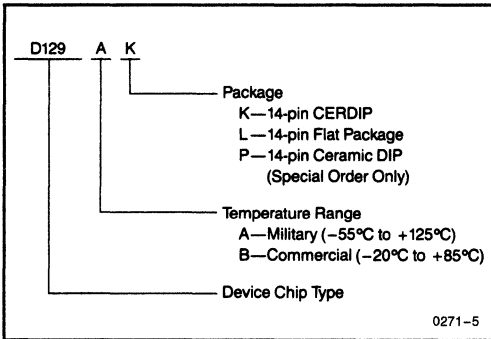
The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

FEATURES

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible With Low Power TTL and DTL, $I_F = 200\mu A$ Max
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V_O - V^-$	50V	Current (any terminal)	30mA
$GND - V^-$	33V	Storage Temperature	-65°C to +150°C
$V^+ - GND$	8V	Operating Temperature	-55°C to +125°C
$V_{IN} - GND$	±5V	Power Dissipation (note)	750mW
		Lead Temperature (Soldering, 10sec)	300°C

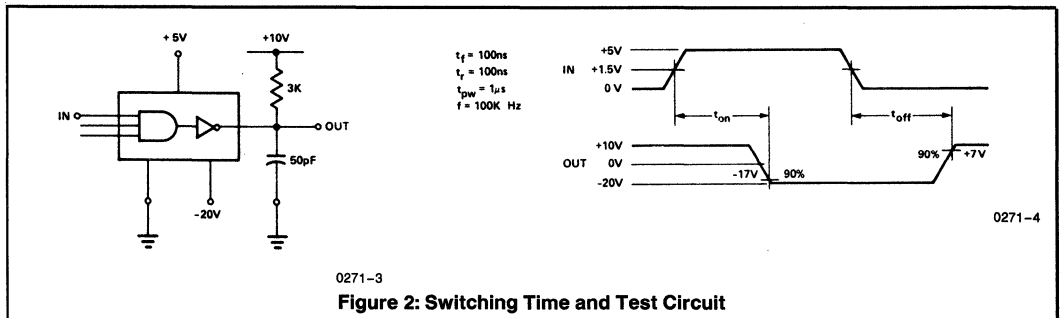
Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperatures.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Test conditions unless otherwise specified $V^- = -20V, V^+ = 5V$

Symbol	Parameter	Test Conditions	Maximum Limit						Units
			D129M			D129I			
			-55°C	25°C	125°C	-20°C	25°C	85°C	
OUT									
V_{OL}	Output Voltage, Low	$I_O = 10mA$ $V_{IN} = 2.2V, V^+ = 4.5V$	-19.3	-19.3	-19	-19.25	-19.25	-19	V
V_{OL}	Output Voltage, Low	$I_O = 1mA$	-19.8	-19.8	-19.75				
I_{OH}	Output Current, High	$V_O = 10V, V_{IN} = 0.7V$	0.1	0.1	20	0.2	0.2	10	µA
INPUT									
I_{INH}^*	Input Current Input Voltage High	$V_{IN} = 5V$ Input Under Test, $V_{IN} = 0$ All Other Inputs	0.25	0.25	5	1	1	5	µA
I_{INL}^*	Input Current Input Voltage Low	$V_{IN} = 0, V^+ = 5.5V$	-250	-200	-160	-250	-225	-200	
TIME									
t_{on}	Turn-ON Time	See Switching Time Test Circuit		0.25			0.3		µs
t_{off}	Turn-OFF Time			1.0			1.5		
SUPPLY									
I_{EE}	Negative Supply Current	$V^- = -20V$	One Channel "ON"			-2		-2.25	mA
I_L	Logic Supply Current					3		3.3	
I_{EE}	Negative Supply Current	$V^+ = 5.5V$	All $V_{IN} = 0,$			-10		-25	µA
I_L	Logic Supply Current		All Channels "OFF"			0.75		1	mA

*Per gate Input



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NOTE: All typical values have been characterized but are not tested.

DG123/DG125

4 & 5-Channel SPST Driver With Switch



DG123/DG125

GENERAL DESCRIPTION

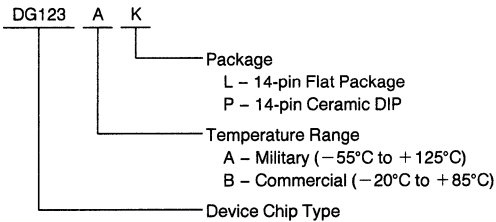
This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOSFET switch. Two driver versions are supplied for inverting and noninverting applications. A MOSFET, used as a current source provides an active pull-up for faster switching.

FEATURES

- Available With and Without Programmable Constant Current Pull-up
- Zener Protection on All Gates
- P-Channel Enhancement-Type MOSFET Switches
- Each Switch Summed to One Common Point

An external biasing connection is brought out for biasing the current source, for optimization of speed and power.

ORDERING INFORMATION



TRUTH TABLE

DG123		DG125		Switch Cond.
V _{IN}	V _R	V _{IN}	V _L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

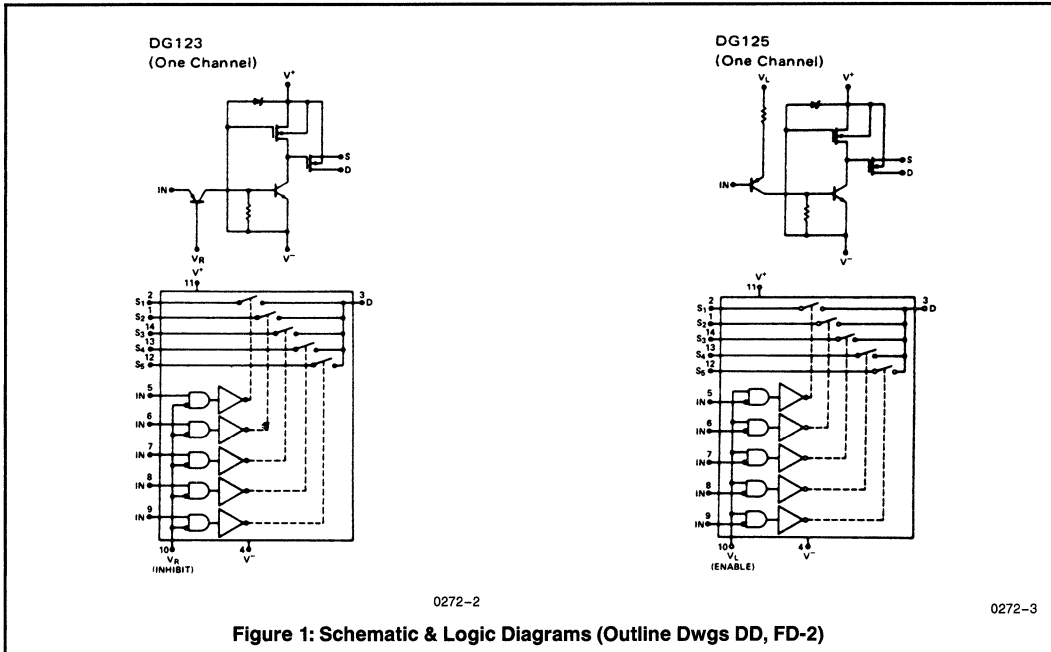


Figure 1: Schematic & Logic Diagrams (Outline Dwgs DD, FD-2)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V^+ - V^-$)	33V
Collector to Pull-up ($V^+ - V_P$)	33V
Drain to Emitter ($V_D - V^-$)	32V
Source to Emitter ($V_S - V^-$)	32V
Drain to Source ($V_D - V_S$)	28V
Source to Drain ($V_S - V_D$)	28V
Logic to Emitter ($V_L - V^-$)	33V
Reference to Emitter ($V_R - V^-$)	31V
Reference to Input ($V_R - V_{IN}$)	6V

Logic to Input ($V_L - V_{IN}$)	$\pm 6V$
Input to Emitter ($V_{IN} - V^-$)	33V
Current (any terminal)	30mA
Storage Temperature	-65°C to $+150^\circ\text{C}$
Operating Temperature	-55°C to $+125^\circ\text{C}$
Dissipation (Note)	750mW
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C . Derate 10mW/ $^\circ\text{C}$ for higher ambient temperature.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test conditions unless specified otherwise are as follows: $V_L = 4.5V$, $V_R = 0$, $V^- = -20V$. Input ON and OFF test conditions used for output and power supply specifications.

Device No.	Parameter (Note)	Test Conditions	Max Limits			Units
			-55°C	$+25^\circ\text{C}$	$+125^\circ\text{C}$	
Input						
DG123	$I_{IN(OFF)}$	$V_{IN} = 0.4V$	1	1	100	μA
	$V_{IN(ON)}$	$I_{IN} = 1\text{mA}$	1.3	1.0	0.8	V
DG125	$I_{IN(ON)}$	$V_{IN} = 0.5V$	-0.7	-0.7	-0.7	mA
OUTPUT						
All circuits	$r_{DS(ON)}$	$V_D = 10V, I_S = -1\text{mA}$	100	100	125	Ω
		$V_D = 0, I_S = -100\mu\text{A}$	200	200	250	Ω
		$V_D = -10V, I_S = -100\mu\text{A}$	450	450	600	Ω
	$I_{D(ON)}$	$V_D = 10V, I_{S(all)} = 0$		4	4000	nA
	$I_{D(OFF)}$	$V_{S(all)} = 10V, V_D = -10V$		-4	-4000	nA
	$I_{S(OFF)}$	$V_D = 10V, V_S = -10V$		-1	-1000	nA
POWER SUPPLY						
All circuits	$I_{CC(ON)}$	One Channel (ON)		3		mA
	$I_L(ON)$			3		mA
	$I_R(ON)$			-0.5		mA
	$I_{EE(ON)}$			-6		mA
All circuits	$I_{CC(OFF)}$	All Channels (OFF)		10		μA
	$I_L(OFF)$			10		μA
	$I_R(OFF)$			-15		μA
	$I_{EE(OFF)}$			-20		μA
SWITCHING TIMES						
All circuits	$t_{(ON)}$	See Switching Times		0.3		μs
	$t_{(OFF)}$			1		μs

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOSFET switch for the given test condition.

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NOTE: All typical values have been characterized but are not tested.

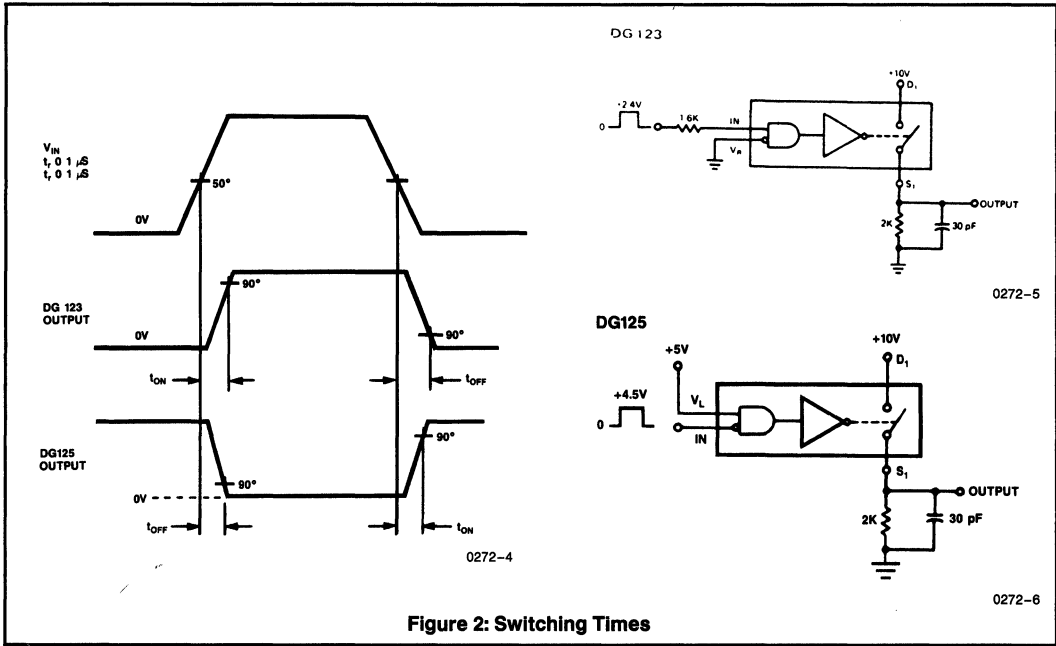
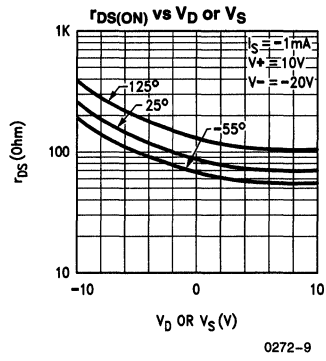
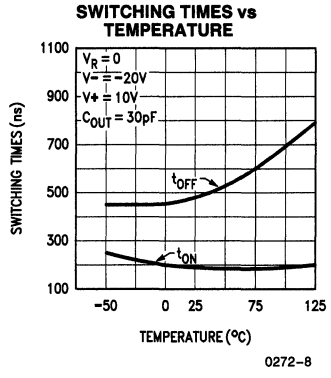
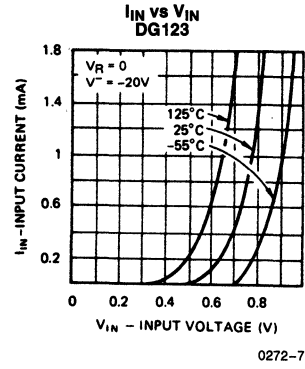


Figure 2: Switching Times

TYPICAL PERFORMANCE CHARACTERISTICS



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NOTE: All typical values have been characterized but are not tested.

DG123/DG125



APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and TTL Logic are shown in Figures 3 and 4.

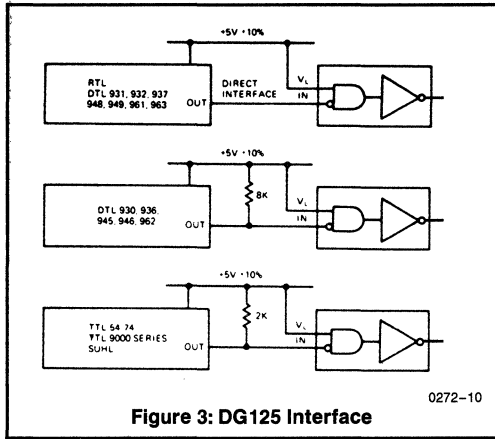


Figure 3: DG125 Interface

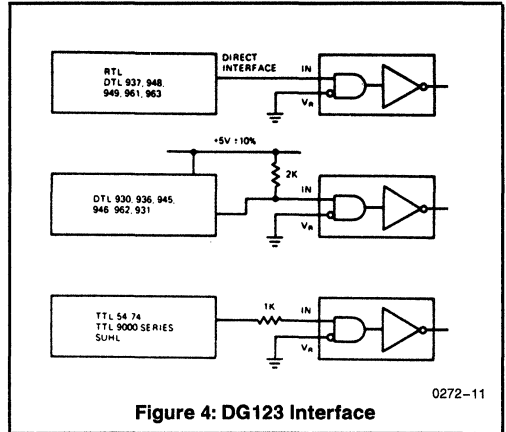


Figure 4: DG123 Interface

Enable Control

The V_R and V_L terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)} \times \text{No. of channels used}$, for the DG125, and $I_{R(ON)} \times \text{No. of channels used}$ for the DG123 devices. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

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NOTE: All typical values have been characterized but are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151-154

DUAL JFET Analog Switch

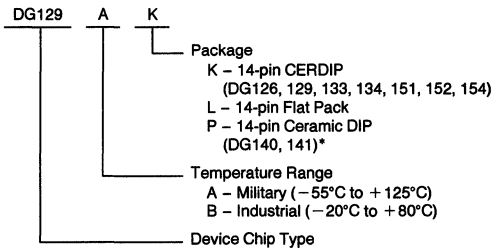


DG126, DG129, DG133, DG134, DG140, DG141, DG151-154

GENERAL DESCRIPTION

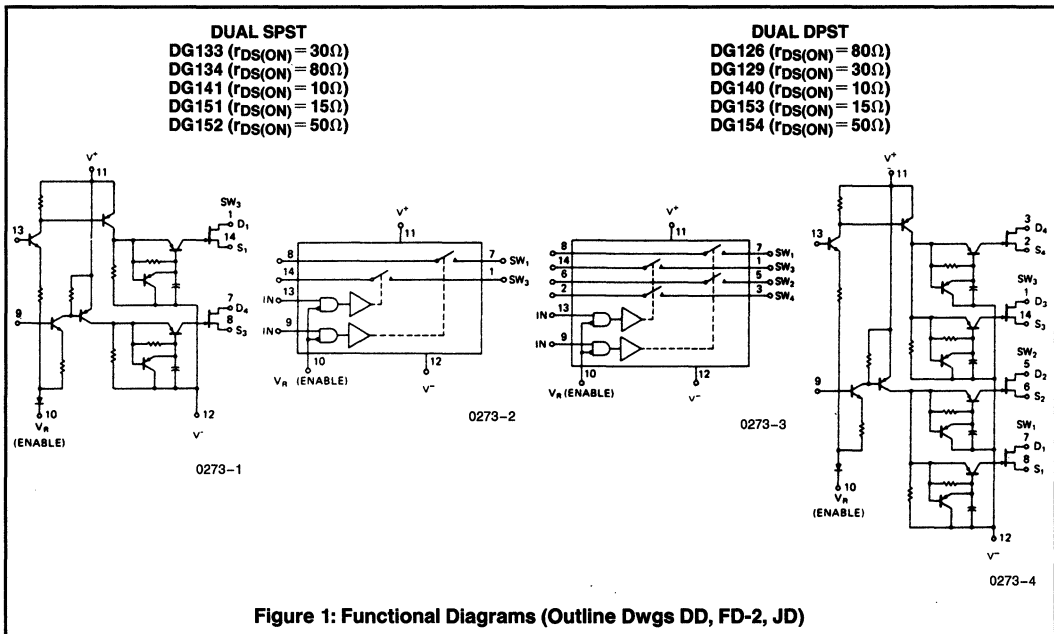
These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, computing, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it off.

ORDERING INFORMATION



FEATURES

- Each Channel Complete—Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, 1mW
- Switches Analog Signals Up to 20 Volts Peak-to-Peak
- Low $r_{DS(ON)}$, 10 Ohms Max on DG140/A and DG141/A
- Switching Times Improved 100%—'A' Versions



8

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NOTE: All typical values have been characterized but are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151-154



ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V^-$ or $V^+ - V_A$)	30V
Total Supply Voltage ($V^+ - V^-$)	36V
Positive Supply Voltage to Ref. Voltage ($V^+ - V_R$)	25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V^-$)	22V
Power Dissipation (Note)	750mW
Current (any terminal)	30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

ELECTRICAL CHARACTERISTICS (Per Channel)

Applied voltages for all test: DG126, DG129, DG133, DG134, DG140, DG141 ($V^+ = +12V$, $V^- = -18V$, $V_R = 0$), and DG151, DG152, DG153, DG154 ($V^+ = +15V$, $V^- = -15V$, $V_R = 0$). Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

SYMBOL (NOTE)	CHARACTERISTIC	TYPE	TEST CONDITIONS	ABSOLUTE MAX LIMIT			UNIT
				-55°C	25°C	125°C	
INPUT							
$V_{IN(ON)}$	Input Voltage-On	All Circuits	$V_2 = -12V$	2.9 min	2.5 min	2.0 min	Volts
$V_{IN(OFF)}$	Input Voltage-Off		$V_2 = -12V$	1.4	1.0	0.6	Volts
$I_{IN(ON)}$	Input Current		$V_{IN} = 2.5V$	120	60	60	μA
$I_{IN(OFF)}$	Input Leakage Current		$V_{IN} = 0.8V$	0.1	0.1	2	μA
SWITCH OUTPUT							
$r_{DS(ON)}$	Drain-Source On Resistance	DG126 DG134	$V_{IN} =$ (See Note) $V_D = 10V, I_S = 10mA$	80	80	150	Ω
		DG129 DG133		30	30	50	Ω
		DG140 DG141		10	10	20	Ω
		DG151 DG153	$V_D = 7.5V, I_S = 10mA$ $V_{IN} =$ (See Note)	15	15	30	Ω
		DG152 DG154		50	50	100	Ω
		$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG126	$V_D = V_S = -10V$		± 2
$I_{S(OFF)}$	Source Leakage Current	DG129	$V_S = 10V, V_D = -10V$		± 1	100	nA
$I_{D(OFF)}$	Drain Leakage Current	DG133 DG134	$V_D = 10V, V_S = -10V$		± 1	100	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG140	$V_D = V_S = -10V$		± 2	100	nA
$I_{S(OFF)}$	Source Leakage Current	DG141	$V_S = 10V, V_D = -10V$		± 10	1000	nA
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 10V, V_S = -10V$		± 10	1000	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG151	$V_D = V_S = -7.5V$		± 2	500	nA
$I_{S(OFF)}$	Source Leakage Current	DG153	$V_S = 7.5V, V_D = -7.5V$		± 10	1000	nA
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 7.5V, V_S = -7.5V$		± 10	1000	nA
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG152	$V_D = V_S = -7.5V$		± 2	500	nA
$I_{S(OFF)}$	Source Leakage Current		$V_S = 7.5V, V_D = -7.5V$		± 2	200	nA
$I_{D(OFF)}$	Drain Leakage Current	DG154	$V_D = 7.5V, V_S = -7.5V$		± 2	200	nA

NOTE: V_{IN} must be a step function with a minimum slew-rate of 1V/ μs .

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NOTE: All typical values have been characterized but are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151-154



DG126, DG129, DG133, DG134, DG140, DG141, DG151-154

ELECTRICAL CHARACTERISTICS (Per Channel) (Continued)

SYMBOL (NOTE)	CHARACTERISTIC	TYPE	TEST CONDITIONS	ABSOLUTE MAX LIMIT			UNIT
				-55°C	25°C	125°C	
POWER SUPPLY							
$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits	One Driver ON, $V_{IN} = 2.5V$		3		mA
$I_{2(ON)}$	Negative Power Supply Drain Current				-1.8		mA
$I_{R(ON)}$	Reference Power Supply				-1.4		mA
$I_{1(OFF)}$	Drain Current Positive Power Supply Leakage Current		Both Drivers OFF, $V_{IN} = 0.8V$		25		μA
$I_{2(OFF)}$	Negative Power Supply Leakage Current				-25		μA
$I_{R(OFF)}$	Reference Power Supply Leakage Current				-25		μA
SWITCHING							
t_{ON}	Turn-On Time	See Below	DG126, DG129, DG133, DG134, DG152, DG154		600		ns
t_{OFF}	Turn-Off Time	See Below	DG126, DG129, DG133, DG134, DG152, DG154		1.6		μs
t_{ON}	Turn-On Time	See Below	DG140, DG141, DG151, DG153		1.0		μs
t_{OFF}	Turn-Off Time	See Below	DG140, DG141, DG151, DG153		2.5		μs
POWER							
P_{ON}	ON Driver Power	All Circuits	Both Inputs $V_{IN} = 2.5V$		175		mW
P_{OFF}	OFF Driver Power		Both Inputs $V_{IN} = 1V$		1		mW

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

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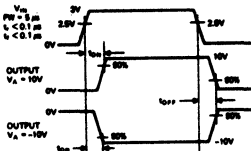
NOTE: All typical values have been characterized but are not tested.

DG126, DG129, DG133, DG134, DG140, DG141, DG151-154



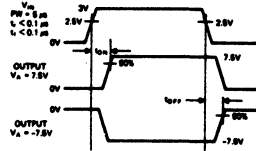
ELECTRICAL CHARACTERISTICS (Continued)

DG126, 129, 133, 134, 140, 141

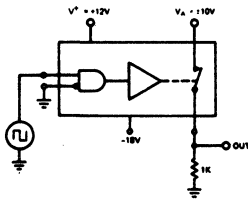


0273-5

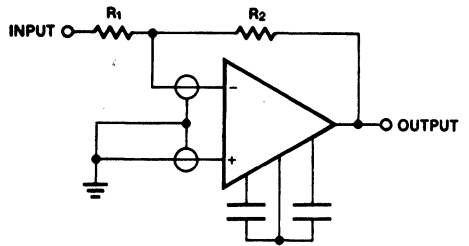
DG151, 152, 153, 154



0273-6



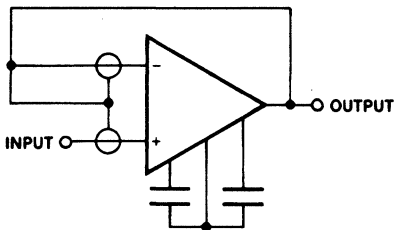
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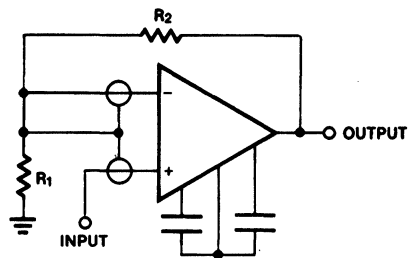
0273-8

OFF MODEL

OFF MODEL



0273-9

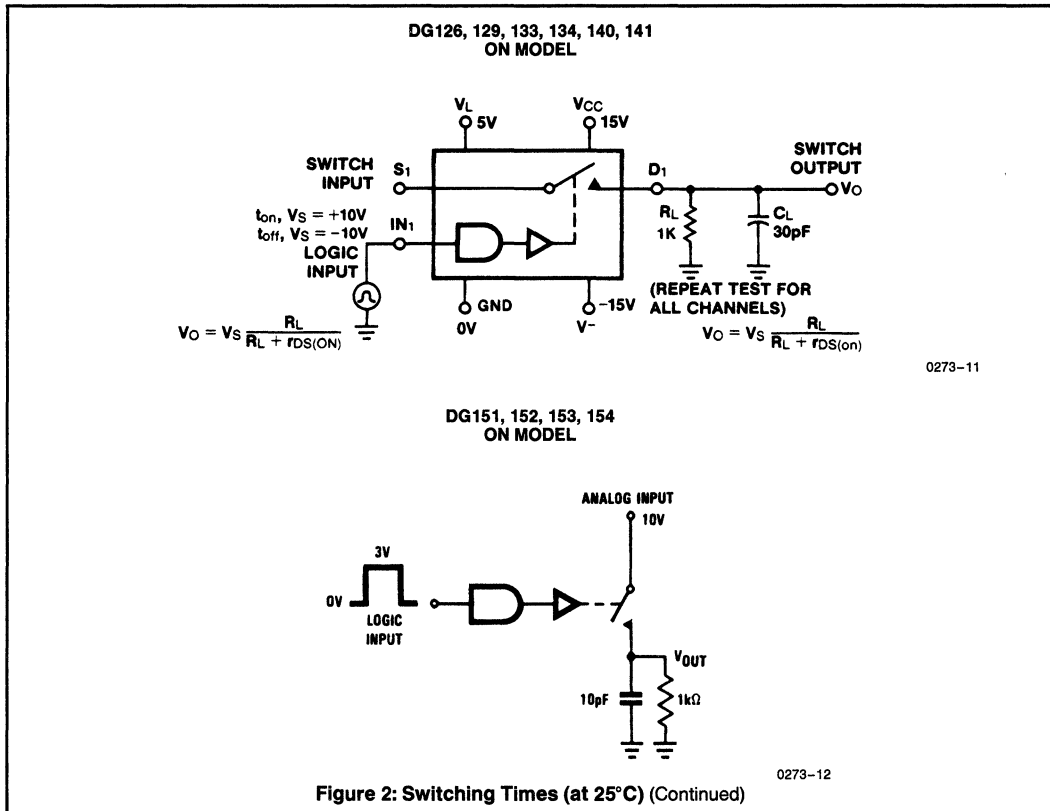


0273-10

Figure 2: Switching Times (at 25°C)

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NOTE: All typical values have been characterized but are not tested.



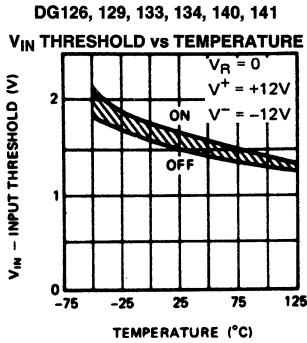
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NOTE: All typical values have been characterized but are not tested.

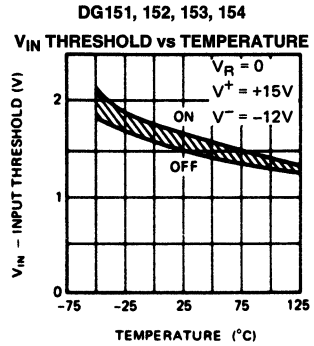
DG126, DG129, DG133, DG134, DG140, DG141, DG151-154



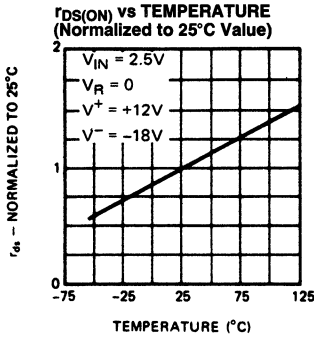
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)



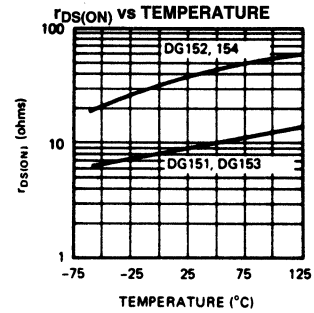
0273-13



0273-14

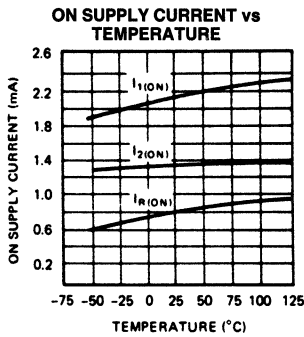


0273-15

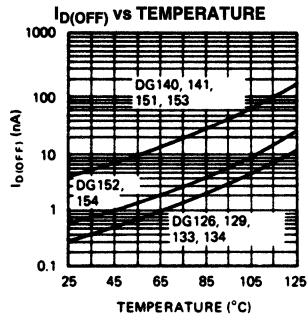


0273-16

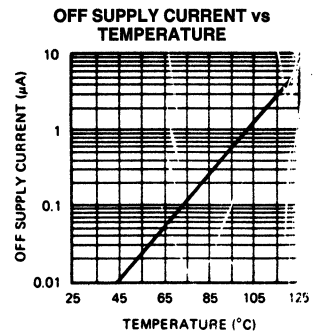
ALL CIRCUITS



0273-17



0273-18



0273-19

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NOTE: All typical values have been characterized but are not tested.

DG139, DG142-DG146, DG161-DG164

DUAL JFET Analog Switch



DG139, DG142-DG146, DG161-DG164

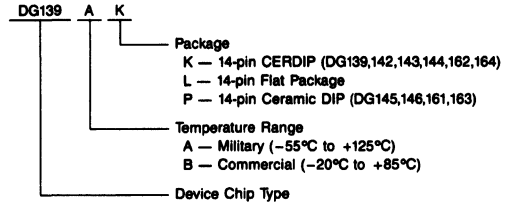
GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

FEATURES

- Each Channel Complete – Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, 1mW
- Switches Analog Signals Up to 20 Volts Peak-to-Peak
- Low $r_{DS(ON)}$, 10 Ohms Max on DG145 and DG146

ORDERING INFORMATION



0274-21

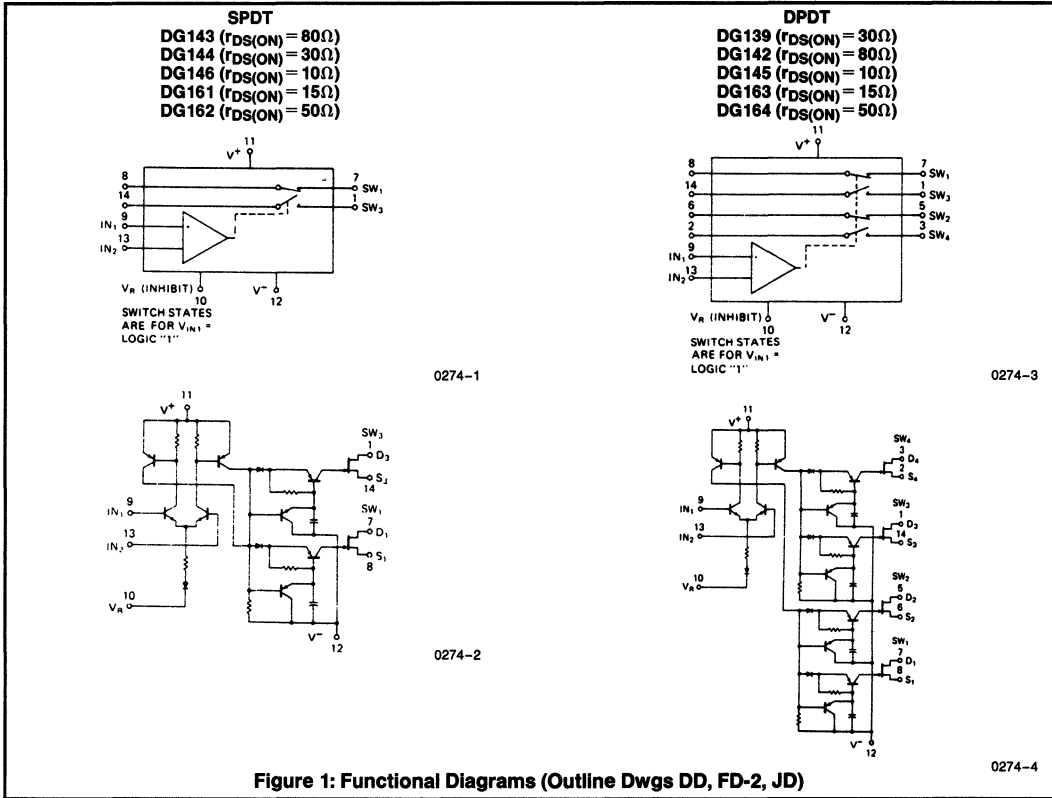


Figure 1: Functional Diagrams (Outline Dwg DD, FD-2, JD)

8

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NOTE: All typical values have been characterized but are not tested.

DG139, DG142-DG146, DG161-DG164



ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	36V	$V_{IN1} - V_R$	$\pm 6V$
$V_S - V^-$	30V	$V_{IN2} - V_R$	$\pm 6V$
$V^+ - V_S$	30V	Power Dissipation (Note)	750mW
$V_S - V_D$	$\pm 22V$	Current (any terminal)	30mA
$V_R - V^-$	21V	Storage Temperature	-65°C to +150°C
$V^+ - V_R$	17V	Operating Temperature	-55°C to +125°C
$V^+ - V_{IN1}$ or V_{IN2}	14V	Lead Temperature (Soldering, 10sec)	300°C
$V_{IN1} - V_{IN2}$	$\pm 6V$		

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: DG139, DG142, DG143, DG144, DG145, DG146 ($V^+ = 12V$, $V^- = -18V$, $V_R = 0$, $V_{IN2} = 2.5V$) and DG161, DG162, DG163, DG164 ($V^+ = 15V$, $V^- = -15V$, $V_R = 0$, $V_{IN2} = 2.5V$). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

Symbol (Note)	Parameter	Type	Test Conditions	Absolute Max Limit			Units
				-55°C	25°C	125°C	
INPUT							
$I_{IN1(ON)}$	Input Current	All Circuits	$V_{IN1} = 3.0V$	120	60	60	μA
$I_{IN2(ON)}$			$V_{IN2} = 2.0V$	120	60	60	μA
$I_{IN1(OFF)}$	Input Leakage Current		$V_{IN1} = 2.0V$	0.1	0.1	2	μA
$I_{IN2(OFF)}$			$V_{IN2} = 3.0V$	0.1	0.1	2	μA
SWITCH OUTPUT							
$r_{DS(ON)}$	Drain-Source On Resistance	DG142 DG143	$V_D = 10V, I_S = -10mA$	80	80	150	Ω
		DG139 DG144		V_{IN} (See Note)	30	30	60
		DG145 DG146	$V_D = 10V, I_S = -10mA$ V_{IN} (See Note)	10	10	20	Ω
		DG161 DG163		$V_D = 7.5V, I_S = -10mA$	15	15	30
		DG162 DG164	V_{IN} (See Note)	50	50	100	Ω
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG139 DG142	$V_D = V_S = -10V$	2	100	nA	
$I_{S(OFF)}$	Source Leakage Current	DG143 DG144	$V_S = 10V, V_D = -10V$	1	100	nA	
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 10V, V_S = -10V$	1	100	nA	
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG145	$V_D = V_S = -10V$	2	100	nA	
$I_{S(OFF)}$	Source Leakage Current	DG146	$V_S = 10V, V_D = -10V$	10	1000	nA	
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 10V, V_S = -10V$	10	1000	nA	
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG161	$V_D = V_S = -7.5V$	2	500	nA	
$I_{S(OFF)}$	Source Leakage Current	DG163	$V_S = 7.5V, V_D = -7.5V$	10	1000	nA	
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 7.5V, V_S = -7.5V$	10	1000	nA	
$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG162	$V_D = V_S = -7.5V$	2	500	nA	
$I_{S(OFF)}$	Source Leakage Current	DG164	$V_S = 7.5V, V_D = -7.5V$	2	200	nA	
$I_{D(OFF)}$	Drain Leakage Current		$V_D = 7.5V, V_S = -7.5V$	2	200	nA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test. V_{IN} must be a step function with a minimum slew-rate of 1V/ μs .

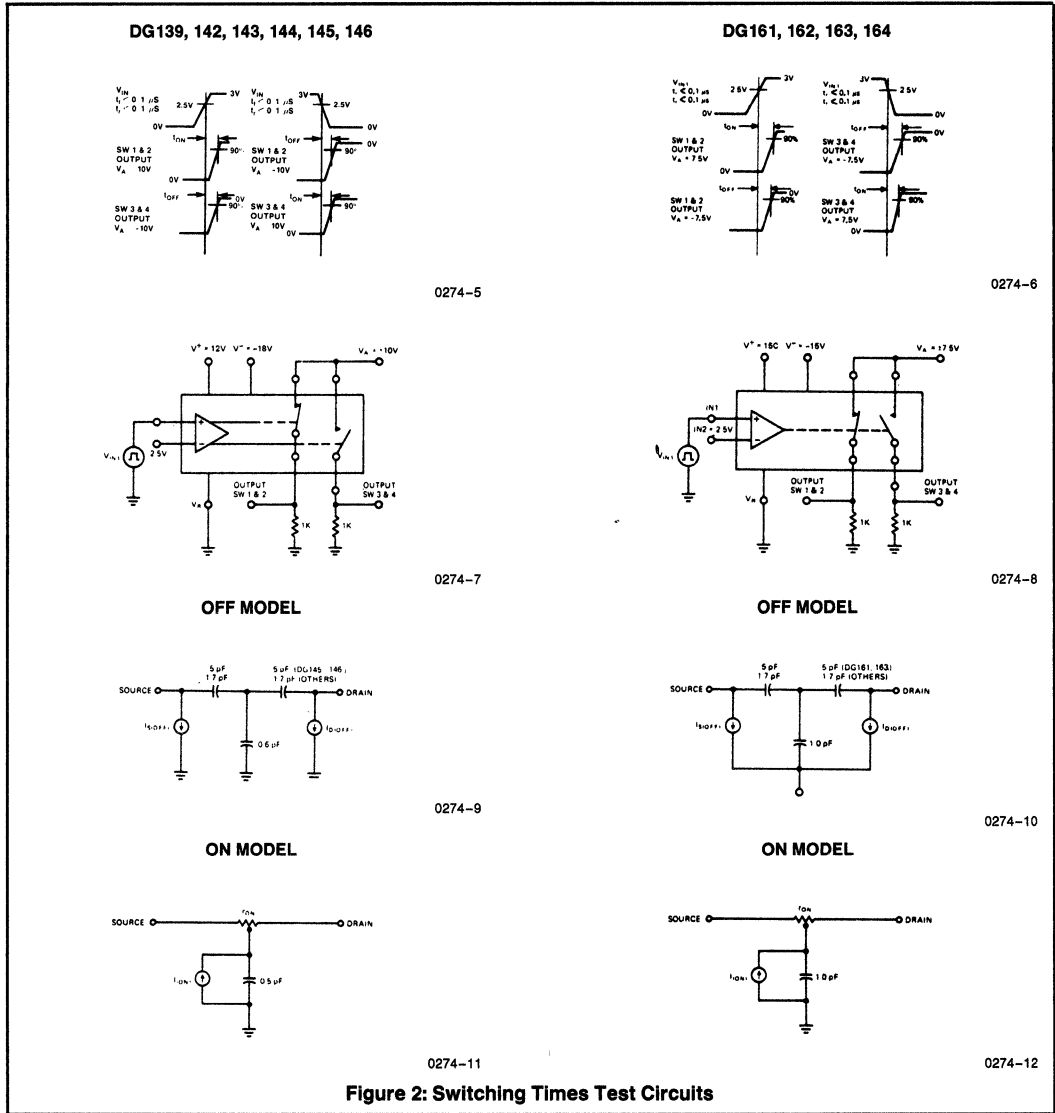
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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

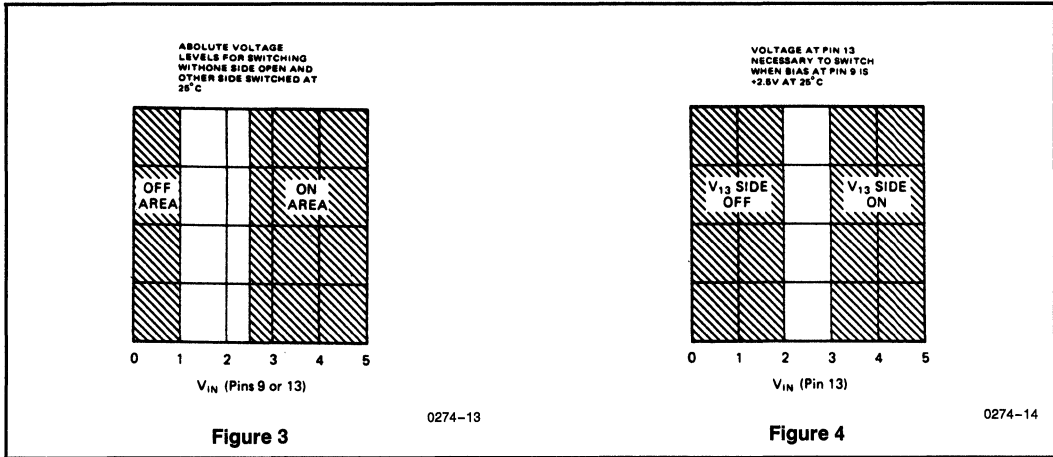
Symbol (Note)	Parameter	Type	Test Conditions	Absolute Max Limit			Units
				-55°C	25°C	125°C	
POWER SUPPLY							
$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits	$V_{IN1} = 3V$ or $V_{IN1} = 2V$		4.2		mA
$I_{2(ON)}$	Negative Power Supply Drain Current				-2.0		mA
$I_{R(ON)}$	Reference Power Supply Drain Current				-2.2		mA
$I_{1(OFF)}$	Positive Power Supply Leakage Current		$V_{IN1} = V_{IN2} = 0.8V$		25		μA
$I_{2(OFF)}$	Negative Power Supply Leakage Current				-25		μA
$I_{R(OFF)}$	Reference Power Supply Leakage Current				-25		μA
SWITCHING							
t_{ON}	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164	See Switching Times		0.8		μs
t_{OFF}	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164	See Switching Times		1.6		μs
t_{ON}	Turn-On Time	DG145, DG146 DG161, DG163	See Switching Times		1.0		μs
t_{OFF}	Turn-Off Time	DG145, DG146 DG161, DG163	See Switching Times		2.5		μs

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.



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NOTE: All typical values have been characterized but are not tested.

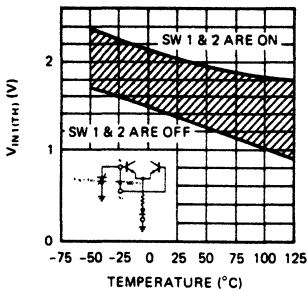


NOTE 1: An example of Absolute Minimum Differential Voltage, $|V_G - V_{13}|$, is when $V_G = 3V$ and $V_{13} = 2.5V$, the V_G side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when $V_G = 2V$ and $V_{13} = 2.5V$, the V_G side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

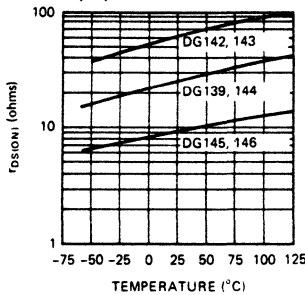
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

DG139, 142, 144, 145, 146

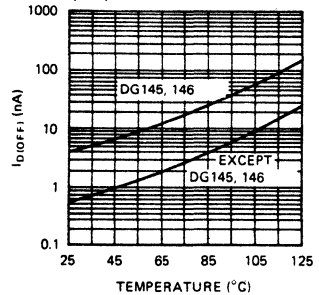
V_{IN1} THRESHOLD vs TEMPERATURE



$R_{DS(ON)}$ vs TEMPERATURE

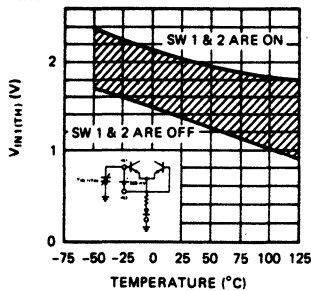


$I_{D(OFF)}$ vs TEMPERATURE

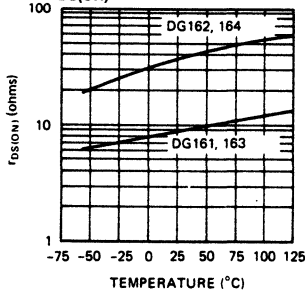


DG161, 162, 163, 164

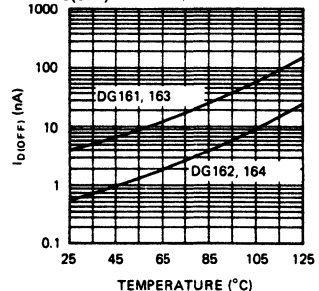
V_{IN1} THRESHOLD vs TEMPERATURE



$R_{DS(ON)}$ vs TEMPERATURE



$I_{S(OFF)}$ vs TEMPERATURE



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NOTE: All typical values have been characterized but are not tested.

DG180-191

High-Speed Driver With JFET Switch



GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consist of 2 or 4 N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output isolation is 50dB at 10MHz, due to the low output impedance of the FET-gate driving circuit.

ORDERING INFORMATION

Part Number	Type	r _{DS(on)} (Max)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75

FEATURES

- Constant ON-Resistance for Signals to ±10V (DG182, 185, 188, 191), to ±7.5V (All Devices)
- ±15V Power Supplies
- <2nA Leakage From Signal Channel in Both ON and OFF States
- TTL, DTL, RTL Direct Drive Compatibility
- t_{on}, t_{off} < 150ns, Break-Before-Make Action
- Cross-talk and Open Switch Isolation > 50dB at 10MHz (75Ω Load)
- JAN 38510 Approved

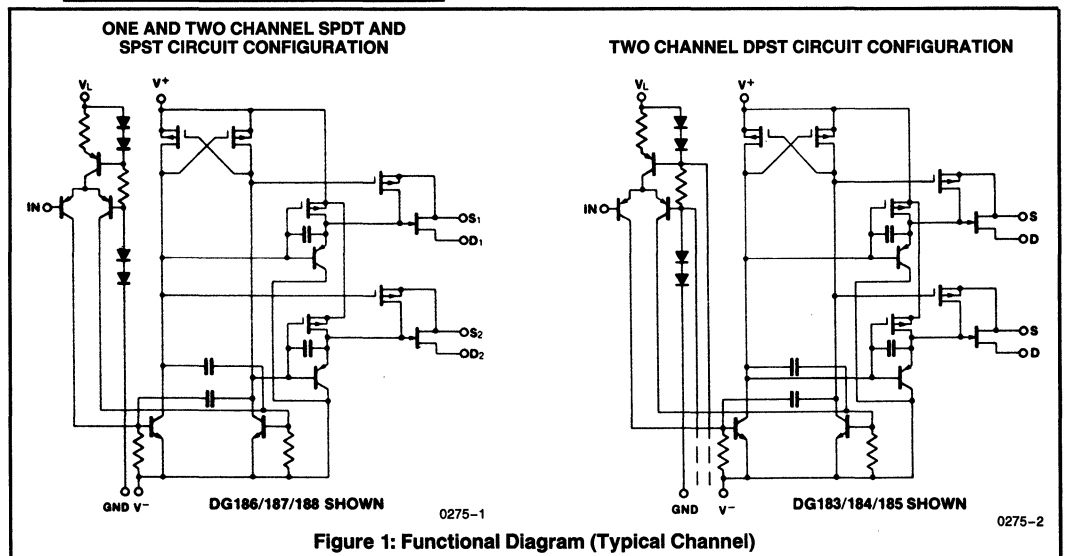
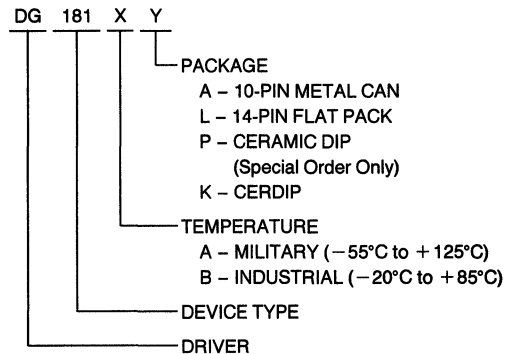


Figure 1: Functional Diagram (Typical Channel)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V+ - V-	36V
V+ - V _D	33V
V _D - V-	33V
V _D - V _S	±22V
V _L - V-	36V
V _L - V _{IN}	8V
V _L - GND	8V
V _{IN} - GND	8V

GND - V-	27V
GND - V _{IN}	20V
Current (S or D)	See Note 3
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Power Dissipation*	450 (TW), 750 (FLAT), 825 (DIP)mW
Lead Temperature (Soldering, 10sec)	300°C

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

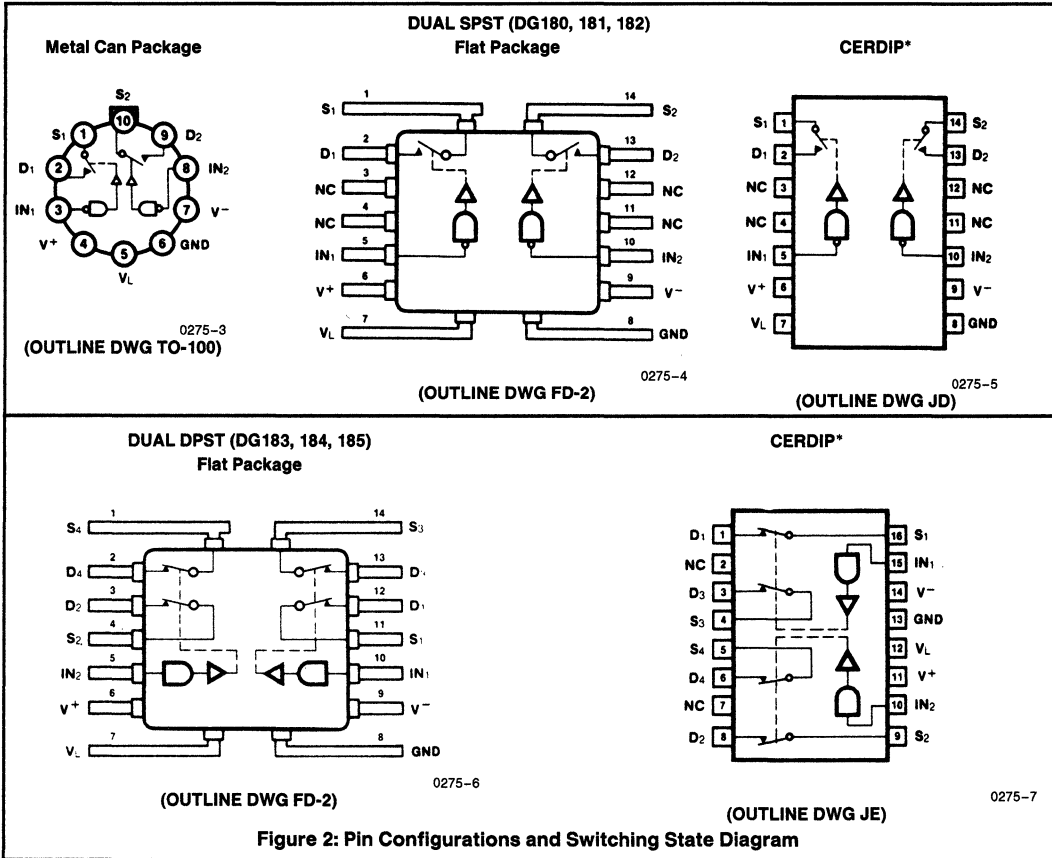


Figure 2: Pin Configurations and Switching State Diagram

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NOTE: All typical values have been characterized but are not tested.

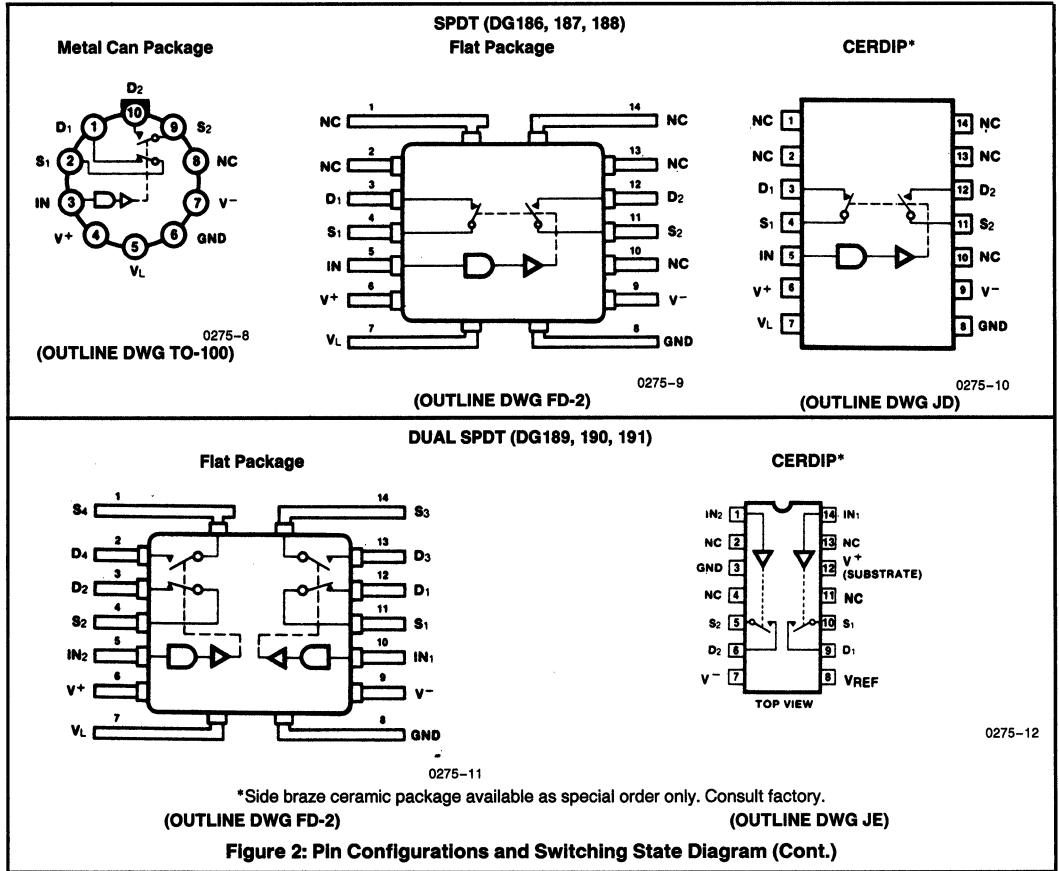


Figure 2: Pin Configurations and Switching State Diagram (Cont.)

ELECTRICAL CHARACTERISTICS ($V^+ = +15V, V^- = -15V, V_L = 5V$, Unless Noted)

Parameter	Device No.	Test Conditions (Note 1)	A Series			B Series			Units
			-55°C	+25°C	+125°C	-20°C	+25°C	+85°C	
SWITCH									
$I_{S(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V, V_D = -10V, V^+ = 10V$ $V^- = -20V, V_{IN} = \text{"OFF"}$		± 1	100		± 5	100	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	$V_S = 7.5V, V_D = -7.5V$ $V_{IN} = \text{"OFF"}$		± 1	100		± 5	100	nA
	DG182, 185, 188, 191	$V_S = 10V, V_D = -10V$ $V_{IN} = \text{"OFF"}$		± 1	100		± 5	100	nA
$I_{D(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V, V_D = -10V, V^+ = 10V$ $V^- = -20V, V_{IN} = \text{"OFF"}$		± 1	100		± 5	100	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	$V_S = 7.5V, V_D = -7.5V$ $V_{IN} = \text{"OFF"}$		± 1	100		± 5	100	nA
	DG182, 185, 188, 191	$V_S = 10V, V_D = -10V$ $V_{IN} = \text{"OFF"}$		± 1	100		± 5	100	nA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $(V^+ = +15V, V^- = -15V, V_L = 5V, \text{Unless Noted})$ (Continued)

Parameter	Device No.	Test Conditions (Note 1)	A Series			B Series			Units	
			-55°C	+25°C	+125°C	-20°C	+25°C	+85°C		
SWITCH (Continued)										
$I_{D(on)} + I_{S(on)}$	DG180, 181, 183, 184 186, 187, 189, 190	$V_D = V_S = -7.5V, V_{IN} = \text{"ON"}$		± 2	-200		-10	-200	nA	
	DG182, 185, 188, 191	$V_D = V_S = -10V, V_{IN} = \text{"ON"}$		± 2	-200		-10	-200	nA	
INPUT										
I_{INL}	ALL	$V_{IN} = 0V$	-250	-250	-250	-250	-250	-250	μA	
I_{INH}	ALL	$V_{IN} = 5V$		10	20		10	20	μA	
DYNAMIC										
t_{on}	10 Ω Switches	See switching time test circuit		300			350		ns	
	30 Ω Switches			150			180			
	75 Ω Switches			250			300			
t_{off}	10 Ω Switches			250			300			
	30 Ω and 75 Ω Switches			130			150			
	$C_{S(off)}$		DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = -5V, I_D = 0, f = 1MHz$	9 typical (21 typical)			pF		
$C_{D(off)}$		$V_D = +5V, I_S = 0, f = 1MHz$	6 typical (17 typical)							
$C_{D(on)} + C_{S(on)}$		$V_D = V_S = 0, f = 1MHz$	14 typical (17 typical)							
OFF Isolation		$R_L = 75\Omega, C_L = 3pF$	Typically > 50dB at 10MHz (See Note 2)							
SUPPLY										
I^+	DG180, 181, 182, 189 190, 191	$V_{IN} = 5V$		1.5			1.5		mA	
	DG183, 184, 185			0.1			0.1			
	DG186, 187, 188			0.8			0.8			
I^-	DG180, 181, 182, 189 190, 191			-5.0			-5.0			
	DG183, 184, 185			-4.0			-4.0			
	DG186, 187, 188			-3.0			-3.0			
I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191			4.5			4.5			
	DG186, 187, 188			3.2			3.2			
	I_{GND}		ALL	-2.0			-2.0			
I^+	DG180, 181, 182, 189 190, 191		$V_{IN} = 0V$		1.5			1.5		
	DG183, 184, 185				3.0			3.0		
	DG186, 187, 188				0.8			0.8		
I^-	DG180, 181, 182, 189 190, 191			-5.0			-5.0			
	DG183, 184, 185			-5.5			-5.5			
	DG186, 187, 188			-3.0			-3.0			
I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191			4.5			4.5			
	DG186, 187, 188			3.2			3.2			
	I_{GND}	ALL		-2.0			-2.0			

NOTES 1. See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.

2. Off Isolation typically > 55dB at 1MHz for DG180, 183, 186, 189.

3. Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2ms Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

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ELECTRICAL CHARACTERISTICS MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX) (Continued)

Device Number	Conditions (Note 1) $V^+ = 15V, V^- = -15V, V_L = 5V$		Military Temperature			Industrial Temperature			Units
			-55°C	+25°C	+125°C	-20°C	+25°C	+85°C	
DG180	$V_D = -7.5V$	$I_S = -10mA$ $V_{IN} = "ON"$	10	10	20	15	15	25	Ω
DG181	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG182	$V_D = -10V$		75	75	100	100	100	150	Ω
DG183	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG184	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG185	$V_D = -10V$		75	75	150	100	100	150	Ω
DG186	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG187	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG188	$V_D = -10V$		75	75	150	100	100	150	Ω
DG189	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG190	$V_D = -7.5V$		30	30	60	50	50	50	Ω
DG191	$V_D = -10V$		75	75	150	100	100	150	Ω

APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75 Ω switches and 15V peak-to-peak for the 10 Ω and 30 Ω (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V^- \leq V_{ANALOG(peak)} - V_P$ where $V_P = 7.5V$ for the 10 Ω AND 30 Ω switches and $V_P = 5.0V$ for 75 Ω switches e.g., -10V minimum (-peak) analog signal and a 75 Ω switch ($V_P = 5V$), requires that $V^- \leq -10V - 5V = -15V$.

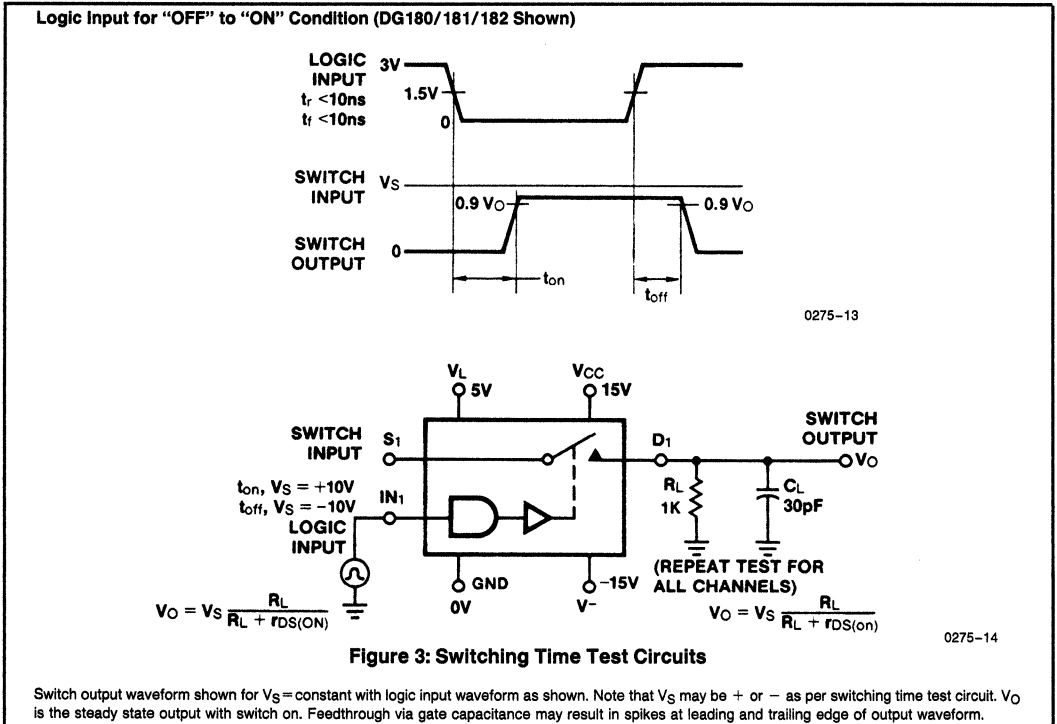


Figure 3: Switching Time Test Circuits

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

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NOTE: All typical values have been characterized but are not tested.

DUAL SPST - DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

SPDT - DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

DUAL DPST - DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

DUAL SPDT - DG189/190/191

TEST CONDITIONS

DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

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NOTE: All typical values have been characterized but are not tested.

DG200 CMOS Dual SPST Analog Switches



GENERAL DESCRIPTION

The DG200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

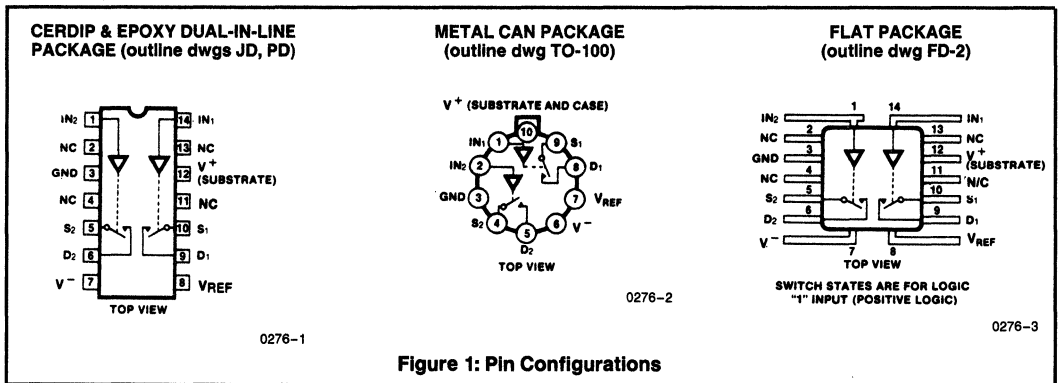
The DG200 is completely spec and pin-out compatible with the industry standard device.

FEATURES

- Switches Greater Than 28Vpp Signals With $\pm 15V$ Supplies
- Break-Before-Make Switching t_{off} 250ns, t_{on} 700ns Typical
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200)

ORDERING INFORMATION

Industry Standard Part	Package	Temperature Range
DG200AA	10-Pin Metal Can	-55°C to +125°C
DG200AK	14-Pin Cerdip	-55°C to +125°C
DG200AL	14-Pin Flat Pak	-55°C to +125°C
DG200BA	10-Pin Metal Can	-25°C to +85°C
DG200BK	14-Pin Cerdip	-25°C to +85°C
DG200BL	14-Pin Flat Pak	-25°C to +85°C
DG200CJ	14-Pin Epoxy Dip	0°C to +70°C



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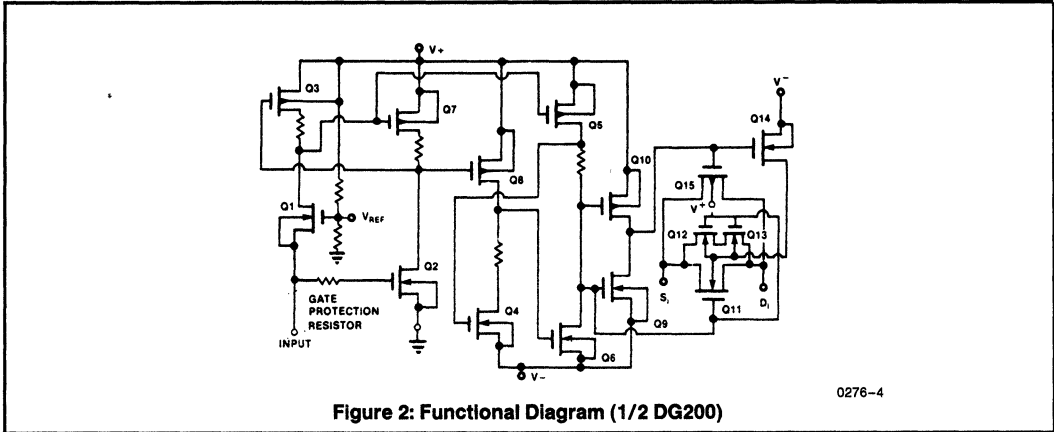
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ -V ⁻	<36V
V ⁺ -V _D	<30V
V _D -V ⁻	<30V
V _D -V _S	<28V
V _{IN} -GND	<20V
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	450mW

(All Leads Soldered to a P.C. Board.) Derate 6mW/°C Above 75°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS (T_A=25°C, V⁺ = +15V, V⁻ = -15V)

Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Com'l/Industrial			
			-55°C	+25°C	+125°C	0/ -25°C	+25°C	+70°C/ +85°C	
I _{IN(ON)}	Input Logic Current	V _{IN} = 0.8V See Notes 2, 3	±10	±1	±10		±10	±10	µA
I _{IN(OFF)}	Input Logic Current	V _{IN} = 2.4V See Notes 2, 3	±10	±1	±10		±10	±10	µA
r _{DS(ON)}	Drain-Source On Resistance	I _S = 10mA V _{ANALOG} = ±10V	70	70	100	80	80	100	Ω
r _{DS(ON)}	Channel-to-Channel r _{DS(ON)} Match			25 (typ)			30 (typ)		Ω
V _{ANALOG}	Min. Analog Signal Handling Capability			±15			±15		V
I _{D(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -14V to +14V		±2	100		±5	100	nA
I _{S(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -14V to +14V		±2	100		±5	100	nA

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NOTE: All typical values have been characterized but are not tested.

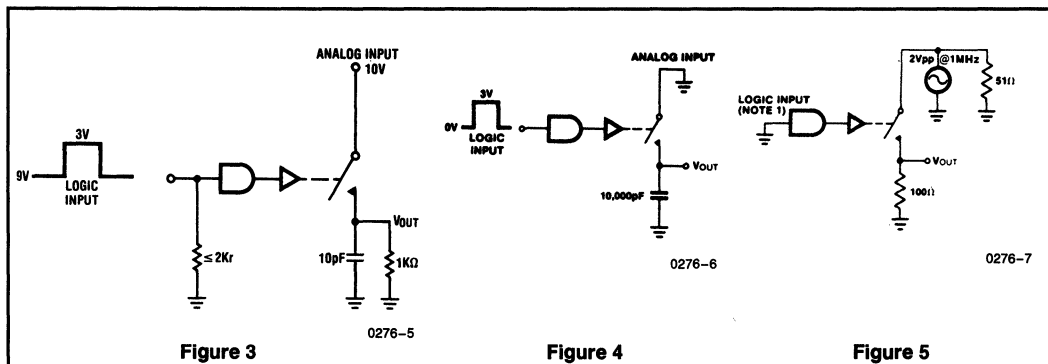
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V^+ = +15\text{V}$, $V^- = -15\text{V}$) (Continued)

Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Com'l/Industrial			
			-55°C	+25°C	+125°C	0/-25°C	+25°C	+70°C/+85°C	
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	$V_D = V_S = -14\text{V to } +14\text{V}$		± 2	200		± 10	200	nA
t_{on}	Switch "ON" Time See Note 1	$R_L = 1\text{k}\Omega$, $V_{ANALOG} = -10\text{V to } +10\text{V}$ See Fig. 3		1.0			1.0		μs
t_{off}	Switch "OFF" Time	$R_L = 1\text{k}\Omega$, $V_{ANALOG} = -10\text{V to } +10\text{V}$ See Fig. 3		0.5			0.5		μs
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1\text{MHz}$, $R_L = 100\Omega$, $C_L \leq 5\text{pF}$ See Fig. 5 (Note 1)		54 (typ)			50 (typ)		dB
I_{V1}	+ Power Supply Quiescent Current	$V_{IN} = 0\text{V or } 5\text{V}$	1000	1000	2000	1000	1000	2000	μA
I_{V2}	- Power Supply Quiescent Current		1000	1000	2000	1000	1000	2000	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Pull Down Resistor must be $\leq 2\text{k}\Omega$

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

TEST CIRCUITS

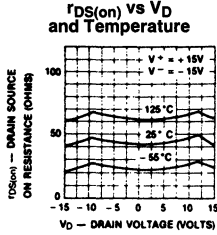


NOTE 3: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically $-120\mu\text{A}$.

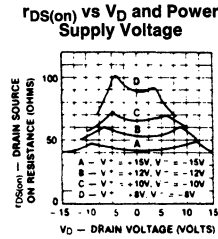
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NOTE: All typical values have been characterized but are not tested.

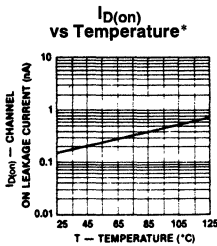
TYPICAL PERFORMANCE CHARACTERISTICS



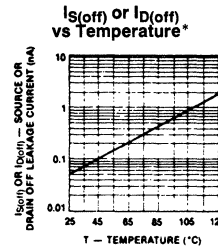
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0276-10



0276-11

APPLICATIONS

Using the VREF Terminal

The DG200 has an internal voltage divider setting the TTL threshold on the input control lines for V+ equal to +15V. The schematic shown here with nominal resistor values, gives approximately 2.4V on the VREF pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor must be added between V+ and the VREF pin, to restore +2.4V at VREF. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds >1.5V, allowing the user to define the "low" as <1.5V (consult factory). The VREF point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27kΩ between V+ and VREF is required, for a +15V supply.

V+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	-	-
+12	100	-
+10	51	-
+9	(34)	34
+8	(27)	27
+7	18	18

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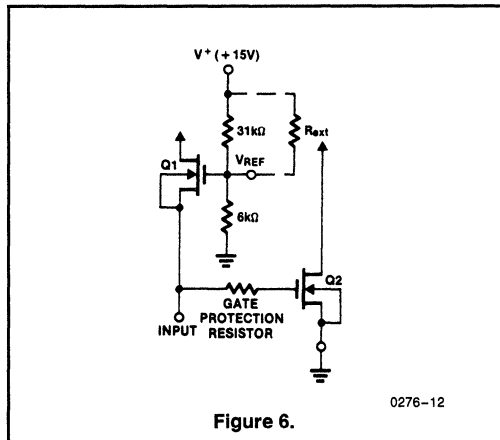


Figure 6.

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NOTE: All typical values have been characterized but are not tested.

DG201

Quad SPST

CMOS Analog Switch



GENERAL DESCRIPTION

The DG201 solid-state analog switches are designed using an improved, high-voltage CMOS monolithic technology. They provide performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERMIL's CMOS technology.

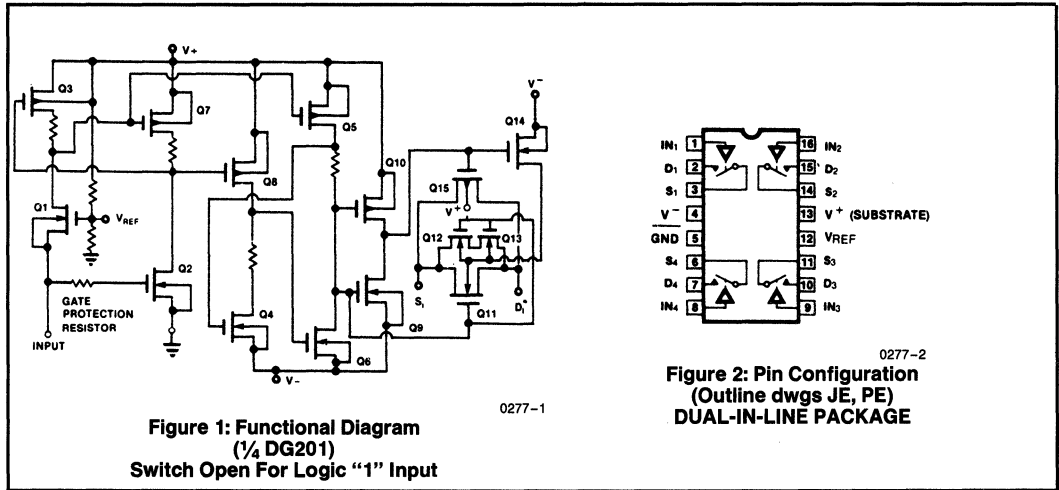
The DG201 is completely specification and pin-out compatible with the industry standard device.

FEATURES

- Switches Greater Than 28V_{p-p} Signals With ±15V Supplies
- Break-Before-Make Switching $t_{off} = 250ns$, $t_{on} = \text{Typically } 500ns$
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG201)

ORDERING INFORMATION

Industry Standard Part Number	Temperature Range	Package
DG201AK	-55°C to +125°C	16-Pin CERDIP
DG201BK	-25°C to +85°C	16-Pin CERDIP
DG201CJ	0°C to +70°C	16-Pin Plastic DIP



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻	<36V	V _{IN} to GND	<20V
V ⁺ to V _D	<30V	Current (Any Terminal)	<30mA
V _D to V ⁻	<30V	Storage Temperature	-65°C to +150°C
V _D to V _S	<28V	Operating Temperature	-55°C to +125°C
V _{REF} to V ⁻	<33V	Lead Temperature (Soldering, 10sec)	300°C
V _{REF} to V _{IN}	<30V	Power Dissipation	450mW
V _{REF} to GND	<20V	Derate 6mW/°C Above 70°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DG201 ELECTRICAL CHARACTERISTICS (T_A = 25°C, V⁺ = +15V, V⁻ = -15V)

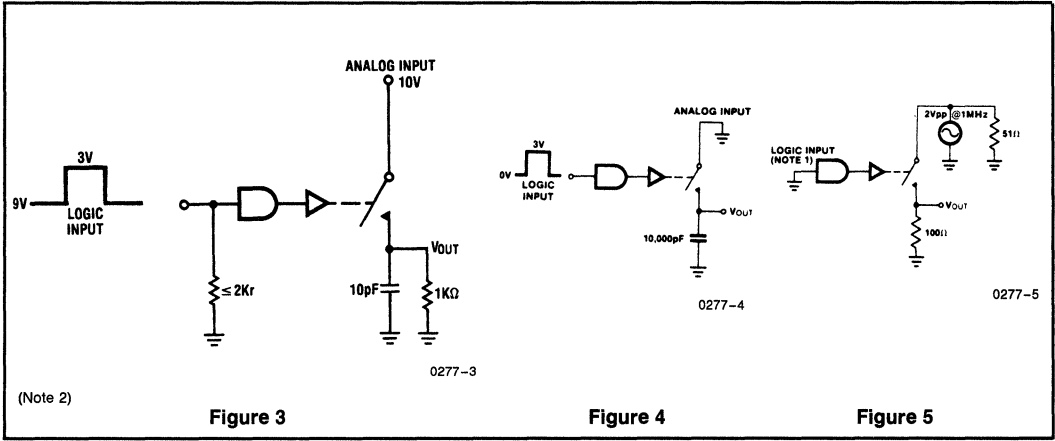
Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Commercial			
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C/ +85°C	
I _{IN(ON)}	Input Logic Current	V _{IN} = 0.8V See Note 1	10	±1	10	±1	±1	10	µA
I _{IN(OFF)}	Input Logic Current	V _{IN} = 2.4V See Note 1	10	±1	10	±1	±1	10	µA
R _{DS(ON)}	Drain-Source On Resistance	I _S = 10mA V _{ANALOG} = ±10V	80	80	125	100	100	125	Ω
R _{DS(ON)}	Channel to Channel R _{DS(ON)} Match			25 (typ)			30 (typ)		Ω
V _{ANALOG}	Analog Signal Handling Capability			±15 (typ)			±15 (typ)		V
I _{D(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -14V to +14V		±1	100		±5	100	nA
I _{S(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -14V to +14V		±1	100		±5	100	nA
I _{D(ON)} + I _{S(ON)}	Switch ON Leakage Current	V _D = V _S = ±14V		±2	200		±5	200	nA
t _{on}	Switch "ON" Time See Note 2	R _L = 1kΩ, V _{ANALOG} = -10V to +10V See Figure 3		1.0			1.0		µs
t _{off}	Switch "OFF" Time See Note 2	R _L = 1kΩ, V _{ANALOG} = -10V to +10V See Figure 3		0.5			0.5		µs
Q _(INJ.)	Charge Injection	See Figure 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R _L = 100Ω, C _L ≤ 5pF See Figure 5		54 (typ)			50 (typ)		dB
I ⁺ _Q	+ Power Supply Quiescent Current	V _{IN} = 0V to 5V	2000	1000	2000	2000	1000	2000	µA
I ⁻ _Q	- Power Supply Quiescent Current		2000	1000	2000	2000	1000	2000	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

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NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



(Note 2)

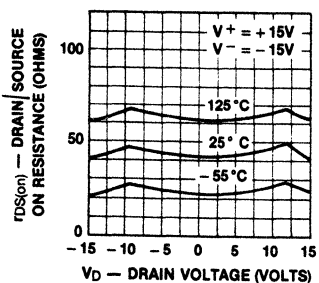
Figure 3

Figure 4

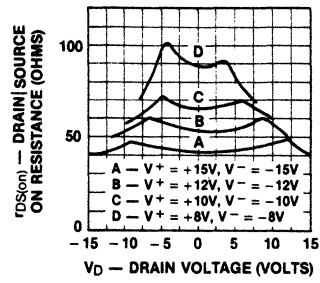
Figure 5

NOTE 2: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically $-120\mu\text{A}$. Pull down resistor, if used, $\leq 2\text{K}\Omega$.

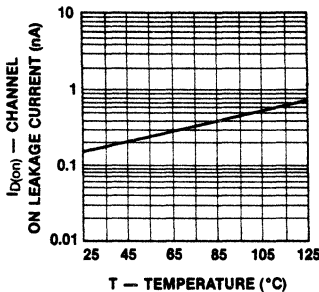
TYPICAL PERFORMANCE CHARACTERISTICS



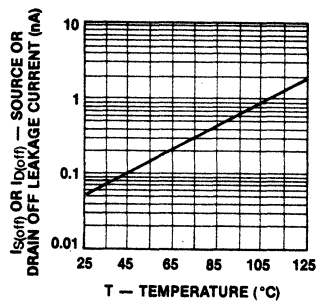
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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

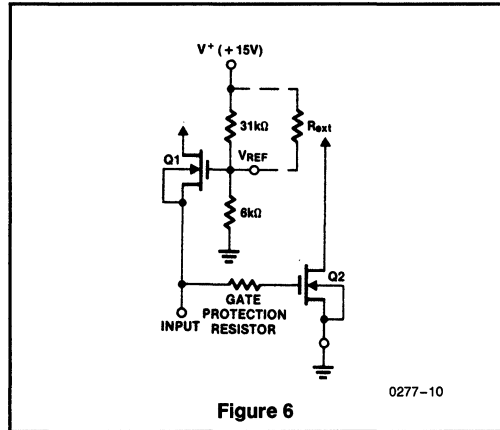
Using the V_{REF} Terminal

The DG201 has an internal voltage divider that sets the TTL threshold on the input control lines for $V^+ = 15V$. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and V_{REF} pin, to restore +2.4V at V_{REF} . The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic 'low' level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds >1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27k Ω and V_{REF} is required, for a +15V supply.

V ⁺ Supply (V)	TTL Resistor (k Ω)	CMOS Resistor (k Ω)
+15	-	-
+12	100	-
+10	51	-
+9	(34)	34
+8	(27)	27
+7	18	18



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NOTE: All typical values have been characterized but are not tested.

DG201A/DG202

Quad Monolithic SPST CMOS Analog Switches



GENERAL DESCRIPTION

The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Intersil's new 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to 30V peak-to-peak in the OFF state, the DG201A/DG202 offer the advantages of low on resistance ($\leq 175\Omega$), wide input signal range ($\pm 15V$) and provide both TTL and CMOS compatibility.

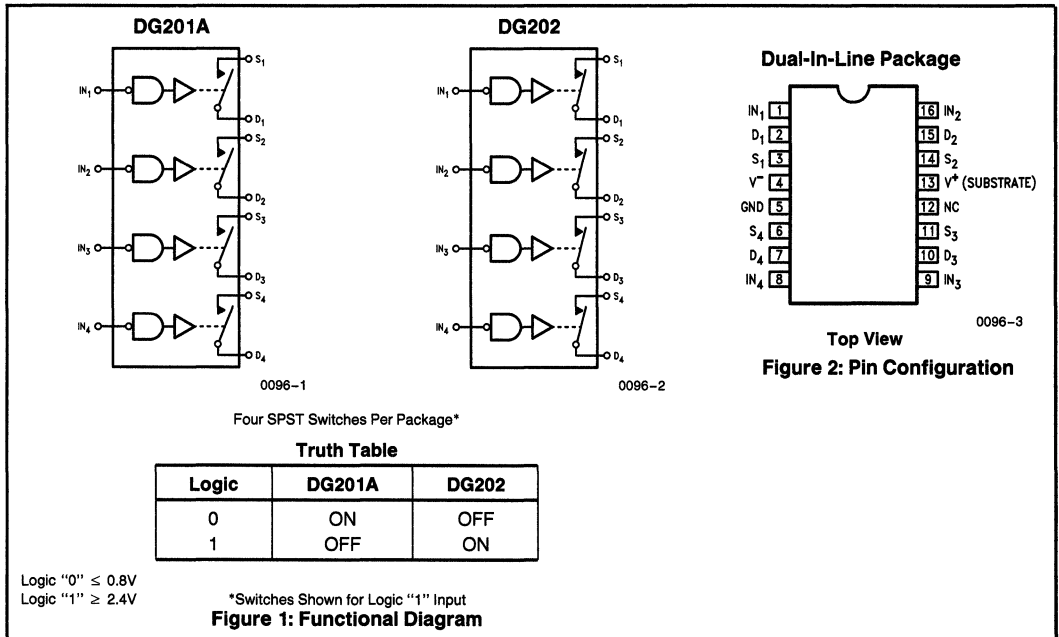
The DG201A/DG202 are specification and pin-out compatible with the industry standard devices.

FEATURES

- $\pm 15V$ Input Signal Range
- Low $R_{DS(on)}$ ($\leq 175\Omega$)
- TTL, CMOS Compatible
- Latch Proof
- True Second Source
- 44V Maximum Supply Ratings
- Logic Inputs Accept Negative Voltages

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG201AAK	-55°C to +125°C	16-Pin Cerdip
DG201ABK	-25°C to +85°C	16-Pin Cerdip
DG201ACK	0°C to +70°C	16-Pin Cerdip
DG201ACJ	0°C to +70°C	16-Pin Plastic DIP
DG202AK	-55°C to +125°C	16-Pin Cerdip
DG202BK	-25°C to +85°C	16-Pin Cerdip
DG202CK	0°C to +70°C	16-Pin Cerdip
DG202CJ	0°C to +70°C	16-Pin Plastic DIP



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻	44V
V ⁻ to Ground	-25V
V _{in} to Ground (Note 1)	(V ⁻ - 2V), (V ⁺ + 2V)
V _S or V _D to V ⁺ (Note 1)	+2, (V ⁻ - 2V)
V _S or V _D to V ⁻ (Note 1)	-2, (V ⁺ + 2V)
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	70 mA
Operating Temperature	
C Suffix	0°C to +70°C
B Suffix	-25°C to +85°C
A Suffix	-55°C to +125°C

Storage Temperature	
C Suffix	-65°C to +125°C
A & B Suffix	-65°C to +150°C
Lead Temperature (Soldering, 10s)	300°C
Power Dissipation*	
CERDIP Package**	900 mW
Plastic Package***	470 mW
*Device mounted with all leads soldered or welded to PC board.	
**Derate 12 mW/°C above 75°C	
***Derate 6.5 mW/°C above 25°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS V⁺ = 15V, V⁻ = -15V, GND = 0V, T_A = 25°C

Symbol	Parameter	Test Conditions	DG201AA/DG202A			DG201AB, C/DG202B, C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH									
V _{ANALOG}	Analog Signal Range		-15		15	-15		15	V
R _{DS(on)}	Drain Source On Resistance	V _D = ±10V, V _{in} = 0.8V (DG201A) I _S = 1 mA, V _{in} = 2.0V (DG202)		115	175		115	200	Ω
I _{S(off)}	Source OFF Leakage Current	V _{in} = 2.4V (DG201A) V _{in} = 0.8V (DG202)	V _S = 14V, V _D = -14V	0.01	1.0	0.01	5.0		nA
I _{D(off)}	Drain OFF Leakage Current	V _{in} = 0.8V (DG202)	V _S = -14V, V _D = 14V	-1.0	-0.02	-5.0	-0.02		nA
			V _S = 14V, V _D = -14V	-1.0	-0.02	-5.0	-0.02		
I _{D(on)} (Note 4)	Drain ON Leakage Current	V _{in} = 0.8V (DG201A) V _{in} = 2.4V (DG202)	V _D = V _S = 14V		0.1	1.0	0.1	5.0	μA
			V _D = V _S = -14V	-1.0	-0.15	-5.0	-0.15		
INPUT									
I _{INH}	Input Current with Voltage High	V _{in} = 2.4V	-1.0	-0.0004		-1.0	-0.0004		μA
		V _{in} = 15V		0.003	1.0	0.003	1.0		
I _{INL}	Input Current with Voltage Low	V _{in} = 0V	-1.0	-0.0004		-1.0	-0.0004		μA

NOTE 1: Signals on V_S, V_D, or V_{in} exceeding V⁺ or V⁻ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

4: I_{D(on)} is leakage from driver into ON switch.

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25^\circ C$ (Continued)

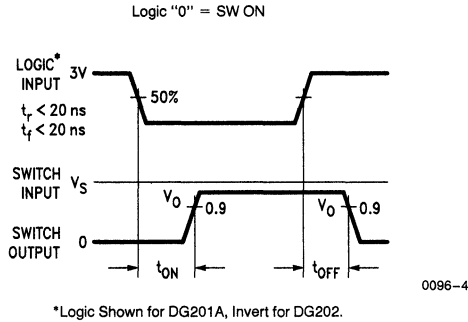
Symbol	Parameter	Test Conditions	DG201AA/DG202A			DG201AB, C/DG202B, C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
DYNAMIC									
t_{on}	Turn-ON Time	See Figure 3		480	600		480	600	ns
t_{off}	Turn-OFF Time			370	450		370	450	ns
Q	Charge Injection	$C_L = 1000 \text{ pF}, R_S = 0, V_S = 0V$		20			20		pC
$C_{S(off)}$	Source OFF Capacitance	$f = 140 \text{ kHz}, V_{in} = 5V, V_S = 0V$		5.0			5.0		pF
$C_{D(off)}$	Drain OFF Capacitance	$f = 140 \text{ kHz}, V_{in} = 5V, V_D = 0V$		5.0			5.0		pF
$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	$f = 140 \text{ kHz}, V_{in} = 0V, V_S = V_D = 0V$		16			16		pF
DIRR	OFF Isolation	$V_{in} = 5V, Z_L = 75\Omega$		70			70		dB
CCRR	Crosstalk (Channel to Channel)	$V_S = 2.0V, f = 100 \text{ kHz}$		90			90		
SUPPLY									
I^+	Positive Supply Current	All Channels ON or OFF		0.9	2		0.9	2	mA
I^-	Negative Supply Current		-1	-0.3		-1	-0.3		mA
$T_A =$ over operating temperature range									
SWITCH									
V_{ANALOG}	Analog Signal Range		-15		15	-15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	$V_D = \pm 10V, V_{in} = 0.8V$ (DG201A) $I_S = 1 \text{ mA}, V_{in} = 2.4V$ (DG202)			250			250	Ω
$I_{S(off)}$	Source OFF Leakage Current	$V_{in} = 2.4V$ (DG201A) $V_{in} = 0.8V$ (DG202)	$V_S = 14V, V_D = -14V$		100		100		nA
$I_{D(off)}$	Drain OFF Leakage Current	$V_S = -14V, V_D = 14V$	-100			-100			
$I_{D(on)}$ (Note 4)	Drain ON Leakage Current	$V_{in} = 0.8V$ (DG201A) $V_{in} = 2.4V$ (DG202)	$V_D = V_S = 14V$		200		200		μA
		$V_D = V_S = -14V$	-200			-200			
INPUT									
I_{INH}	Input Current with Voltage High	$V_{in} = 2.4V$	-10			-10			μA
		$V_{in} = 15V$			10		10		
I_{INL}	Input Current with Voltage Low	$V_{in} = 0V$	-10			-10			μA

- NOTE 1:** Signals on $V_S, V_D,$ or V_{in} exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- 2:** Typical values are for design aid only, not guaranteed and not subject to production testing.
- 3:** The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
- 4:** $I_{D(on)}$ is leakage from driver into ON switch.

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NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



$$V_O = V_S \frac{R_L}{R_L + R_{DS(on)}}$$

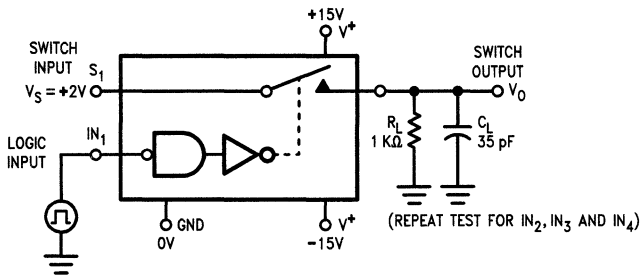
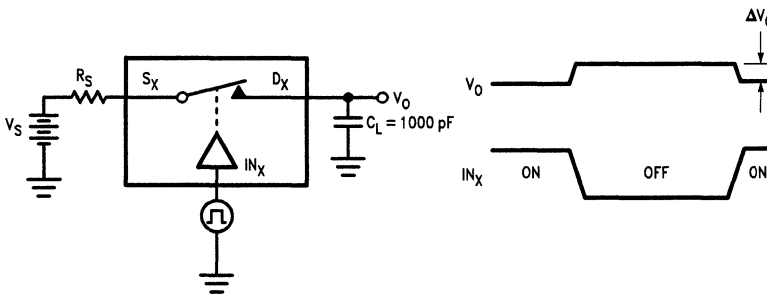


Figure 3: t_{on} and t_{off} Switching Test

0096-5

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ΔV_O = measured voltage error due to charge injection
 The error voltage in coulombs is $\Delta Q = C_L = \Delta V_O$.

Figure 4: Charge Injection Test Circuit

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NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS (Continued)

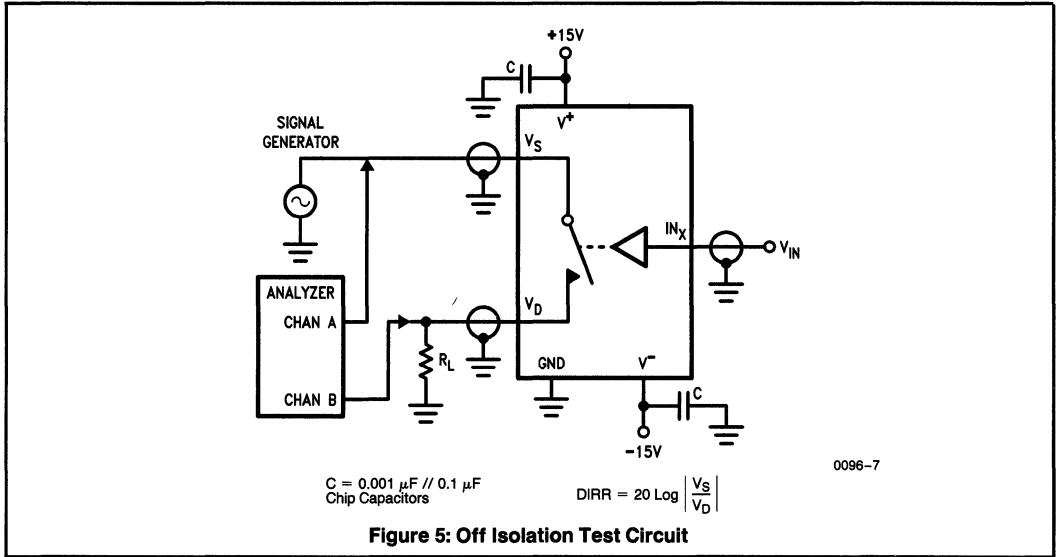


Figure 5: Off Isolation Test Circuit

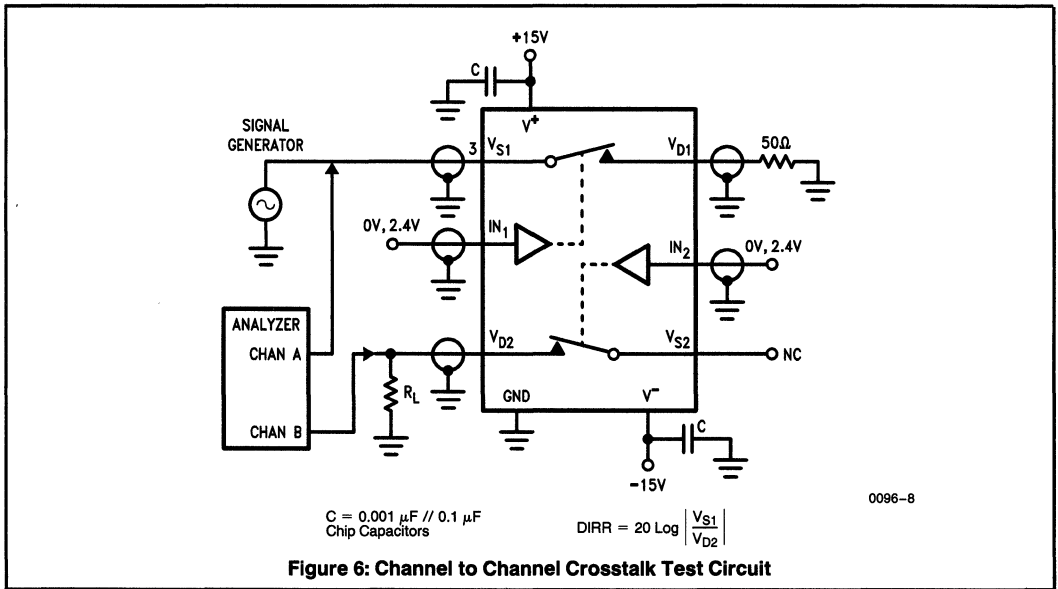


Figure 6: Channel to Channel Crosstalk Test Circuit

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NOTE: All typical values have been characterized but are not tested.

DG211/DG212

SPST 4-Channel Analog Switch



DG211/DG212

GENERAL DESCRIPTION

The DG211 and DG212 are low cost, CMOS monolithic, QUAD SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

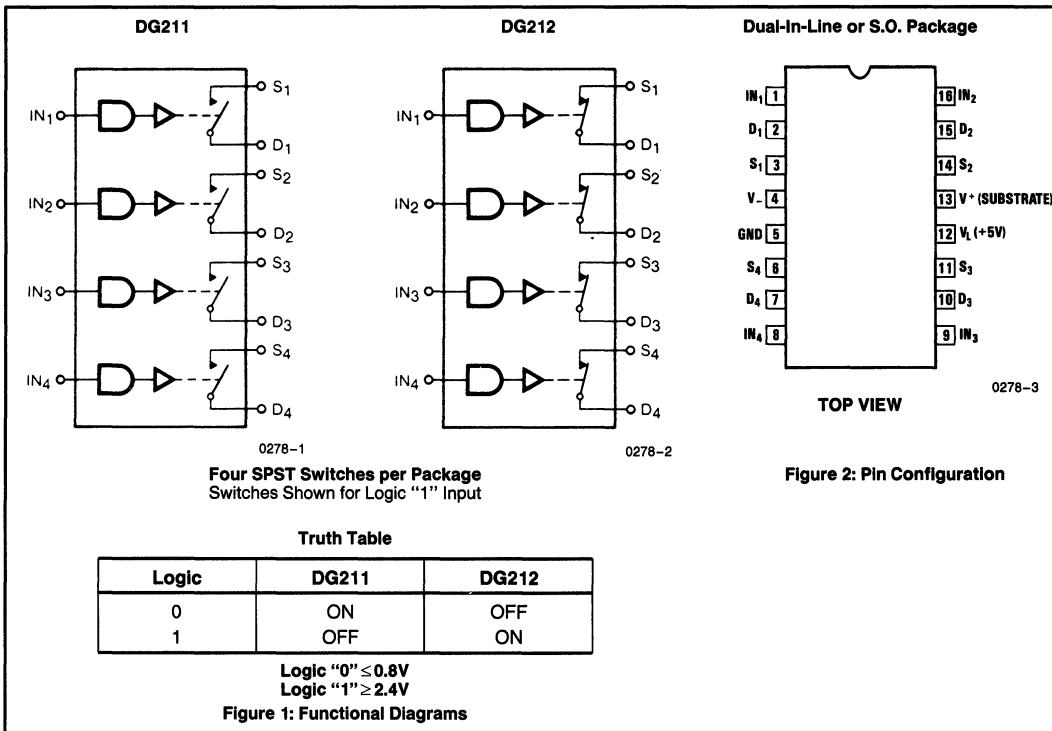
DG211 and DG212 are available in 16-pin Dual-In-Line plastic packages or 16-pin small outline packages and are rated for operation over 0°C to 70°C.

FEATURES

- Switches $\pm 15V$ Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- $R_{ON} \leq 175 \text{ Ohm}$

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG211CJ DG212CJ	0°C to +70°C 0°C to +70°C	16-Pin Plastic DIP 16-Pin Plastic DIP
DG211CY	0°C to +38°C	16-Pin S.O.
DG211CY	0°C to +38°C	16-Pin S.O.



Four SPST Switches per Package
Switches Shown for Logic "1" Input

Truth Table

Logic	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" $\leq 0.8V$
Logic "1" $\geq 2.4V$

Figure 1: Functional Diagrams

8

DG211/DG212



ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻	44V
V _{IN} to Ground	V ⁻ , V ⁺
V _L to Ground	-0.3V, 25V
V _S or V _D to V ⁺	0, -36V
V _S or V _D to V ⁻	0, 36V
V ⁺ to Ground	25V
V ⁻ to Ground	-25V
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D	70mA
(Pulsed at 1msec, 10% duty cycle max)	70mA
Storage Temperature	-65°C to +125°C

Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation (Package)*	16 Pin Plastic DIP**
.....	470mW

* Device mounted with all leads soldered or welded to PC board.
 ** Derate 6.5mW/°C above 25°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

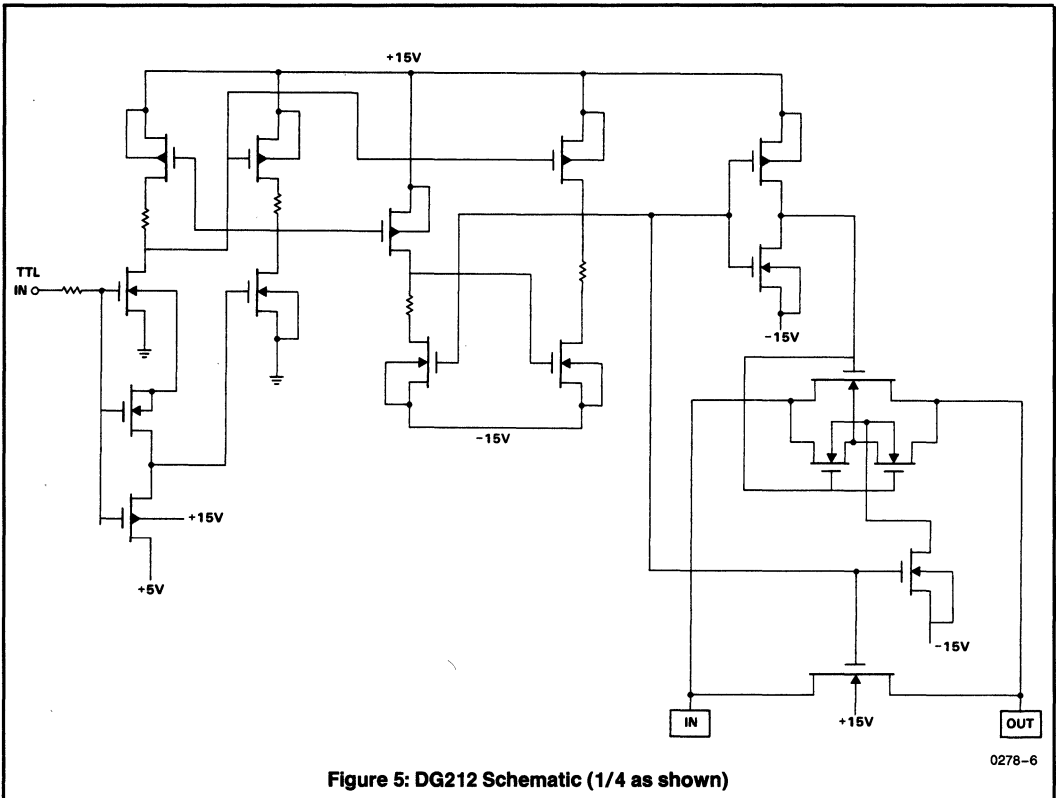
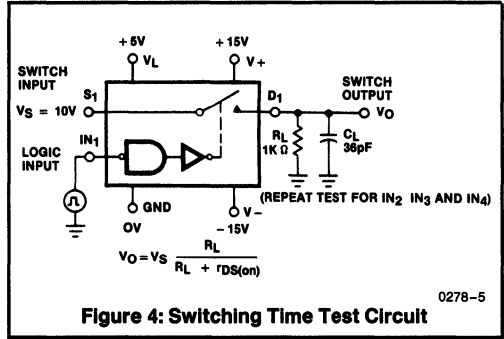
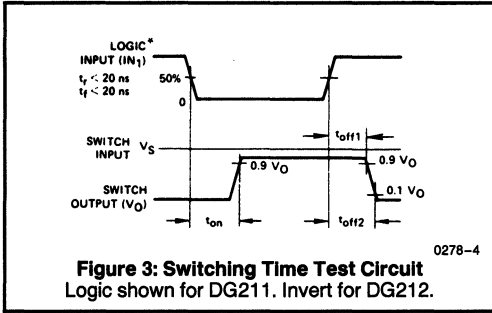
Symbol	Parameter	Test Conditions V ₁ = +15V, V ₂ = -15V, V _L = +5V, GND	Limits			Units	
			MIN ¹	TYP ²	MAX		
SWITCH							
V _{ANALOG}	Analog Signal Range	V ⁻ = -15V, V _L = +5V	-15		15	V	
R _{DS(ON)}	Drain-Source On Resistance	V _D = ±10V, V _{IN} = 2.4V — DG212 I _S = 1mA, V _{IN} = 0.8V — DG211		150	175	Ω	
I _{S(off)}	Source OFF Leakage Current	V _{IN} = 2.4V DG211	V _S = 14V, V _D = -14V	0.01	5.0	nA	
I _{D(off)}	Drain OFF Leakage Current	V _{IN} = 0.8V DG212	V _S = -14V, V _D = 14V	-5.0	-0.02		
			V _D = 14V, V _S = -14V		0.01		5.0
			V _D = -14V, V _S = 14V	-5.0	-0.02		
I _{D(ON)}	Drain ON Leakage Current ³	V _S = V _D = -14V, V _{IN} = 0.8V, DG211 V _{IN} = 2.4V, DG212		0.1	5.0		
			-5.0	-0.15			
INPUT							
I _{INH}	Input Current With Input Voltage High	V _{IN} = 2.4V	-10	-0.0004		μA	
		V _{IN} = 15V		0.003	1.0		
I _{INL}	Input Current With Input Voltage Low	V _{IN} = 0V	-1.0	-0.0004			
DYNAMIC							
t _{on}	Turn-ON Time	See Switching Time Test Circuit ⁵ V _S = 10V, R _L = 1kΩ, C _L = 35pF		460	1000	ns	
t _{off1}	Turn-OFF Time			360	500		
t _{off2}				450			
C _{S(off)}	Source OFF Capacitance	V _S = 0V, V _{IN} = 5V, f = 1MHz ²		5		pF	
C _{D(off)}	Drain OFF Capacitance	V _D = 0V, V _{IN} = 5V, f = 1MHz ²		5			
C _{D+S(on)}	Channel ON Capacitance	V _D = V _S = 0V, V _{IN} = 0V, f = 1MHz ²		16			
OIRR	OFF Isolation ⁴	V _{IN} = 5V, R _L = 1kΩ, C _L = 15pF, V _S = 1VRMS, f = 100kHz ²		70		dB	
CCRR	Crosstalk (Channel to Channel)				90		
SUPPLY							
I ⁺	Positive Supply Current	V _{IN} = 0 and 2.4V		.1	10	μA	
I ⁻	Negative Supply Current			.1	10		
I _L	Logic Supply Current			.1	10		

- NOTES:**
- The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
 - For design reference only, not 100% tested.
 - I_{D(on)} is leakage from driver into "ON" switch.
 - OFF Isolation = 20 log $\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.
 - Switching times only sampled.

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NOTE: All typical values have been characterized but are not tested.

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



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NOTE: All typical values have been characterized but are not tested.

DG300A/DG301A/ DG302A/DG303A

TTL Compatible CMOS Analog Switches



GENERAL DESCRIPTION

The DG300A–303A family of monolithic CMOS switches are a truly compatible second source of the original manufacturer. The switches are latch-proof and are designed to block signals up to 30 volts peak-to-peak when OFF. Featuring low leakage and low power consumption, these switches are ideally suited for precision application in instrumentation, communication, data acquisition and battery-powered applications. Other key features include Break-Before-Make switching, TTL and CMOS compatibility, and low ON resistance. Single supply operation (for positive switch voltages) is possible by connecting V^- to 0 volts.

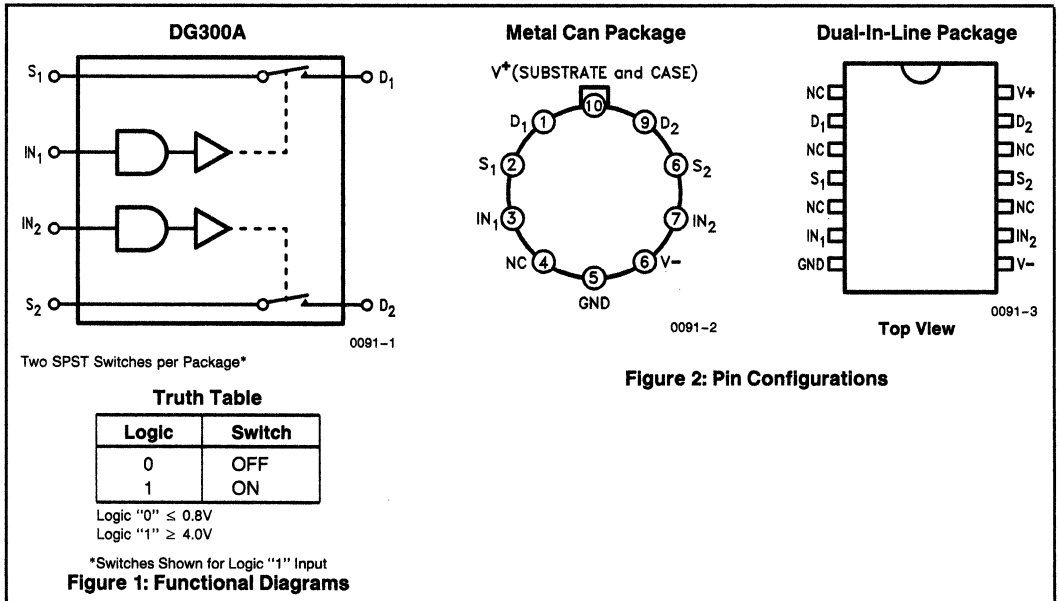
The DG300A–DG303A family is available over commercial, industrial, and military temperature range.

FEATURES

- Low Power Consumption
- Break-Before-Make Switching t_{off} 130 ns, t_{on} 150 ns Typical
- TTL, CMOS Compatible
- Low $R_{DS(on)}$ ($\leq 50\Omega$)
- Single Supply Operation
- True Second Source

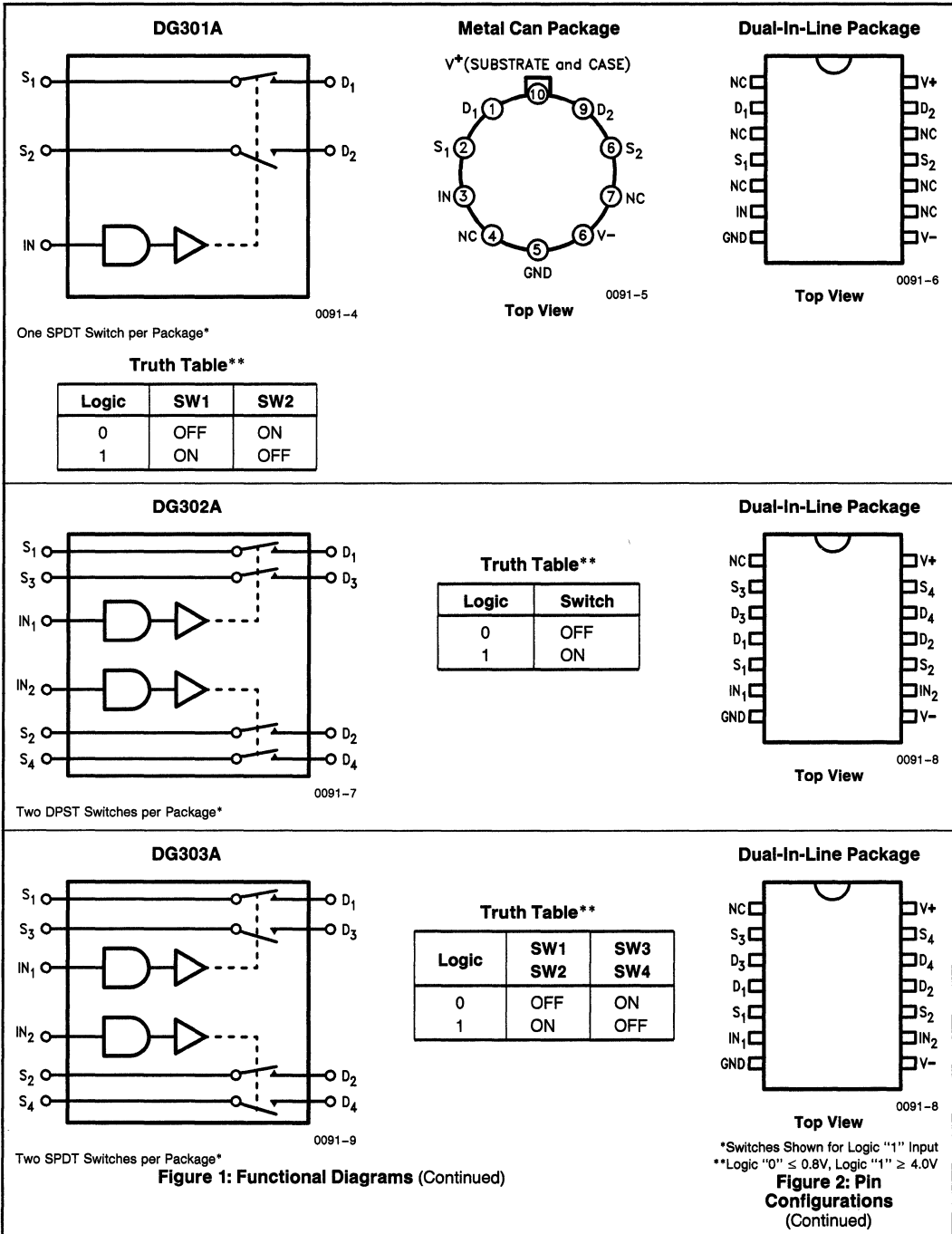
ORDERING INFORMATION

Part Number	Temperature Range	Package
DG300A/301A/302A/303AAK	-55°C to +125°C	14-Pin Cerdip
DG300A/301A/302A/303ABK	-25°C to +85°C	14-Pin Cerdip
DG300A/301A/302A/303ACK	0°C to +70°C	14-Pin Cerdip
DG300A/301A/302A/303ACJ	0°C to +70°C	14-Pin Plastic Dip
DG300A/301AAA	-55°C to +125°C	10-Pin Metal Can
DG300A/301ABA	-25°C to +85°C	10-Pin Metal Can
DG300A/301ACA	0°C to +70°C	10-Pin Metal Can



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NOTE: All typical values have been characterized but are not tested.



DG300A/DG301A/DG302A/DG303A



ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻	44V
V ⁻ to Ground	-25V
V _{IN} to Ground (Note 1)	(V ⁻ - 2V), (V ⁺ + 2V)
V _S or V _D to V ⁺ (Note 1)	+2, (V ⁻ - 2V)
V _S or V _D to V ⁻ (Note 1)	-2, (V ⁺ + 2V)
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Operating Temperature	
C Suffix	0°C to +70°C
B Suffix	-25°C to +85°C
A Suffix	-55°C to +125°C

Storage Temperature	
C Suffix	-65°C to +125°C
A & B Suffix	-65°C to +150°C
Lead Temperature (Soldering, 10s)	300°C
Power Dissipation*	
CERDIP Package**	825 mW
Plastic Package***	470 mW
Metal Can****	450 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 11 mW/°C above 75°C

***Derate 6.5 mW/°C above 25°C

****Derate 6 mW/°C above 75°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS V⁺ = 15V, V⁻ = -15V, GND = 0V, T_A = 25°C

Symbol	Parameter	Test Conditions	DG300A-DG303AA			DG300A-DG303AB/C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH									
V _{ANALOG}	Analog Signal Range	I _S = 10 mA, V _{IN} = 0.8V or 4V	-15		15	-15		15	V
R _{DS(on)}	Drain-Source ON Resistance	V _{IN} = 0.8V or 4.0V	I _S = -10 mA, V _D = 10V	30	50		30	50	Ω
			I _S = 10 mA, V _D = -10V	30	50		30	50	
I _{S(off)}	Source OFF Leakage Current		V _S = 14V, V _D = -14V	0.1	1		0.1	5	nA
			V _S = -14V, V _D = 14V	-1	-0.1		-5	-0.1	
I _{D(off)}	Drain OFF Leakage Current	V _S = -14V, V _D = 14V	0.1	1		0.1	5	nA	
		V _S = 14V, V _D = -14V	-1	-0.1		-5	-0.1		
I _{D(on)}	Drain ON Leakage Current	V _D = V _S = 14V	0.1	1		0.1	5	nA	
		V _D = V _S = -14V	-2	-0.1		-5	-0.1	nA	
INPUT									
I _{INH}	Input Current w/Voltage High	V _{IN} = 5.0V	-1	-0.001		-1	-0.001		μA
		V _{IN} = 15V		0.001	1		0.001	1	
I _{INL}	Input Current w/Voltage Low	V _{IN} = 0V	-1	-0.001		-1	-0.001		μA
DYNAMIC									
t _{on}	Turn-ON Time	See Figure 5		150	300		150		ns
t _{off}	Turn-OFF Time			130	250		130		ns
t _{on-toff}	Break-Before-Make Interval	See Figure 4 DG301A/303A		50			50		ns
Q	Charge Injection	C _L = 1 μF, R _S = 0, V _S = 0		3			3		mV
C _{S(off)}	Source OFF Capacitance	f = 1 MHz, V _S = 0		14			14		pF
C _{D(off)}	Drain OFF Capacitance	V _{IN} = 0.8V or 4.0V, V _D = 0		14			14		pF
C _{D(on)} + C _{S(on)}	Channel ON Capacitance	V _{IN} = 4.0V, V _S = V _D = 0		40			40		pF

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25^\circ C$ (Continued)

Symbol	Parameter	Test Conditions	DG300A-DG303AA			DG300A-DG303AB/C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
DYNAMIC (Continued)									
C_{IN}	Input Capacitance	$f = 1\text{ MHz}$	$V_{IN} = 0$	6		6		pF	
			$V_{IN} = 15V$	7		7			
DIRR (Note 4)	OFF Isolation	$V_{IN} = 0, R_L = 1k$ $V_S = 1V_{RMS}, f = 500\text{ kHz}$		62		62		dB	
CCRR	Crosstalk (Channel to Channel)			74		74			
SUPPLY									
I^+	Positive Supply Current	$V_{IN} = 4V$ (One Input) (All Others = 0)		0.23	0.5		0.23	0.5	mA
I^-	Negative Supply Current		-10	-0.001		-10	-0.001		μA
I^+	Positive Supply Current	$V_{IN} = 0.8V$ (All Inputs)		0.001	10		0.001	10	μA
I^-	Negative Supply Current		-10	-0.001		-10	-0.001		μA

T_A = over operating temperature range

Symbol	Parameter	Test Conditions	DG300A-DG303AA			DG300A-DG303AB/C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH									
V_{ANALOG}	Analog Signal Range	$I_S = 10\text{ mA}, V_{IN} = 0.8V$ or $4V$	-15		15	-15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	$I_S = -10\text{ mA}, V_D = 10V$			75			75	Ω
			$I_S = 10\text{ mA}, V_D = -10V$			75			
$I_{S(off)}$	Source OFF Leakage Current	$V_{IN} = 0.8V$ or $V_{IN} = 4.0V$	$V_S = 14V, V_D = -14V$		100			100	nA
			$V_S = -14V, V_D = 14V$	-100			-100		
$I_{D(off)}$	Drain OFF Leakage Current	$V_{IN} = 0.8V$ or $V_{IN} = 4.0V$	$V_S = -14V, V_D = 14V$		100			100	nA
			$V_S = 14V, V_D = -14V$	-100			-100		
$I_{D(on)}$	Drain ON Leakage Current	$V_{IN} = 0.8V$ or $V_{IN} = 4.0V$	$V_D = V_S = 14V$		100			100	nA
			$V_D = V_S = -14V$	-200			-200		
INPUT									
I_{INH}	Input Current w/Voltage High	$V_{IN} = 5.0V$	-1						μA
		$V_{IN} = 15V$			1				
I_{INL}	Input Current w/Voltage Low	$V_{IN} = 0V$	-1					μA	
SUPPLY									
I^+	Positive Supply Current	$V_{IN} = 4V$ (One Input) (All Others = 0)			1				mA
I^-	Negative Supply Current		-100						μA
I^+	Positive Supply Current	$V_{IN} = 0.8V$ (All Inputs)			100				μA
I^-	Negative Supply Current		-100						μA

NOTE 1: Signals on V_S, V_D , or V_{IN} exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

2: For design only, not 100% tested.

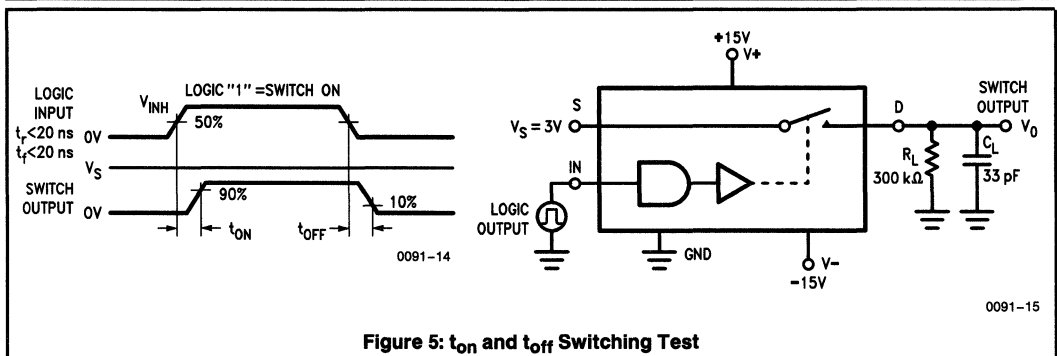
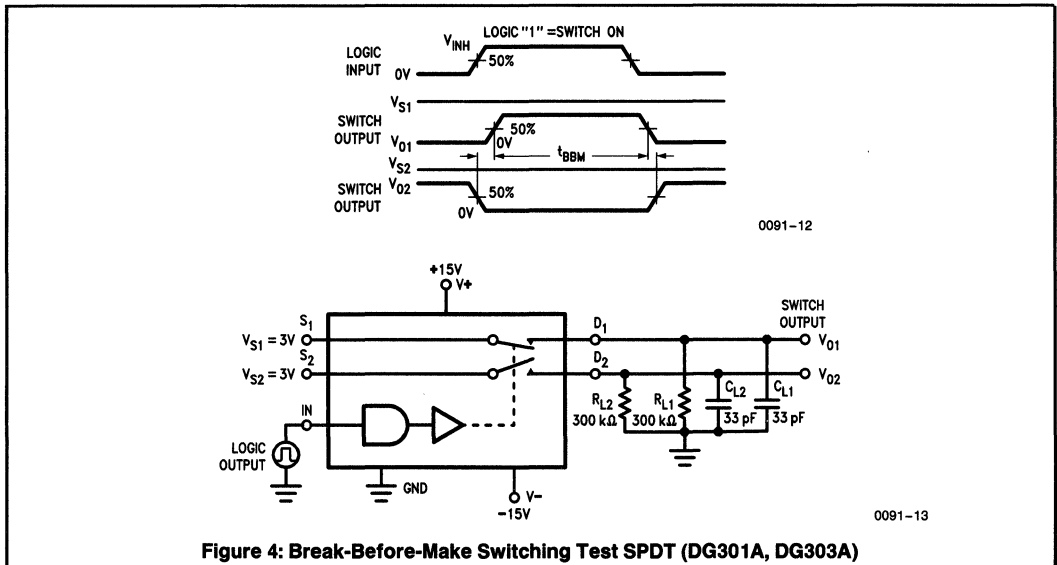
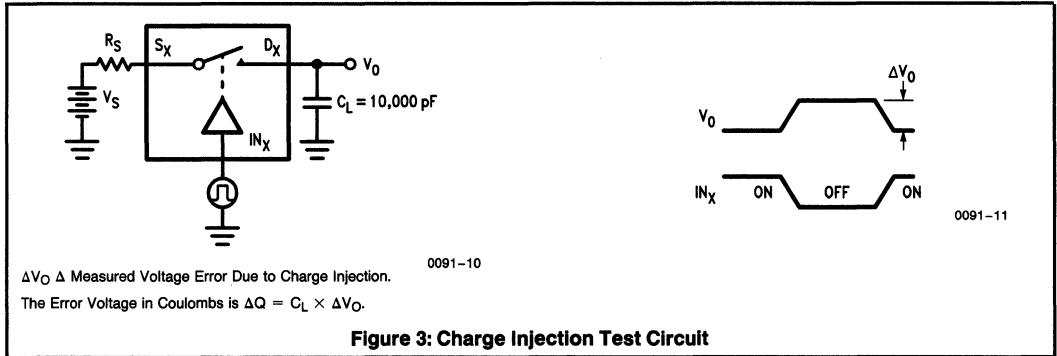
3: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4: OFF isolation = $20 \log V_S/V_D$, where V_S = input to OFF switch, and V_D = output.

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NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION



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NOTE: All typical values have been characterized but are not tested.

DGM181-186, DGM189-191

High-Speed CMOS Analog Switch



DGM181-186, DGM189-191

GENERAL DESCRIPTION

The DGM181 family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to combine the speed of the hybrid DG181 family with the reliability and low power consumption of a monolithic CMOS construction. These devices, therefore, are a cost effective replacement for the DG181 family.

The DGM181 family has a high state threshold of 2.4V; and a low state of +0.8V.

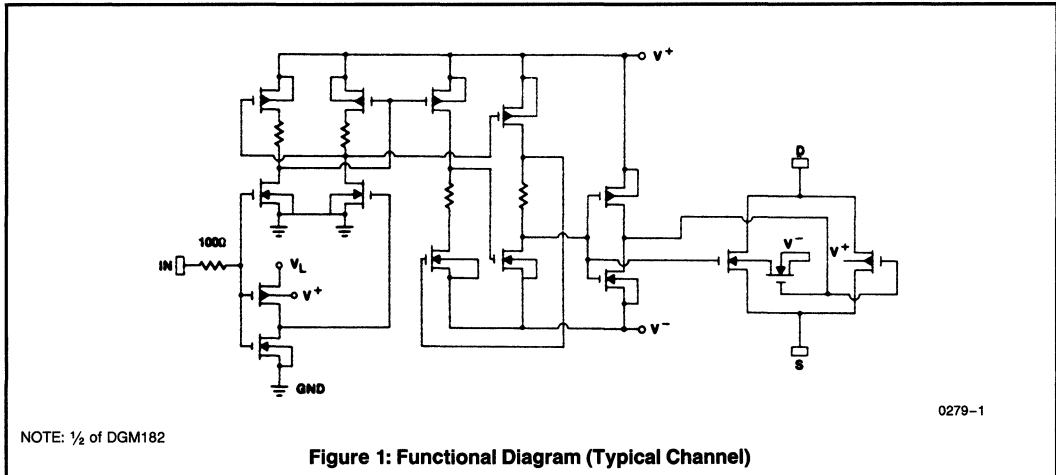
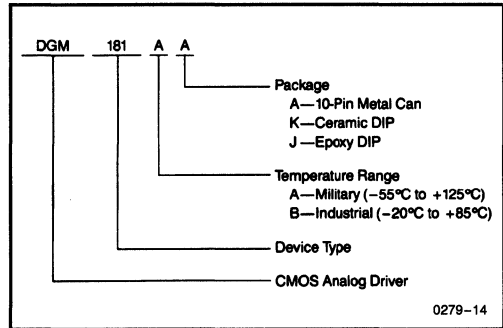
Very low quiescent power is dissipated in either the ON or OFF state of the switch. Maximum power supply current is 10 μ A from any supply, and typical quiescent currents are in the 10nA range. OFF leakages are typically less than 200pA at 25°C.

ORDERING INFORMATION

Type	Standard Part Number	$t_{DS(on)}$ Max at 25°C
Dual SPST	DGM181BX	50
	DGM182AX	50
	DGM182BX	75
Dual DPST	DGM184BX	50
	DGM185AX	50
	DGM185BX	75
Dual SPDT	DGM190BX	50
	DGM191AX	50
	DGM191BX	75

FEATURES

- Pin and Function Replacement for DG181 Family
- Meets or Exceeds All DG181 Family Specifications With Monolithic Reliability
- Low Power Consumption
- 1nA Leakage From Signal Channel in Both ON and OFF States
- TTL, DTL, RTL Direct Drive Capability
- t_{on} , t_{off} < 150ns, Break-Before-Make Action
- Crosstalk and Open Load Switch Isolation > 50dB at 10MHz (75 Ω Load)

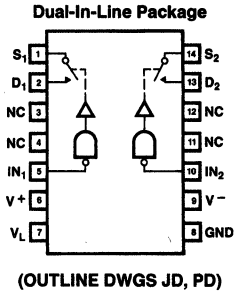
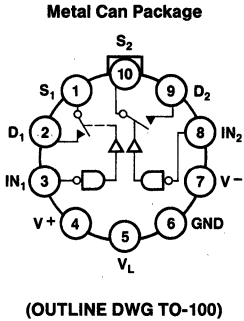


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NOTE: All typical values have been characterized but are not tested.

DGM181-186
DGM189-191

DUAL SPST (DGM181, 182)

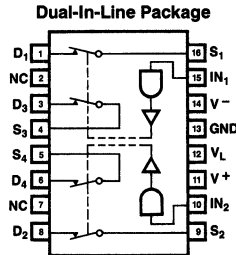


0279-2

0279-4

SWITCH STATES ARE FOR LOGIC "1" INPUT

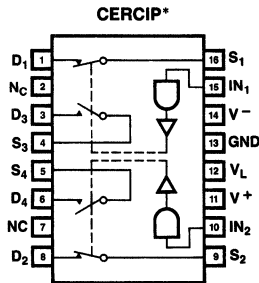
DUAL DPST (DGM184, 185)



0279-6

SWITCH STATES ARE FOR LOGIC "1" INPUT

DUAL SPDT (DGM190, 191)



0279-11

SWITCH STATES ARE FOR LOGIC "1" INPUT

Figure 2: Pin Configuration and Switching State Diagram

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NOTE: All typical values have been characterized but are not tested.

DGM181-186 DGM189-191



DGM181-186, DGM189-191

ABSOLUTE MAXIMUM RATINGS

V ⁺ -V ⁻	36V
V ⁻ -V _D	33V
V _D -V ⁻	33V
V _D -V _S	28V
V _L -V ⁻	36V
V _L -V _{IN}	30V
V _L -V _{GND}	20V
V _{IN} -V _{GND}	20V
GND-V ⁻	27V

GND-V _{IN}	20V
Current (Any Terminal)	30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation*	450 (TW), 750 (FLAT), 825 (DIP)mW

* Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V⁺ = +15V, V⁻ = -15V, V_L = 5V, unless noted)

Parameter	Device No.	Test Conditions (Note 1)	A Series			B Series			Units
			-55°C	+25°C	+125°C	-20°C	+25°C	+85°C	
SWITCH									
I _{S(off)}	DGM181, 184, 190	V _S = 7.5V, V _D = -7.5V V _{IN} = "OFF"		±1	100		±2.0	200	nA
	DGM182, 185, 191	V _S = 10V, V _D = -10V V _{IN} = "OFF"		±1	100		±2	200	nA
I _{D(off)}	DGM181, 184, 190	V _S = 7.5V, V _D = -7.5V V _{IN} = "OFF"		±1	100		±2	200	nA
	DGM182, 185, 191	V _S = 10V, V _D = -10V V _{IN} = "OFF"		±1	100		±2	200	nA
I _{D(on)} + I _{S(on)}	DGM181, 184, 190	V _D = V _S = -7.5V, V _{IN} = "ON"		±2	±200		±5	500	nA
	DGM182, 185, 191	V _D = V _S = -10V, V _{IN} = "ON"		±2	±200		±5	500	nA
INPUT									
I _{INL}	ALL	V _{IN} = 0V		±1.0	20		10	20	μA
I _{INH}	ALL	V _{IN} = 5V		±1.0	20		10	20	μA
DYNAMIC									
t _{on}	DGM181, 184, 190 DGM182, 185, 191	See switching time test circuit		450			500		ns
t _{off}	ALL			250			275		
C _{S(off)}	DGM181, 182, 184, 185, 190, 191	V _S = -5V, I _D = 0, f = 1MHz		5pF typical					pF
C _{D(off)}		V _D = +5V, I _S = 0, f = 1MHz		6pF typical					
C _{D(on)} + C _{S(on)}		V _D = V _S = 0, f = 1MHz		11pF typical					
OFF Isolation		R _L = 75Ω, C _L = 3pF		Typically > 50dB at 10MHz					
SUPPLY									
I ⁺	ALL	V _{IN} = 5V	10	10	100		100		μA
I ⁻	ALL		10	10	100		100		
I _L	ALL		10	10	100		100		
I _{GND}	ALL		10	10	100		100		
I ⁺	ALL	V _{IN} = 0V	10	10	100		100		
I ⁻	ALL		10	10	100		100		
I _L	ALL		10	10	100		100		
I _{GND}	ALL		10	10	100		100		

Note: 1. See Switching State Diagrams for V_{IN} and V_{IN} "OFF" Test Conditions.

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NOTE: All typical values have been characterized but are not tested.

DGM181-186 DGM189-191



ELECTRICAL CHARACTERISTICS MAXIMUM RESISTANCES $r_{DS(ON)}$

Device Number	Conditions (Note 1) $V^+ = 15V, V^- = -15V, V_L = 5V$		Military Temperature			Industrial Temperature			Units
			-55°C	+25°C	+125°C	-20°C	+25°C	+85°C	
DGM181	$V_D = -7.5V$	$I_S = -10mA$	-	-	-	50	50	75	Ω
DGM182	$V_D = -10V$		50	50	75	75	75	100	Ω
DGM184	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DGM185	$V_D = -10V$		50	50	75	75	75	100	Ω
DGM190	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DGM191	$V_D = -10V$		50	50	75	75	75	100	Ω

APPLICATION COMMENT: The charge injection in these switches is of opposite polarity to that of the standard DG180 family, but considerably smaller.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state

output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

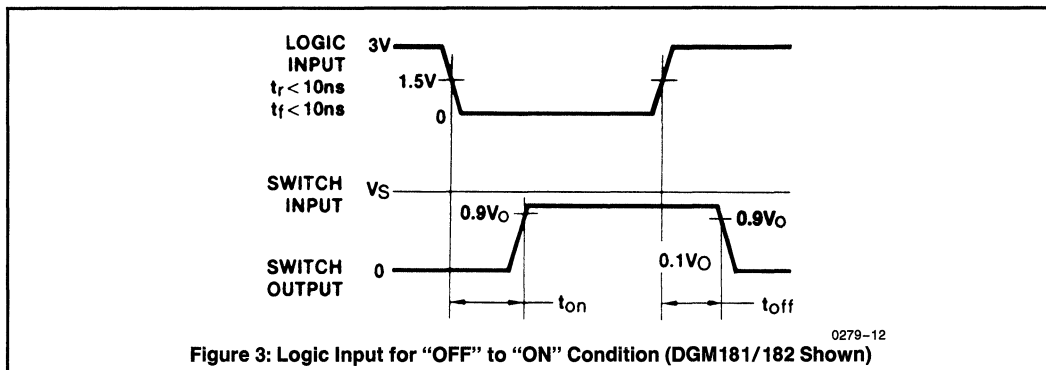


Figure 3: Logic Input for "OFF" to "ON" Condition (DGM181/182 Shown)

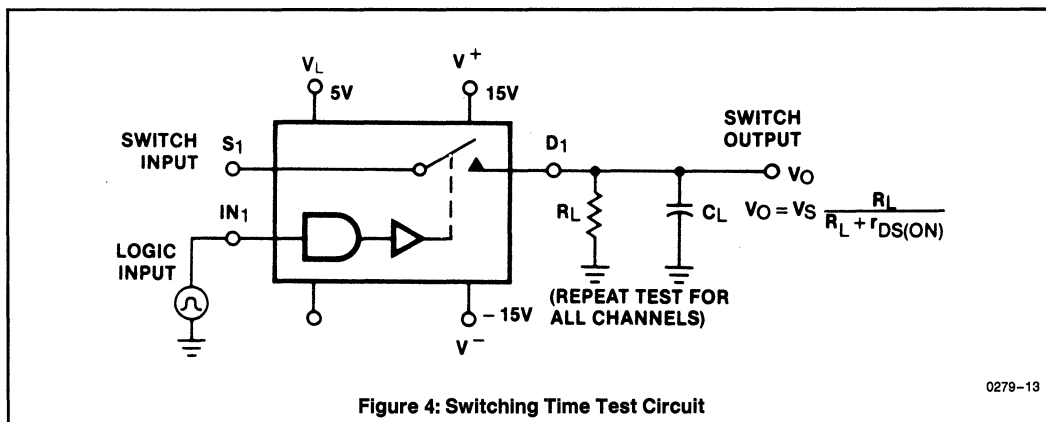


Figure 4: Switching Time Test Circuit

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NOTE: All typical values have been characterized but are not tested.

DGM181-186 DGM189-191



DGM181-186, DGM189-191

SWITCH STATES

DUAL SPST DGM181/182

Test Conditions

DGM181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.4V	All Channels

DUAL DPST DGM184/185

Test Conditions

DGM184/185	
V_{IN} "ON" = 2.4V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

DUAL SPDT DGM190/191

Test Conditions

DGM190/191	
V_{IN} "ON" = 2.4V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.4V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

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NOTE: All typical values have been characterized but are not tested.

IH311/IH312 High Speed SPST 4-Channel Analog Switch



GENERAL DESCRIPTION

The IH311 and IH312 are CMOS, monolithic, QUAD, SPST analog switches for use in high-speed switching applications for communications, instrumentation, process control and computer peripherals. Both devices provide true bi-directional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The IH311 and IH312 differ only in that the digital control logic is inverted, as shown in the truth table.

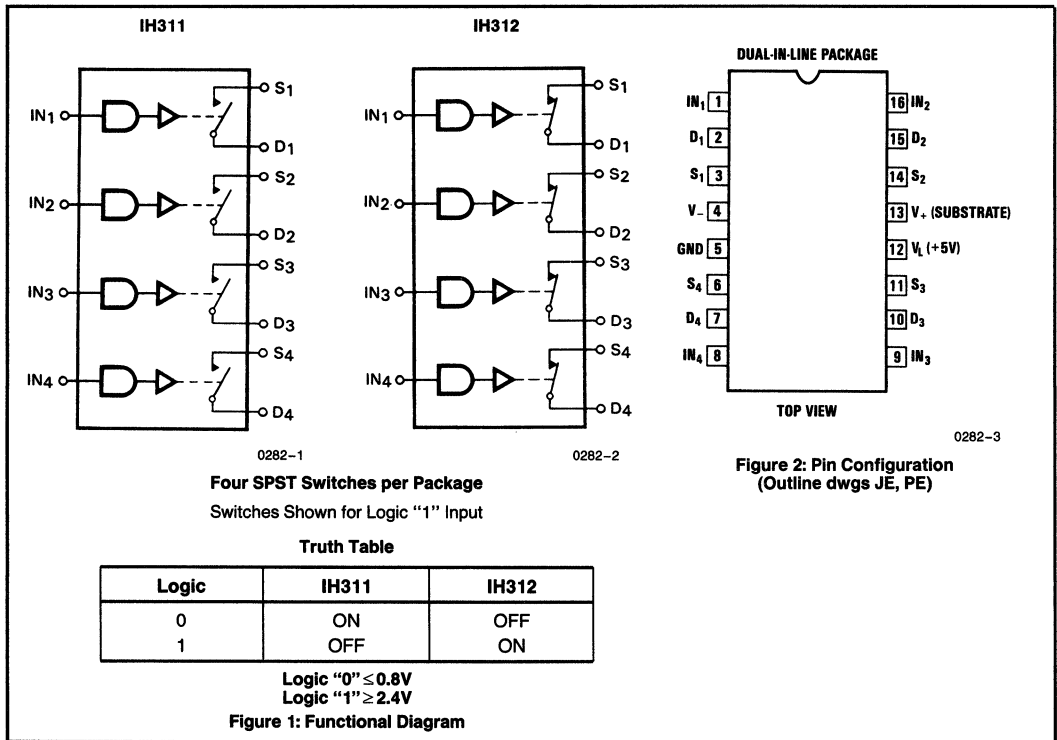
The IH311 and IH312 are available in 16-pin Dual-In-Line packages and are offered in both military and commercial temperature ranges.

FEATURES

- Switches $\pm 15V$ Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- $R_{ON} \leq 175 \text{ Ohm}$

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH311MJE	-55°C to +125°C	16 Pin CERDIP
IH311CJE	0°C to +70°C	16 Pin CERDIP
IH311CPE	0°C to +70°C	16 Pin Plastic DIP
IH312MJE	-55°C to +125°C	16 Pin CERDIP
IH312CJE	0°C to +70°C	16 Pin CERDIP
IH312CPE	0°C to +70°C	16 Pin Plastic DIP



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻	44V
V _{IN} to Ground	V ⁺ , V ⁺
V _L to Ground	-0.3V, 25V
V _S or V _D to V ⁺	0, -36V
V _S or V _D to V ⁻	0, 40V
V ⁺ to Ground	25V
V ⁻ to Ground	-25V
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA

Peak Current, S or D (Pulsed at 1msec, 10% duty cycle max)	70mA
Storage Temperature	-65°C to +125°C
Operating Temperature	-55°C to +125°C
Power Dissipation (Package)* 16 Pin Plastic DIP**	470mW

* Device mounted with all leads soldered or welded to PC board.
** Derate 6.5mW/°C above 25°C

ELECTRICAL CHARACTERISTICS — MILITARY TEMPERATURE RANGE

Symbol	Parameter	Test Conditions V ₁ = +15V, V ₂ = -15V V _L = 5V, GND	Limits			Units
			-55°C	+25°C	+125°C	
SWITCH						
V _{ANALOG}	Analog Signal Range	V ⁻ = -15V, V _L = +5V		±15		V
R _{DS(ON)}	Drain-Source On Resistance	V _D = ±10V, V _{IN} = 2.4V — IH312 I _S = 1mA, V _{IN} = 0.8V — IH311	150 175	150 175	200 250	Ω
I _{S(off)}	Source OFF Leakage Current	V _{IN} = 2.4V IH311 V _{IN} = 0.8V IH312	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V	±1	100	nA
I _{D(off)}	Drain OFF Leakage Current		V _D = 14V, V _S = -14V V _D = -14V, V _S = 14V	±1	100	
I _{D(ON)}	Drain ON Leakage Current ³	V _S = V _D = -14V, V _{IN} = 0.8V, IH311 V _{IN} = 2.4V, IH312		±2	200	
				±2	200	
INPUT						
I _{INH}	Input Current With Input Voltage High	V _{IN} = 2.4V V _{IN} = 15V	10 10	±1 ±1	10 10	μA
I _{INL}	Input Current With Input	V _{IN} = 0V	10	±1	10	
DYNAMIC						
t _{on}	Turn-ON Time	See Switching Time Test Circuit		300		ns
t _{off1}	Turn-OFF Time	V _S = 10V, R _L = 1kΩ, C _L = 35pF		150		
t _{off2}						
C _{S(off)}	Source OFF Capacitance	V _S = 0V, V _{IN} = 5V, f = 1MHz ²		5		pF
C _{D(off)}	Drain OFF Capacitance	V _D = 0V, V _{IN} = 5V, f = 1MHz ²		5		
C _{D + S(on)}	Channel ON Capacitance	V _D = V _S = 0V, V _{IN} = 0V, f = 1MHz ²		16		
OIRR	OFF Isolation ⁴	V _{IN} = 5V, R _L = 1kΩ, C _L = 15pF, V _S = 1VRMS, f = 100kHz ²		70		dB
CCRR	Crosstalk (Channel to Channel)			90		
SUPPLY						
I ⁺	Positive Supply Current	V _{IN} = 0 and 2.4V	10	1	10	μA
I ⁻	Negative Supply Current		10	1	10	
I _L	Logic Supply Current		10	1	10	

- NOTES: 1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. I_{D(ON)} is leakage from driver into "ON" switch.
4. OFF Isolation = 20log $\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻	44V
V _{IN} to Ground	V ⁺ , V ⁺
V _L to Ground	-0.3V, 25V
V _S or V _D to V ⁺	0, -36V
V _S or V _D to V ⁻	0, 40V
V ⁺ to Ground	25V
V ⁻ to Ground	-25V
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA

Peak Current, S or D (Pulsed at 1msec, 10% duty cycle max)	70mA
Storage Temperature	-65°C to +125°C
Operating Temperature	0°C to +70°C
Power Dissipation (Package)* 16 Pin Plastic DIP**	470mW

* Device mounted with all leads soldered or welded to PC board.
** Derate 6.5mW/°C above 25°C

ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE

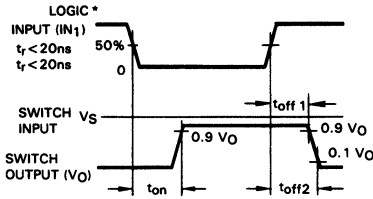
Symbol	Parameter	Test Conditions V ₁ = +15V, V ₂ = -15V, V _L = 5V, GND	Limits		Units
			+25°C	+70°C	
SWITCH					
V _{ANALOG}	Analog Signal Range	V ⁻ = -15V, V _L = +5V	±15		V
R _{DS(ON)}	Drain-Source On Resistance	V _D = ±10V, V _{IN} = 2.4V — IH212 I _S = 1mA, V _{IN} = 0.8V — IH211	175	200	Ω
I _{S(off)}	Source OFF Leakage Current	V _{IN} = 2.4V IH311 IH312	V _S = 14V, V _D = -14V ±5	100	nA
I _{D(off)}	Drain OFF Leakage Current	V _{IN} = 0.8V	V _S = -14V, V _D = 14V ±5	100	
I _{D(ON)}	Drain ON Leakage Current ³	V _S = V _D = -14V, V _{IN} = 0.8V, IH211 V _{IN} = 2.4V, IH212	V _D = 14V, V _S = -14V ±5	100	
			V _D = -14V, V _S = 14V ±5	100	
INPUT					
I _{IINH}	Input Current With Input Voltage High	V _{IN} = 2.4V	±1	-10	μA
		V _{IN} = 15V	±1	10	
I _{IINL}	Input Current With Input Voltage Low	V _{IN} = 0V	±1	-10	
DYNAMIC					
t _{on}	Turn-ON Time	See Switching Time Test Circuit ⁵ V _S = 10V, R _L = 1kΩ, C _L = 35pF	500		ns
t _{off1}	Turn-OFF Time		250		
t _{off2}					
C _{S(off)}	Source OFF Capacitance	V _S = 0V, V _{IN} = 5V, f = 1MHz ²	5		pF
C _{D(off)}	Drain OFF Capacitance	V _D = 0V, V _{IN} = 5V, f = 1MHz ²	5		
C _{D+S(on)}	Channel ON Capacitance	V _D = V _S = 0V, V _{IN} = 0V, f = 1MHz ²	16		
OIRR	OFF Isolation ⁴	V _{IN} = 5V, R _L = 1kΩ, C _L = 15pF, V _S = 1VRMS, f = 100kHz ²	70		dB
CCRR	Crosstalk (Channel to Channel)		90		
SUPPLY					
I ⁺	Positive Supply Current	V _{IN} = 0 and 2.4V	±1	10	μA
I ⁻	Negative Supply Current		±1	-10	
I _L	Logic Supply Current		±1	10	

- NOTES:** 1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For frequency reference only, not 100% tested.
3. I_{D(on)} is leakage from driver into "ON" switch.
4. OFF Isolation = 20log $\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.
5. Switching times only sampled.

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NOTE: All typical values have been characterized but are not tested.

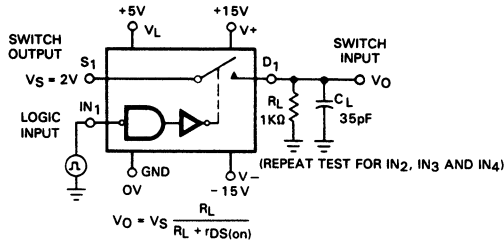
Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



*LOGIC SHOWN FOR DG211. INVERT FOR DG212

0282-4

Figure 3: Switching Time Test Circuit
Logic shown for IH311. Invert for IH312.

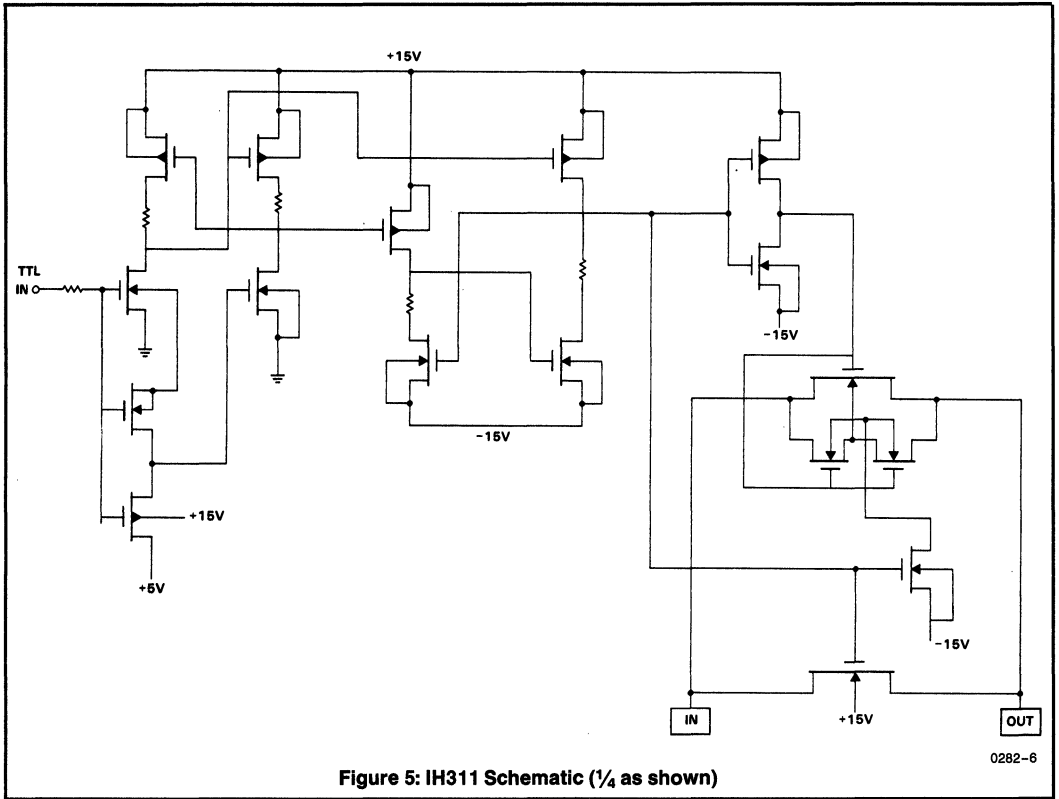


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Figure 4: Switching Time Test Circuit

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

IH401/IH401A

QUAD Varafet Analog Switch



IH401/IH401A

GENERAL DESCRIPTION

The IH401 is made up of 4 monolithically constructed combinations of a varactor type diode and an N-channel JFET. The JFET itself is very similar to the popular 2N4391, and the driver diode is specially designed, such that its capacitance is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel FET and simulates a back-to-back diode structure. This structure is needed to prevent forward biasing the source-to-gate or drain-to-gate junctions of the JFET when used in switching applications.

Previous applications of JFETs required the addition of diodes, in series with the gate, and then perhaps a gate-to-source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401 does this same job in one component (with a great deal better performance characteristics).

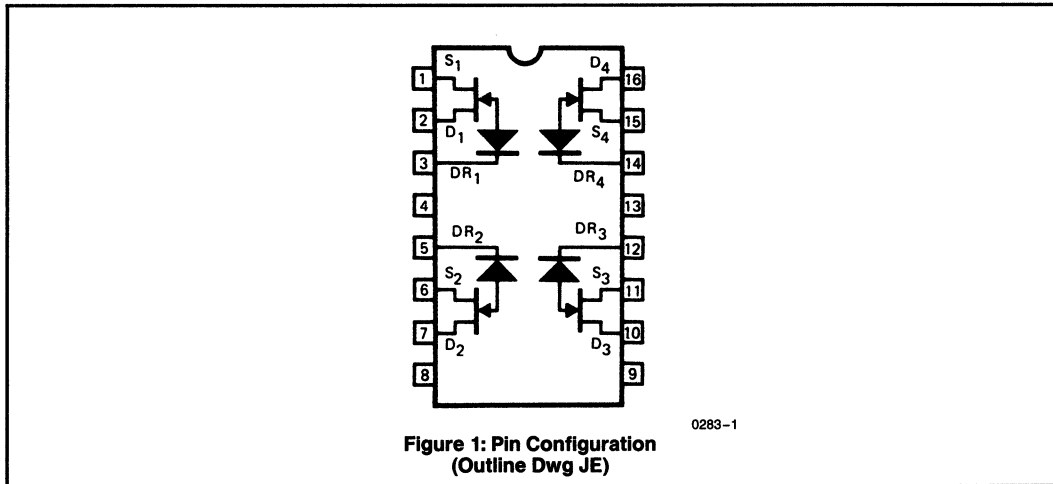
Like a standard JFET, to practically perform a solid state switch function a translator should be added to drive the diode. This translator takes the TTL levels and converts them to voltages required to drive the diode/FET system (typically a 0V to -15V translation and a 3V to +15V shift). With $\pm 15V$ power supplies, the IH401 will typically switch 18V_{p-p} at any frequency from DC to 20MHz, with less than 30 Ω $R_{DS(on)}$. The IH401A will typically switch 22V_{p-p} with less than 50 Ω $R_{DS(on)}$.

FEATURES

- $R_{DS(on)} = 25\Omega$ Typical (IH401)
- $I_{D(off)}$ of 10pA Typical
- Switching Times of 25ns for t_{on} and 75ns for t_{off} ($R_L = 1k\Omega$)
- Built-in Overvoltage Protection ($\pm 25V$)
- Charge Injection Error of 3mV Typical into 0.01 μF Capacitor
- $C_{iss} < 1pF$ Typical
- Can Be Used for Hybrid Construction

ORDERING INFORMATION

Part Number	Package
IH401	CERDIP
IH401A	CERDIP



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V_S to V_D	35V
V_G to V_S , V_D	35V
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

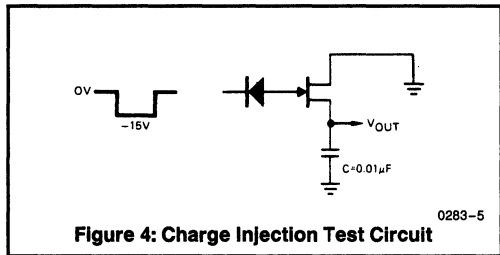
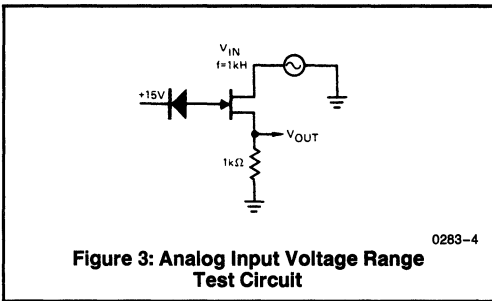
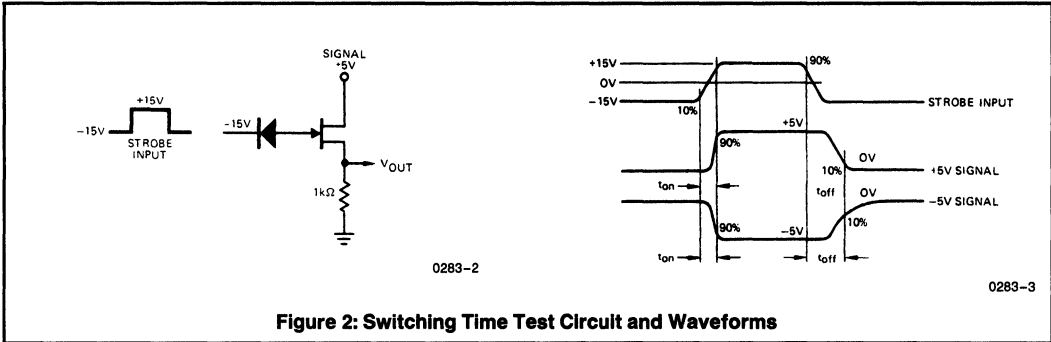
ELECTRICAL CHARACTERISTICS AT 25°C/125°C

Symbol	Characteristic	Test Conditions	IH401			Units
			Min	Typ	Max	
$R_{DS(on)}$	Switch "on" Resistance	$V_{DRIVE} = 15V$, $V_{DRAIN} = -7.5V$ $I_D = 10mA$		20	30	Ω
V_P	Pinch-Off Voltage	$I_D = 1nA$, $V_{DS} = 10V$	3	6	7.5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	$V_{DRIVE} = -15V$, $V_{SOURCE} = -7.5V$, $V_{DRAIN} = +7.5V$		10	± 500	μA
$I_{D(off)}$	Switch "off" Leakage at 125°C	$V_{DRIVE} = -15V$, $V_{SOURCE} = -7.5V$, $V_{DRAIN} = +7.5V$		0.25	50	nA
$I_{S(off)}$	Switch "off" Current	$V_{DRIVE} = -15V$, $V_{DRAIN} = -7.5V$, $V_{SOURCE} = +7.5V$		10	± 500	μA
$I_{S(off)}$	Switch "off" Leakage at 125°C	$V_{DRIVE} = -15V$, $V_{SOURCE} = -7.5V$, $V_{DRAIN} = +7.5V$		0.3	50	nA
$I_{D(on)} + I_{S(on)}$	Switch Leakage when Turned "on"	$V_D = V_S = -7.5V$, $V_{DRIVE} = +15V$		0.02	± 2	nA
V_{analog}	AC Input Voltage Range without Distortion	See Figure 3	15	18		V_{p-p}
V_{inject}	Charge Injection Error Voltage	See Figure 4		3		mV_{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S = -V$, $I_{DRIVE} = 1\mu A$, $DRIVE = 0V$	-30	-45		V
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V$, $V_D = V_S = 0V$, $DRIVE = 1\mu A$	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	$V_{DRIVE} = 15V$, $V_S = 0V$, $D = +10V$	45	70		mA
t_{on}	Switch "on" time (Note 1)	See Figure 2		50		ns
t_{off}	Switch "off" time (Note 1)	See Figure 2		150		ns

NOTE: 1. Driving waveform must be > 100ns rise and fall time.

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NOTE: All typical values have been characterized but are not tested.



ELECTRICAL CHARACTERISTICS AT 25°C/125°C

Symbol	Characteristic	Test Conditions	IH401A			Units
			Min	Typ	Max	
$R_{DS(on)}$	Switch "on" Resistance	$V_{DRIVE} = 15V$, $V_{DRAIN} = -10V$, $I_D = 10mA$		35	50	Ω
V_P	Pinch-Off Voltage	$I_D = 1nA$, $V_{DS} = 10V$	2	4	5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	$V_{DRIVE} = -15V$, $V_{SOURCE} = -10V$, $V_{DRAIN} = +10V$		10	± 500	pA
$I_{D(off)}$	Switch "off" Leakage at 125°C	$V_{DRIVE} = -15V$, $V_{SOURCE} = -10V$, $V_{DRAIN} = +10V$		0.25	50	nA
$I_{S(off)}$	Switch "off" Current	$V_{DRIVE} = -15V$, $V_{DRAIN} = -10V$, $V_{SOURCE} = +10V$		10	± 500	pA
$I_{S(off)}$	Switch "off" Leakage at 125°C	$V_{DRIVE} = -15V$, $V_{SOURCE} = -10V$, $V_{DRAIN} = +10V$		0.3	50	nA
$I_{D(on)} + I_{S(on)}$	Switch Leakage when Turned "on"	$V_D = V_S = -10V$, $V_{DRIVE} = +15V$		0.02	± 2	nA
V_{analog}	AC Input Voltage Range without Distortion	See Figure 3	20	22		V_{p-p}

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS AT 25°C/125°C (Continued)

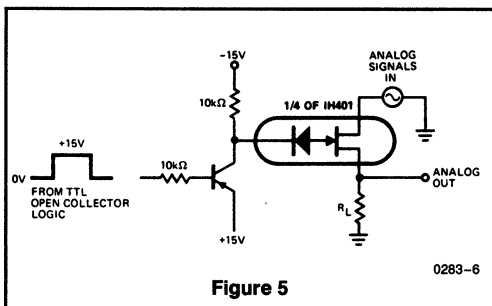
Symbol	Characteristic	Test Conditions	IH401A			Units
			Min	Typ	Max	
V_{inject}	Charge Injection Amplitude	See Figure 4		3		mV _{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S = -V$, $I_{DRIVE} = 1\mu A$, $DRIVE = 0V$	-30	-45		V
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	$V_{DRIVE} = -V$, $V_D = V_S = 0V$, $DRIVE = 1\mu A$	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	$V_{DRIVE} = 15V$, $V_S = 0V$, $D = +10V$	35	55		mA
t_{on}	Switch "on" time (Note 1)	See Figure 2		50		ns
t_{off}	Switch "off" time (Note 1)	See Figure 2		150		ns

NOTE: Driving waveform must be > 100ns rise and fall time.

APPLICATIONS

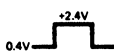
IH401 Family

In general, the IH401 family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401 requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401 to handle ±7.5V analog signals (or IH401A to handle ±10V analog signals). A typical simple PNP translator is shown in Figure 5.



Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and t_{off} is limited by the collector load resistor (approximately 1.5μs for 10kΩ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

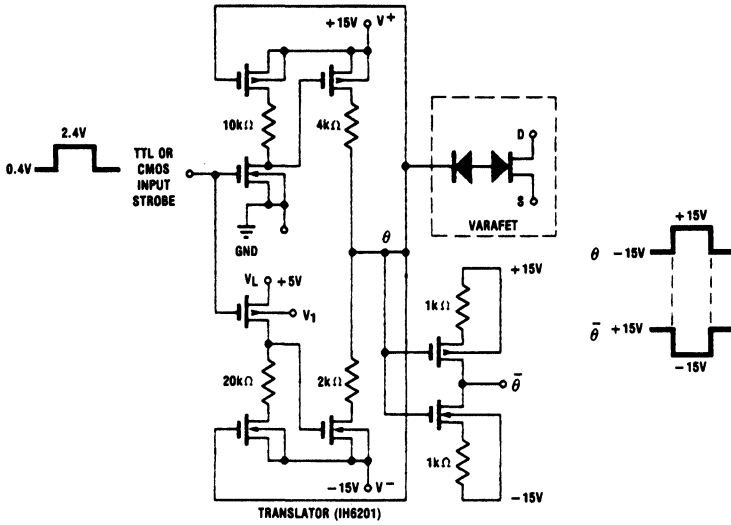
A translator which overcomes the problems of the simple PNP stage is the Intersil IH6201.* This translator driving an IH401 varafet produces the following typical features:

- t_{on} time of approx. 200ns } break before
- t_{off} time of approx. 80ns } make switch
- TTL compatible strobing levels of 
- $I_{D(on)} + I_{S(on)}$ typically 20pA up to ±10V analog signals
- $I_{D(off)}$ or $I_{S(off)}$ typically 20pA
- Quiescent current drain of approx. 100nA in either "on" or "off" case

*The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 6.

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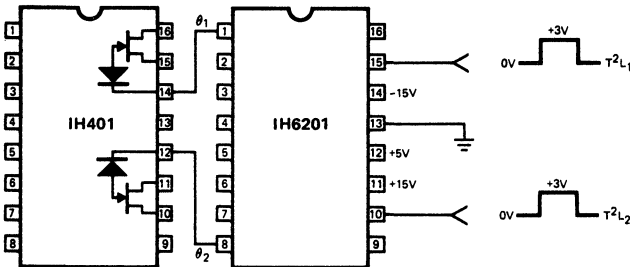
NOTE: All typical values have been characterized but are not tested.



0283-8

NOTE: Each translator output has a θ and $\bar{\theta}$ output. $\bar{\theta}$ is just the inverse of θ i.e., ($\bar{\theta}$ output is 180° out of phase with respect to θ output).

Figure 6: IH6201 Driving An IH401



0283-9

NOTE: Either switch is turned on when strobe input goes high.

Figure 7: Dual SPST Analog Switch

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NOTE: All typical values have been characterized but are not tested.

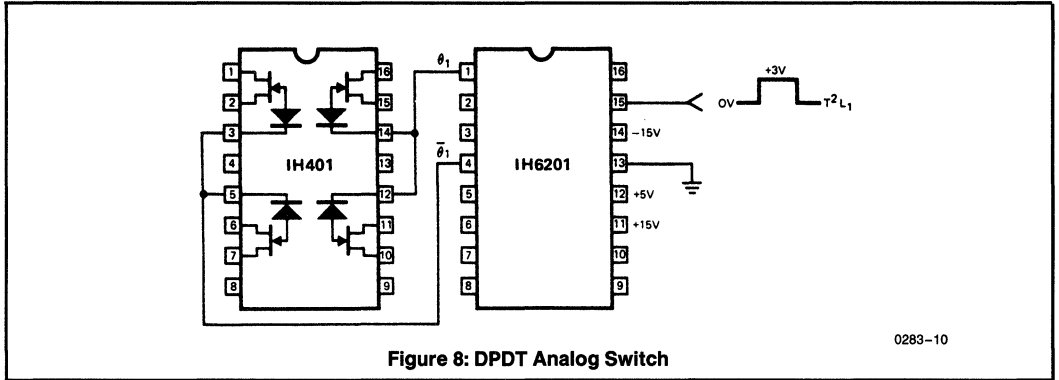


Figure 8: DPDT Analog Switch

0283-10

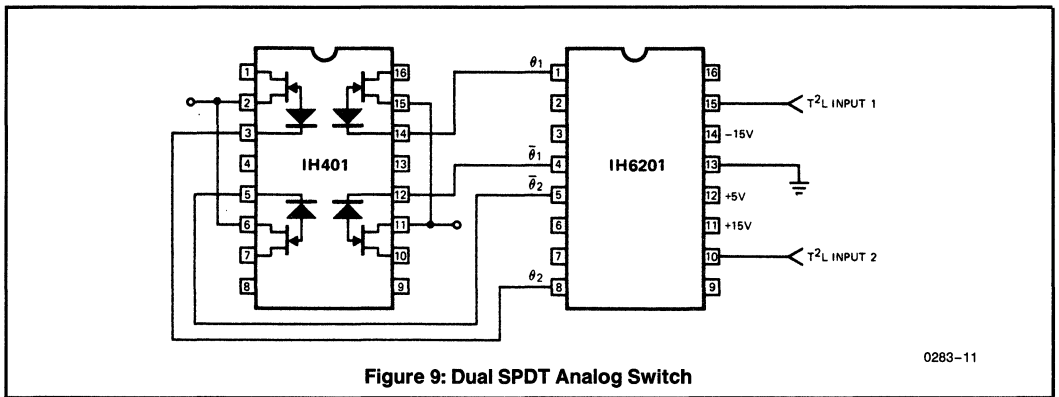


Figure 9: Dual SPDT Analog Switch

0283-11

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See Figure 9)

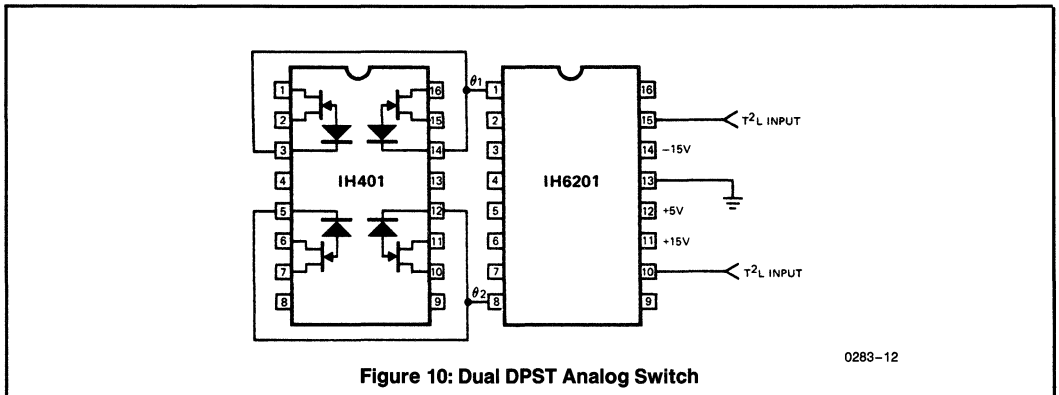


Figure 10: Dual DPST Analog Switch

0283-12

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NOTE: All typical values have been characterized but are not tested.

IH5009-IH5024

Virtual Ground Analog Switch



IH5009-IH5024

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from TTL open collector logic (15 volts) while the even numbered devices are driven directly from low level TTL logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

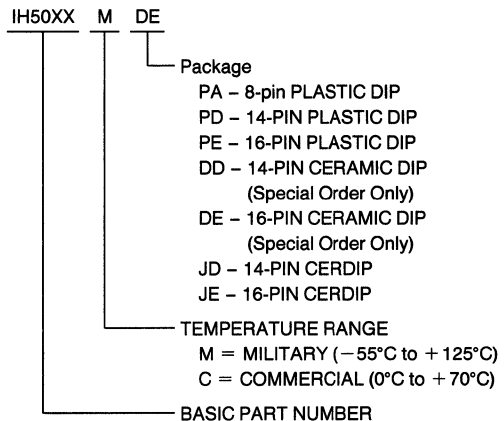
ORDERING INFORMATION

Basic Part Number	Channels	Logic Level	Packages
IH5009	4	+ 15	JD,DD,PD
IH5010	4	+ 5	JD,DD,PD
IH5011	4	+ 15	JE,DE,PE
IH5012	4	+ 5	JE,DE,PE
IH5013	3	+ 15	JD,DD,PD
IH5014	3	+ 5	JD,DD,PD
IH5015	3	+ 15	JE,DE,PE
IH5016	3	+ 5	JE,DE,PE
IH5017	2	+ 15	JD,DD,PA
IH5018	2	+ 5	JD,DD,PA
IH5019	2	+ 15	JE,DE,PA
IH5020	2	+ 5	JE,DE,PA
IH5021	1	+ 15	JD,DD,PA
IH5022	1	+ 5	JD,DD,PA
IH5023	1	+ 15	JE,DE,PA
IH5024	1	+ 5	JE,DE,PA

NOTE: Mil-Temperature range (-55°C to +125°C) available in ceramic packages only.

FEATURES

- Switches Analog Signals Up to 20 Volts Peak-to-Peak
- Each Channel Complete - Interfaces With Most Integrated Logic
- Switching Speeds Less Than 0.5 μ s
- $I_D(\text{OFF})$ Less Than 500pA Typical at 70°C
- Effective $r_{ds(\text{ON})}$ - 5 Ω to 50 Ω
- Commercial and Military Temperature Range Operation



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage -15V
Diode Current 10mA
Power Dissipation (Note) 500mW
Storage Temperature -65°C to +150°C

Lead Temperature (Soldering, 10sec) 300°C
Operating Temperature	
5009C Series 0°C to +70°C
5009M Series -55°C to +125°C
Lead Temperature (Soldering, 10sec) 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

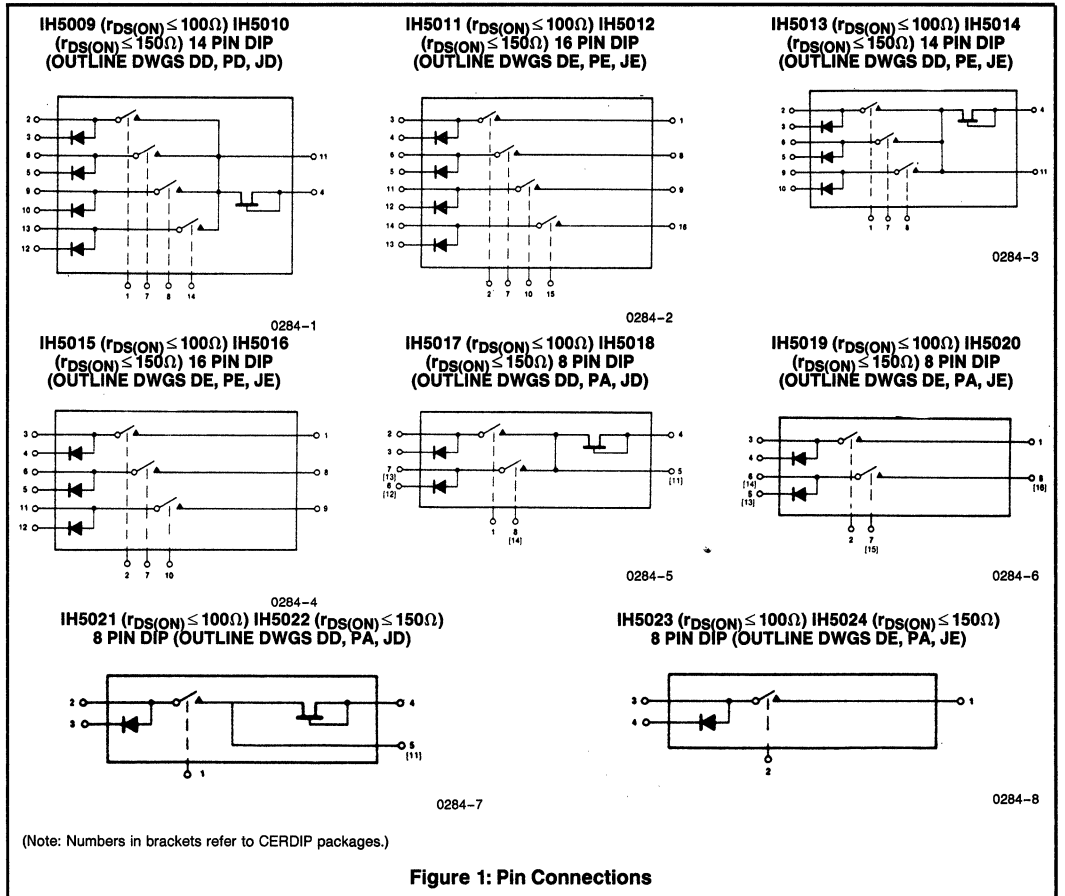
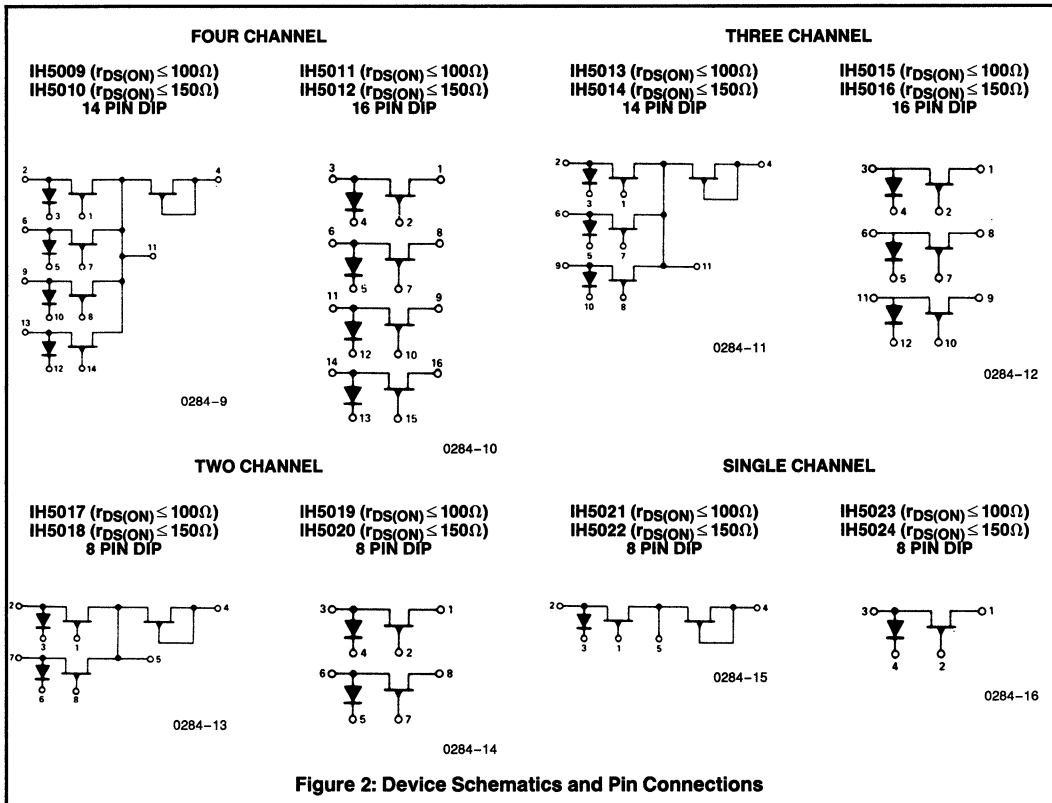


Figure 1: Pin Connections

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (per channel)

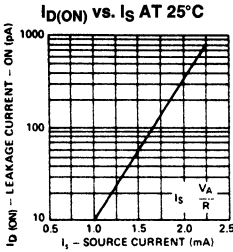
Symbol (Note 1)	Characteristic	Type (Note 4)	TEST Conditions (Note 2)	Specification Limit				Units
				-55°C (M) 0°C (C) Min/Max	25°C		+125°C (M) +70°C (C) Min/Max	
					Typ	Min/Max		
$I_{IN(ON)}$	Input Current-ON	ALL	$V_{IN}=0V, I_D=2mA$		0.01	± 0.5	100	μA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	$V_{IN}=+4.5V, V_A=\pm 10V$		0.04	± 0.5	20	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	$V_{IN}=+11V, V_A=\pm 10V$		0.04	± 0.5	20	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 7, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 8, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 6, Note 3			4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 8, Note 3			11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	$V_{IN}=+4.5V, V_A=\pm 10V$		0.02	± 0.5	20	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	$V_{IN}=+11V, V_A=\pm 10V$		0.02	± 0.5	20	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN}=0V, I_S=1mA$		0.30	± 1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN}=0V, I_S=1mA$		0.10	± 0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN}=0V, I_S=2mA$			1.0	10	μA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN}=0V, I_S=2mA$			2.0	100	μA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	$I_D=2mA, V_{IN}=0.5V$	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	$I_D=2mA, V_{IN}=1.5V$	100	80	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 5 & 6		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 5 & 6		300	500		ns
CT	Cross Talk	All	$f=100Hz$		120			dB

- NOTES: 1. (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.
 2. Refer to Figure 2 for definition of terms.
 3. $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of $r_{DS(ON)}$ and $I_{D(OFF)}$ respectively.
 4. "5V Logic CKTS" applies to even-numbered devices. "15V Logic CKTS" applies to odd-numbered devices.

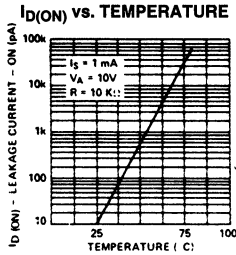
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NOTE: All typical values have been characterized but are not tested.

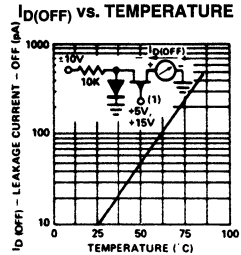
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)



0284-17

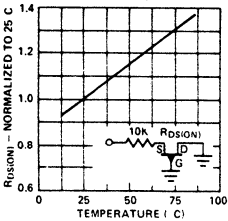


0284-18



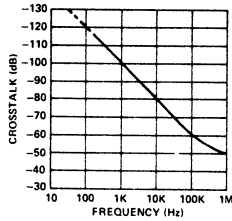
0284-19

RDs(ON) vs. TEMPERATURE (NORMALIZED TO 25°C VALUE)



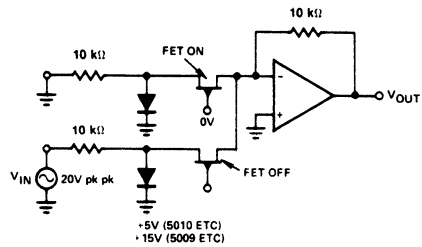
0284-20

CROSSTALK AS A FUNCTION OF FREQUENCY



0284-21

CROSSTALK MEASUREMENT CIRCUIT



0284-22

DETAILED DESCRIPTION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than $\pm 200\text{mV}$, and those which are greater than $\pm 200\text{mV}$. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to $\pm 200\text{mV}$, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS}=0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 3) the gain is given by:

$$\text{GAIN} = \frac{10\text{k}\Omega + r_{DS(\text{ON})}(\text{compensator})}{10\text{k}\Omega + r_{DS}(\text{switch})}$$

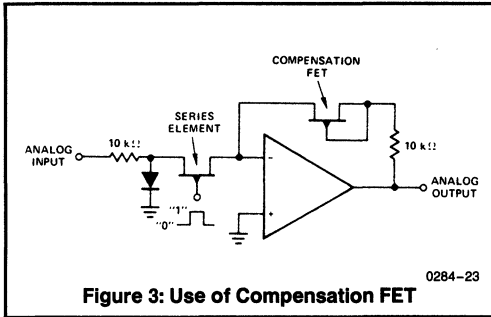


Figure 3: Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

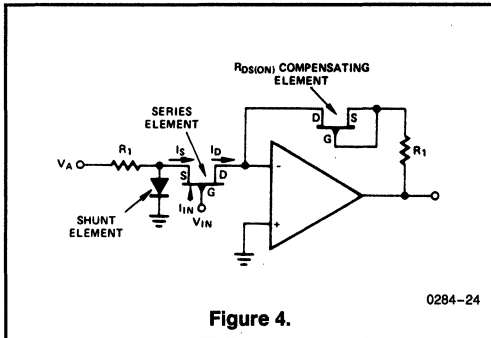


Figure 4.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by TTL open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

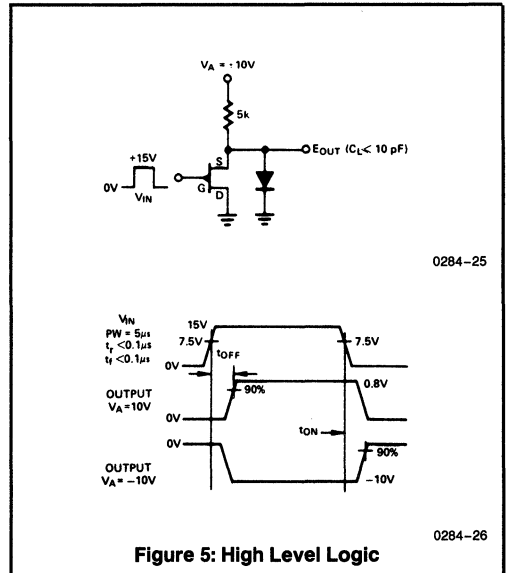


Figure 5: High Level Logic

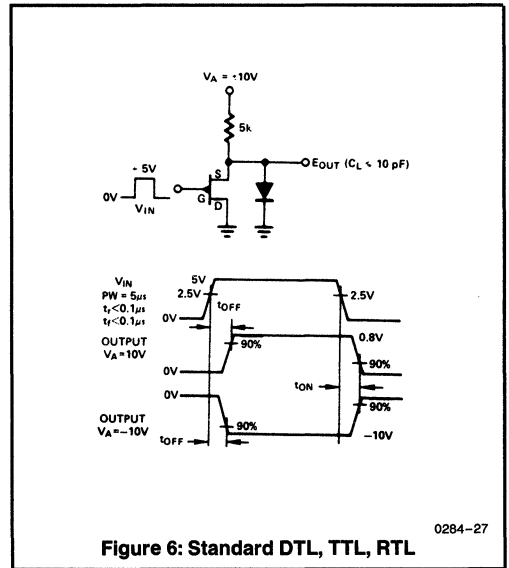


Figure 6: Standard DTL, TTL, RTL

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NOTE: All typical values have been characterized but are not tested.

LOGIC INTERFACE CIRCUITS

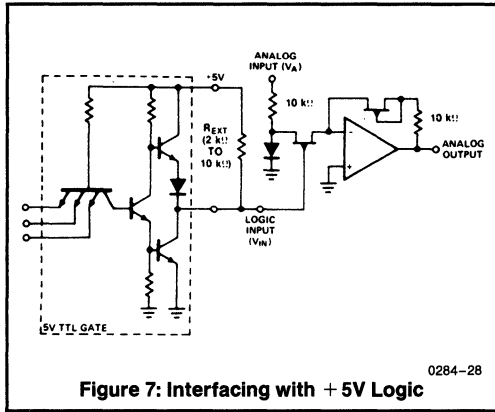


Figure 7: Interfacing with +5V Logic

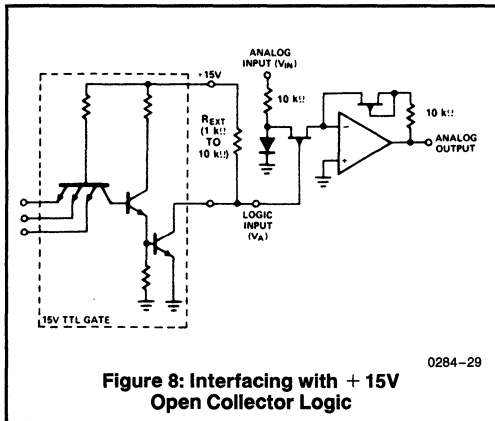


Figure 8: Interfacing with +15V Open Collector Logic

APPLICATIONS (Note)

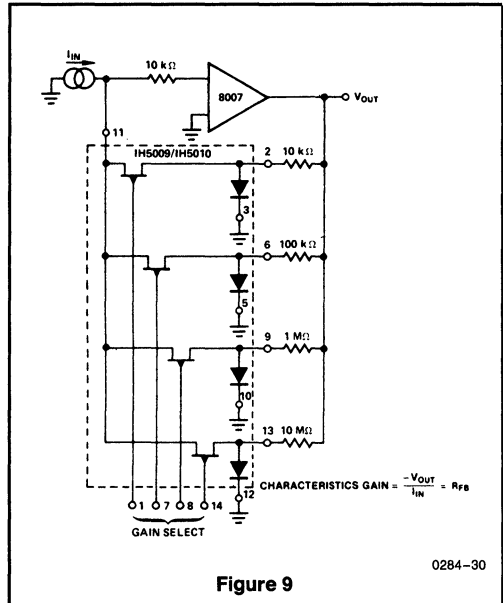


Figure 9

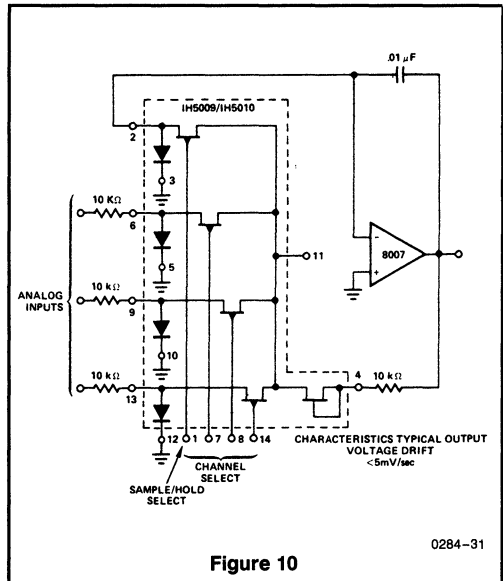


Figure 10

NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches".

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NOTE: All typical values have been characterized but are not tested.

IH5040-IH5047

High-Level CMOS Analog Switch



GENERAL DESCRIPTION

The IH5040 family of solid state analog switches use an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ± 25 volts without damage to the device, and destructive latch-up has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than $1\mu A$. Also, the 5040 guarantees Break-Before-Make switching, accomplished by extending the t_{on} time (300ns TYP.) so that it exceeds t_{off} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FEATURES

- Switches Greater Than 20Vpp Signals With $\pm 15V$ Supplies
- Quiescent Current Less Than $1\mu A$
- Overvoltage Protection to $\pm 25V$
- Break-Before-Make Switching t_{off} 200ns, t_{on} 300ns Typical
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- New DPDT & 4PST Configurations
- Complete Monolithic Construction

ORDERING INFORMATION

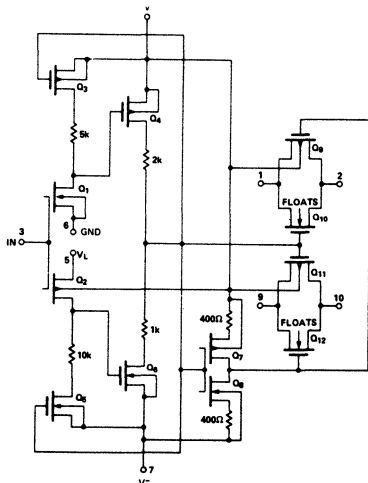
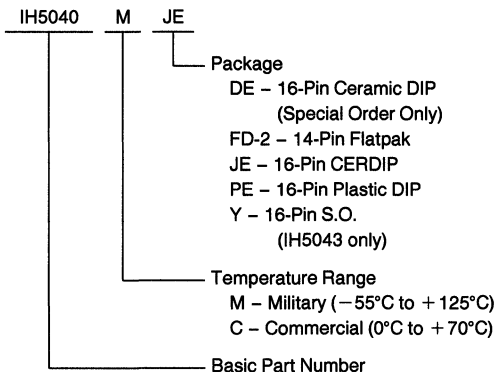


Figure 1: Functional Driver, Typical Driver, Gate — IH5042

FUNCTIONAL DESCRIPTION

INTERMIL Part No.	Type	$r_{DS(on)}$	Pin for Pin Compatible
IH5040	SPST	75Ω	HI5040/DG5040
IH5041	Dual SPST	75Ω	HI5041/DG5041
IH5042	SPDT	75Ω	HI5042/DG5042
IH5043	Dual SPDT	75Ω	HI5043/DG5043
IH5044	Dual DPST	75Ω	HI5044/DG5044
IH5045	Dual DPST	75Ω	HI5045/DG5045
IH5046	DPDT	75Ω	HI5046
IH5047	4PST	75Ω	HI5047

NOTE 1. See Switching State diagrams for applicable package equivalency.

0286-1

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ -V ⁻	<36V
V ⁺ -V _D	<30V
V _D -V ⁻	<30V
V _D -V _S	<±22V
V _L -V ⁻	<33V
V _L -V _{IN}	<30V
V _L -GND	<20V
V _{IN} -GND	<20V

Current (Any Terminal)	<30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
M	-55°C to +125°C
C	0°C to +70°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6mW/°C Above 70°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V⁺ = +15V, V⁻ = -15V, V_L = +5V)

Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Commercial			
			-55°C	+25°C	+125°C	0	+25°C	+70°C	
I _{IN(ON)}	Input Logic Current	V _{IN} = 2.4V	±1	±1	10	±1	±1	10	μA
I _{IN(OFF)}	Input Logic Current	V _{IN} = 0.8V	±1	±1	10	±1	±1	10	μA
r _{DS(on)}	Drain-Source On Resistance	I _S = 10mA V _{ANALOG} = -10V to +10V	75	75	150	80	80	130	Ω
Δr _{DS(ON)}	Channel to Channel r _{DS(ON)} Match			25 (typ)			30 (typ)		Ω
V _{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
I _{D(OFF)} / I _{S(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -10V to +10V		±1	100		±5	100	nA
I _{D(ON)} + I _{S(ON)}	Switch On Leakage Current	V _D = V _S = -10V to +10V		±2	200		±10	100	nA
t _{on}	Switch "ON" Time	R _L = 1kΩ, V _{ANALOG} = -10V to +10V See Fig. 3		1000			1000		ns
t _{off}	Switch "OFF" Time	R _L = 1kΩ, V _{ANALOG} = -10V to +10V See Fig. 3		500			500		ns
Q _(INJ.)	Charge Injection	See Fig. 3		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R _L = 100Ω, C _L ≤ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I ⁺ Q	V ⁺ Power Supply Quiescent Current		±1	±1	10	10	10	100	μA
I ⁻ Q	V ⁻ Power Supply Quiescent Current	V ⁺ = +15V, V ⁻ = -15V, V _L = +5V	±1	±1	10	10	10	100	μA
I ⁻ LQ	+5V Supply Quiescent Current		±1	±1	10	10	10	100	μA
I _{GND}	Gnd Supply Quiescent Current		±1	1	10	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Fig. 6		54 (typ)			50 (typ)		dB

Note: Typical values are for design aid only, not guaranteed and not subject to production testing.

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NOTE: All typical values have been characterized but are not tested.

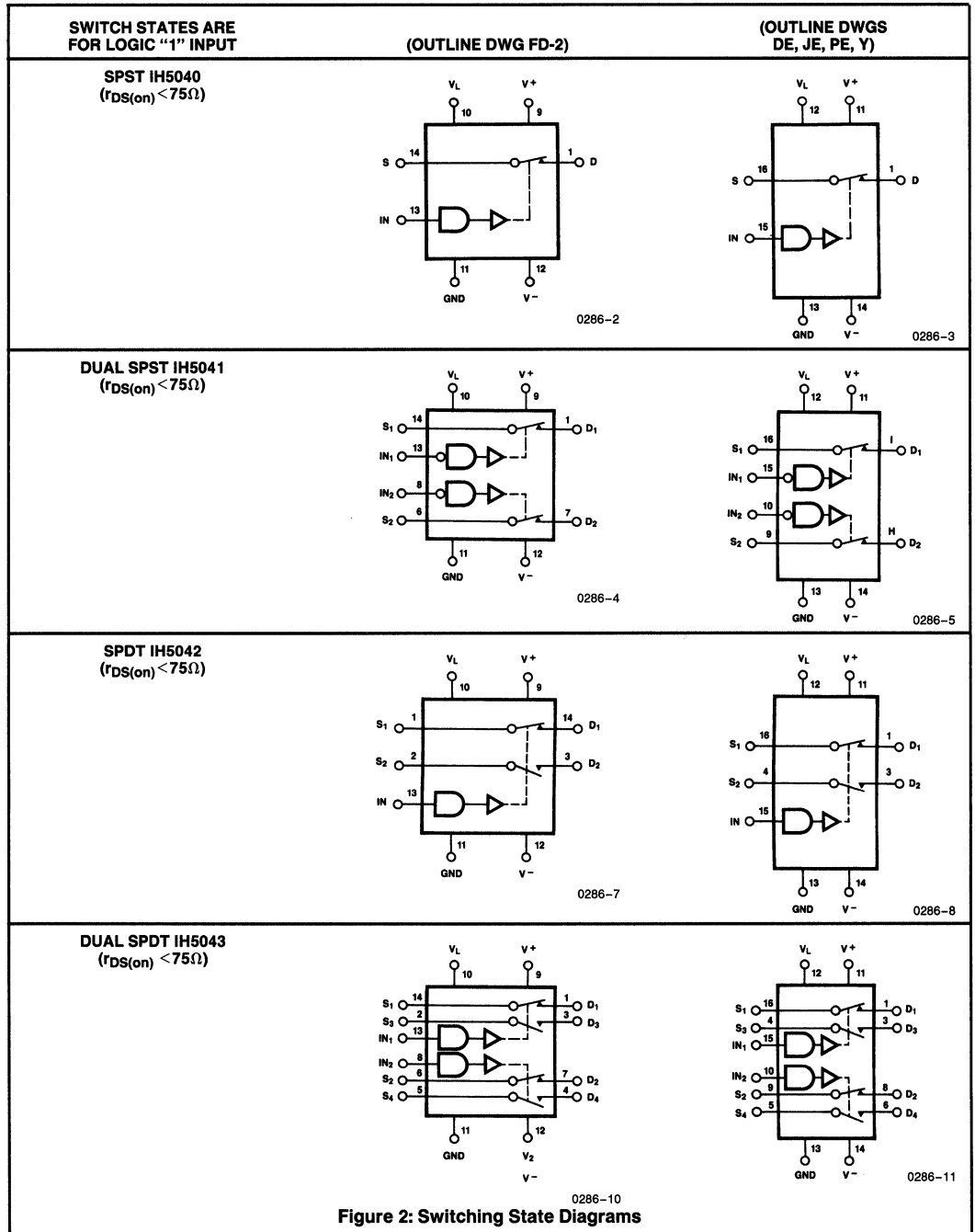


Figure 2: Switching State Diagrams

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NOTE: All typical values have been characterized but are not tested.

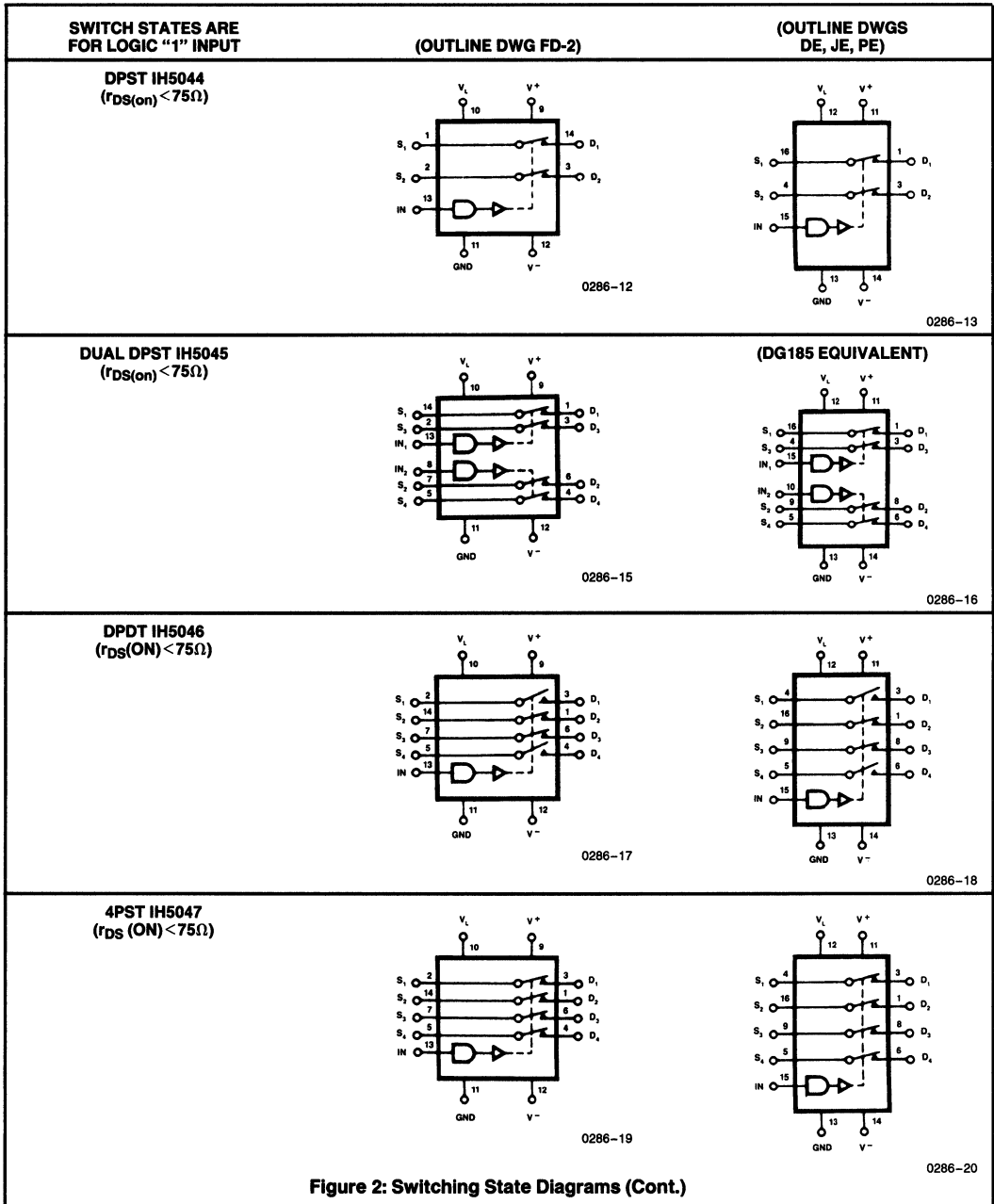
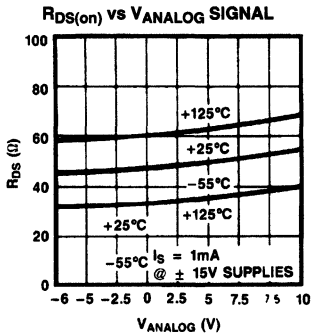


Figure 2: Switching State Diagrams (Cont.)

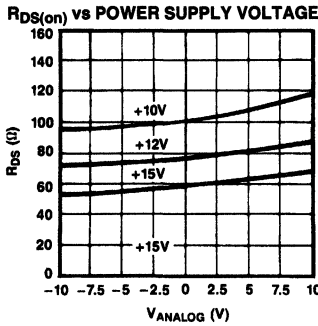
INTERSIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

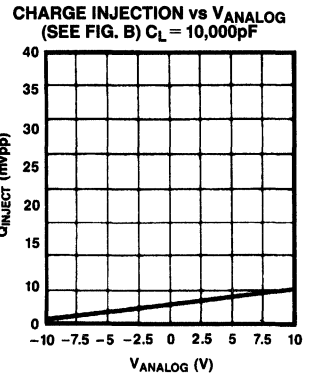
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)



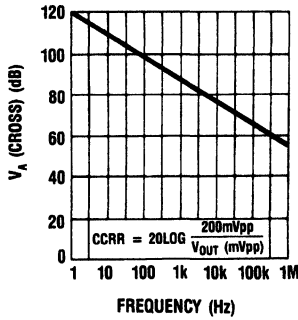
0286-21



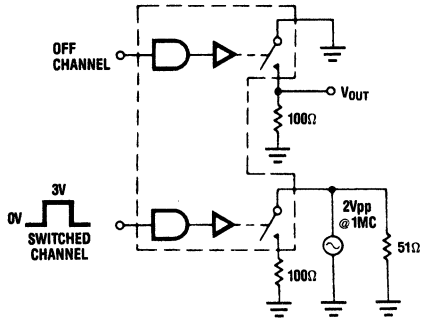
0286-22



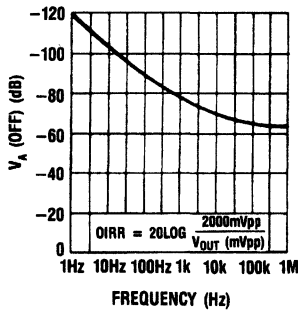
0286-23



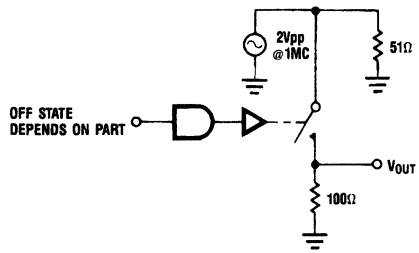
0286-24



0286-25



0286-26



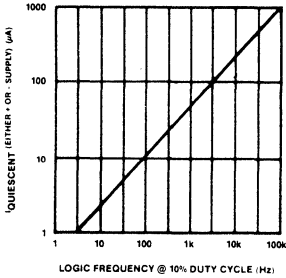
0286-27

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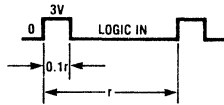
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

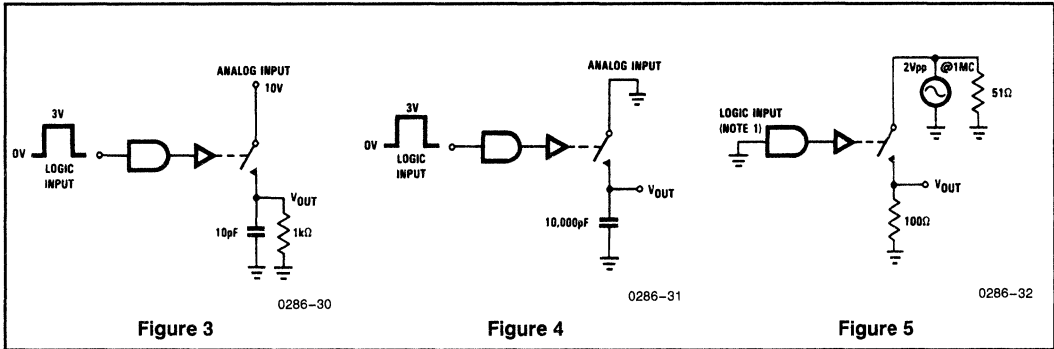


0286-28



0286-29

TEST CIRCUITS



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

APPLICATIONS

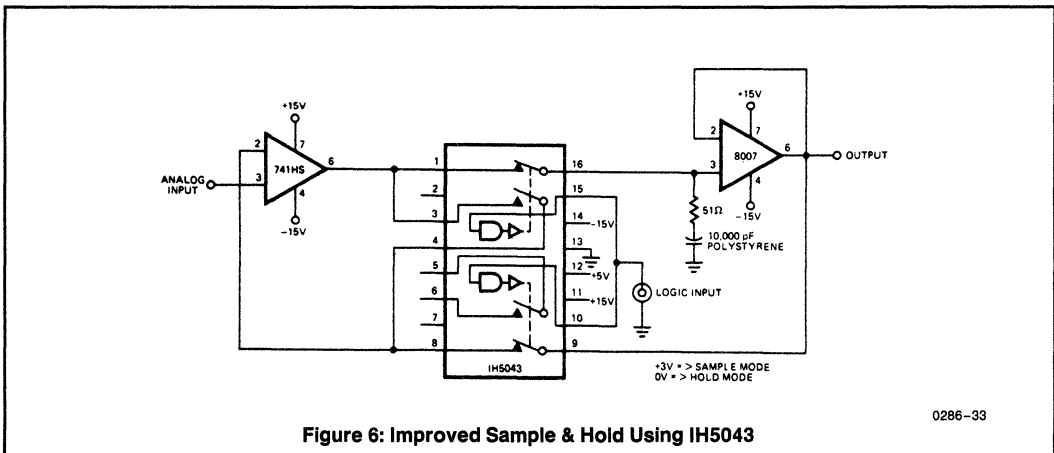


Figure 6: Improved Sample & Hold Using IH5043

0286-33

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

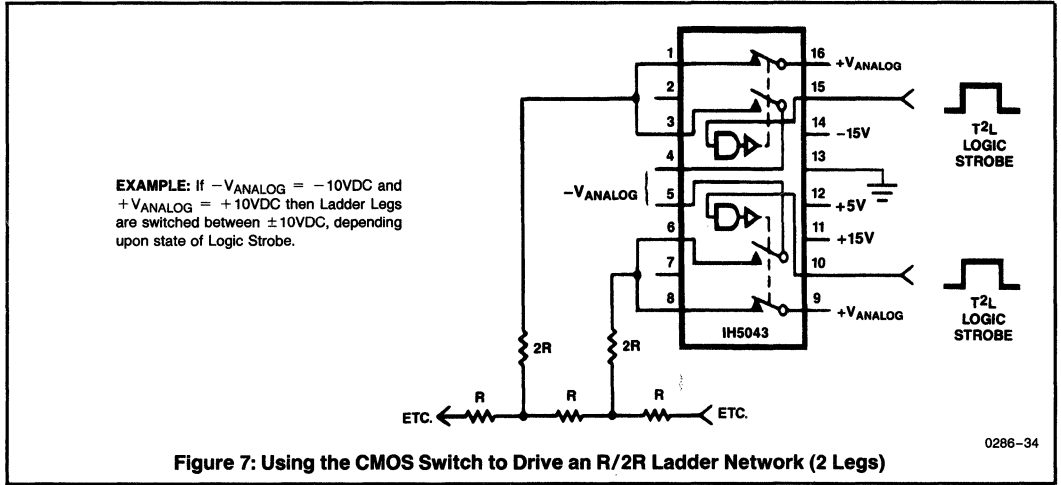


Figure 7: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

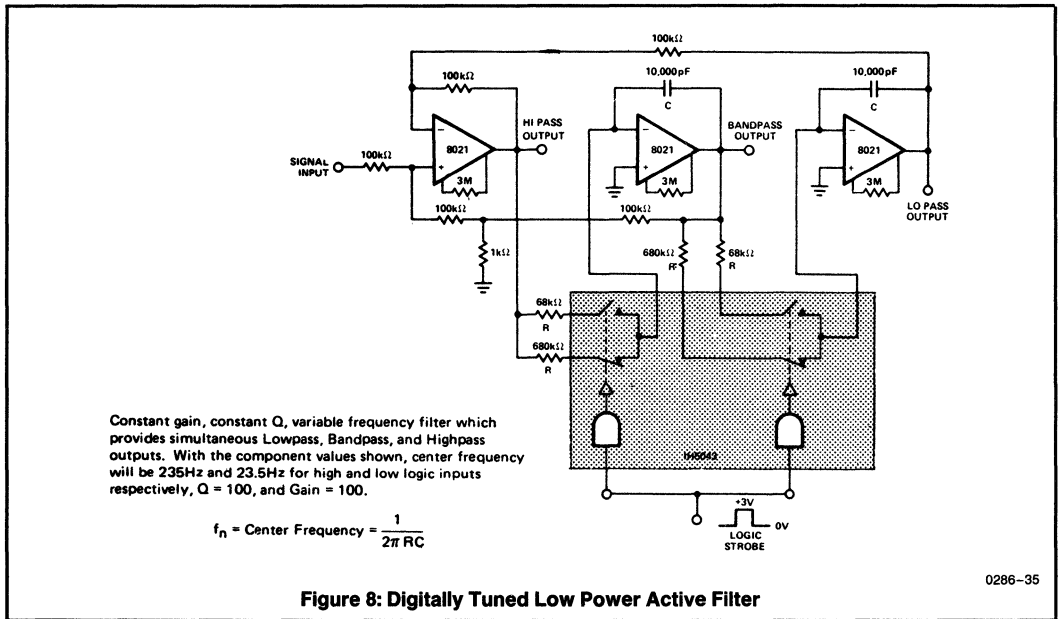


Figure 8: Digitally Tuned Low Power Active Filter

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

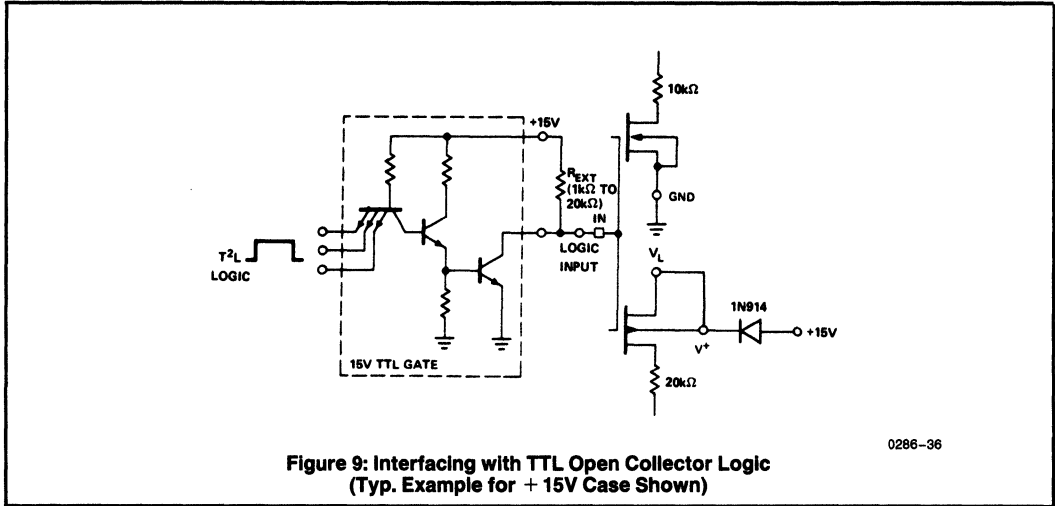


Figure 9: Interfacing with TTL Open Collector Logic (Typ. Example for +15V Case Shown)

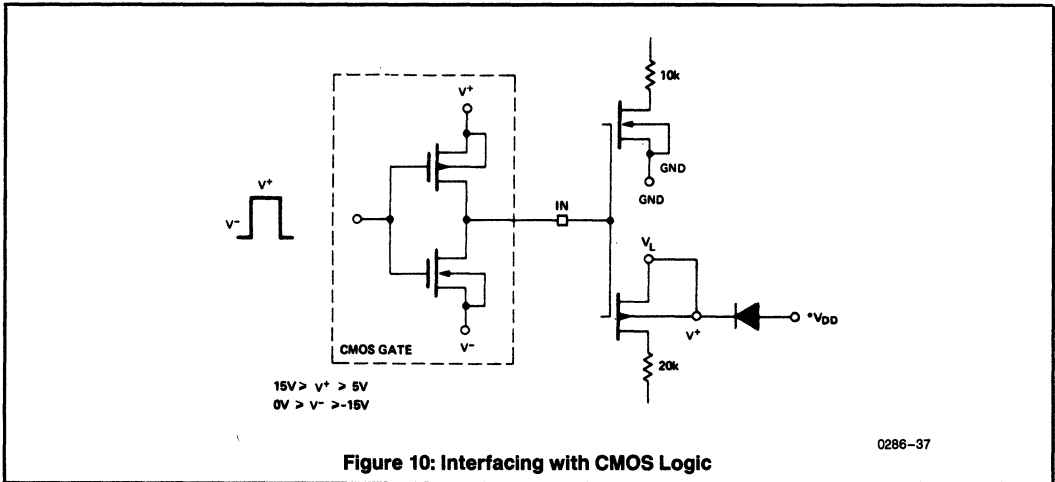


Figure 10: Interfacing with CMOS Logic

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

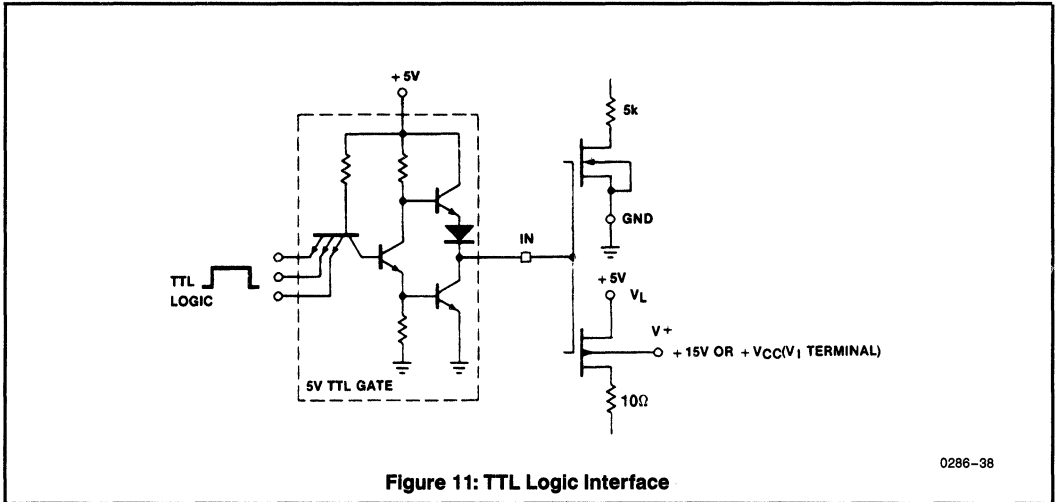


Figure 11: TTL Logic Interface

0286-38

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NOTE: All typical values have been characterized but are not tested.

IH5048-IH5051

Low Charge Injection CMOS Analog Switches



IH5048-IH5051

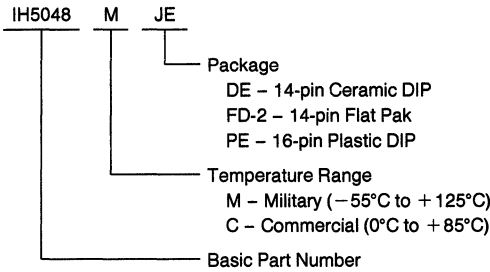
GENERAL DESCRIPTION

The IH5048 family of analog switches is especially made for low charge injection and low leakage. Construction includes our CMOS high level driver circuitry combined with unique "VARAFET" switches.

FEATURES

- Low Charge Injection—1mV (Typ.)
- Quiescent Current Less Than 1 μ A
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low $r_{DS(on)}$ - 35 Ω (Typ.)
- Pin-Out Compatible With IH5040 Family
- Low Leakage 100 pA Typical

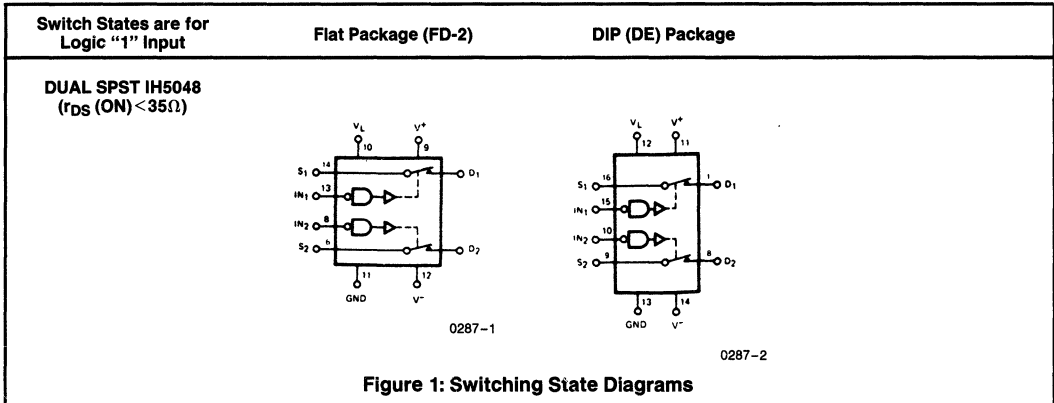
ORDERING INFORMATION



ORDERING INFORMATION

Intersil Part No.	Type	$r_{DS(on)}$
IH5048 Dual	SPST	35 Ω
IH5049 Dual	DPST	35 Ω
IH5050	SPDT	35 Ω
IH5051 Dual	SPDT	35 Ω

NOTE 1. See Switching State diagrams for applicable package equivalency.



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NOTE: All typical values have been characterized but are not tested.

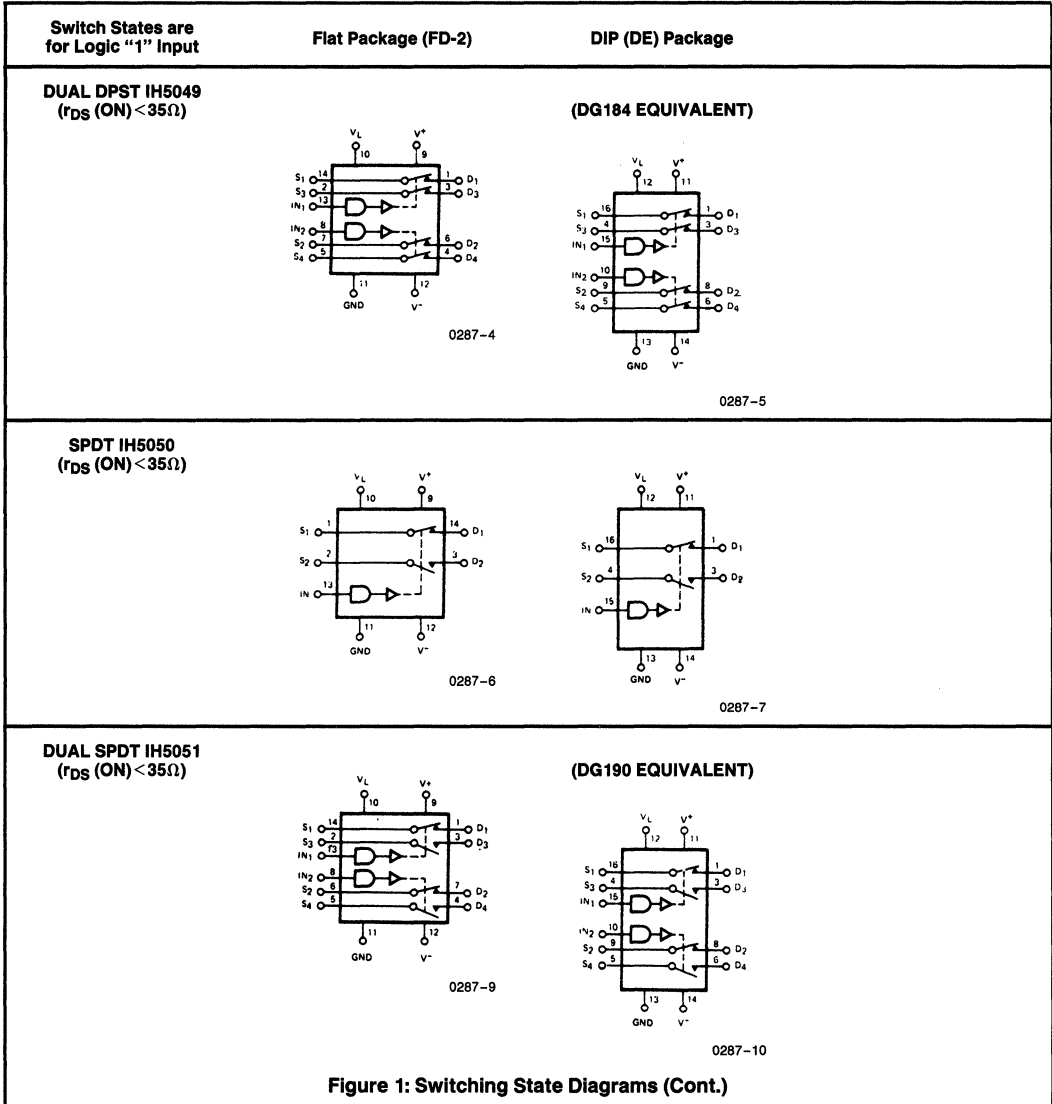


Figure 1: Switching State Diagrams (Cont.)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	< 36V
$V^+ - V_D$	< 30V
$V_D - V^-$	< 30V
$V_D - V_S$	< ± 22V
$V_L - V^-$	< 33V
$V_L - V_{IN}$	< 30V
$V_L - GND$	< 20V
$V_{IN} - GND$	< 20V

Current (Any Terminal)	< 30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6mW/°C Above 70°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

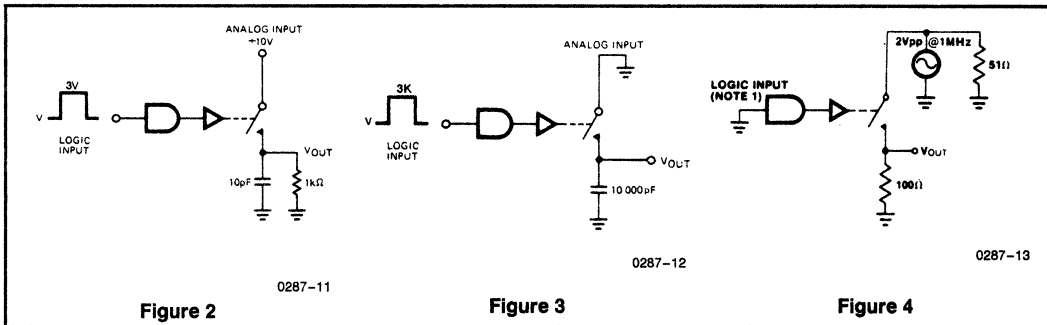
Per Channel		Test Conditions	Min/Max Limits						Units	
Symbol	Characteristic		Military			Commercial				
			-55°C	+25°C	+125°C	0	+25°C	+70°C		
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 2.4V$ Note 1	±1	±1	10	±1	±1	10	μA	
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 0.8V$ Note 1	±1	±1	10	±1	±1	10	μA	
$r_{DS(on)}$	Drain-Source On Resistance	$I_S = -10mA$ $V_{ANALOG} = -10V$			40			45	75	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			15 (Typ)			15 (Typ)			Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±10			±10			V
$I_{D(OFF)}/I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -10V$ to +10V		±1	100			±5	100	nA
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to +10V		±2	200			±10	200	nA
t_{on}	Switch "ON" Time	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to +10V See Fig. 2		500				1000		ns
t_{off}	Switch "OFF" Time	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to +10V See Fig. 2		250				500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 3		1 (Typ)				2 (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. 4, (Note 1)		54 (Typ)				50 (Typ)		dB
$I^+ Q$	V^+ Power Supply Quiescent Current		±1	±1	10	10	10	10	100	μA
$I^- Q$	V^- Power Supply Quiescent Current	$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$	±1	±1	10	10	10	10	100	μA
$I^+ LQ$	+5V Supply Quiescent Current		±1	±1	10	10	10	10	100	μA
I_{GND}	Gnd Supply Quiescent Current		±1	±1	10	10	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Performance Characteristics (Note 1)		54 (Typ)				50 (Typ)		dB

Note 1: Not tested in production.

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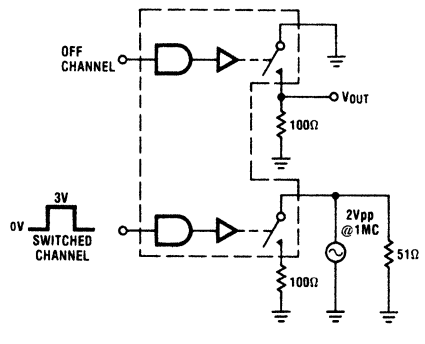
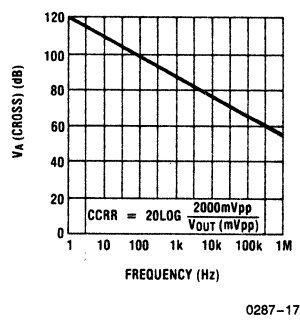
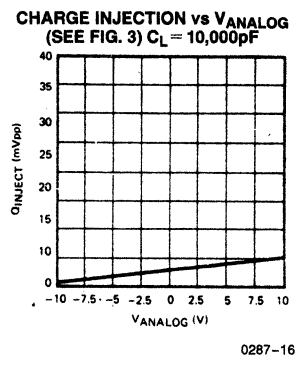
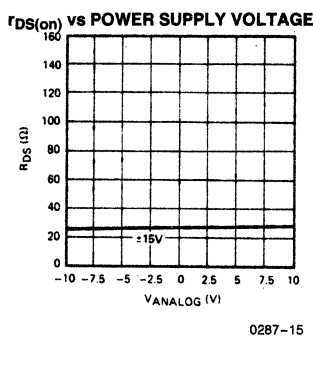
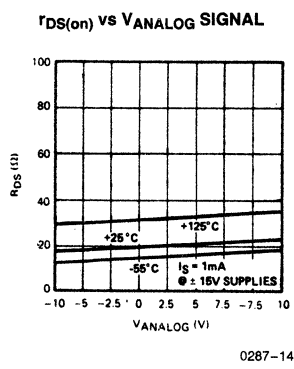
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

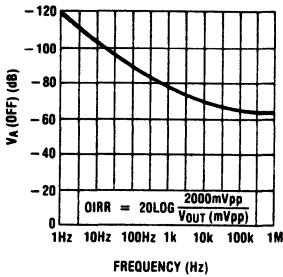
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)



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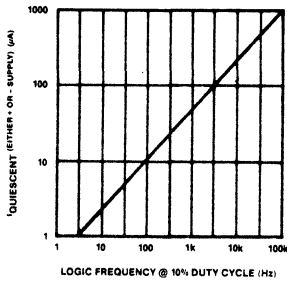
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)

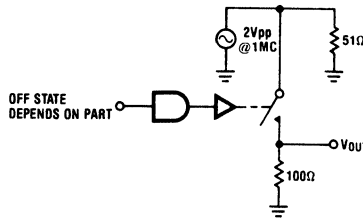


0287-19

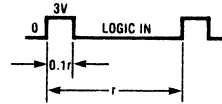
POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



0287-21



0287-20



0287-22

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NOTE: All typical values have been characterized but are not tested.

IH5052/IH5053 QUAD CMOS Analog Switch



GENERAL DESCRIPTION

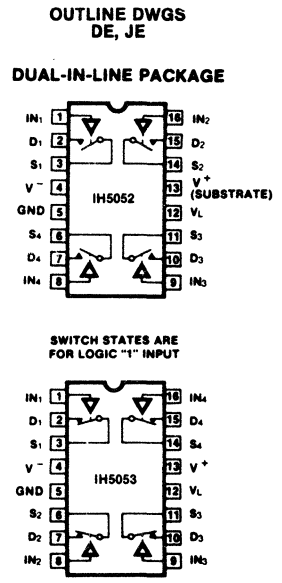
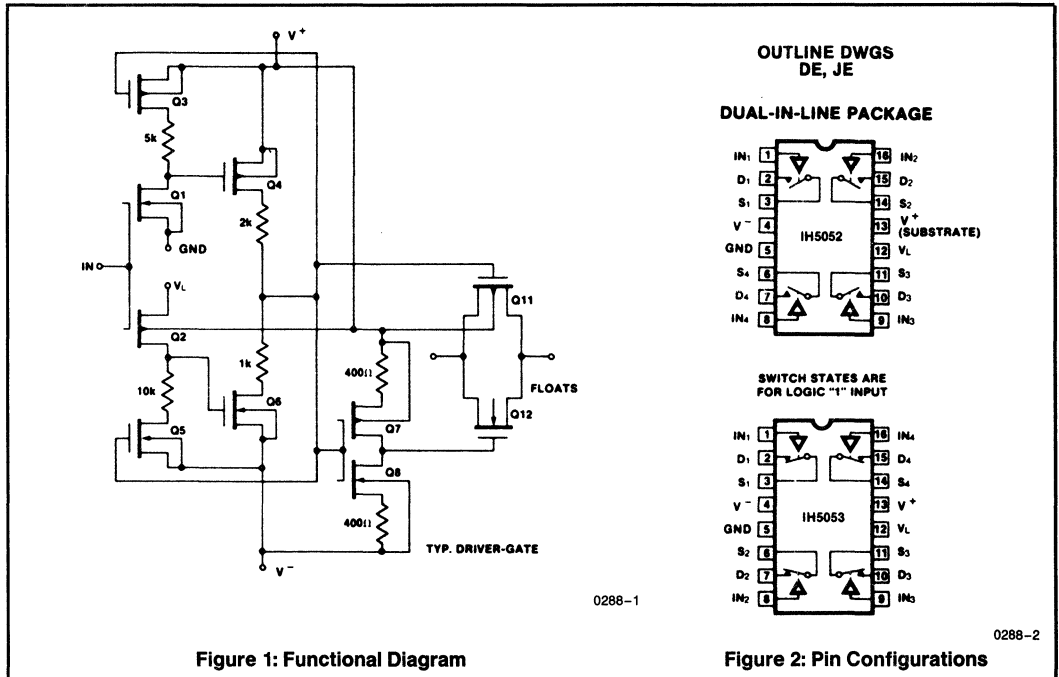
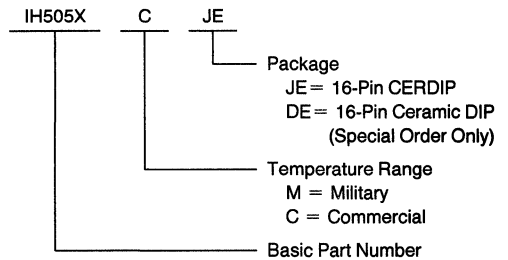
The IH5052/3 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The INTERMIL CMOS technology has eliminated this serious systems problem. Key performance advantages are TTL compatibility and ultra low-power operation — the quiescent current requirement is less than 10 μ A.

The IH5052/3 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (400ns TYP.) such that it exceeds t_{OFF} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logical "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logical "1" (2.4V or more) at its control inputs.

FEATURES

- Switches Greater Than 20Vpp Signals With $\pm 15V$ Supplies
- Quiescent Current Less Than 10 μ A
- Overvoltage Protection to $\pm 25V$
- Break-Before-Make Switching t_{off} 100ns, t_{on} 250ns Typical
- TTL, CMOS Compatible
- Non-Latching With Supply Turn-Off
- IH5052 4 Normally Closed Switches
- IH5053 4 Normally Open Switches
- Low $R_{DS(ON)}$ 50 Ω Typical

ORDERING INFORMATION



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	< 36V
$V^+ - V_D$	< 30V
$V_D - V^-$	< 30V
$V_D - V_S$	< ± 22V
$V_L - V^-$	< 33V
$V_L - V_{IN}$	< 30V
$V_L - GND$	< 20V
$V_{IN} - GND$	< 20V
Current (Any Terminal)	< 30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C

Power Dissipation 450mW
 (All Leads Soldered to a P.C. Board)
 Derate 6mW/°C Above 70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V⁺ = +15V, V⁻ = -15V, V_L = +5V)

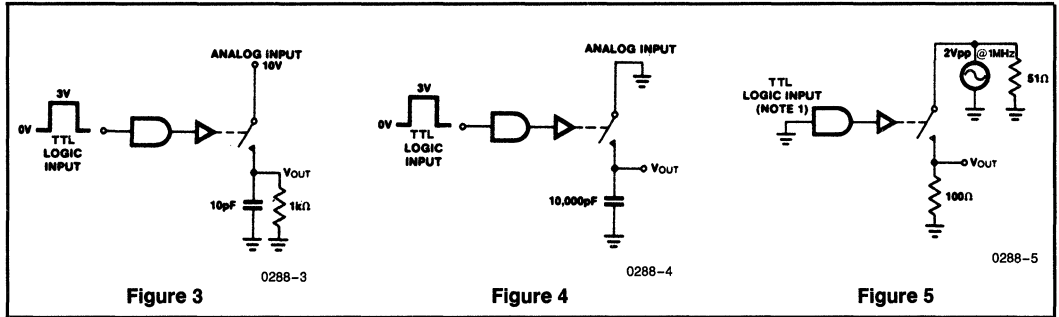
Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		-55°C	+25°C	+125°C	0	+25°C	+70°C	
I _{IN(ON)}	Input Logic Current	V _{IN} = 2.4V (IH5053) = 0.8V (IH5052)	10	± 1	10		± 10		μA
I _{IN(OFF)}	Input Logic Current	V _{IN} = 0.8V (IH5053) = 2.4V (IH5052)	10	± 1	10		± 10		μA
r _{DS(ON)}	Drain-Source On Resistance	I _S = 10mA, V _{analog} = -10V to +10V	75	75	100	80	80	100	Ω
Δr _{DS(ON)}	Channel to Channel r _{DS(ON)} Match			25 (typ)			30 (typ)		Ω
V _{ANALOG}	Min. Analog Signal Handling Capability			± 11 (typ)			± 10 (typ)		V
I _{D(OFF)} / I _{S(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -10V to +10V		± 1	100		± 5	100	nA
I _{D(ON)} + I _{S(ON)}	Switch On Leakage Current	V _D = V _S = -10V to +10V		± 2	200		± 10	100	nA
t _{ON}	Switch "ON" Time	R _L = 1kΩ, V _{analog} = -10V to +10V See Fig. 3		500			1000		ns
t _{OFF}	Switch "OFF" Time	R _L = 1kΩ, V _{analog} = -10V to +10V See Fig. 3		250			500		ns
Q _(INJ.)	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R _L = 100Ω, C _L ≤ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I ⁺	+ Power Supply Quiescent Current	V ⁺ = +15V, V ⁻ = -15V, V _L = +5V with GND	10	10	100	10	10	100	μA
I ⁻	- Power Supply Quiescent Current		10	10	100	10	10	100	μA
I _{V_L}	+5V Supply Quiescent Current		10	10	100	10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

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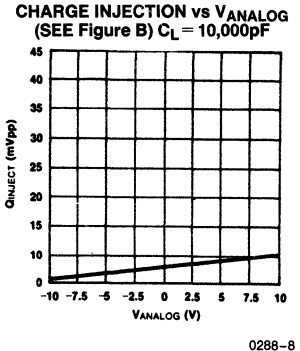
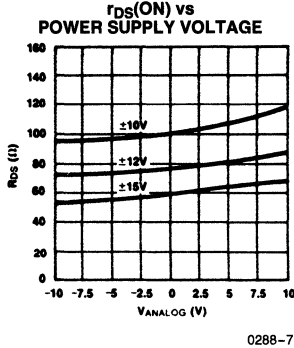
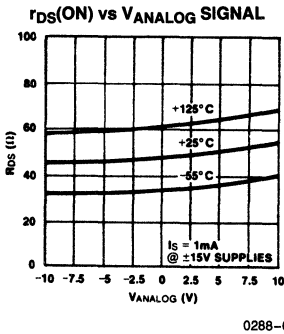
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS

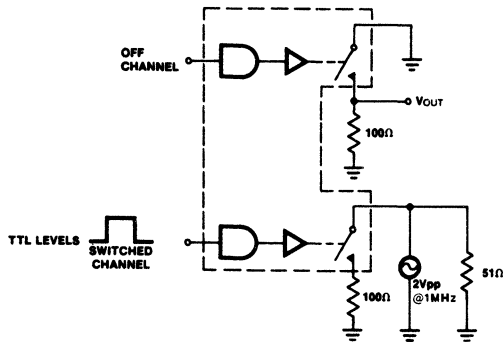
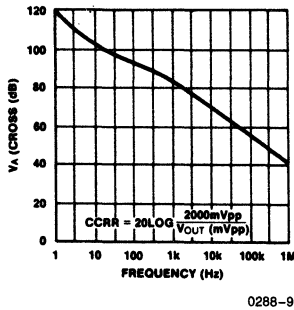


NOTE 1: The 5053 is turned on by high "1" logic inputs and the 5052 is turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)



CROSS COUPLING REJECTION vs FREQUENCY

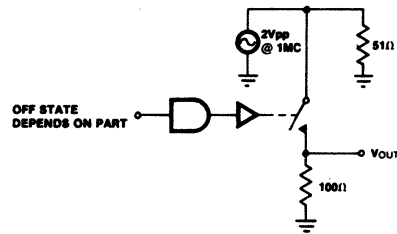
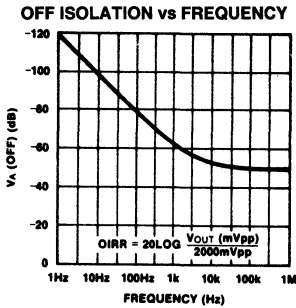


Cross Coupling Rejection Test Circuit

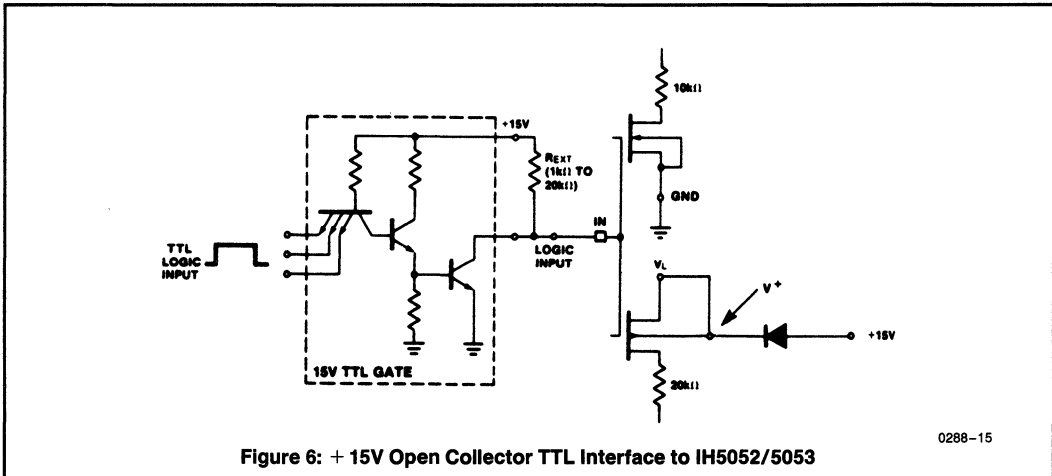
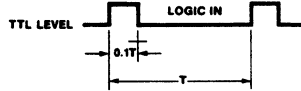
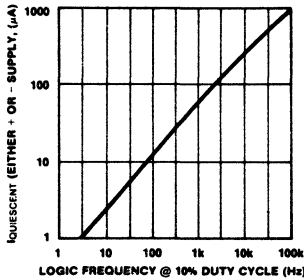
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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)



POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

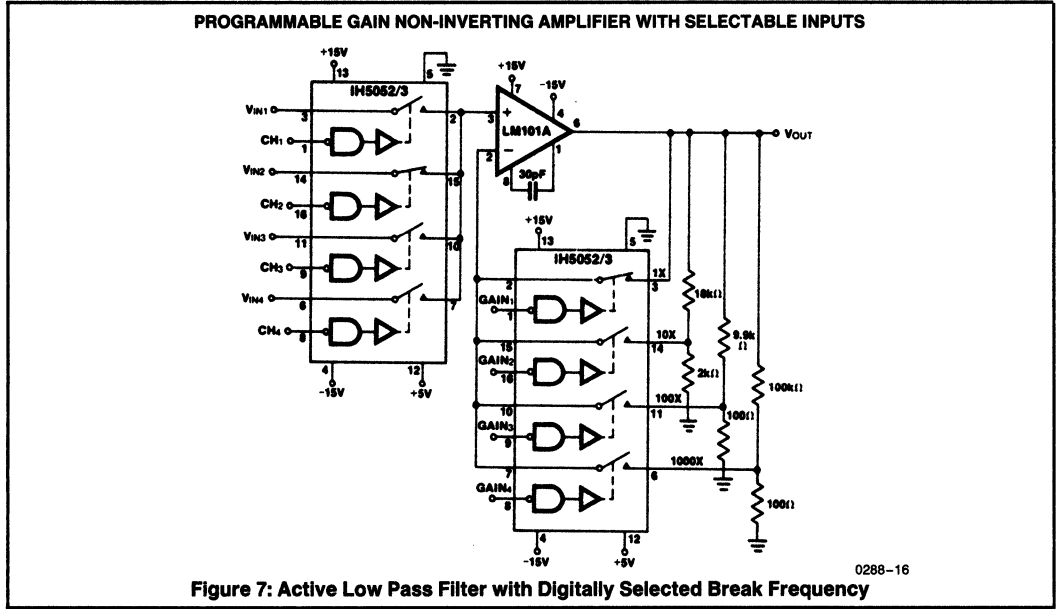
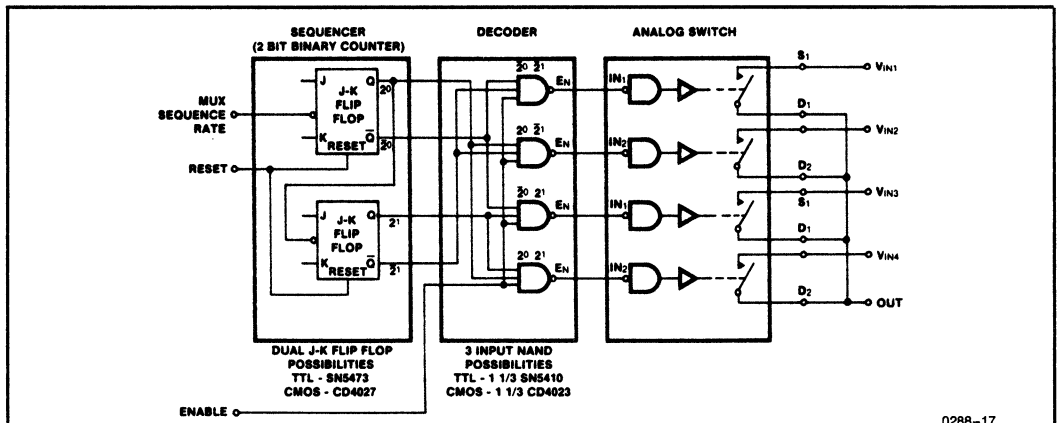


Figure 7: Active Low Pass Filter with Digitally Selected Break Frequency



TRUTH TABLE (IH5052)

Enable	Mux Sequence Rate	Sequencer Output		Switch States (- Denotes Off)			
		20	21	SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

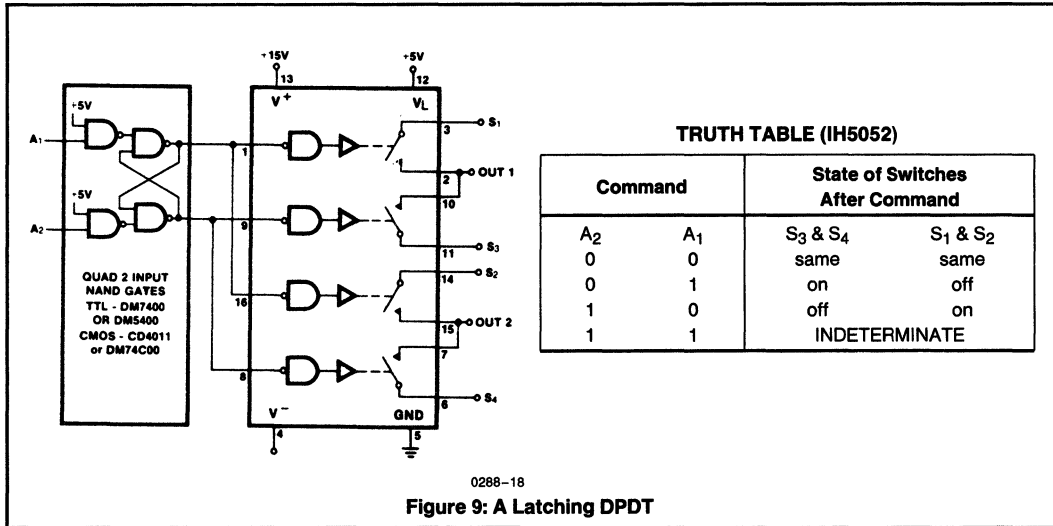
Figure 8: 4-Channel Sequencing MUX

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NOTE: All typical values have been characterized but are not tested.

A LATCHING DPDT SWITCH

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



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NOTE: All typical values have been characterized but are not tested.

IH5140-IH5145

High-Level CMOS Analog Switch



GENERAL DESCRIPTION

The IH5140 Family of CMOS switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 200pA at 25°C. Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1µA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Intersil's IH5040 family and part of the DG180/190 family as shown in the switching state diagrams.

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

- Note:** 1. Ceramic (side braze) devices also available; consult factory.
 2. MIL temp range parts also available with MIL-STD-883 processing.

FEATURES

- Super Fast Break-Before-Make Switching
- t_{on} 80ns Typ, t_{off} 50ns Typ (SPST Switches)
- Power Supply Currents Less Than 1µA
- OFF Leakages Less Than 100pA @ 25°C Typical
- Non-latching With Supply Turn-off
- Single Monolithic CMOS Chip
- Plug-in Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and Leakage
- Greater Than 1MHz Toggle Rate
- Switches Greater Than 20Vp-p Signals With ±15V Supplies
- TTL, CMOS Direct Compatibility
- Internal Diode in Series with V^+ for Fault Protection

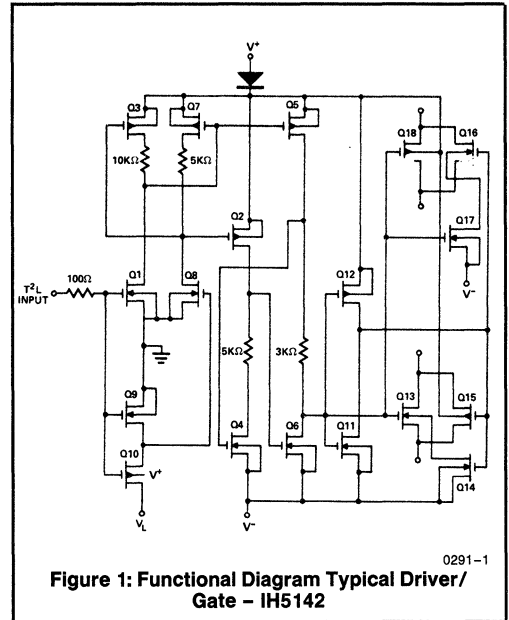


Figure 1: Functional Diagram Typical Driver/Gate - IH5142

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$	<36V
$V^+ - V_D$	<30V
$V_D - V^-$	<30V
$V_D - V_S$	<±22V
$V_L - V^-$	<33V
$V_L - V_{IN}$	<30V
V_L	<20V
V_{IN}	<20V

Current (Any Terminal)	<30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering 10sec)	300°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6 mW/°C Above 70°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

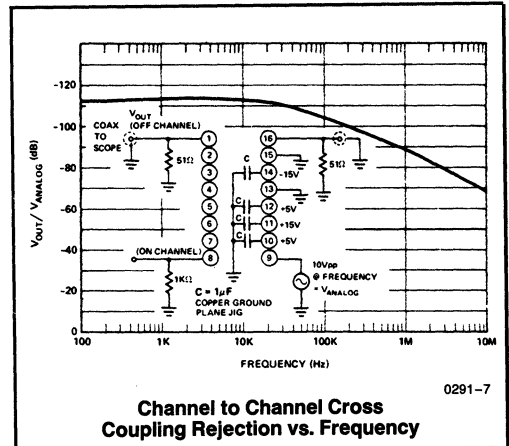
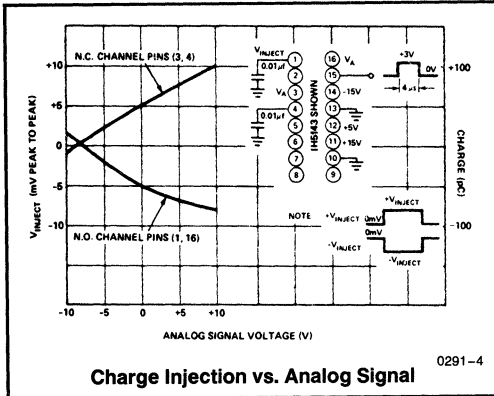
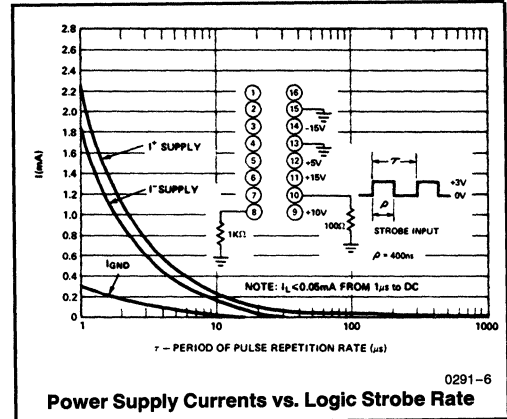
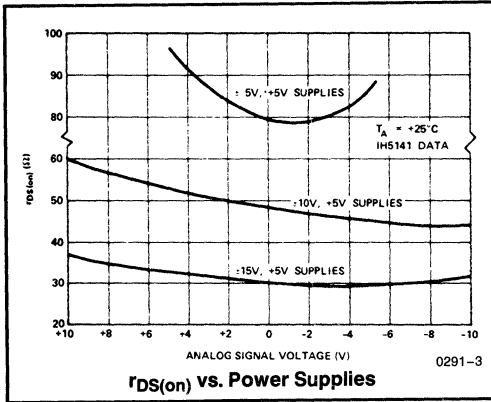
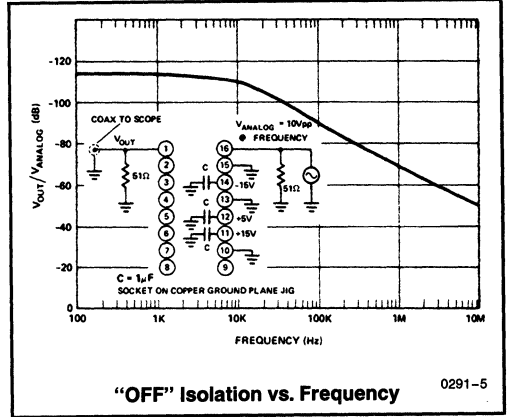
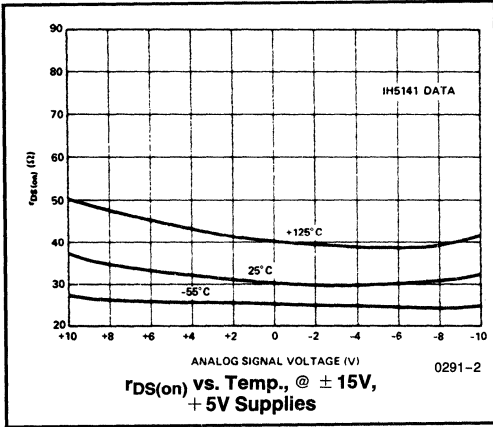
Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Commercial			
			-55°C	+25°C	+125°C	0	+25°C	+70°C	
LOGIC INPUT									
I_{INH}	Input Logic Current	$V_{IN} = 2.4V$ Note 1	±1	±1	10		±10	10	µA
I_{INL}	Input Logic Current	$V_{IN} = 0.8V$ Note 1	±1	±1	10		±10	10	µA
SWITCH									
$r_{DS(on)}$	Drain-Source On Resistance	$I_S = -10mA$ $V_{ANALOG} = -10V$ to $+10V$	50	50	75	75	75	100	Ω
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(off)} + I_{S(off)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$ $V_D = -10V$, $V_S = +10V$		±.5 ±.5	100 100		±5 ±5	100 100	nA
$I_{D(on)} + I_{S(on)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to $+10V$		±1	200		±2	200	nA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches See Performance Characteristics		54 (typ)			50 (typ)		dB
t_{on} t_{off}	Switch "ON" Time Switch "OFF" Time	See switching time specifications and timing diagrams.							
$Q_{(INJ.)}$	Charge Injection	See Performance Characteristics		10 (typ)			15 (typ)		pC
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Performance Characteristics		54 (typ)			50 (typ)		dB
SUPPLY									
I^+	+ Power Supply Quiescent Current	$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$ See Performance Characteristics	1.0	1.0	10.0	10	10	100	µA
I^-	- Power Supply Quiescent Current		1.0	1.0	10.0	10	10	100	µA
I_L	+ 5V Supply Quiescent Current		1.0	1.0	10.0	10	10	100	µA
I_{GND}	Gnd Supply Quiescent Current		1.0	1.0	10.0	10	10	100	µA

- NOTES:** 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



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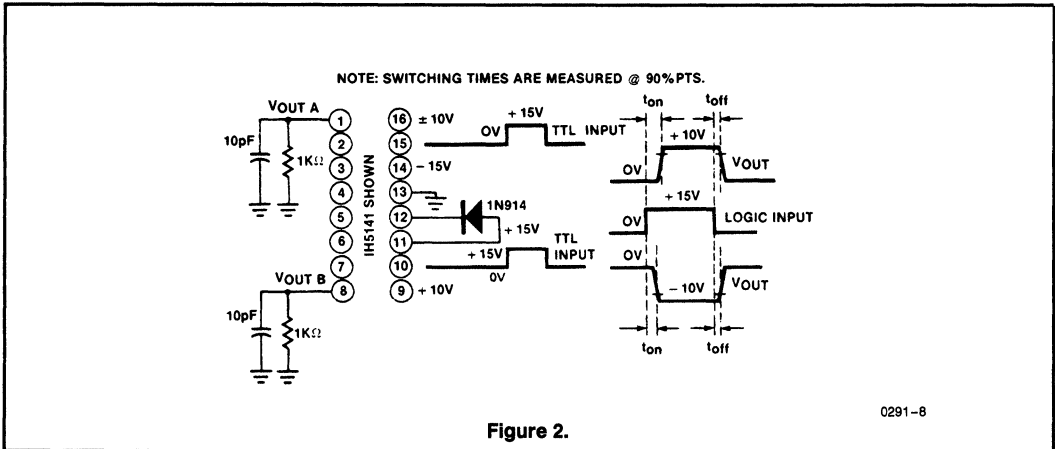
SWITCHING TIME SPECIFICATIONS

(t_{on} , t_{off} are maximum specifications and $t_{on-toff}$ is minimum specifications)

Part Number	Symbol	Characteristic	Test Conditions	Military			Commercial			Units
				-55°C	+25°C	+125°C	0	+25°C	+70°C	
IH5140-5141	t_{on}	Switch "ON" time	Figure 2*		100			150		ns
	t_{off}	Switch "OFF" time			75			125		
	$t_{on-toff}$	Break-before-make			10			5		
IH5142-5143	t_{on}	Switch "ON" time	Figure 3		150			175		ns
	t_{off}	Switch "OFF" time			125			150		
	$t_{on-toff}$	Break-before-make			*10 (typ)			5		
IH5144-5145	t_{on}	Switch "ON" time	Figure 2*		175			250		ns
	t_{off}	Switch "OFF" time			125			150		
	$t_{on-toff}$	Break-before-make			10			5		
	t_{on}	Switch "ON" time		Figure 3		200			300	
t_{off}	Switch "OFF" time		125				150			
$t_{on-toff}$	Break-before-make		10				5			

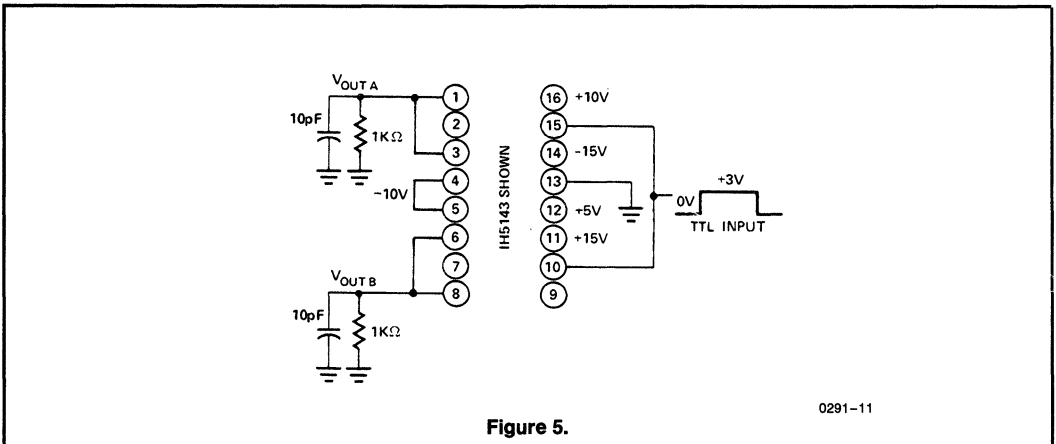
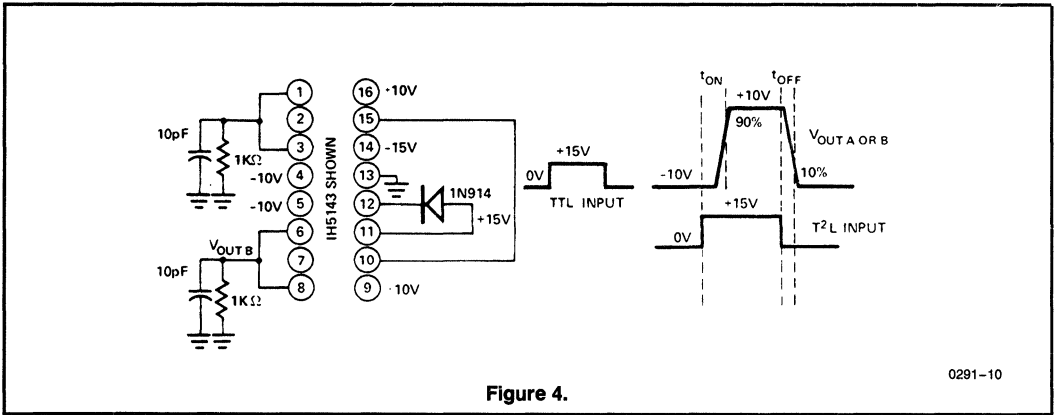
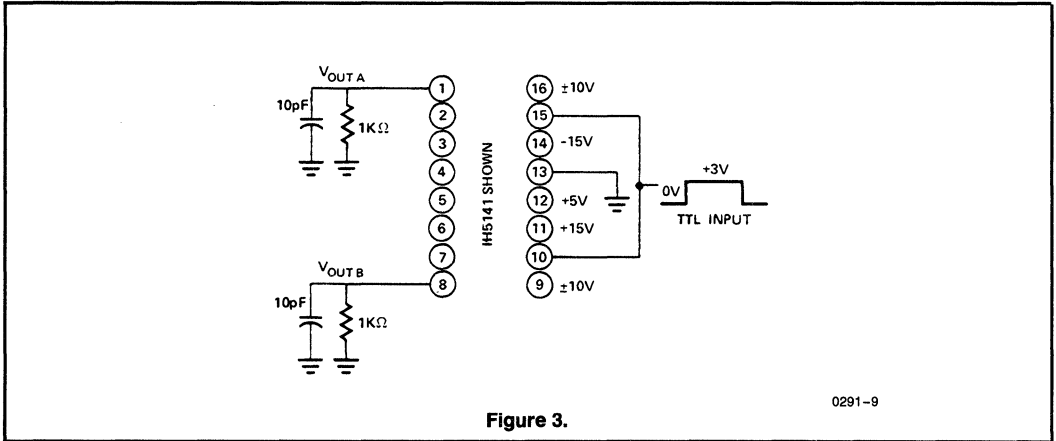
NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS.

* Typical values for design aid only, not guaranteed nor subject to production testing.



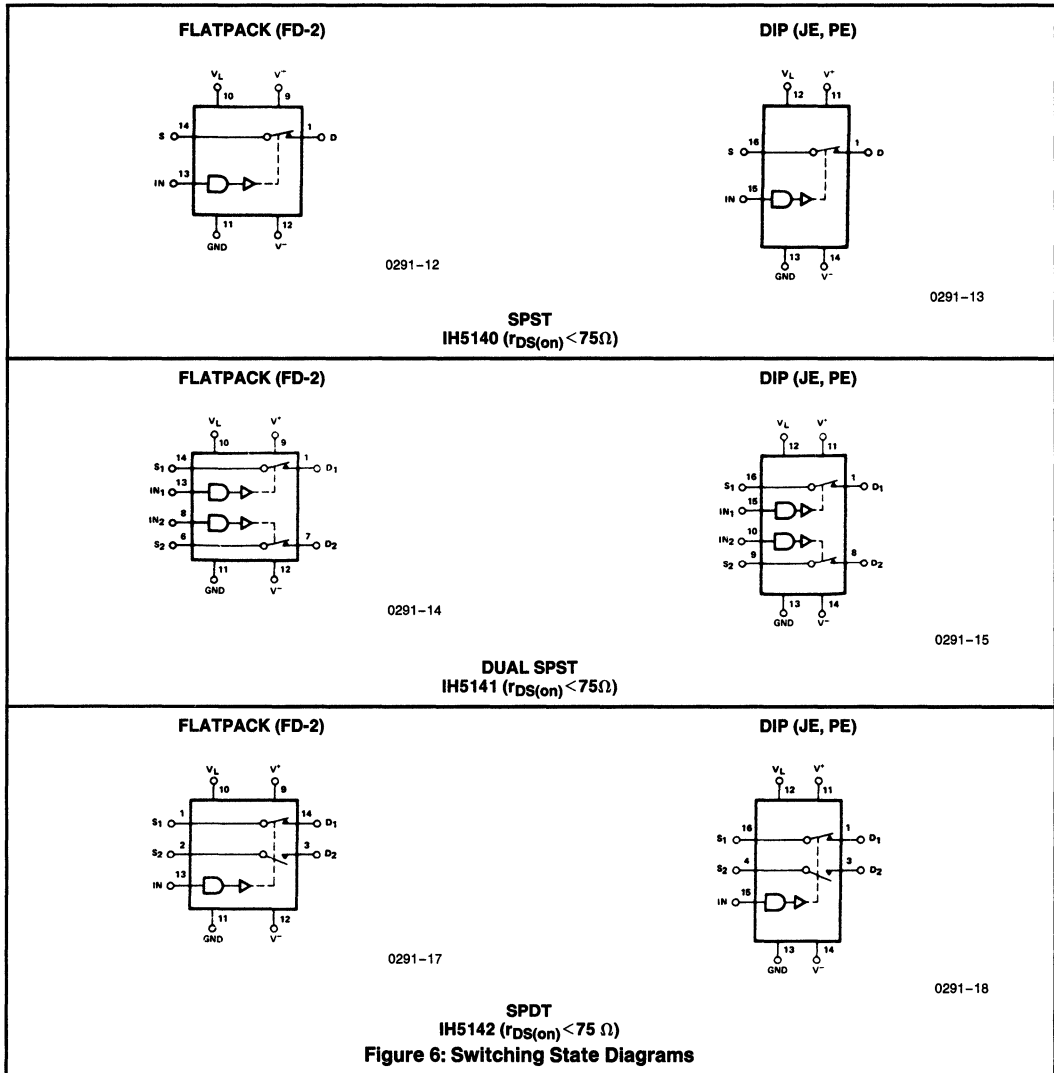
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NOTE: All typical values have been characterized but are not tested.



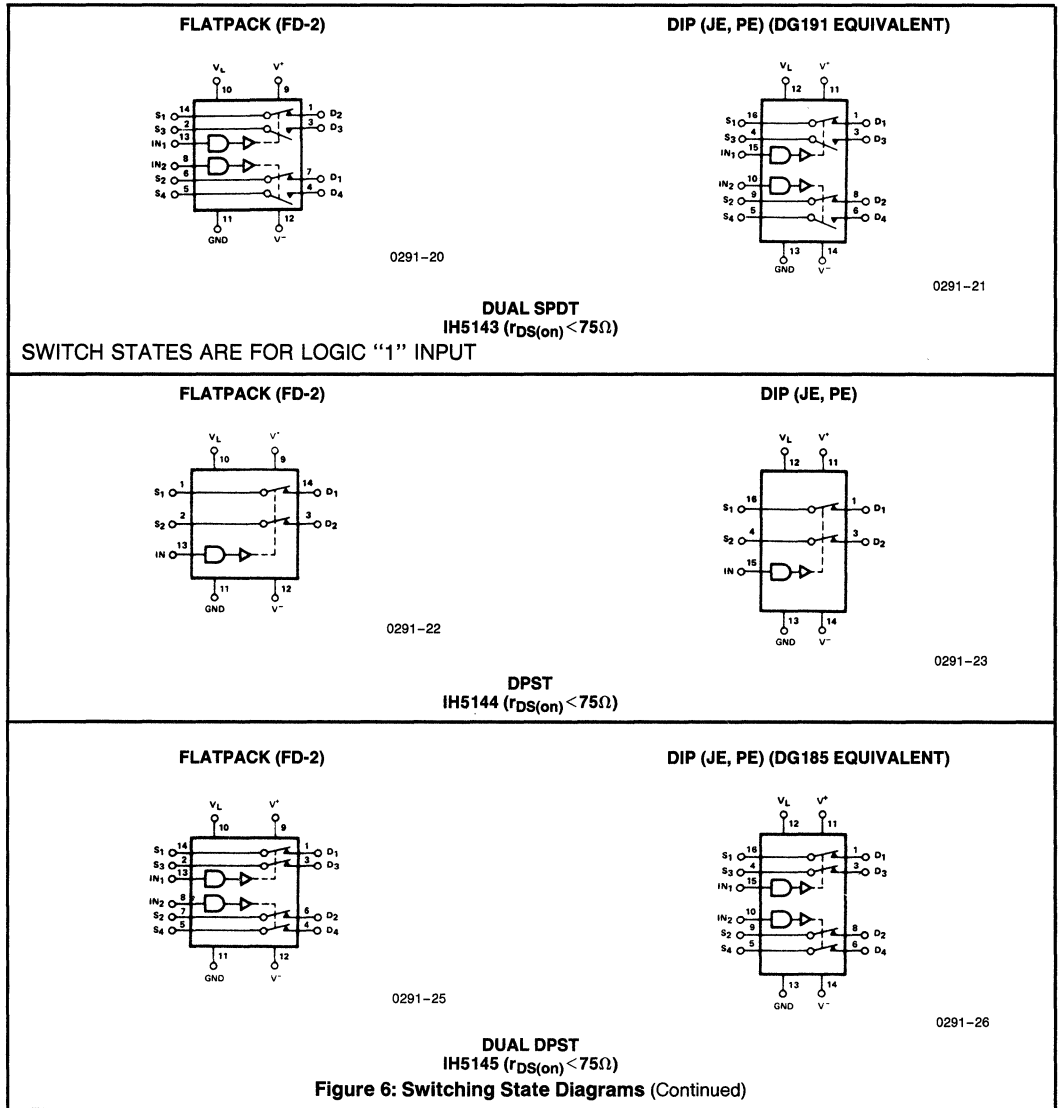
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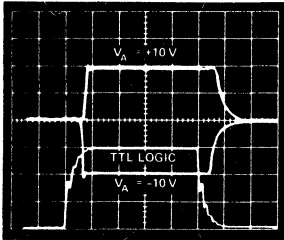


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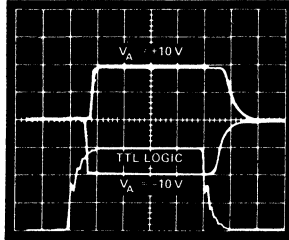
TYPICAL SWITCHING WAVEFORMS SCALE: VERT. = 5V/DIV. HORIZ. = 100ns/DIV.

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



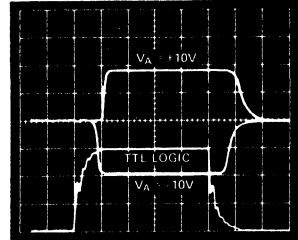
-55°C

0291-27



+25°C

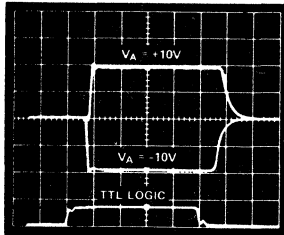
0291-28



+125°C

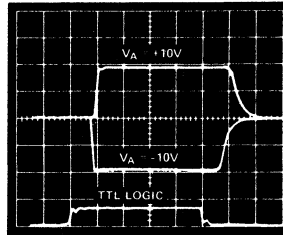
0291-29

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



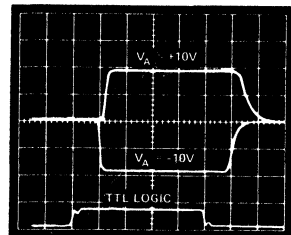
-55°C

0291-30



+25°C

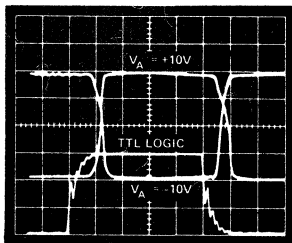
0291-31



+125°C

0291-32

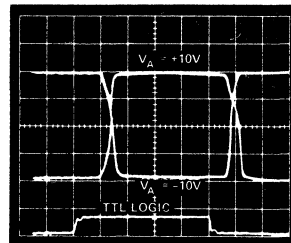
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 10)



+25°C

0291-33

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 11)



+25°C

0291-34

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NOTE: All typical values have been characterized but are not tested.

IH5140-IH5145 Family



APPLICATION NOTE

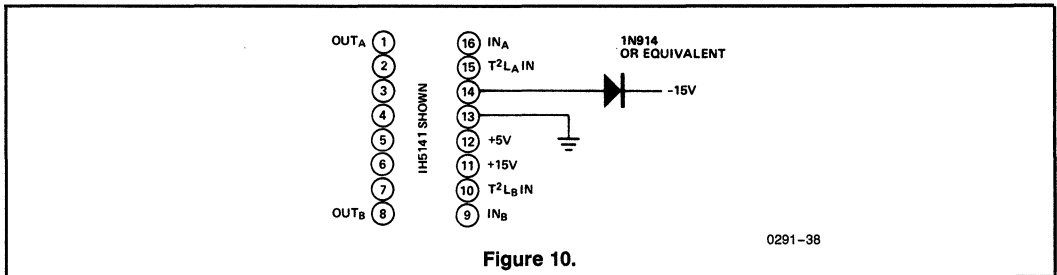
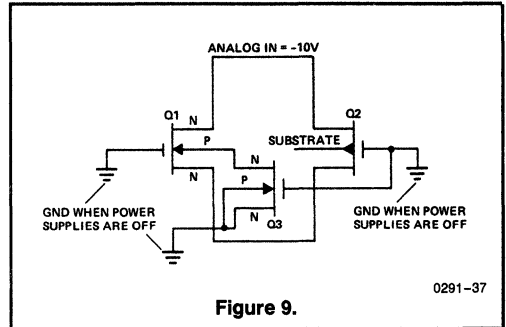
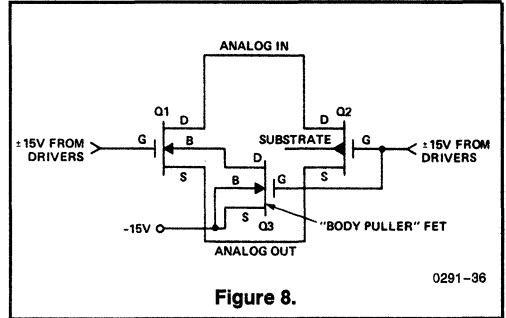
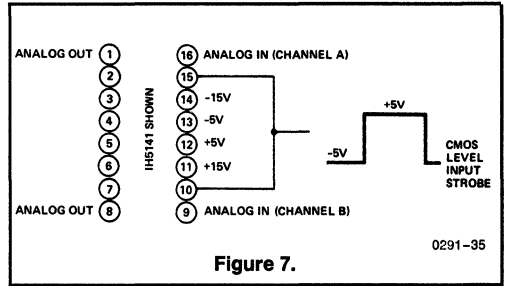
To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1k Ω or less collector resistor) should be used. This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns \rightarrow 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on} , t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if $\pm 5V$ strobe levels are used instead of the usual 0V \rightarrow +3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 7.

The typical channel of the IH5140 family consists of both P and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to -15V ($\pm 15V$ supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 8). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS(ON)}$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 9.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

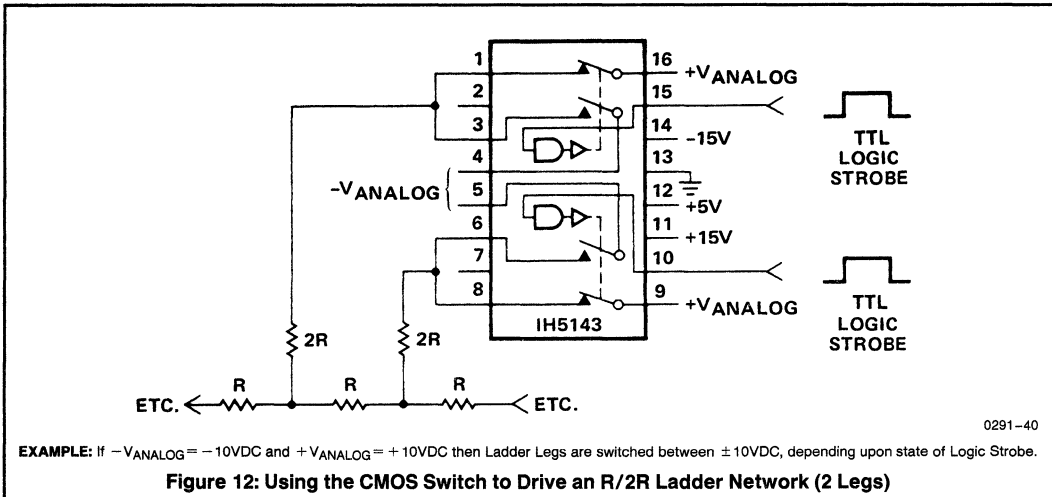
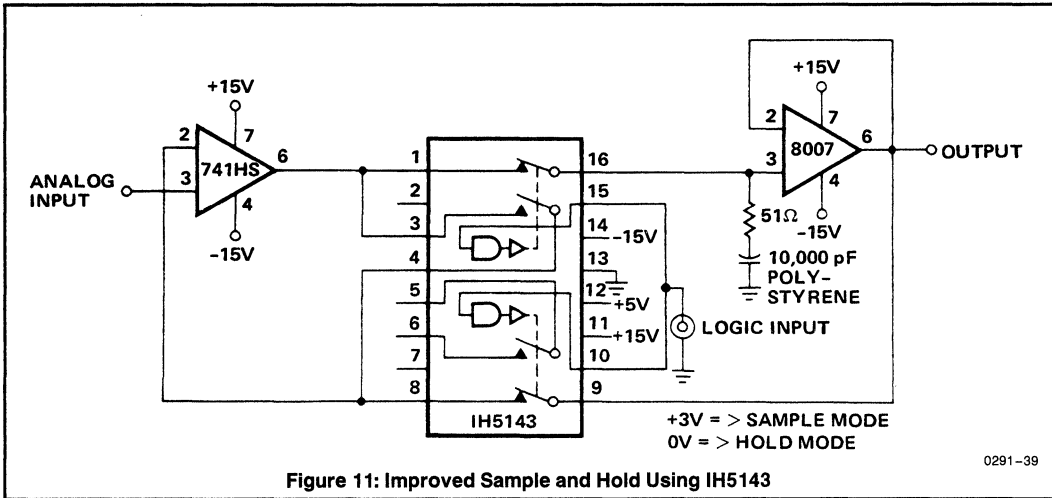
This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 10. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.



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NOTE: All typical values have been characterized but are not tested.

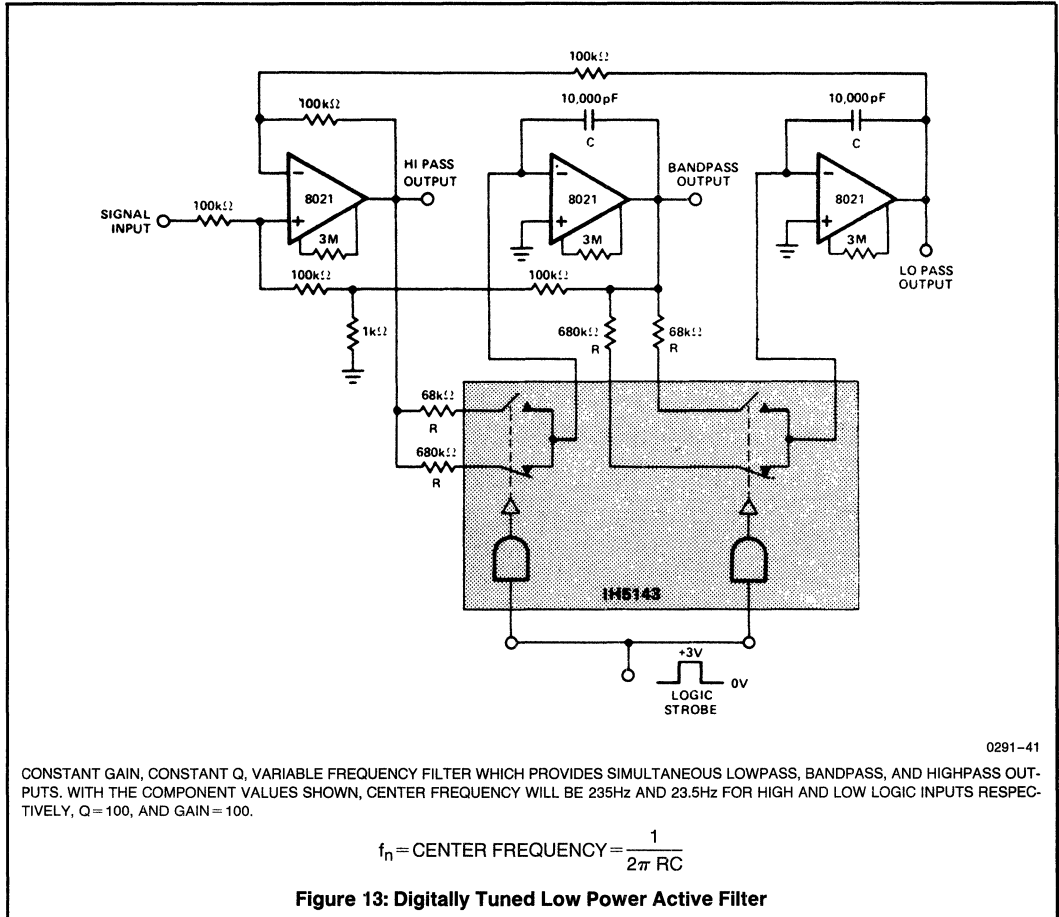
APPLICATIONS



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APPLICATIONS (Continued)



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NOTE: All typical values have been characterized but are not tested.

IH5148 - IH5151

High-Level CMOS Analog Switches



IH5148-IH5151

GENERAL DESCRIPTION

The IH5148 family of solid state analog switches are designed using an improved, high voltage CMOS technology. Destructive latchup has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present; the IH5148 CMOS technology has eliminated this problem.

Key performance advantages of the 5148 series are TTL compatibility and ultra low-power operation. $R_{DS(ON)}$ switch resistance is typically in the 14Ω To 18Ω Area, for signals in the $-10V$ to $+10V$ range. Quiescent current is less than $10\mu A$. The 5148 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200nsec typ.) such that it exceeds t_{OFF} time (120nsec typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Many of the devices in the 5148 series are pin-for-pin compatible with other analog switches, and offer improved electrical characteristics.

FEATURES

- Low $R_{DS(ON)}$ — 25Ω
- Switches Greater Than 20Vpp Signals With $\pm 15V$ Supplies
- Quiescent Current Less Than $100\mu A$
- Break-Before-Make Switching t_{OFF} 120nsec Typ., t_{ON} 200nsec Typical
- TTL, CMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- $\pm 5V$ to $\pm 15V$ Supply Range

CMOS ANALOG SWITCH PRODUCT CONDITIONING

- The Following Processes Are Performed 100% in Accordance With MIL-STD-883
- Precap Visual — Method 2010, Cond. B
- Stabilization Bake — Method 1008
- Temperature Cycle — Method 1010
- Centrifuge — Method 2001, Cond. E
- Hermeticity — Method 1014, Cond. A, C
- (Leak Rate $< 5 \times 10^{-7}$ atm cc/s)

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range	Harris Equivalent
IH5148MJE	Dual SPST	16 Pin CERDIP	$-55^{\circ}C$ to $125^{\circ}C$	HI-5048
IH5148CJE	Dual SPST	16 Pin CERDIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5048
IH5148CPE	Dual SPST	16 Pin Plastic DIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5048
IH5148MFD	Dual SPST	14 Pin Flat Pack	$-50^{\circ}C$ to $125^{\circ}C$	HI-5048
IH5149MJE	Dual DPST	16 Pin CERDIP	$-55^{\circ}C$ to $125^{\circ}C$	HI-5049
IH5149CJE	Dual DPST	16 Pin CERDIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5049
IH5149CPE	Dual DPST	16 Pin Plastic DIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5049
IH5149MFD	Dual DPST	14 Pin Flat Pack	$-50^{\circ}C$ to $125^{\circ}C$	HI-5049
IH5150MJE	SPDT	16 Pin CERDIP	$-55^{\circ}C$ to $125^{\circ}C$	HI-5050
IH5150CJE	SPDT	16 Pin CERDIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5050
IH5150CPE	SPDT	16 Pin Plastic DIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5050
IH5150MFD	SPDT	14 Pin Flat Pack	$-50^{\circ}C$ to $125^{\circ}C$	HI-5050
IH5151MJE	Dual SPDT	16 Pin CERDIP	$-55^{\circ}C$ to $125^{\circ}C$	HI-5051
IH5151CJE	Dual SPDT	16 Pin CERDIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5051
IH5151CPE	Dual SPDT	16 Pin Plastic DIP	$0^{\circ}C$ to $70^{\circ}C$	HI-5051
IH5151MFD	Dual SPDT	14 Pin Flat Pack	$-50^{\circ}C$ to $125^{\circ}C$	HI-5051

- NOTES: 1. Ceramic (side braze) devices also available; consult factory.
 2. MIL temp range parts also available with MIL-STD-883 processing.

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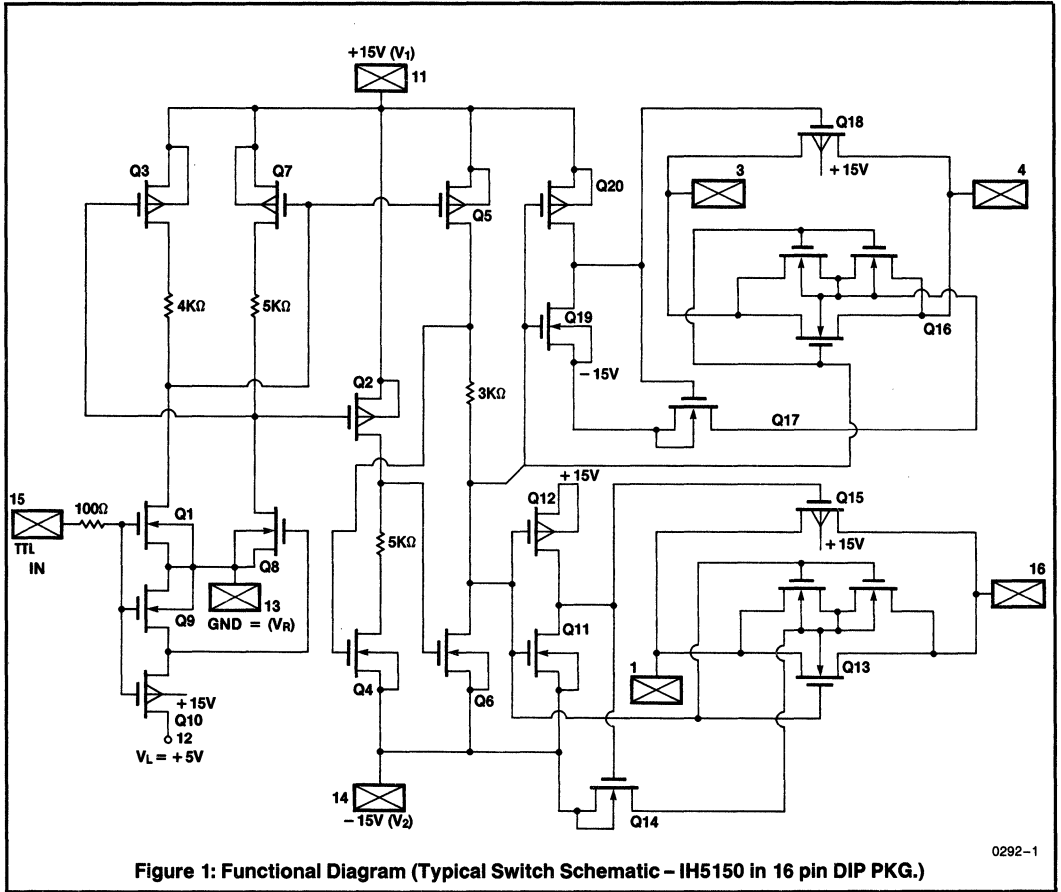
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+, V^-	<36V
V^+, V_D	<30V
V_D, V^-	<30V
V_D, V_S	< $\pm 22V$
V_L, V^-	<33V
V_L, V_{IN}	<30V
V_L	<20V
V_{IN}	<20V
Current (Any Terminal)	<50mA
Storage Temperature	-65°C to +150°C

Operating Temperature -55°C to +125°C
 Lead Temperature (Soldering, 10sec) 300°C
 Power Dissipation 450mW
 (All Leads Soldered to a P.C. Board)
 Derate 6mW/°C Above 70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0292-1

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ELECTRICAL CHARACTERISTICS (T_A @ 25°C, V⁺ = +15V, V⁻ = -15V, V_L = +5V)

Per Channel		Test Conditions	Min/Max Limits						Units
Symbol	Characteristic		Military			Commercial			
			-55°C	+25°C	+125°C	0	+25°C	+70°C	
I _{IN(ON)}	Input Logic Current	V _{IN} = 2.4V (Note 1)	±1	±1	±10		±1	±10	μA
I _{IN(OFF)}	Input Logic Current	V _{IN} = 0.8V (Note 1)	±1	±1	±10		±1	±10	μA
R _{DS(ON)}	Drain-Source On Resistance	V _D = ±10V, I _S = -10mA	25	25	50		30		Ω
ΔR _{DS(ON)}	Channel to Channel R _{DS(ON)} Match			10 (Typ)			15 (Typ)		Ω
V _{ANALOG}	Min. Analog Signal Handling Capability			±14 (Typ)			±14 (Typ)		V
I _{D(OFF)} I _{S(OFF)}	Switch OFF Leakage Current	V _{ANALOG} = -10V to +10V		±1.0	100		±2.0	100	nA
I _{D(ON)} + I _{S(ON)}	Switch On Leakage Current	V _D = V _S = -10V to +10V		±1.0	100		±2.0	100	nA
Q _(INJ)	Charge Injection	See Figure 4		(10) (Typ)			(10) (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	I = 1MHz, R _L = 100Ω, C _L ≤ 5pF, See Figure 5		54 (Typ)			50 (Typ)		dB

SUPPLY

I ⁺	+ Power Supply Quiescent Current		10	10	100		10		μA
I ⁻	- Power Supply Quiescent Current	V ₁ = +15V, V ₂ = -15V.	10	10	100		10		μA
I _L	+5V Supply Quiescent Current	V _L = +5V, V _R = 0	10	10	100		10		μA
I _{GND}	Gnd Supply Quiescent Current		10	10	100		10		μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Figure 8		54 (Typ)			50 (Typ)		dB

NOTE 1. Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce "ON" or "OFF" state.

SWITCHING TIME SPECIFICATION IH5148 SPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t _{on}	Switch "on" time	R _L = 1KΩ, V _{ANALOG} = -10V		250	ns
t _{off}	Switch "off" time	T _O + 10V; See Figures 3 and 6		200	ns

IH5149 DPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t _{on}	Switch "on" time	R _L = 1KΩ, V _{ANALOG} = -10V		350	ns
t _{off}	Switch "off" time	T _O + 10V; See Figures 3 and 6		250	ns

IH5150 & IH5151 SPDT SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t _{on}	Switch "on" time	R _L = 1KΩ, V _{ANALOG} = -10V		500	ns
t _{off}	Switch "off" time	T _O + 10V; See Figures 3 and 6		250	ns

NOTE 2. For IH5150 & IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 & 4 on 5150, & Pins 3 & 4, 5 & 6 on 5151) have slower t_{on} time, than channels on Pins 1, 16, & 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

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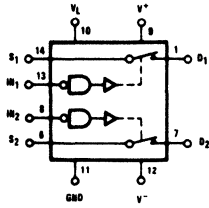
NOTE: All typical values have been characterized but are not tested.

SWITCH STATES ARE FOR LOGIC "1" INPUT

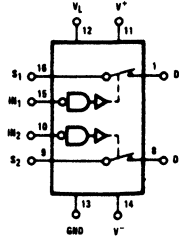
FLAT PACKAGE

DIP (DE) PACKAGE

DUAL SPST IH5148

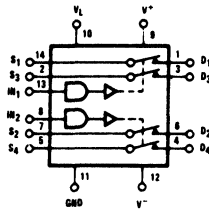


0292-2

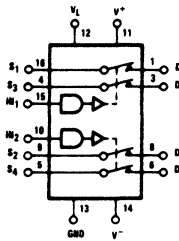


0292-3

DUAL DPST IH5149

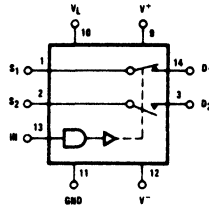


0292-5

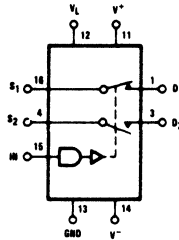


0292-6

SPDT IH5150

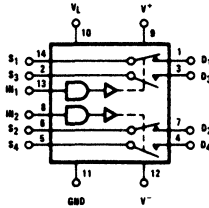


0292-7

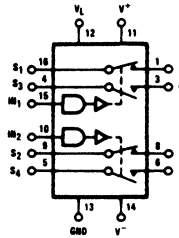


0292-8

DUAL SPDT IH5151



0292-10



0292-11

Figure 2: Switching State Diagrams

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TEST CIRCUITS

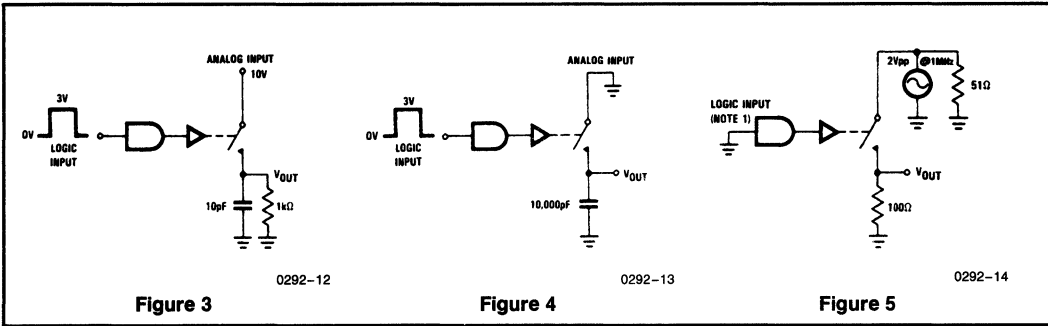


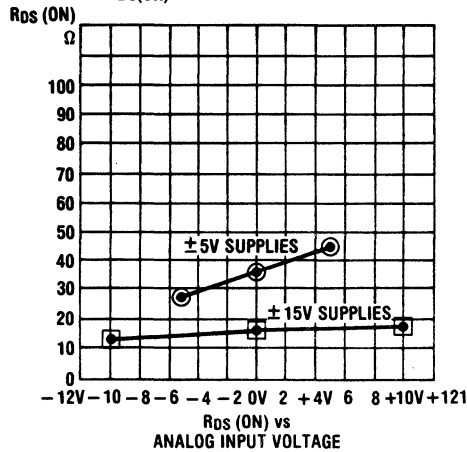
Figure 3

Figure 4

Figure 5

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

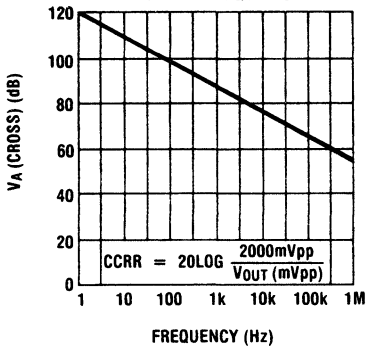
$R_{DS(ON)}$ @ $\pm 15V, \pm 5V$ SUPPLIES



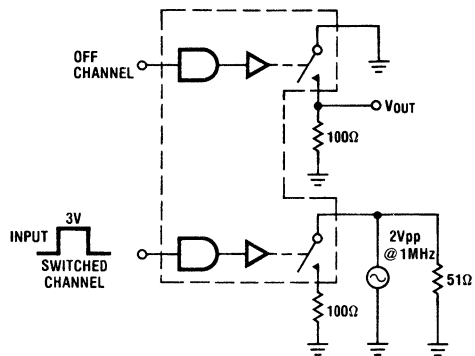
0292-15

8

CROSS COUPLING REJECTION vs FREQUENCY



0292-16



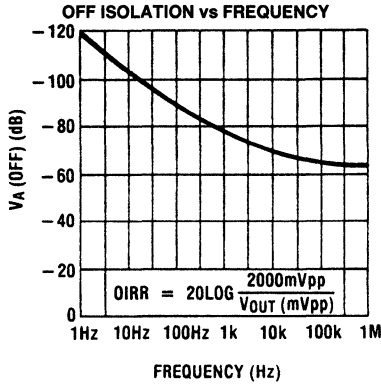
0292-17

CROSS COUPLING REJECTION TEST CIRCUIT

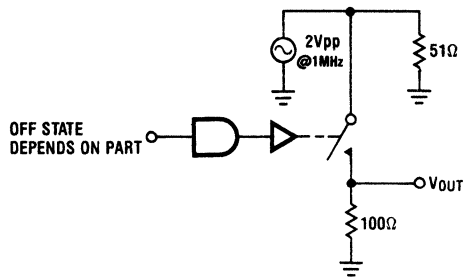
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TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)



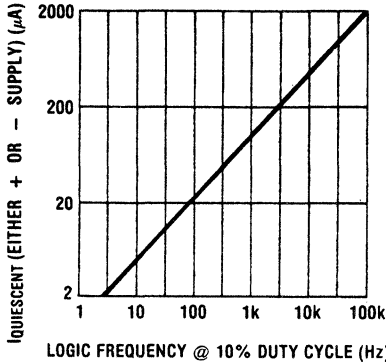
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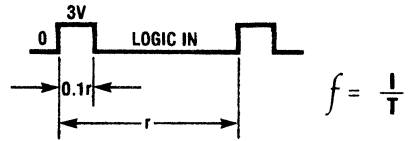
OFF ISOLATION TEST CIRCUIT

0292-19

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



0292-20



LOGIC INPUT WAVEFORM

0292-21

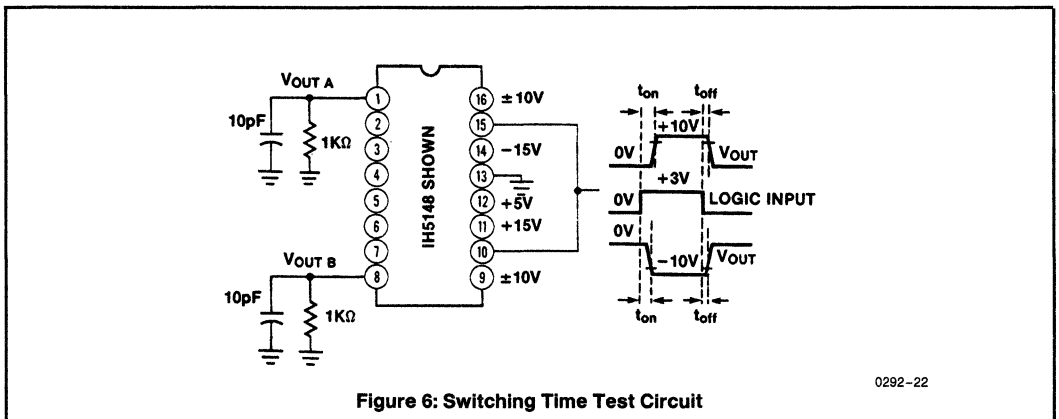


Figure 6: Switching Time Test Circuit

0292-22

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Nulling Out Charge Injection:

Charge injection (Q_{inj} , on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFET. The gates of these MOSFETs typically swing from $-15V$ to $+15V$ as a rapidly changing pulse; thus this $30V_{pp}$ pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$Q_{inject}(V_{pp}) \approx \frac{C_{gate}}{C_{Load}} \times 30V \text{ step.}$$

i.e.

$$C_{gate} = 1.5pF, C_{Load} = 1000pF, \text{ then}$$

$$Q_{inject}(V_{pp}) = \frac{1.5pF}{1000pF} \times 30V \text{ step} = 45mV_{pp}$$

Thus if you are using switch in a Sample & Hold application with $C_{sample} = 1000pF$, a $45mV_{pp}$ "Sample to Hold error step" will occur.

To null this error step out to zero the following circuit can be used:

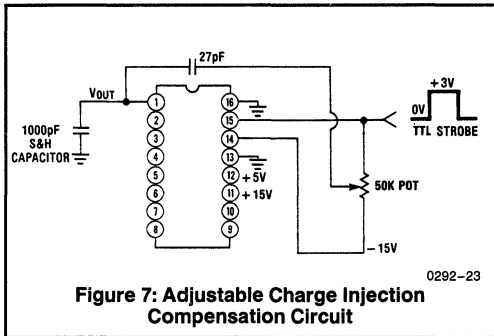


Figure 7: Adjustable Charge Injection Compensation Circuit

The circuit shown above nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until $V_{OUT} = 0mV_{pp}$ pulse, with $V_{ANALOG} = 0V$.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the following circuit should be used:

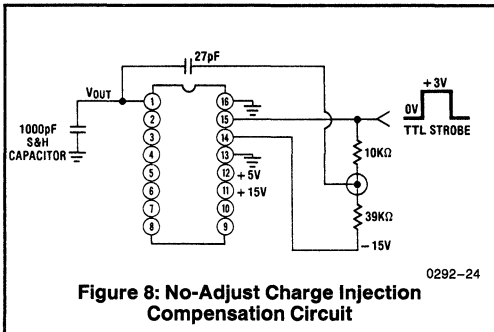


Figure 8: No-Adjust Charge Injection Compensation Circuit

This configuration will produce a typical charge injection of $V_{OUT} \leq 10mV_{pp}$ into the $1000pF$ S & H capacitor shown.

Fault Condition Protection

If your system has analog voltage levels which are independent of the $\pm 15V$ (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown below:

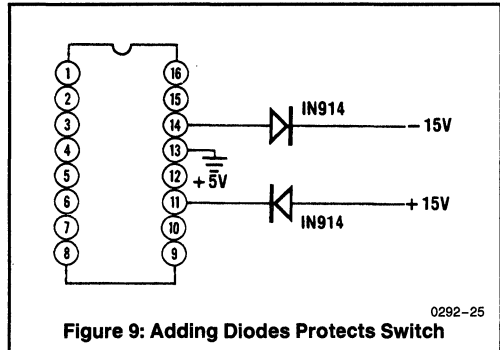


Figure 9: Adding Diodes Protects Switch

If the analog input levels are below $\pm 15V$, the pn junctions of Q13 & Q15 are reversed biased. However if the $\pm 15V$ supplies are shut off and analog levels are still present, the configuration becomes:

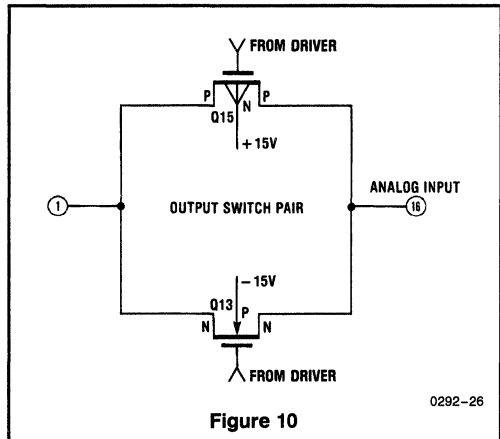
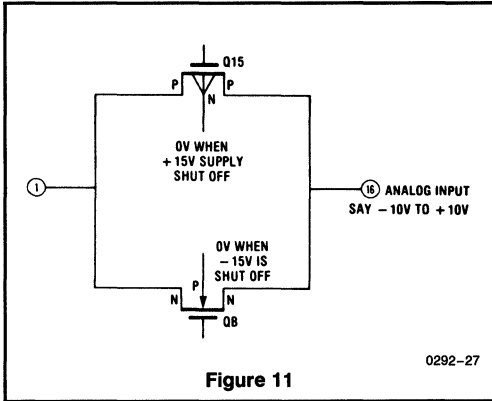


Figure 10

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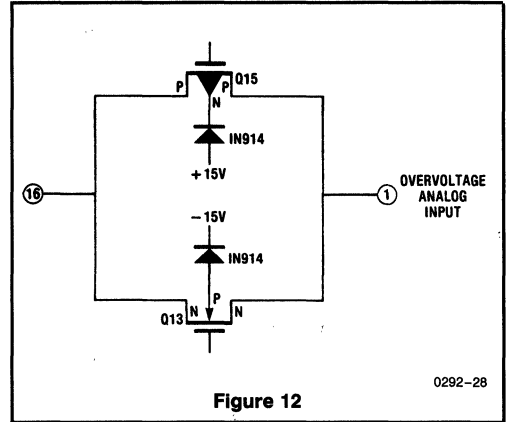
The need for these diodes, in this circumstance, is shown below:



If ANALOG in is greater than 1V, then the pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG in was less than or equal to -1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 & Q15 bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about $\pm 18V$ ANALOG overvoltages. Beyond this drain(N) to body(P) breakdown VOLTAGE of Q13 limits overvoltage protection.



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NOTE: All typical values have been characterized but are not tested.

IH5341

Dual SPST CMOS RF/Video Switch



IH5341

GENERAL DESCRIPTION

The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically $t_{on} = 150ns$ and $t_{off} = 80ns$, and "Break-Before-Make" switching is guaranteed.

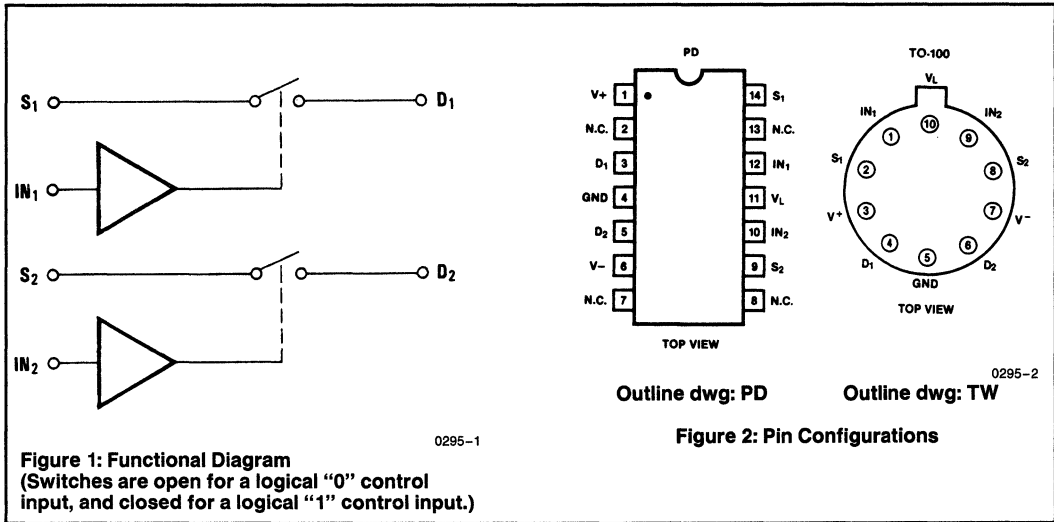
Switch "ON" resistance is typically $40\Omega - 50\Omega$ with $\pm 15V$ power supplies, increasing to typically 175Ω for $\pm 5V$ supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

FEATURES

- $R_{DS(on)} < 75\Omega$
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation $> 70dB$ Typical @ 10MHz
- Cross Coupling Isolation $> 60dB$ @ 10MHz
- Compatible With TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current $\leq 1\mu A$
- "Break-Before-Make" Switching
- Fast Switching (80ns/150ns Typ)

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5341CPD	0 to +70°C	14-pin PLASTIC DIP
IH5341ITW	-20°C to +85°C	10-pin TO-100
IH5341MTW	-55°C to +125°C	10-pin TO-100



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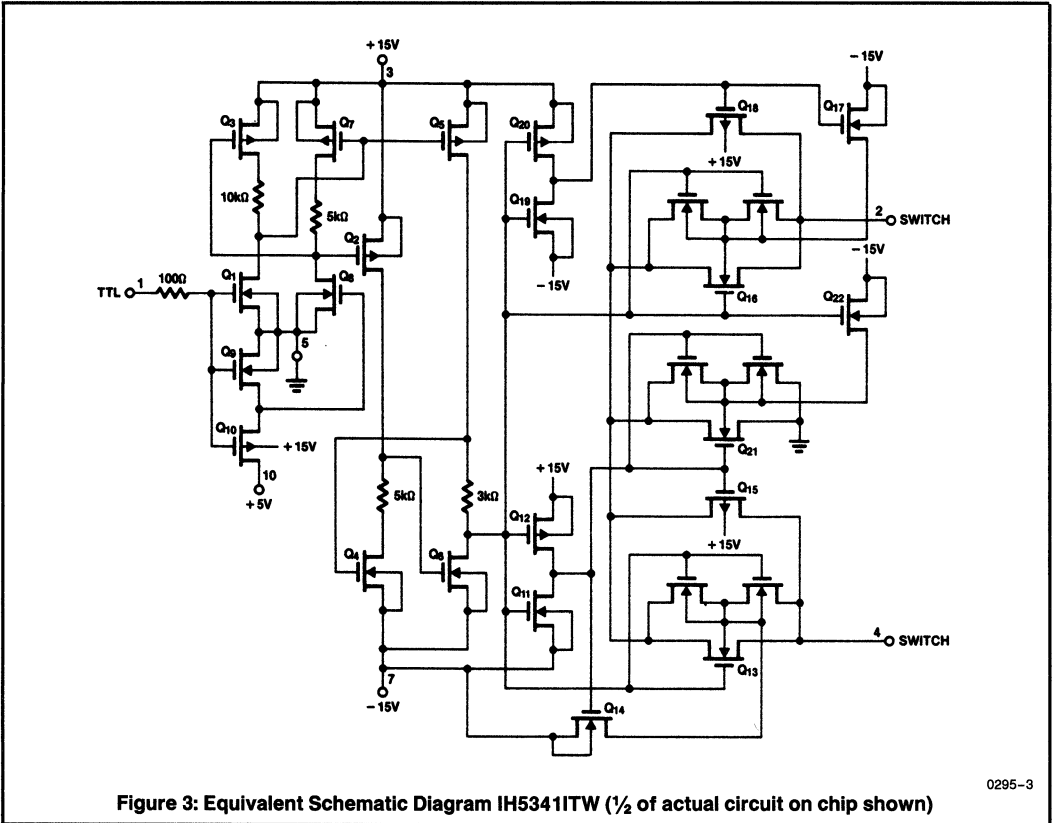
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V ⁺ to Ground	+ 18V
V ⁻ to Ground	- 18V
V _I to Ground	V ⁺ to V ⁻
Logic Control Voltage	V ⁺ to V ⁻
Analog Input Voltage	V ⁺ to V ⁻
Current (any Terminal)	50mA
Operating Temperature:		
(M Version)	-55°C to + 125°C
(I Version)	-25°C to + 85°C
(C Version)	0°C to + 70°C

Storage Temperature	- 65°C to + 150°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	250mW
Derate above 25°C @	7.5mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0295-3

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NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS

 $V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25^\circ C$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Typ	M Grade Device			I/C Grade Device			Units
				-55°C	+25°C	+125°C	-25/ 0°C	+25°C	+85/ +70°C	
V^+ V_L V^-	Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	(Note 3)	4.5 > 16 4.5 > V^+ -4 > -16							V
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	$V_D = \pm 5V$ $I_S = 10mA$, $V_{IN} \geq 2.4V$ $V_D = \pm 10V$		75	75	100	75	75	100	Ω
$R_{DS(on)}$	Switch "ON" Resistance	$V^+ = V_L = +5V$, $V_{IN} = 3V$ $V^- = -5V$, $V_D = \pm 3V$ $I_S = 10mA$		125	125	175	150	150	175	
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	$I_S = 10mA$, $V_D = \pm 5V$	5	250	250	350	300	300	350	
V_{IH} V_{IL}	Logical "1" Input Voltage Logical "0" Input Voltage		>2.4 <0.8							V
$I_{D(off)}$ or $I_{S(off)}$	Switch "OFF" Leakage (Notes 2 and 4)	$V_{S/D} = \pm 5V$ $V_{IN} \leq 0.8V$ $V_{S/D} = \pm 14V$		± 0.5	50		± 1.0	100		nA
$I_{D(on)}$ + $I_{S(on)}$	Switch "ON" Leakage	$V_{S/D} = \pm 5V$ $V_{IN} \geq 2.4V$ $V_{S/D} = \pm 14V$		± 1	50		± 2	100		
I_{IN}	Input Logic Current	$V_{IN} \geq 2.4V$ or $< 0V$	0.1	± 1	± 1	10	± 1	± 1	10	μA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	
I^-	Negative Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	
I_L	Logic Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	

NOTES: 1. Typical values are not tested in production. They are given as a design aid only.

2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.

3. These are the operating voltages at which the other parameters are tested, and are not directly tested.

4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

AC ELECTRICAL CHARACTERISTICS

 $V^+ = +15V$, $V_L = +5V$, $V^- = 0V$, $T_A = 25^\circ C$ unless otherwise specified (Note 5).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{on}	Switch "ON" Time	See Figure 4		150	300	ns
t_{off}	Switch "OFF" Time	See Figure 4		80	150	
OIRR	"OFF" Isolation Rejection Ratio	See Figure 5 (Note 6)		70		dB
CCRR	Cross Coupling Rejection Ratio	See Figure 6 (Note 6)		60		
f_{3dB}	Switch Attenuation 3dB Frequency	See Figure 7 (Note 6)		100		

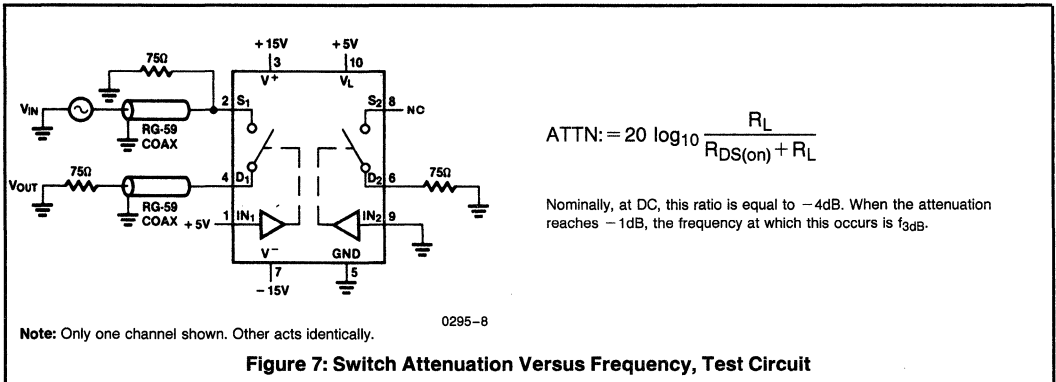
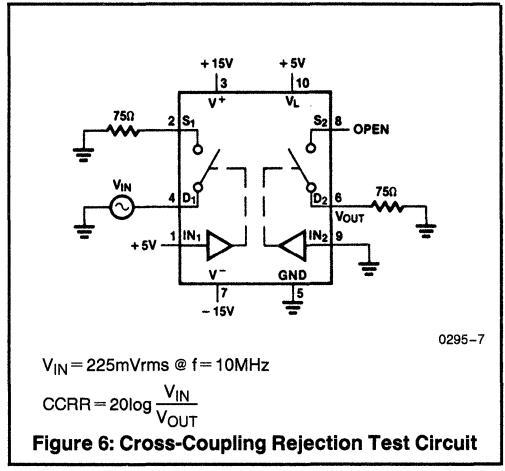
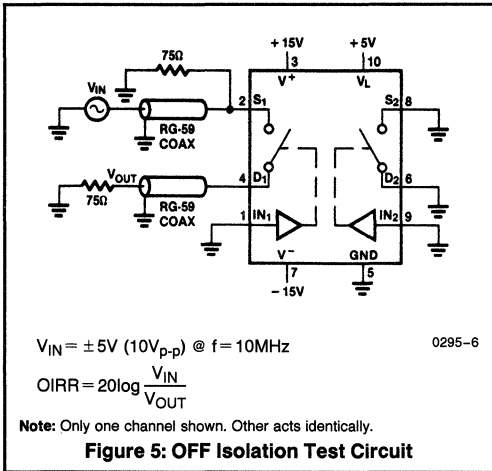
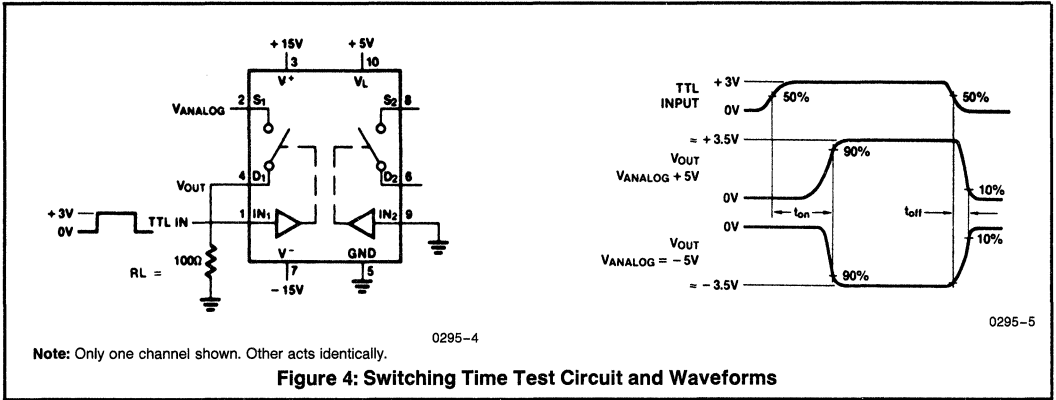
NOTES: 5. All AC parameters are sample tested only.

6. Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

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NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS

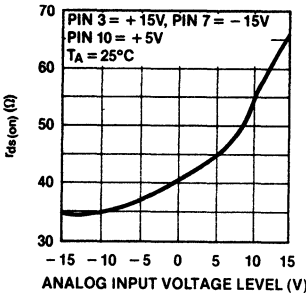


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NOTE: All typical values have been characterized but are not tested.

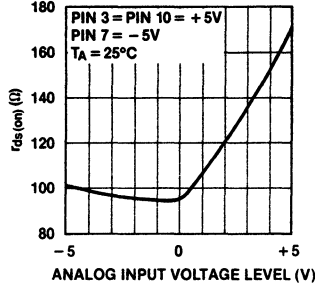
TYPICAL PERFORMANCES CHARACTERISTICS

$R_{DS(on)}$ Versus Analog Input Voltage with $\pm 15V$ Power Supplies



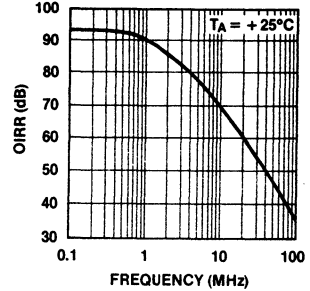
0295-9

$R_{DS(on)}$ Versus Analog Input Level with $\pm 5V$ Power Supplies



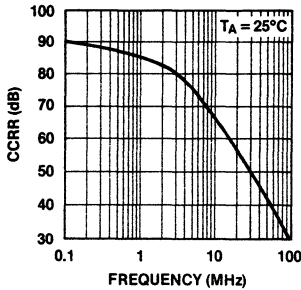
0295-10

OIRR (OFF Isolation Rejection) Versus Frequency (See Figure 5)



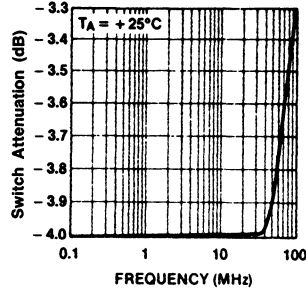
0295-11

CCRR (Cross Coupling Rejection) Versus Frequency (See Figure 6)

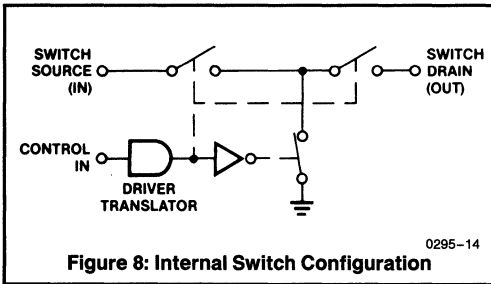


0295-12

Typical Switch Attenuation Versus Frequency ($R_L = 75\Omega$, See Figure 7)



0295-13



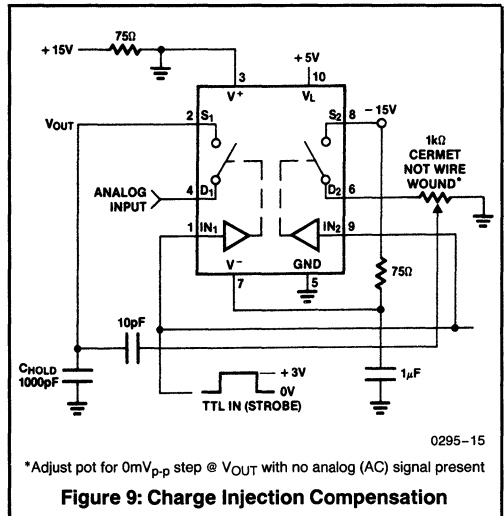
0295-14

Figure 8: Internal Switch Configuration

DETAILED DESCRIPTION

As can be seen in Figure 8, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much better isolation between the input and the output than a single series switch does, especially at high frequencies. The result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, giving very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility.



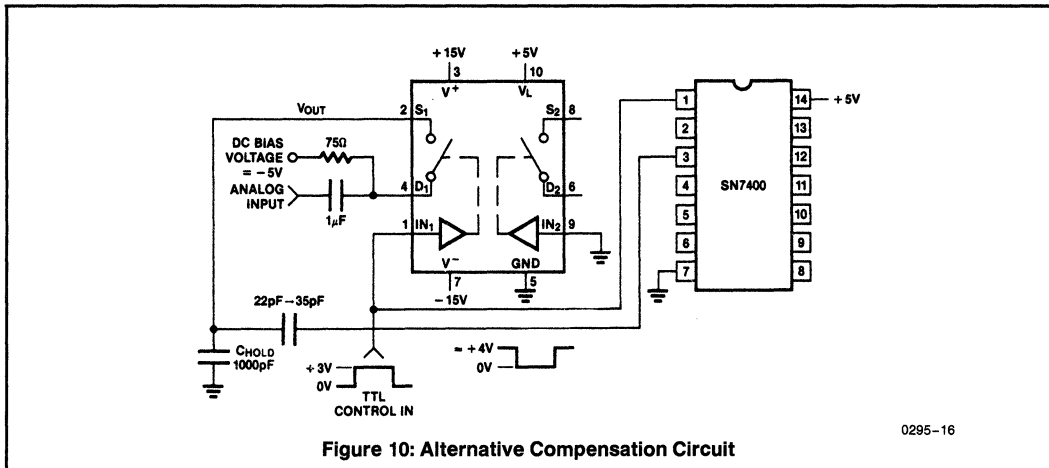
0295-15

*Adjust pot for 0mV_{p-p} step @ V_{OUT} with no analog (AC) signal present

Figure 9: Charge Injection Compensation

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NOTE: All typical values have been characterized but are not tested.



0295-16

APPLICATIONS

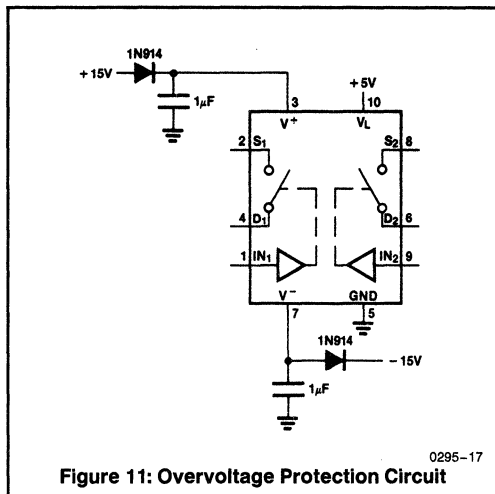
Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 9 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the -5V to +5V range.

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 10. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to -5V as shown in the figure. The choice of -5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.



0295-17

Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 11.

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NOTE: All typical values have been characterized but are not tested.

IH5352

QUAD SPST CMOS

RF/Video Switch



IH5352

GENERAL DESCRIPTION

The IH5352 is a QUAD SPST, CMOS monolithic video switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically $t_{on} = 150ns$ and $t_{off} = 80ns$, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically $40\Omega - 50\Omega$ with $\pm 15V$ power supplies, increasing to typically 175Ω for $\pm 5V$ supplies.

ORDERING INFORMATION

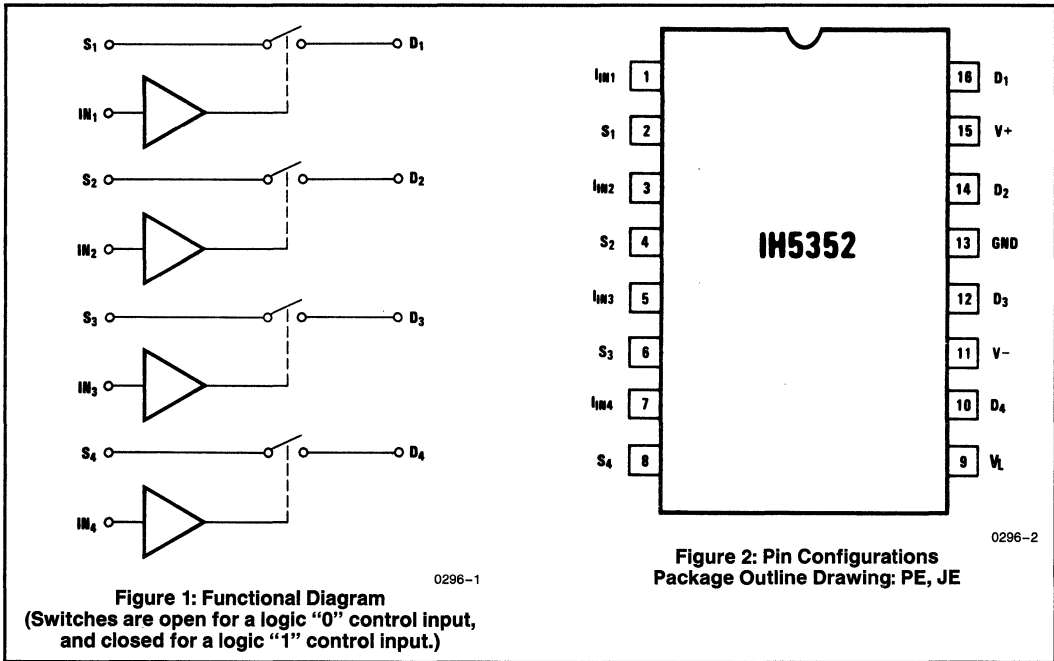
Part Number	Temperature Range	Package
IH5352CPE	0°C to +70°C	16-PIN PLASTIC DIP
IH5352JE	-25°C to +85°C	16-PIN CERDIP
IH5352MJE	-55°C to +125°C	16-PIN CERDIP

FEATURES

- $R_{DS(on)} < 75\Omega$
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation $> 70dB$ Typical @ 10MHz
- Cross Coupling Isolation $> 60dB$ @ 10MHz
- Directly Compatible with TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current $< 1\mu A$
- "Break-Before-Make" Switching
- Fast Switching (80ns/150ns Typ)

APPLICATIONS

- Video Switch
- Communications Equipment
- Disk Drives
- Instrumentation
- CATV



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

V^+ to Ground +18V	Storage Temperature -65°C to $+160^\circ\text{C}$
V^- to Ground -18V	Lead Temperature	
V_L to Ground V^+ to V^-	(Soldering, 10sec) 300°C
Logic Control Voltage V^+ to V^-	Power Dissipation:	
Analog Input Voltage V^+ to V^-	CERDIP 450mW
Current (any terminal) $<50\text{mA}$	derate $4\text{mW}/^\circ\text{C}$ above 25°C	
Operating Temperature:		Plastic 350mW
(M Version) -55°C to $+125^\circ\text{C}$	derate $3\text{mW}/^\circ\text{C}$ above 25°C	
(I Version) -20°C to $+85^\circ\text{C}$		
(C Version) 0°C to $+70^\circ\text{C}$		

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V^+ = +15\text{V}$, $V^- = -15\text{V}$, $V_L = +5\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Typ @25°C	Maximum Ratings						Units
				M Grade Device			I/C Grade Device			
				-55°C	+25°C	+125°C	-25/0°C	+25°C	+85/ +70°C	
V^+	Supply Voltage Ranges: Positive Supply	(Note 3)	5 to 15							V
V_L	Logic Supply		5 to 15							
V^-	Negative Supply		-5 to -15							
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	$I_S = 10\text{mA}$, $V_D = \pm 5\text{V}$ $V_{IN} \geq 2.4\text{V}$, $V_D = \pm 10\text{V}$	50	75	75	100	75	75	100	Ω
$R_{DS(on)}$	Switch "ON" Resistance	$I_S = 10\text{mA}$, $V^+ =$ $V_L = +5\text{V}$, $V^- = -5\text{V}$, $V_D = \pm 3\text{V}$, $V_{IN} = 3\text{V}$	175	250	250	350	300	300	350	
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	$I_S = 10\text{mA}$, $V_D = \pm 5\text{V}$	5							
V_{IH}	Logical "1" Input Voltage		>2.4							V
V_{IL}	Logical "0" Input Voltage		<0.8							
$I_{D(off)}$ or $I_{S(off)}$	Switch 'OFF' Leakage (Note 2 and 4)	$V_{S/D} = \pm 5\text{V}$ $V_{S/D} = \pm 14\text{V}$ $V_{IN} \leq 0.8\text{V}$			± 1.0	50		± 2.0	100	nA
$I_{D(on)}$ +	Switch 'ON' Leakage	$V_{S/D} = \pm 5\text{V}$ $V_{S/D} = \pm 14\text{V}$ $V_{IN} \geq 2.4\text{V}$			± 1.0	100		± 2.0	100	
$I_{S(on)}$					± 1.0	100		± 2.0	100	
I_{IN}	Logic Control Input Current	$V_{IN} \geq 2.4\text{V}$ or $<0\text{V}$	0.1	± 1	± 1	10	± 1	± 1	10	μA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0\text{V}$ or $+5\text{V}$	0.1	1	1	10	1	1	10	
I^-	Negative Supply Quiescent Current	$V_{IN} = 0\text{V}$ or $+5\text{V}$	0.1	1	1	10	1	1	10	
I_L	Logic Supply Quiescent Current	$V_{IN} = 0\text{V}$ or $+5\text{V}$	0.1	1	1	10	1	1	10	

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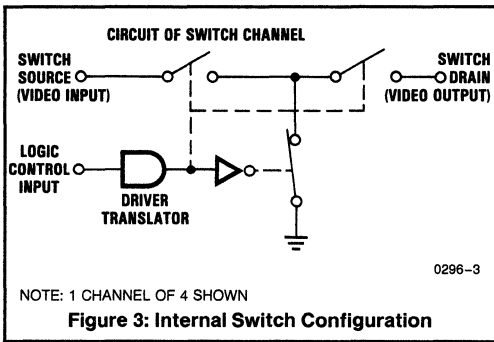
NOTE: All typical values have been characterized but are not tested.

AC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +15V$, $V^- = -15V$, $T_A = 25^\circ C$ unless otherwise specified (Note 5).

Symbol	Parameter	Min	Typ	Max	Unit
t_{on}	Switch "ON" Time		150	300	ns
t_{off}	Switch "OFF" Time		80	150	
OIRR	"OFF" Isolation Rejection Ratio		70		dB
CCRR	Cross Coupling Rejection Ratio		60		
f_{3dB}	Switch Attenuation 3dB Frequency		100		MHz

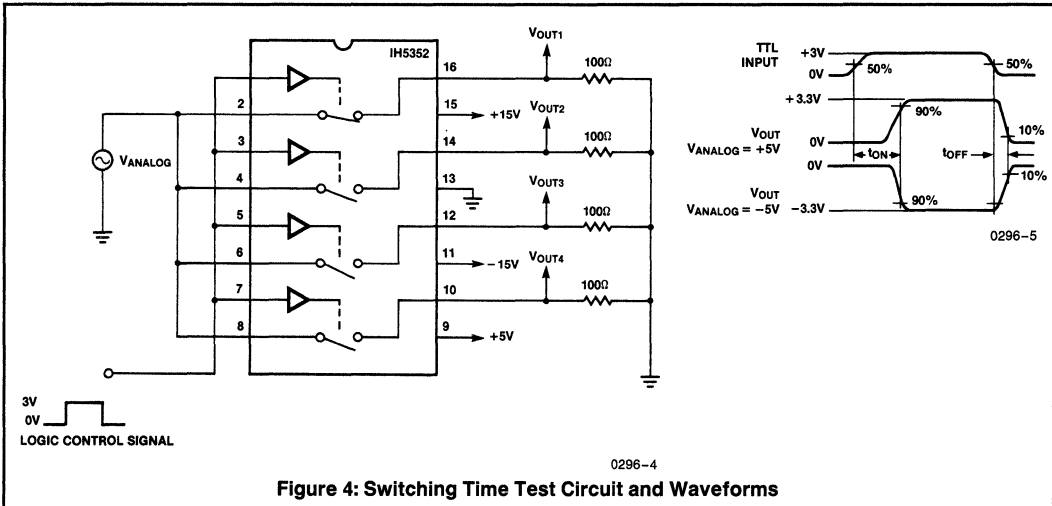
- Notes: 1. Typical values are not tested in production. They are given as a design aid only.
 2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
 3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
 4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.
 5. All AC parameters are sample tested only.



DETAILED DESCRIPTION

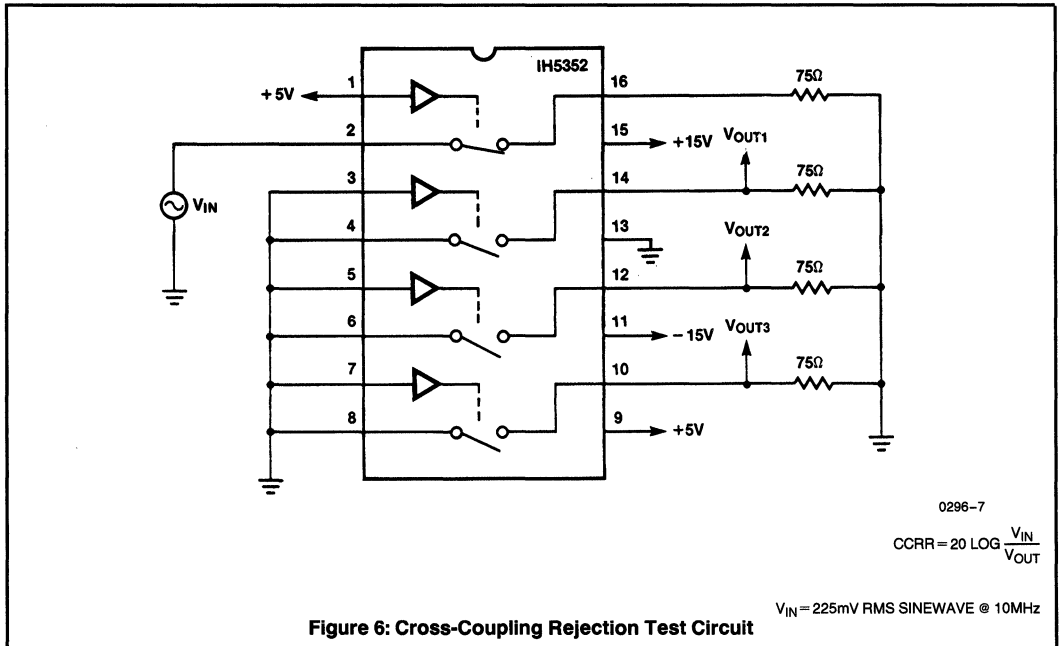
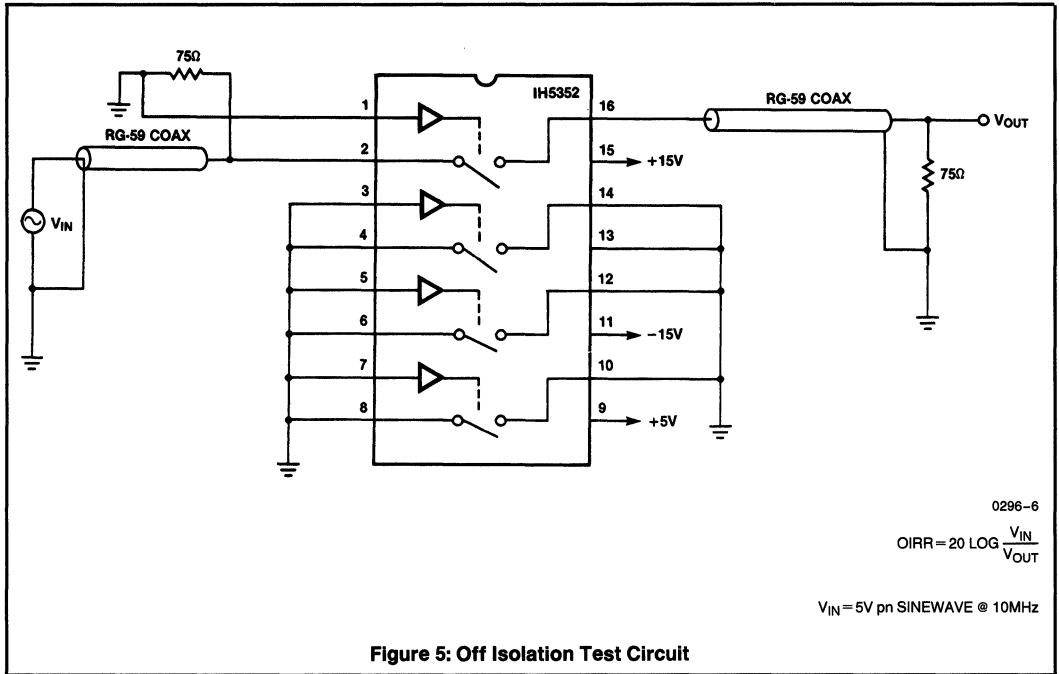
Figure 3 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.



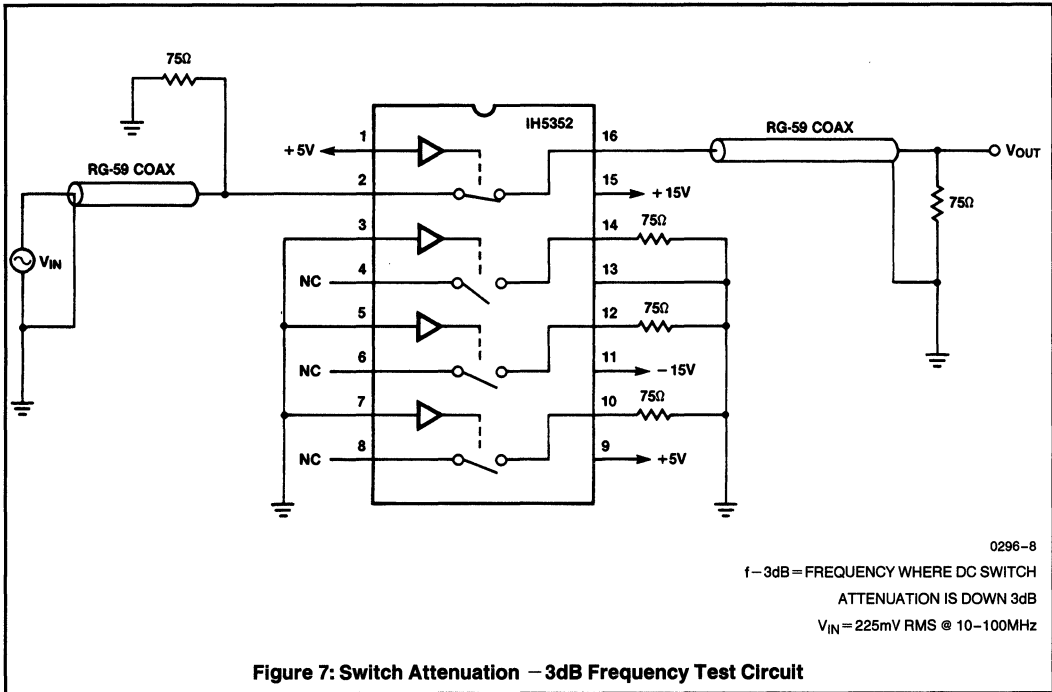
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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

MM450/451/452/455 MM550/551/552/555 High Voltage Analog Switch

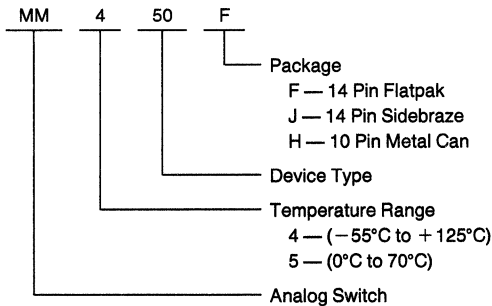


GENERAL DESCRIPTION

The MM450, and MM550 series each contain p channel MOS enhancement mode transistors. These devices are useful in airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors ($V_{TH}=2$ volts) permits operations with large analog input swings (± 10 volts) at low gate voltages (-20 volts).

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

ORDERING INFORMATION



FEATURES

- Large Analog Input — $\pm 10\text{V}$
- Low Supply Voltage — $V_{BULK} = +10\text{V}$
 $V_{GG} = -20\text{V}$
- Typical ON Resistance — $V_{IN} = -10\text{V}, 150\Omega$
 $V_{IN} = +10\text{V}, 75\Omega$
- Low Leakage Current — 200pA Typical @ 25°C
- Input Gate Protection

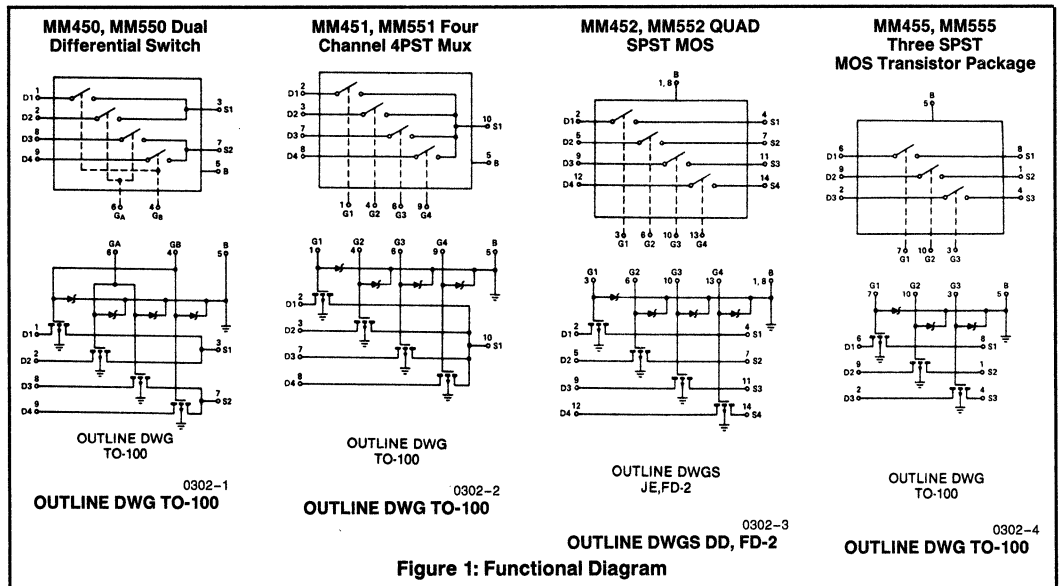


Figure 1: Functional Diagram

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NOTE: All typical values have been characterized but are not tested.

MM450/451/452/455 MM550/551/552/555



MM450/451/452/455 MM550/551/552/555

ABSOLUTE MAXIMUM RATINGS (Note 1)

Gate Voltage (V_{GG}) + 14.5V to -30V
Bulk Voltage (V_{BULK}) + 14V
Analog Input (V_{IN}) + 14V to -20V
Power Dissipation 200mW

Operating Temperature	MM450, MM451, MM452, MM455	... -55°C to +125°C
	MM550, MM551, MM552, MM555 0°C to 70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10mW/°C for FD package and 6.5 mW/°C for TW package.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel unless noted)

Symbol	Characteristic	Type	Test Conditions	Limits				
				25°C	70°C	125°C	Min Max	Units
V_{IN}	Analog Input Voltage	All		± 10			Max	V
$V_{GS(TH)}$	Threshold Voltage	All	$V_{DG} = 0$ $I_D = -10\mu A$	-3.0			Min	V
				-1.0			Max	
$R_{DS(ON)}$	Drain-Source On Resistance	All	$V_{IN} = -10V$	$I_D = 10mA$ $V_B = 10V$	600	700	Max	Ω
			$V_{IN} = +10V$					
I_{GBS}	Gate Leakage Current	All	$V_{GS} = -25V, V_{BS} = V_{DS} = 0$	± 5		100	Max	nA
$I_{D(OFF)}$	Drain Leakage Current	MM450, MM451 MM452, MM455	$V_{DB} = -25V$ $V_{GB} = V_{SB} = 0$	± 0.5		200	Max	nA
		MM550, MM551 MM552, MM555						
$I_{S(OFF)}$	Source Leakage Current	MM450, MM451 MM452, MM455	$V_{SB} = -25V$ $V_{DB} = V_{GB} = 0$	± 0.5		400	Max	nA
		MM550, MM551 MM552, MM555						
C_{DB}	Drain-Body Capacitance	All	$V_{DB} = V_{GB} = V_{SB} = 0$ $f = 1MHz$ (Note 1)	10			Typ	pF
C_{SB}	Source-Body Capacitance	MM450, MM550		14			Typ	pF
		MM451, MM551		24			Typ	pF
		MM452, MM552		11			Typ	pF
		MM455, MM555		11			Typ	pF
C_{GB}	Gate-Body Capacitance	MM450, MM550		13			Typ	pF
		MM451, MM551		8			Typ	pF
		MM452, MM552		9			Typ	pF
		MM455, MM555		9			Typ	pF
C_{GS}	Gate-Source Capacitance	All		5			Typ	pF

NOTE 1: Typical characteristics not tested in production

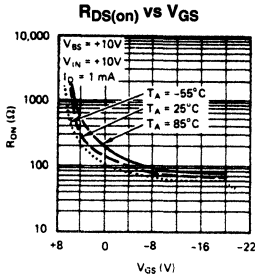
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NOTE: All typical values have been characterized but are not tested.

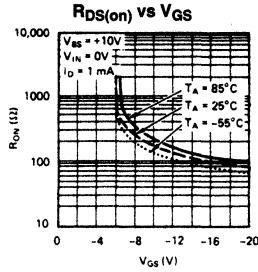
MM450/451/452/455 MM550/551/552/555



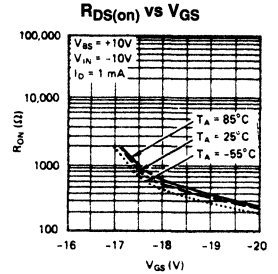
TYPICAL PERFORMANCE CHARACTERISTICS



0302-5

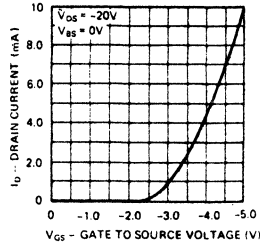


0302-6



0302-7

DRAIN CURRENT vs GATE TO SOURCE VOLTAGE



0302-8

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NOTE: All typical values have been characterized but are not tested.

Section 9 — Multiplexers

IH5108	9-1
IH5116	9-10
IH5208	9-14
IH5216	9-23
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IH5108

8-Channel Fault Protected CMOS Analog Multiplexer



IH5108

GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI508A and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to $\pm 25V$, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

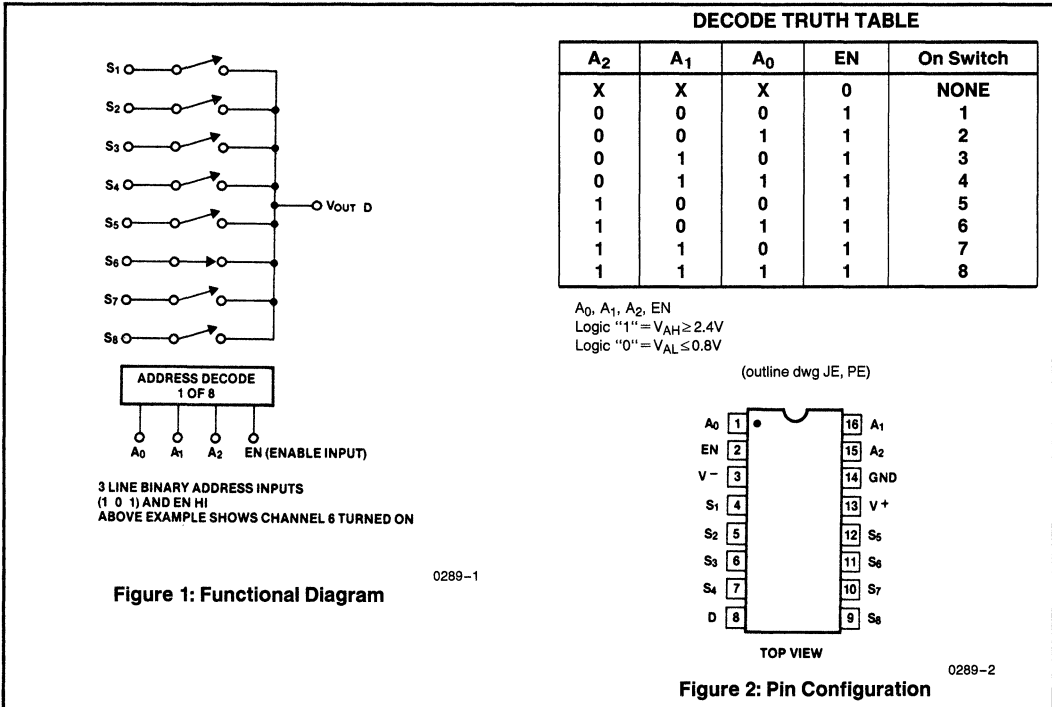
A binary 3-bit address code together with the ENable input allows selection of any one channel, or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5108MJE	-55°C to +125°C	16 pin CERDIP
IH5108IJE	-20°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

FEATURES

- All Channels OFF When Power OFF, for Analog Signals up to $\pm 25V$
- Power Supply Quiescent Current Less Than 1mA
- $\pm 13V$ Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- Pin Compatible With HI-508A
- Any Channel Turns OFF if Input Exceeds Supply Rails by Up to $\pm 25V$
- TTL and CMOS Compatible Binary Address and ENable Inputs



9

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V_{IN}(A, EN)$	V^- to $(V^+ - 0.05)$
$V_{IN}(A, EN)$ to Ground	-15V to 15V
V_S or V_D to V^+	+25V, -40V
V_S or V_D to V^-	-25V, +40V
V^+ to Ground	20V
V^- to Ground	-20V
Current (Any Terminal)	20mA
Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C

Lead Temperature (Soldering, 10sec) 300°C
 Power Dissipation* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	-20°C/ 0°C	25°C	85°C/ 70°C		
SWITCH												
$r_{DS(on)}$	S to D	8	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		8	$V_D = -10V$ $I_S = -100\mu A$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta r_{DS(on)}$			$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	8	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	0.02		± 0.5	50		± 1.0	50	mA
		8	$V_S = -10V$, $V_D = 10V$		0.02		± 0.5	50		± 1.0	50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0.8V$	0.02		± 1.0	100		± 2.0	100	mA
		1	$V_D = -10V$, $V_S = 10V$		0.05		± 1.0	100		± 2.0	100	
$I_{D(on)}$	D	8	$V_{S(All)} = V_D = 10V$	Sequence each switch on	0.1		± 2.0	100		± 5	100	mA
		8	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$ $V_{EN} = 2.4V$	0.1		± 2.0	100		± 5	100	
FAULT												
I_S with Power OFF	S	8	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$		1.0		2.0			5.0		μA
$I_{S(off)}$ with Overvoltage	S	8	$V_{IN} = \pm 25V$, $V_O = \pm 10V$		1.0		5.0			10		μA

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NOTE: All typical values have been characterized but are not tested.

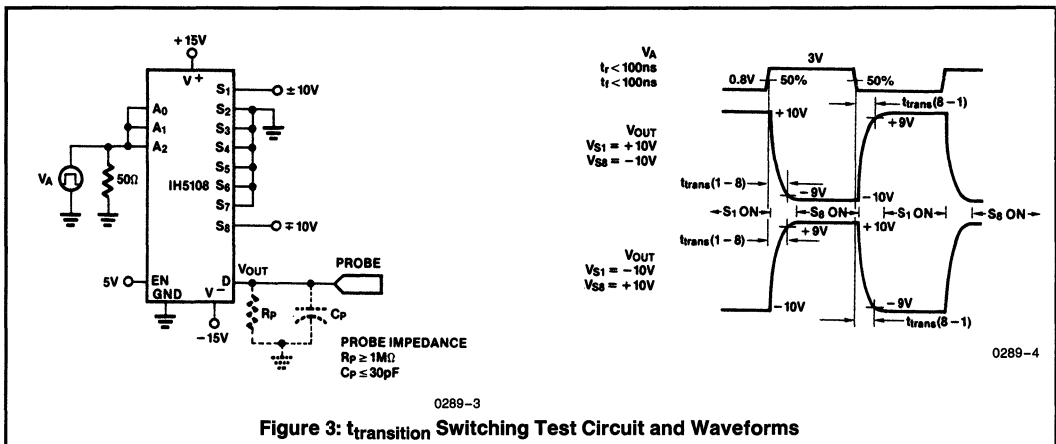
ELECTRICAL CHARACTERISTICS

(V⁺ = 15V, V⁻ = -15V, V_{EN} = 2.4V, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units
					M Suffix			C Suffix			
					-55°C	25°C	125°C	-20°C/0°C	25°C	85°C/70°C	
INPUT											
I _{EN(on)} I _{A(on)} or I _{EN(off)} I _{A(off)}	A ₀ , A ₁ , A ₂ or EN	4	V _A = 2.4V or 0V	0.01		± 1.0	-30		-10	-30	μA
			V _A = 15V or 0V	0.01		± 1.0	30		10	30	
DYNAMIC											
t _{transition}	D		See Figure 3	0.3		1					μs
t _{open}	D		See Figure 4	0.2							
t _{on(EN)}	D		See Figure 5	0.6		1.5					
t _{off(EN)}	D			0.4		1					
t _{on} ⁺ t _{off} Break-Before-Make Delay Settling Time	D	8	V _{EN} = +5V, A ₀ , A ₁ , A ₂ Strobed V _{IN} = ±10V, Figure 6	10							
"OFF" Isolation	D		V _{EN} = 0, R _L = 200Ω, C _L = 3pF, V _S = 3 VRMS, f = 500kHz	60							dB
C _{S(off)}	S		V _S = 0	V _{EN} = 0V, f = 140kHz to 1 MHz	5						pF
C _{D(off)}	D		V _D = 0		25						
C _{DS(off)}	D to S		V _S = 0, V _D = 0		1						
SUPPLY											
Supply Current	I ⁺	1	V _{EN} = 5V All V _{ADD} = 0V/5V	0.5	0.7	0.6	0.5		1.0		mA
	I ⁻	1		0.02	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.

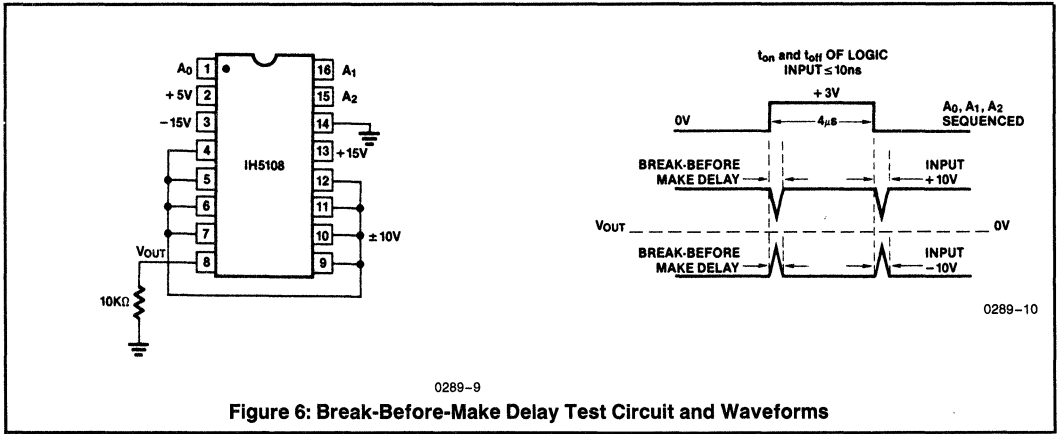
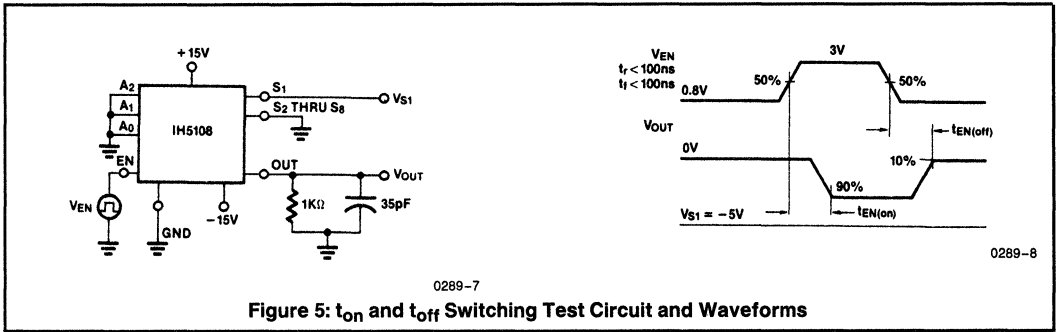
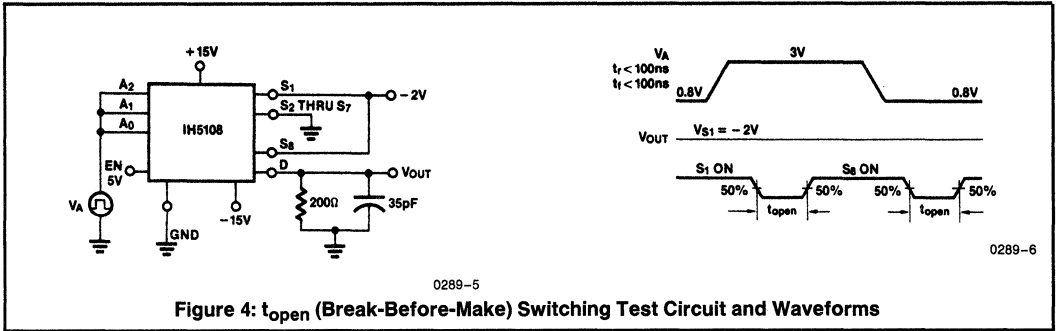
SWITCHING TIME TEST CIRCUITS



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NOTE: All typical values have been characterized but are not tested.

SWITCHING TIME TEST CIRCUITS (Continued)



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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5108, like all Intersil's multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with a dielectrically isolated process to eliminate these problems.

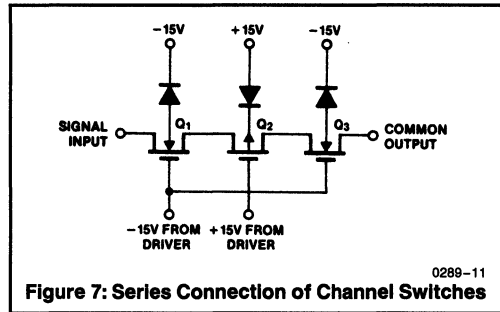
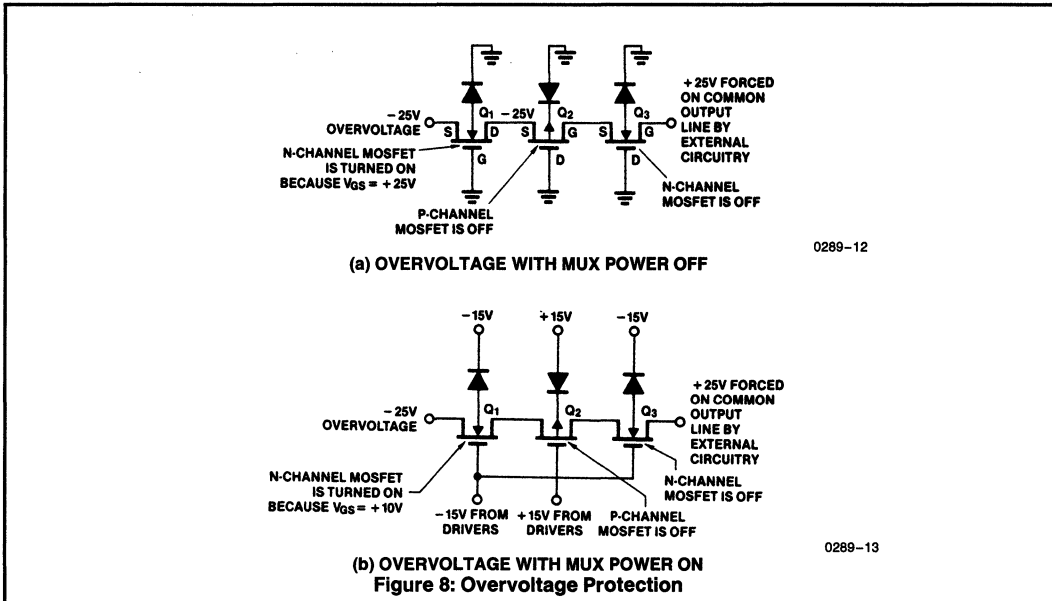


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION (Continued)

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

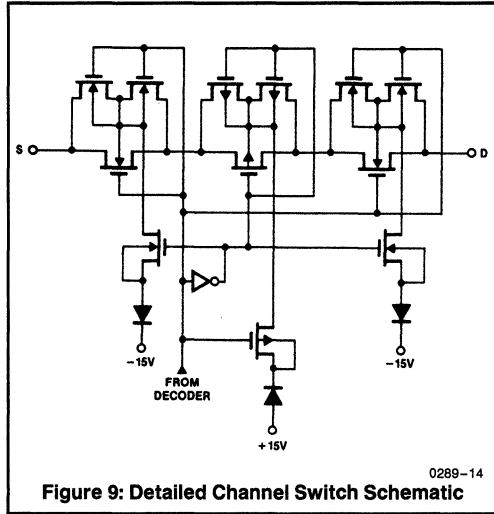


Figure 9: Detailed Channel Switch Schematic

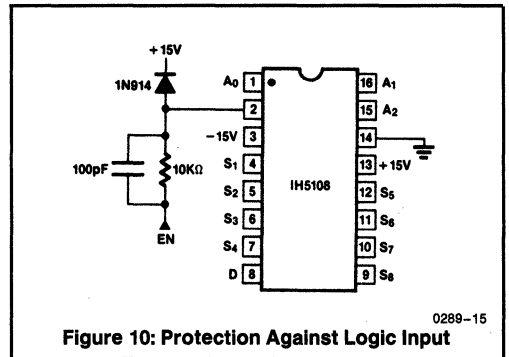


Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the $\pm 10V$ range, with a typical $r_{DS(on)}$ of 600Ω ; it can successfully handle signals up to $\pm 13V$, however, $r_{DS(on)}$ will increase to about $1.8k\Omega$. Beyond $\pm 13V$ the device approaches an open circuit, and thus $\pm 12V$ is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

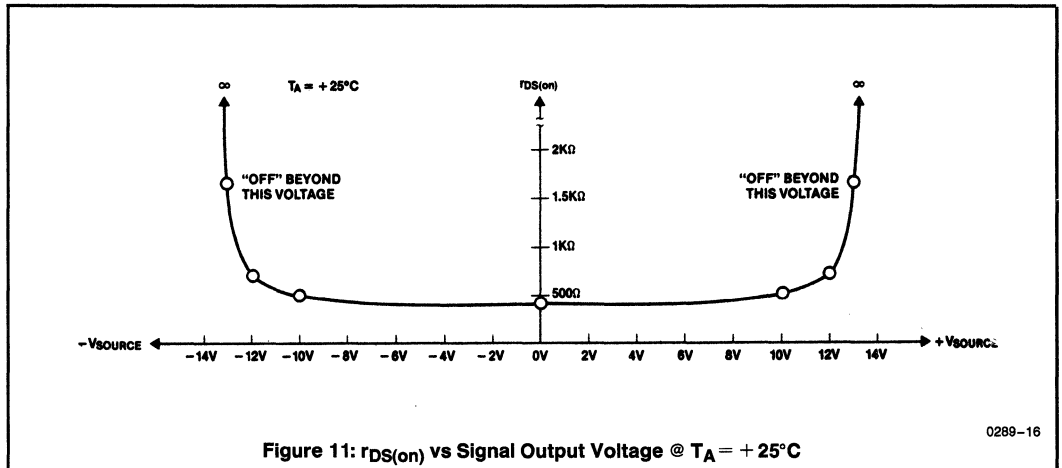


Figure 11: $r_{DS(on)}$ vs Signal Output Voltage @ $T_A = +25^\circ C$

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NOTE: All typical values have been characterized but are not tested.

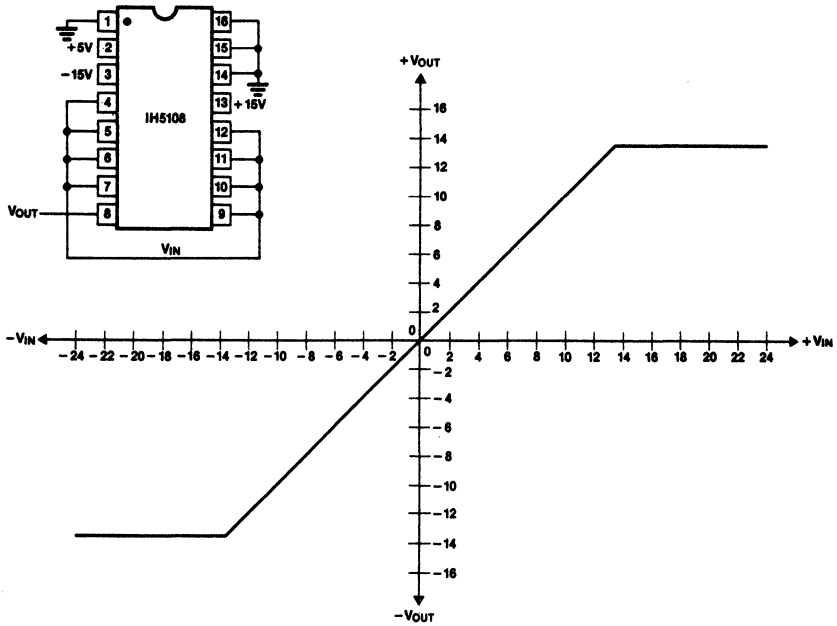


Figure 12: MUX Output Voltage vs Input Voltage (Channel 1 Shown; All Channels Similar)

0289-17

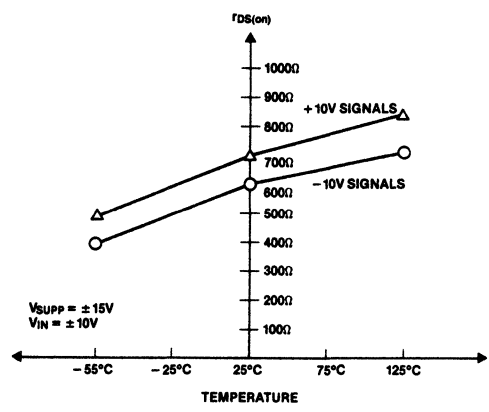


Figure 13: Typical $r_{DS(on)}$ Variation With Temperature

0289-18

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NOTE: All typical values have been characterized but are not tested.

IH5108



USING THE IH5108 WITH SUPPLIES OTHER THAN $\pm 15V$

The IH5108 will operate successfully with supply voltages from $\pm 5V$ to $\pm 15V$, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 14. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels remain TTL compatible.

APPLICATION NOTES

Further information may be found in:

- A003 "Understanding and Applying the Analog Switch"
- A006 "A New CMOS Analog Gate Technology"
- A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

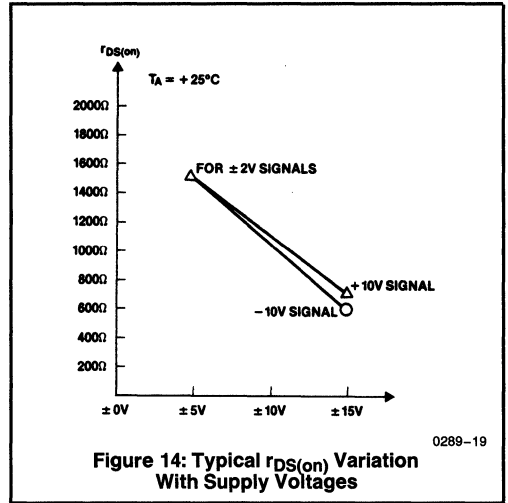


Figure 14: Typical $r_{DS(on)}$ Variation With Supply Voltages

IH5108 APPLICATIONS INFORMATION

0289-20

DECODE TRUTH TABLE

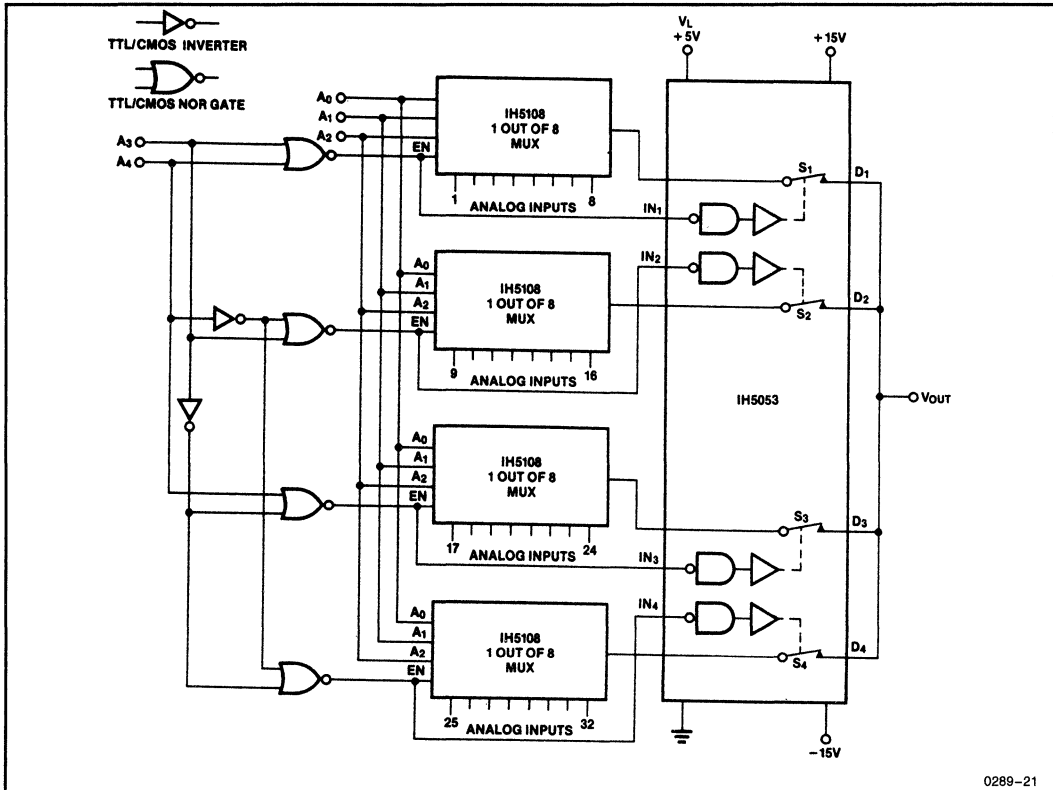
A ₃	A ₂	A ₁	A ₀	On Switch
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 15: 1 of 16 Channel Multiplexer Using Two IH5108s. Overvoltage Protection Is Maintained Between All Channels, As Is Break-Before-Make Switching.

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NOTE: All typical values have been characterized but are not tested.

IH5108 APPLICATIONS INFORMATION (Continued)



0289-21

DECODE TRUTH TABLE

A ₄	A ₃	A ₂	A ₁	A ₀	On Switch
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A ₄	A ₃	A ₂	A ₁	A ₀	On Switch
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 16: 1 Of 32 Multiplexer Using 4 IH5108s and An IH5053 As A Submultiplexer. Note That The IH5053 is Protected Against Overvoltages By The IH5108s. Submultiplexing Reduces Output Leakage and Capacitance.

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NOTE: All typical values have been characterized but are not tested.

IH5116

16-Channel Fault Protected CMOS Analog Multiplexer



GENERAL DESCRIPTION

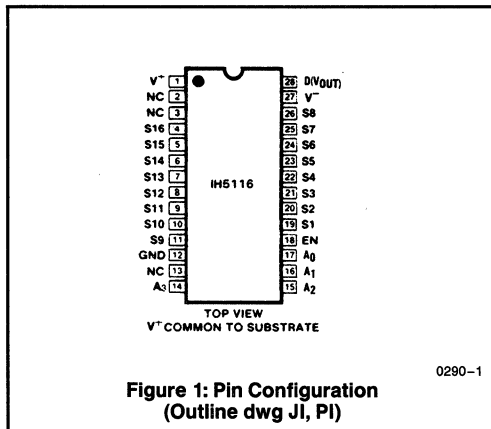
The IH5116 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI506A and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to $\pm 25V$, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5116MJ1	$-55^{\circ}C$ to $+125^{\circ}C$	28 pin CERDIP
IH5116CJ1	$0^{\circ}C$ to $+70^{\circ}C$	28 pin CERDIP
IH5116CPI	$0^{\circ}C$ to $+70^{\circ}C$	28 pin Plastic DIP

Ceramic package available as special order only (IH5116MDI/CD)



FEATURES

- All Channels OFF When Power OFF, for Analog Signals Up to $\pm 25V$
- Power Supply Quiescent Current Less Than 1mA
- $\pm 13V$ Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI506A
- Any Channel Turns OFF If Input Exceeds Supply Rails By Up to $\pm 25V$
- TTL and CMOS Compatible Binary Address and ENable Inputs

DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 2.4V$

Logic "0" = $V_{AL} \leq 0.8V$

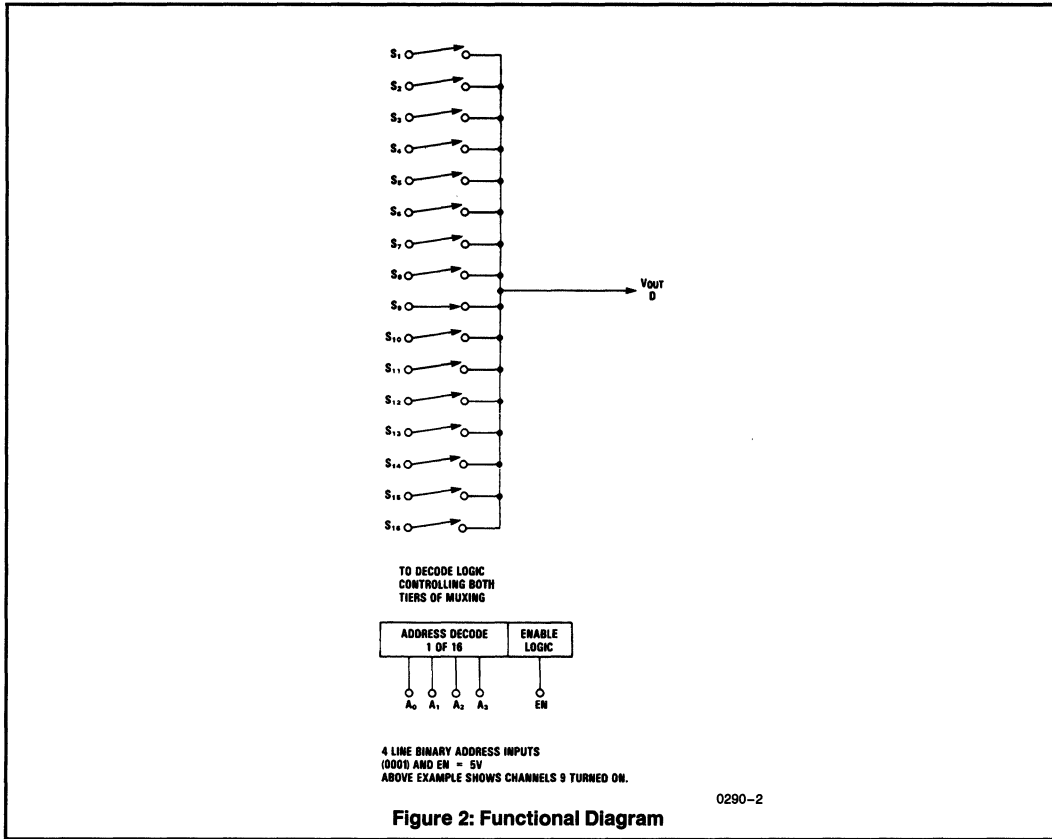


Figure 2: Functional Diagram

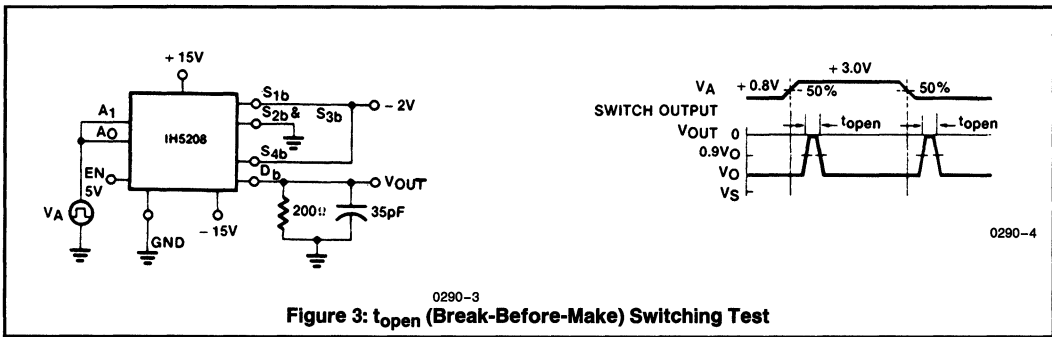


Figure 3: t_{open} (Break-Before-Make) Switching Test

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground	V^- to V^+
V_S or V_D to V Ground	+25V to -40V
V_S or V_D to V^-	-25V to +40V
V^+ to Ground	20V
V^- to Ground	-20V
V^- to V^+	+25V
Current (Any Terminal)	20mA
Operating Temperature	-55 to +125°C
Storage Temperature	-65 to +150°C

Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation*	1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	0°C	25°C	70°C		
SWITCH												
$R_{DS(on)}$	S to D	16	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		16	$V_D = -10V$, $I_S = -100\mu A$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	16	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	0.02		± 0.5	50		± 1.0	50	nA
		16	$V_S = -10V$, $V_D = 10V$		0.02		± 0.5	50		± 1.0	50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0.8V$	0.05		± 1.0	100		± 2.0	100	nA
		1	$V_D = -10V, V_S = 10V$		0.05		± 1.0	100		± 2.0	100	
$I_{D(on)}$	D	16	$V_{S(All)} = V_D = 10V$	Sequence each switch on	0.1		± 2.0	100		± 4.0	100	nA
		16	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	0.1		± 2.0	100		± 4.0	100	
FAULT												
I_S with Power OFF	S	16	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$ or $5V$		1.0		2.0			5.0		μA
$I_{S(off)}$ with Overvoltage	S	16	$V_{IN} = \pm 25V$, $V_O = \pm 10V$		1.0		2.0			5.0		μA
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2, A_3 or EN	4	$V_A = 2.4V$ or $0V$		0.01		-10	-30		-10	-30	μA
		4	$V_A = 15V$		0.01		10	30		10	30	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units
					M Suffix			C Suffix			
					-55°C	25°C	125°C	0°C	25°C	70°C	
DYNAMIC											
$t_{transition}$	D			0.3		1					μs
t_{open}	D			0.2							
$t_{on(EN)}$	D			0.6		1.5					
$t_{off(EN)}$	D			0.4		1					
$t_{on-t_{off}}$ Break-Before-Make Delay Settling Time	D	16	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$.	25							ns
"OFF" Isolation	D		$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3V_{RMS}$, $f = 500kHz$	60							dB
$C_{s(off)}$	S		$V_S = 0$	$V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5						pF
$C_{D(off)}$	D		$V_D = 0$		25						
$C_{DS(off)}$	D to S		$V_S = 0$, $V_D = 0$		1						
SUPPLY											
Supply Current	+	I+	1	All $V_A = 0V/5V$ $V_{EN} = 5V$	0.5		0.6			1.0	mA
	-	I-	1		0.02		0.6			1.0	

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NOTE: All typical values have been characterized but are not tested.

IH5208

4-Channel Differential Fault Protected CMOS Analog Multiplexer



GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI509A and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to $\pm 25V$, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

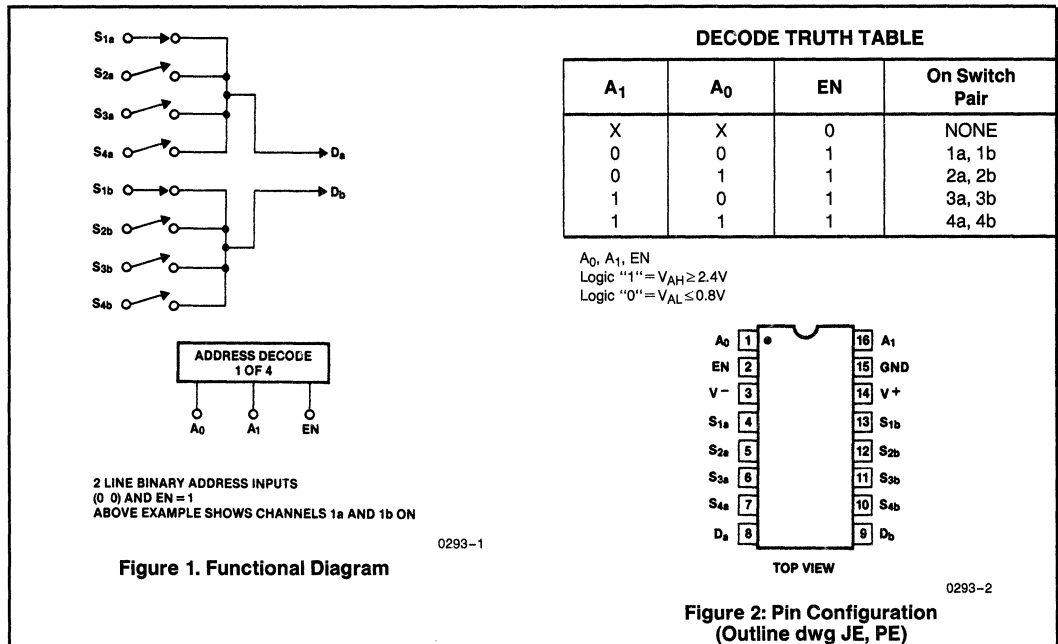
A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5208MJE	-55°C to +125°C	16 pin CERDIP
IH5208IJE	-20°C to +85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP

FEATURES

- All Channels OFF When Power OFF, for Analog Signals Up to $\pm 25V$
- Power Supply Quiescent Current Less Than $1\mu A$
- $\pm 13V$ Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI - 509A
- Any Channel Turns OFF If Input Exceeds Supply Rails by Up to $\pm 25V$
- TTL and CMOS Compatible Binary Address and ENable Inputs



ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground	-15V, +15V
V_S or V_D to V^+	+25V, -40V
V_S or V_D to V^-	-25V, +40V
V^+ to Ground	20V
V^- to Ground	-20V
Current (Any Terminal)	20mA
Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C

Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation (Package)*	1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, V_{EN} = 2.4V$, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	-20°C/0°C	25°C	85°C/70°C		
SWITCH												
$t_{DS(on)}$	S to D	8	$V_D = 10V, I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		8	$V_D = -10V, I_S = -100\mu A$	$V_{AL} = 0.8V, V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta t_{DS(on)}$			$\Delta t_{DS(on)} = \frac{t_{DS(on)max} - t_{DS(on)min}}{t_{DS(on)avg}}$		5							%
$I_{S(off)}$	S	8	$V_S = 10V, V_D = -10V$	$V_{EN} = 0.8V$	0.02		± 0.5	50		± 1.0	50	nA
		8	$V_S = -10V, V_D = 10V$		0.02		± 0.5	50		± 1.0	50	
$I_{D(off)}$	D	1	$V_D = 10V, V_S = -10V$		0.02		± 1.0	100		± 2.0	100	
		1	$V_D = -10V, V_S = 10V$		0.05		± 1.0	100		± 2.0	100	
$I_{D(on)}$	D	8	$V_{S(AII)} = V_D = 10V$	Sequence each switch on	0.1		± 2.0	100		± 5.0	100	
		8	$V_{S(AII)} = V_D = -10V$	$V_{AL} = 0.8V, V_{AH} = 2.4V$	0.1		± 2.0	100		± 5.0	100	
FAULT												
I_S with Power OFF	S	8	$V_{SUPP} = 0V, V_{IN} = \pm 25V, V_{EN} = V_O = 0V, A_0, A_1, A_2 = 0V$		1.0		2			5		μA
$I_{S(off)}$ with Overvoltage	S	8	$V_{IN} = \pm 25V, V_O = \pm 10V$		1.0		5		10			
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2 or EN	4	$V_A = 2.4V$ or 0V		0.01		-10	-30		-10	-30	μA
		4	$V_A = 15V$ or 0V		0.01		10	30		10	30	

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NOTE: All typical values have been characterized but are not tested.

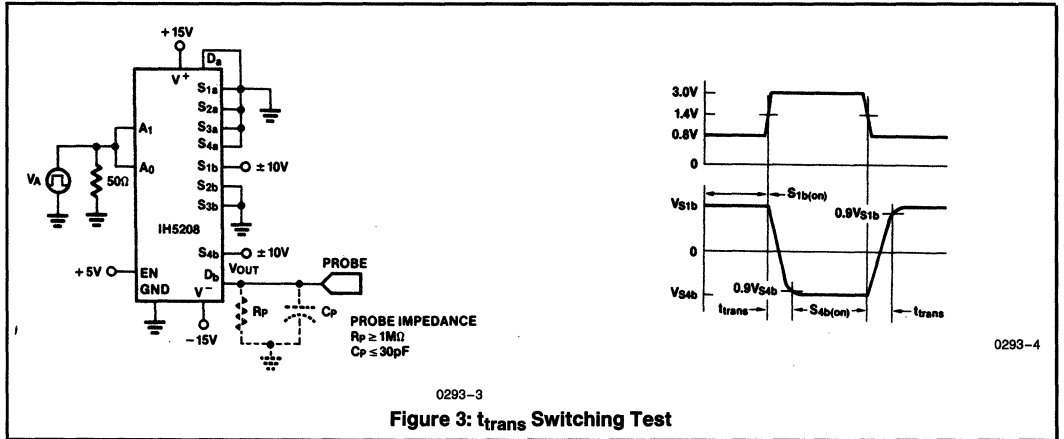
ELECTRICAL CHARACTERISTICS

V⁺ = 15V, V⁻ = -15V, V_{EN} = 2.4V, unless otherwise specified. (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units
					M Suffix			C Suffix			
					-55°C	25°C	125°C	-20°C/0°C	25°C	85°C/70°C	
DYNAMIC											
t _{transition}	D		See Figure 3	0.3							μs
t _{open}	D		See Figure 4	0.2							
t _{on(EN)}	D		See Figure 5	0.6	1.5						
t _{off(EN)}	D			0.4	1						
t _{on-t_{off} Break-Before-Make Delay Settling Time}	D	8	V _{EN} = +5V, A ₀ , A ₁ , A ₂ Strobed V _{IN} = ±10V, Figure 6	10						ns	
"OFF" Isolation	D		V _{EN} = 0, R _L = 200Ω, C _L = 3pF, V _S = 3VRMS, f = 500kHz	60						dB	
C _{S(off)}	S		V _S = 0	5 25 1						pF	
C _{D(off)}	D		V _D = 0								
C _{DS(off)}	D to S		V _S = 0, V _D = 0								
SUPPLY											
Supply Current	+	I ⁺	1	All V _A , V _{EN} = 5V All V _{ADD} = 0V/5V	0.5	0.7	0.6	0.5		1.0	mA
	-	I ⁻	1		0.02	0.7	0.6	0.5		1.0	

Note 1. Readings taken 400ms after the overvoltage occurs.

SWITCHING INFORMATION



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NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

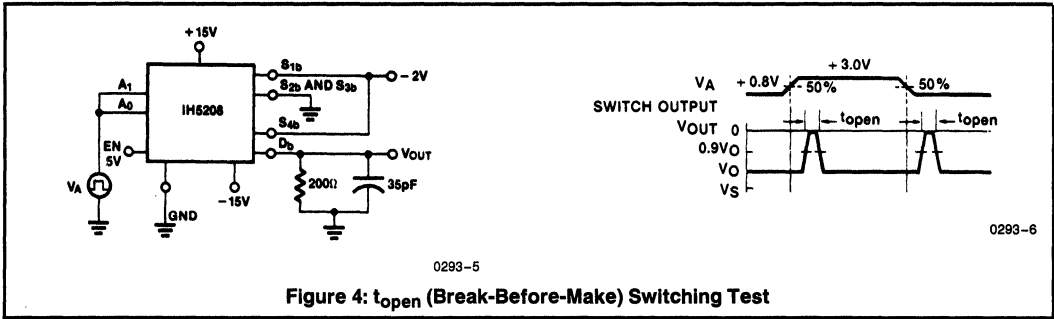


Figure 4: t_{open} (Break-Before-Make) Switching Test

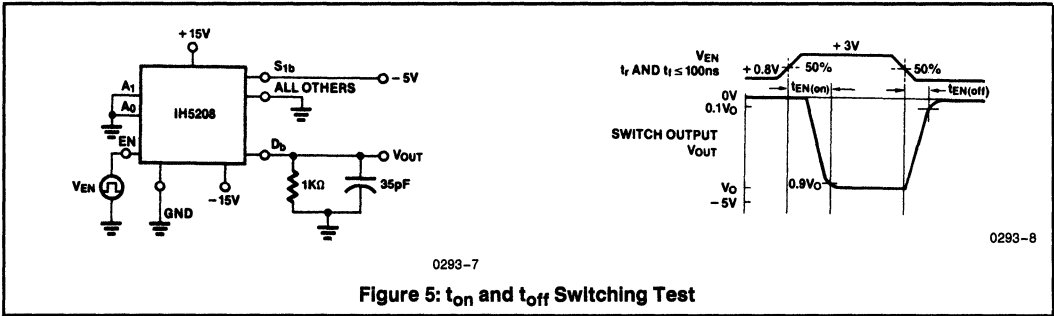


Figure 5: t_{on} and t_{off} Switching Test

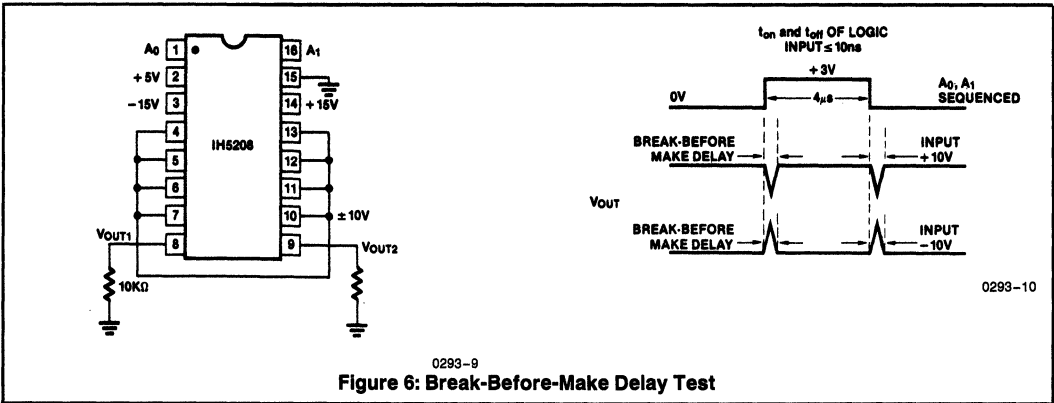


Figure 6: Break-Before-Make Delay Test

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5208, like all Intersil's multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.

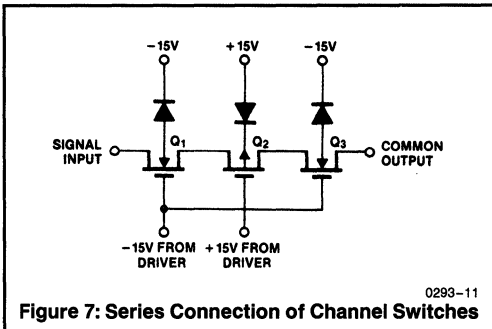
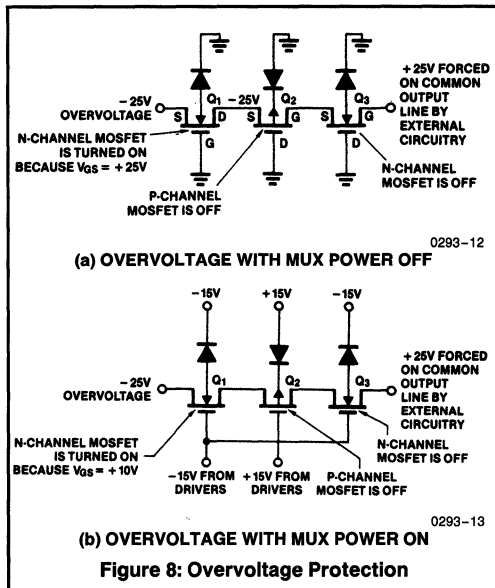


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



(a) OVERVOLTAGE WITH MUX POWER OFF

(b) OVERVOLTAGE WITH MUX POWER ON

Figure 8: Overvoltage Protection

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

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NOTE: All typical values have been characterized but are not tested.

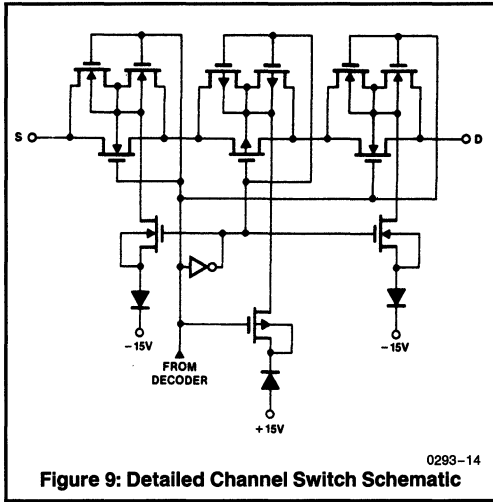


Figure 9: Detailed Channel Switch Schematic

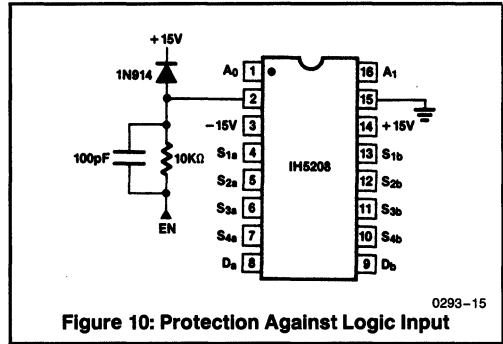


Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the $\pm 10V$ range, with a typical $r_{DS(on)}$ of 600Ω ; it can successfully handle signals up to $\pm 13V$, however, $r_{DS(on)}$ will increase to about $1.8k\Omega$. Beyond $\pm 13V$ the device approaches an open circuit, and thus $\pm 12V$ is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

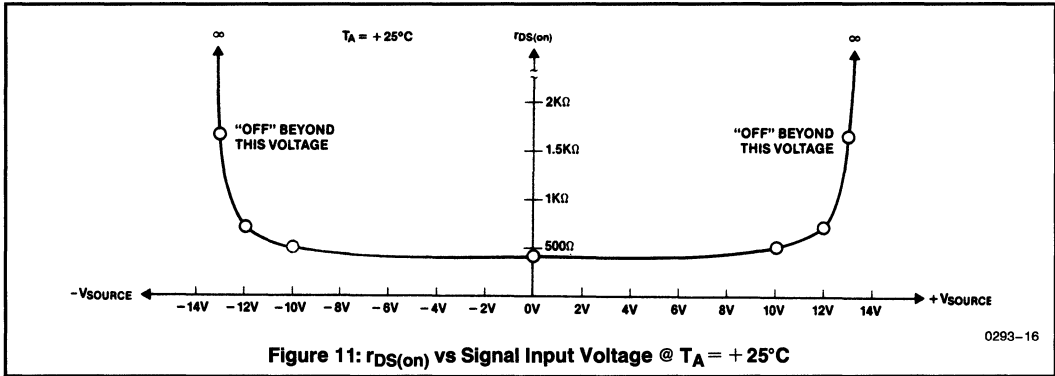


Figure 11: $r_{DS(on)}$ vs Signal Input Voltage @ $T_A = +25^\circ C$

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NOTE: All typical values have been characterized but are not tested.

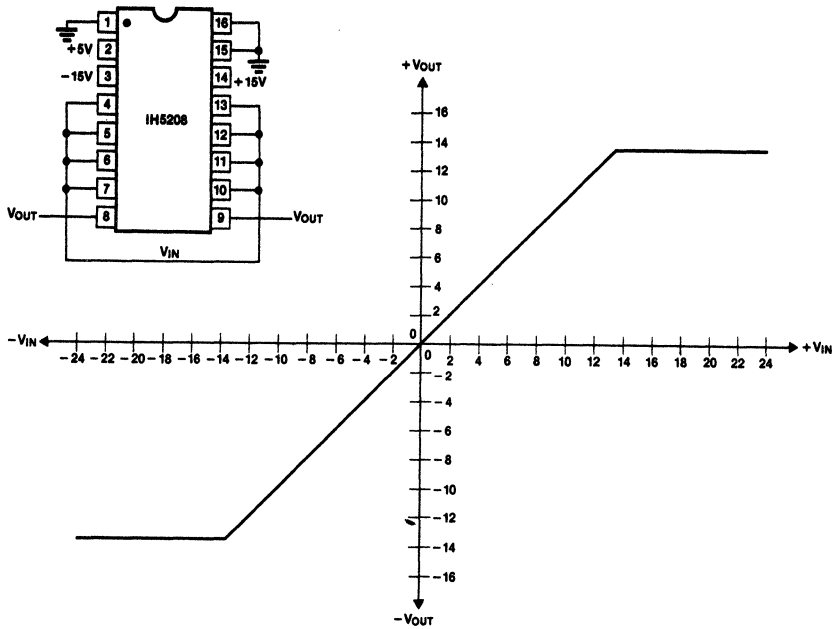


Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar

0293-17

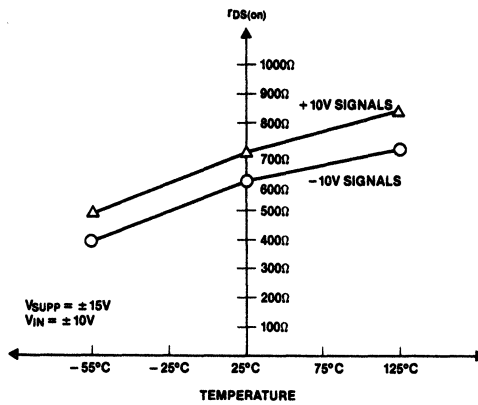


Figure 13: Typical r_{DS(on)} Variation vs Temperature

0293-18

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NOTE: All typical values have been characterized but are not tested.

USING THE IH5208 WITH SUPPLIES OTHER THAN $\pm 15V$

The IH5208 will operate successfully with supply voltages from $\pm 5V$ to $\pm 15V$, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 14. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.

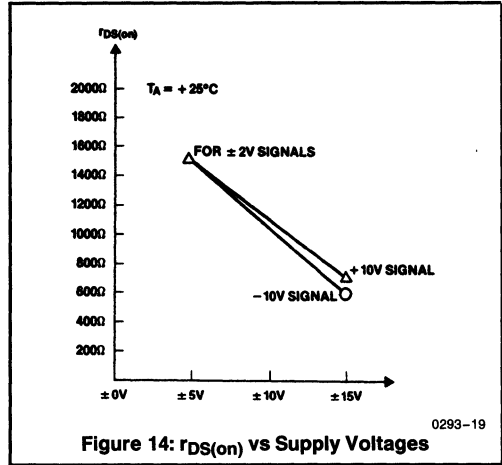
APPLICATION NOTES

Further information may be found in:

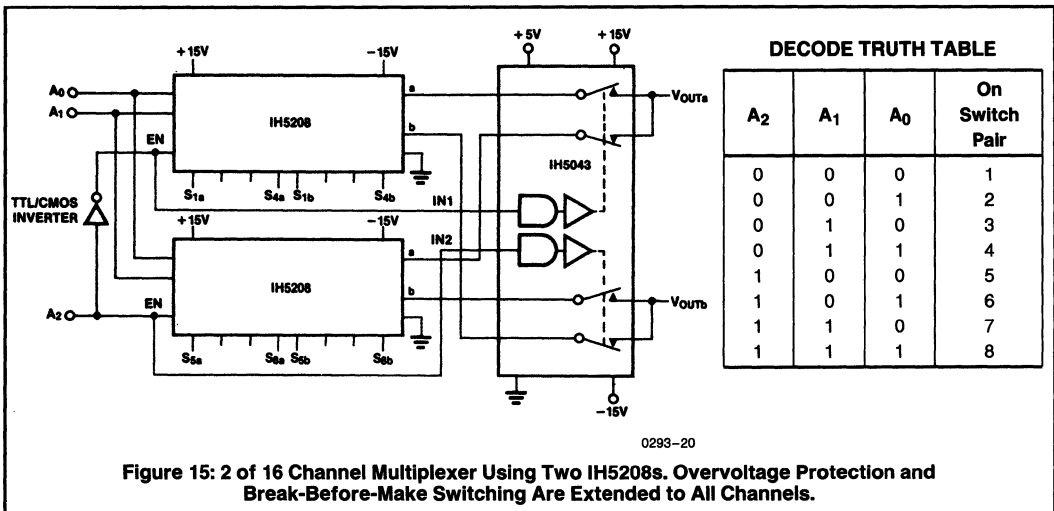
A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"



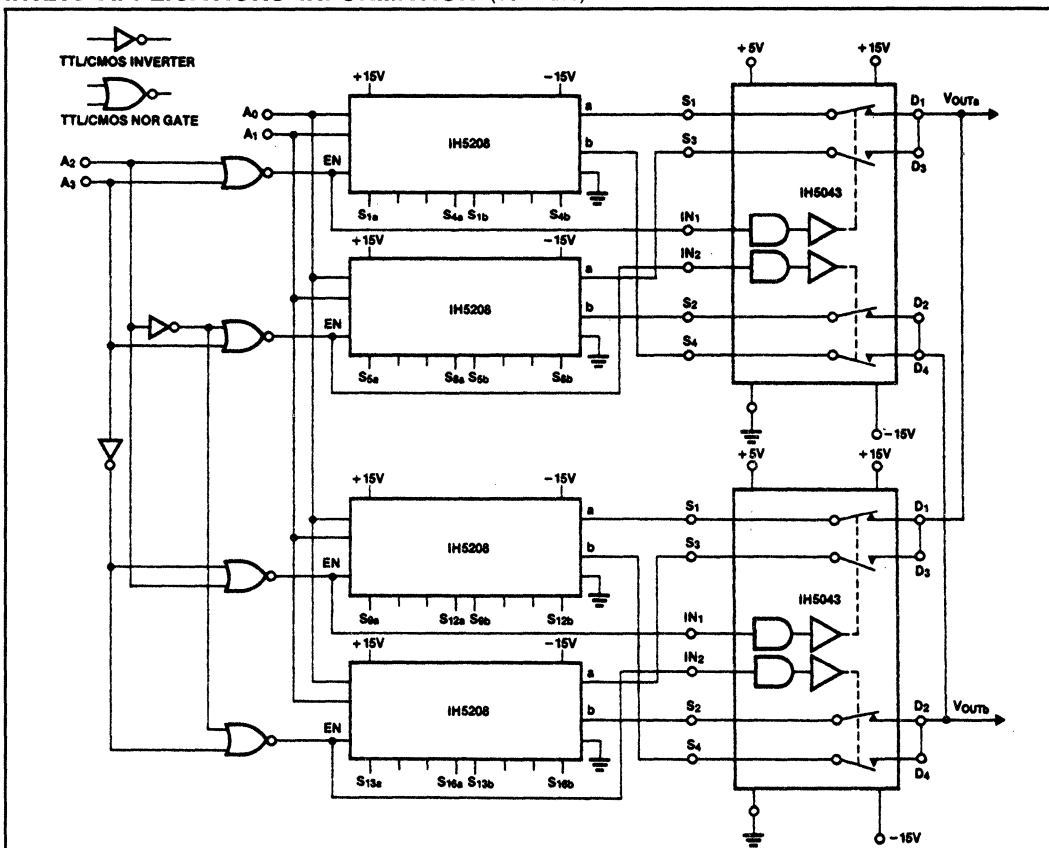
IH5208 APPLICATIONS INFORMATION



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NOTE: All typical values have been characterized but are not tested.

IH5208 APPLICATIONS INFORMATION (Continued)



DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	On Switch		On Switch	
0	0	0	0	S1a		S1b	
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a		S8b	
1	0	0	0	S9a	VOUTa	S9b	VOUTb
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

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Figure 16: Submultiplexed 2 of 32 System. The Two IH5043s Are Overvoltage Protected By The IH5208s. Submultiplexing Reduces Output Capacitance and Leakage Currents.

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NOTE: All typical values have been characterized but are not tested.

IH5216

8-Channel Differential Fault Protected CMOS Analog Multiplexer



IH5216

GENERAL DESCRIPTION

The IH5216 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI507A and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to $\pm 25V$, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5216MJL	-55°C to +125°C	28 pin CERDIP
IH5216CJL	0°C to +70°C	28 pin CERDIP
IH5216CPL	0°C to +70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH5216MDI/CDI)

FEATURES

- All Channels OFF When Power OFF, for Analog Signals Up to $\pm 25V$
- Power Supply Quiescent Current Less Than 1mA
- $\pm 13V$ Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI507A
- Any Channel Turns OFF If Input Exceeds Supply Rails By Up to $\pm 25V$
- TTL and CMOS Compatible Binary Address and ENable Inputs

DECODE TRUTH TABLE

A ₂	A ₁	A ₀	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = $V_{AH} > 2.4V$ $V_{ENH} > 2.4V$
 Logic "0" = $V_{AL} < 0.8V$

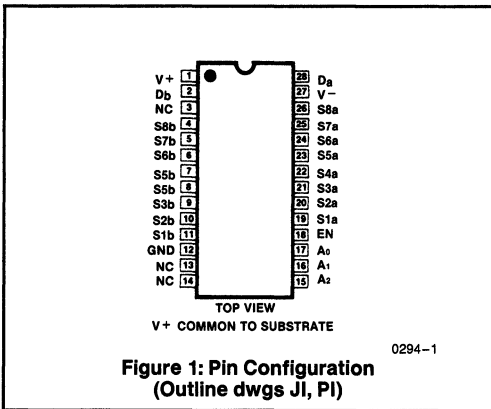


Figure 1: Pin Configuration (Outline dwgs JI, PI)

9

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NOTE: All typical values have been characterized but are not tested.

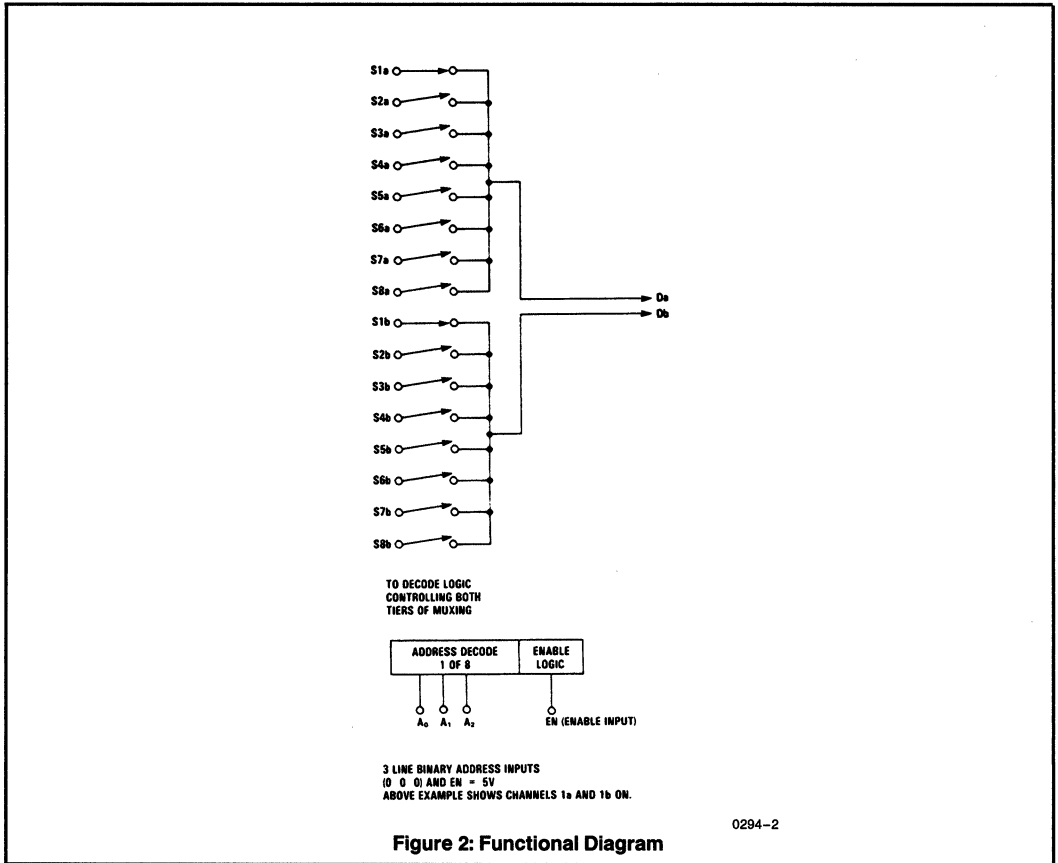


Figure 2: Functional Diagram

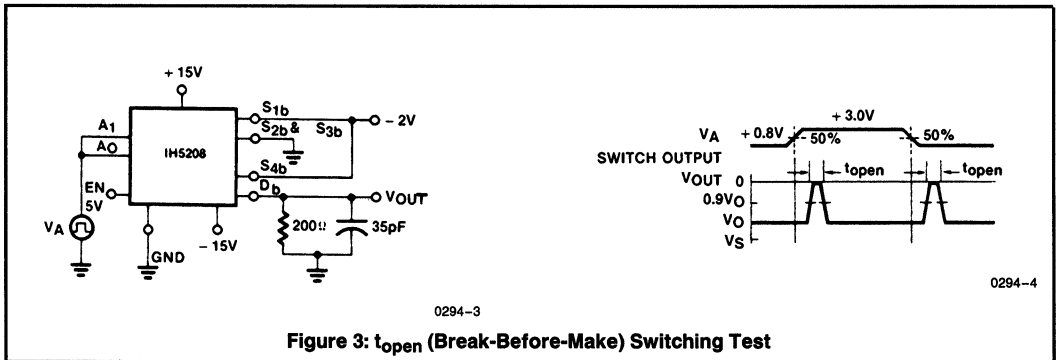


Figure 3: topen (Break-Before-Make) Switching Test

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V _{IN} (A, EN) to Ground	-15V to +15V
V _S or V _D to V ⁺	+25V to -40V
V _S or V _D to V ⁻	-25V to +40V
V ⁺ to Ground	20V
V ⁻ to Ground	-20V
Current (Any Terminal)	20mA
Operating Temperature	-55 to +125°C
Storage Temperature	-65 to +150°C

Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation*	1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V⁺ = 15V, V⁻ = -15V, V_{EN} = 2.4V, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	0°C	25°C	70°C		
SWITCH												
R _{DS(on)}	S to D	16	V _D = 10V, I _S = -100μA	Sequence each switch on	1000	1200	1200	1800	1500	1500	2000	Ω
		16	V _D = -10V I _S = -100μA	V _{AL} = 0.8V, V _{AH} = 2.4V	1000	1200	1200	1800	1500	1500	2000	
ΔR _{DS(on)}			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ V _S = ±10V		5							%
I _{S(off)}	S	16	V _S = 10V, V _D = -10V	V _{EN} = 0.8V	0.02		±0.5	50		±1.0	50	nA
		16	V _S = -10V, V _D = 10V		0.02		±0.5	50		±1.0	50	
I _{D(off)}	D	1	V _D = 10V, V _S = -10V	V _{EN} = 0.8V	0.05		±1.0	100		±2.0	100	
		1	V _D = -10V, V _S = 10V		0.05		±1.0	100		±2.0	100	
I _{D(on)}	D	16	V _{S(All)} = V _D = 10V	Sequence each switch on	0.1		±2.0	100		±4.0	100	
		16	V _{S(All)} = V _D = -10V	V _{AL} = 0.8V, V _{AH} = 2.4V	0.1		±2.0	100		±4.0	100	
FAULT												
I _S with Power OFF	S	16	V _{SUPP} = 0V, V _{IN} = ±25V, V _{EN} = V _O = 0V, A ₀ , A ₁ , A ₂ = 0V or 5V		1.0		2.0			5.0		μA
I _{S(off)} with Overvoltage	S	16	V _{IN} = ±25V, V _O = ±10V		1.0		2.0			5.0		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

(V⁺ = 15V, V⁻ = -15V, V_{EN} = 2.4V, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units
					M Suffix			C Suffix			
					-55°C	25°C	125°C	0°C	25°C	70°C	
INPUT											
I _{EN(on)} / I _{A(on)} or I _{EN(off)} / I _{A(off)}	A ₀ , A ₁ A ₂ , A ₃ or EN	4	V _A = 2.4V or 0V	0.01		-10	-30		-10	-30	μA
		4	V _A = 15V	0.01		10	30		10	30	
DYNAMIC											
t _{transition}	D			0.3		1					μs
t _{open}	D			0.2							
t _{on(EN)}	D			0.6		1.5					
t _{off(EN)}	D			0.4		1					
t _{on} -t _{off} Break-Before-Make Delay Settling Time	D	16	V _{EN} = +5V, A ₀ , A ₁ , A ₂ Strobed V _{IN} = ±10V.	25							ns
"OFF" Isolation	D		V _{EN} = 0, R _L = 200Ω, C _L = 3pF, V _S = 3V _{RMS} , f = 500kHz	60							dB
C _{S(off)}	S		V _S = 0	5							pF
C _{D(off)}	D		V _D = 0	25							
C _{DS(off)}	D to S		V _S = 0, V _D = 0	1							
SUPPLY											
Supply Current	+	I ⁺	1	All V _A = 0V/5V V _{EN} = 5V	0.5		0.6			1.0	mA
	-	I ⁻	1		0.02		0.6			1.0	

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NOTE: All typical values have been characterized but are not tested.

IH6108

8-Channel CMOS

Analog Multiplexer



IH6108

GENERAL DESCRIPTION

The IH6108 is a CMOS one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided for use as a system enable. When the ENable input is high (5V), a channel is selected by the three Address inputs, and when low (0V) all channels are off. The 3 Address inputs are TTL and CMOS logic compatible, with a "1" corresponding to any voltage greater than 2.4V.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6108MJE	-55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

Ceramic package available as special order only (IH6108MDE/CDE)

FEATURES

- Ultra Low Leakage — $I_{D(off)} \leq 100\text{pA}$ Typical
- $r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range
- Power Supply Quiescent Current Less Than $100\mu\text{A}$
- $\pm 14\text{V}$ Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- Binary Address Control (3 Address Inputs Control 8 Channels)
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With DG508, HI-508 & AD7508
- Internal Diode In Series With V^+ for Fault Protection

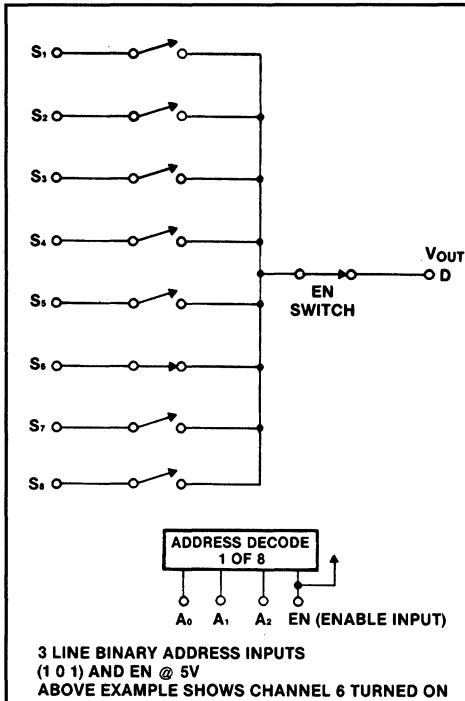


Figure 1: Functional Diagram

0297-1

DECODE TRUTH TABLE

A ₂	A ₁	A ₀	EN	On Switch
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A₀, A₁, A₂
Logic "1" = $V_{AH} \geq 2.4\text{V}$ $V_{ENH} \geq 4.5\text{V}$
Logic "0" = $V_{AL} \leq 0.8\text{V}$

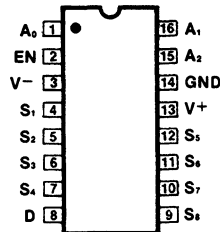


Figure 2: Pin Configuration

0297-2

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V _{IN} (A, EN) to Ground	-15V to 15V
V _S or V _D to V ⁺	0, -36V
V _S or V _D to V ⁻	0, 36V
V ⁺ to Ground	16V
V ⁻ to Ground	-16V
Current (Any Terminal)	30mA

Current (Analog Source or Drain)	20mA
Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Lead Temp (Soldering, 10sec)	300°C
Power Dissipation (Package)*	1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V⁺ = 15V, V⁻ = -15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	0°C	25°C	70°C		
SWITCH												
r _{DS(ON)}	S to D	8	150	V _D = -10V, I _S = -1.0mA	Sequence each switch on	300	300	400	350	350	450	Ω
		8	150	V _D = -10V, I _S = -1.0mA	V _{AL} = 0.8V, V _{AH} = 2.4V	300	300	400	350	350	450	
Δr _{DS(ON)}			20	Δr _{DS(on)} = $\frac{\Delta r_{DS(on)min}}{r_{DS(on)avg}}$ V _S = ±10V								%
I _{S(OFF)}	S	8	0.002	V _S = 10V, V _D = -10V	V _{EN} = 0.8V	±.5	50		±1	50	nA	
		8	0.002	V _S = -10V, V _D = 10V		±.5	50		±1	50		
I _{D(OFF)}	D	1	0.03	V _D = 10V, V _S = -10V	Sequence each switch on	±2	100		±5	100	nA	
		1	0.03	V _D = -10V, V _S = 10V		±2	100		±5	100		
I _{D(ON)}	D	8	0.1	V _{S(ALL)} = V _D = 10V	V _{AL} = 0.8V, V _{AH} = 2.4V	±2	100		±5	100	nA	
		8	0.1	V _{S(ALL)} = V _D = -10V		±2	100		±5	100		
INPUT												
I _{AN(ON)} or I _{A(on)}	A ₀ , A ₁ or A ₂	3	0.01	V _A = 2.4V or 0V		-10	-30		-10	-30	μA	
I _{AN(OFF)} I _{A(off)}	Inputs	3	0.01	V _A = 14V or 0V		10	30		10	30		
I _A	A ₀ , A ₁ , A ₂	3		V _{EN} = 5V	All V _A = 0 (Address pins)	-10	-30		-10	-30		
	EN	1		V _{EN} = 0		-10	-30		-10	-30		
DYNAMIC												
t _{transition}	D		0.3	See Fig. 1		1					μs	
t _{open}	D		0.2	See Fig. 2								
t _{on(EN)}	D		0.6	See Fig. 3		1.5						
t _{off(EN)}	D		0.4			1						
"OFF" Isolation	D		60	V _{EN} = 0, R _L = 200Ω, C _L = 3pF, V _S = 3VRMS, f = 500kHz							dB	
C _{s(off)}	S		5	V _S = 0	V _{EN} = 0V, f = 140kHz to 1MHz						pF	
C _{d(off)}	D		25	V _D = 0								
C _{DS(off)}	D to S		1	V _S = 0, V _D = 0								
SUPPLY												
Supply Current	+	V ⁺	1	40	V _{EN} = 5V		200			1000	μA	
	-	V ⁻	1	2			100			1000		
Standby Current	+	V ⁺	1	1	V _{EN} = 0	All V _A = 0 or 5V						
	-	V ⁻	1	1			100			1000		

NOTE 1: See Enable Input Strobing Levels, in Application Section.

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NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION

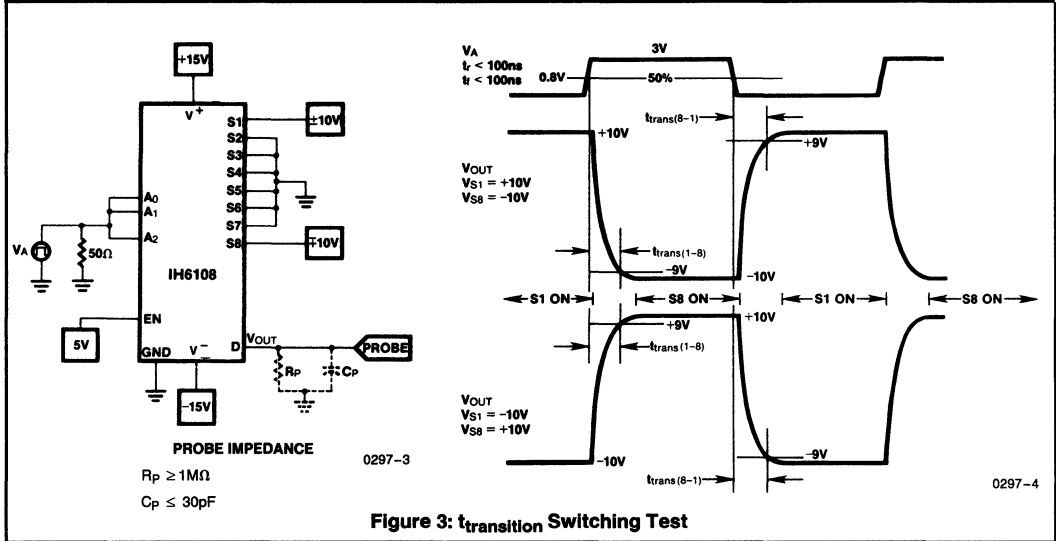


Figure 3: $t_{\text{transition}}$ Switching Test

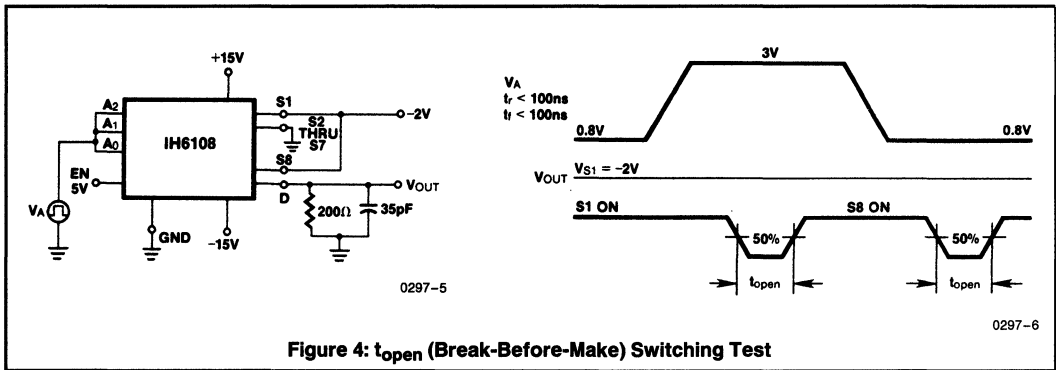


Figure 4: t_{open} (Break-Before-Make) Switching Test

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NOTE: All typical values have been characterized but are not tested.

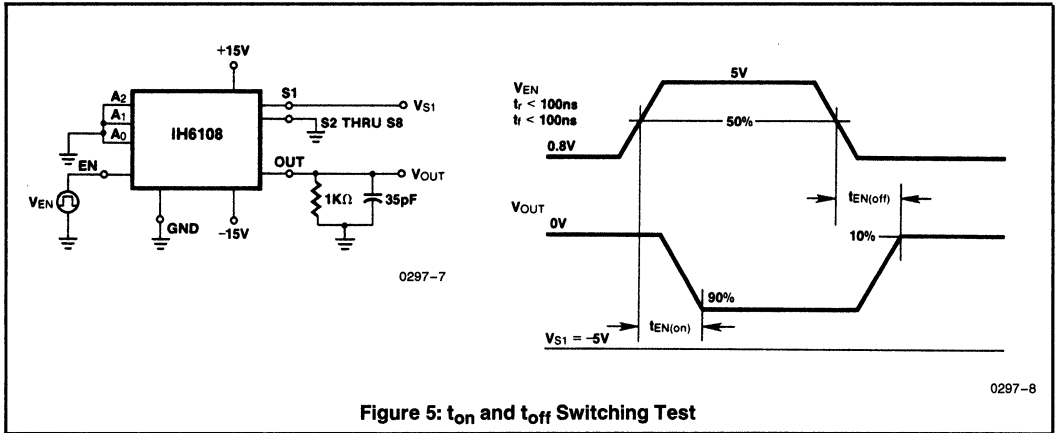


Figure 5: t_{on} and t_{off} Switching Test

IH6108 APPLICATION INFORMATION

Enable Input Strobing Levels

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6)

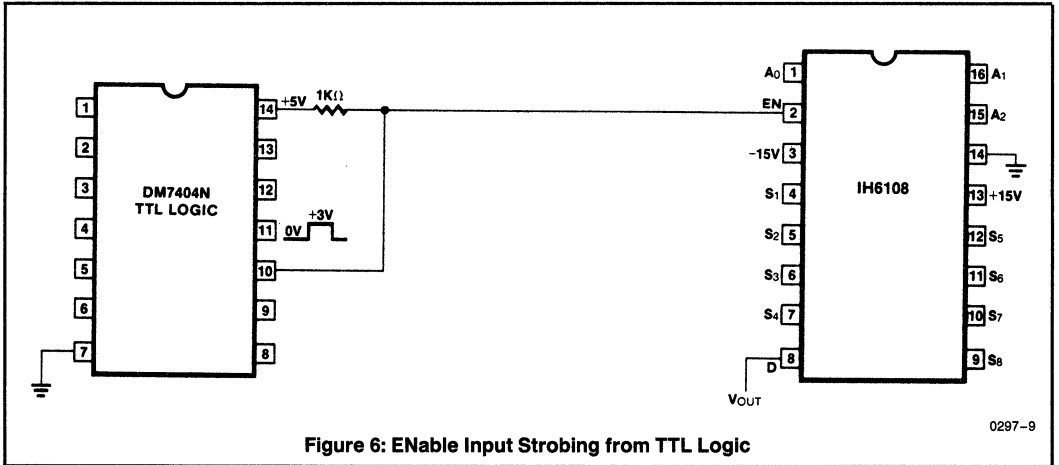


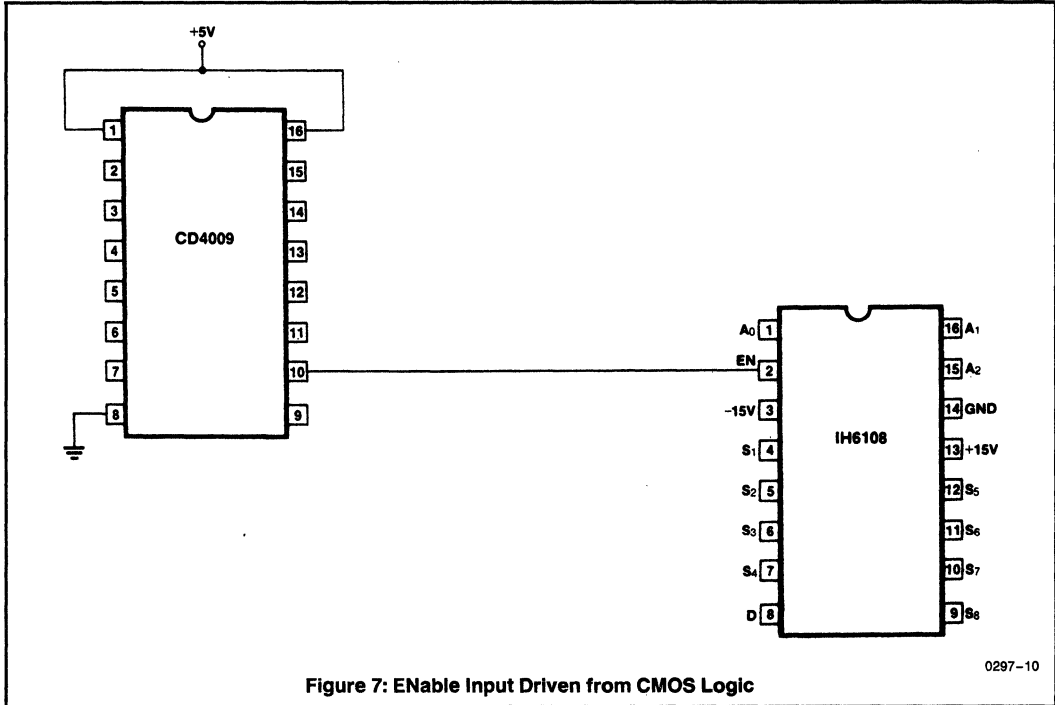
Figure 6: ENable Input Strobing from TTL Logic

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 7.

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NOTE: All typical values have been characterized but are not tested.

IH6108 APPLICATION INFORMATION (Continued)



The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The following chart shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS or TTL Supply Voltage	Typical t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than eight channels is required. In these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

Using the IH6108 with supplies other than $\pm 15V$

The IH6108 can be used with power supplies ranging from $\pm 6V$ to $\pm 16V$. The switch $r_{DS(on)}$ will increase as the

supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

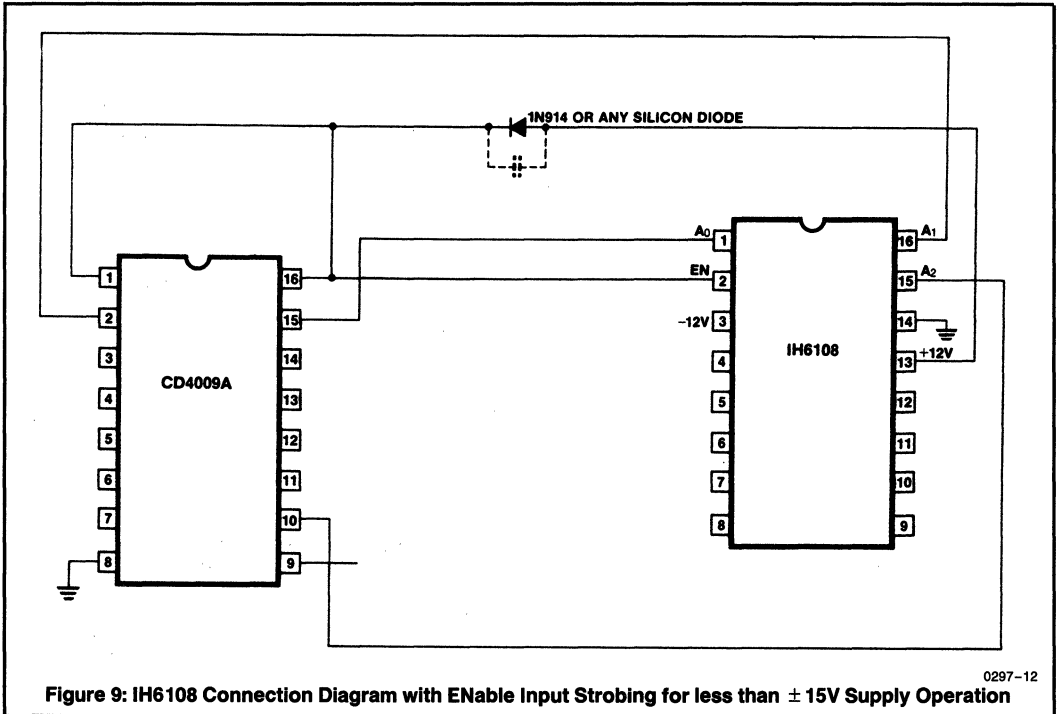
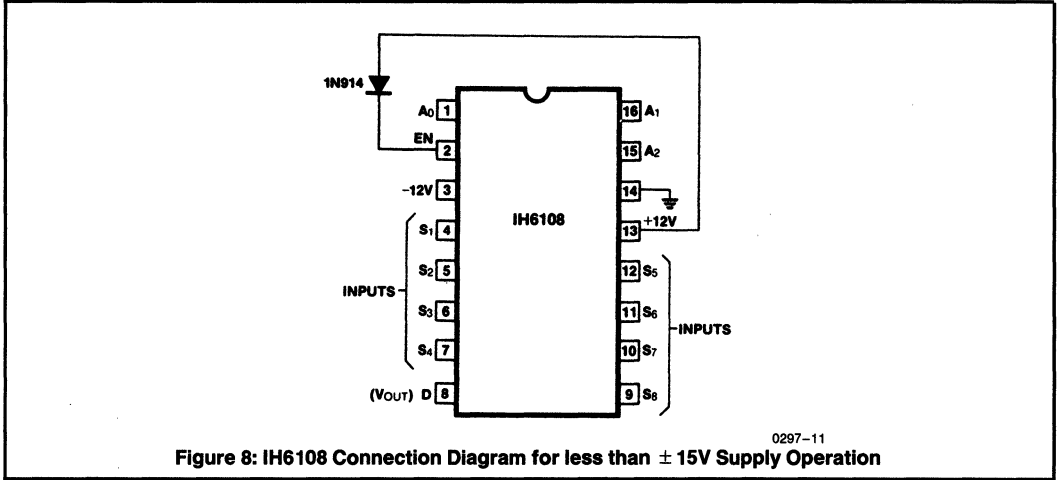
Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done, the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 13) via a silicon diode as shown in Figure 8. When using this type of configuration, a further requirement must be met: the strobe levels of A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN, (See Figure 9). A $1\mu F$ capacitor can be placed across the diode to minimize switching glitches.

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NOTE: All typical values have been characterized but are not tested.

IH6108 APPLICATION INFORMATION (Continued)



Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to $\pm 14V$ (actually $-15V$ to $+14.3V$ because of the input protection diode) when using $\pm 15V$ supplies.

The electrical specifications of the IH6108 are guaranteed for $\pm 10V$ signals, but the specifications have very minor changes for $\pm 14V$ signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

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NOTE: All typical values have been characterized but are not tested.

IH6116

16-Channel CMOS Analog Multiplexer



IH6116

GENERAL DESCRIPTION

The IH6116 is a CMOS one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to be used as a system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6116MJI	-55°C to +125°C	28 pin CERDIP
IH6116CJI	0°C to 70°C	28 pin CERDIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6116MDI/CDI)

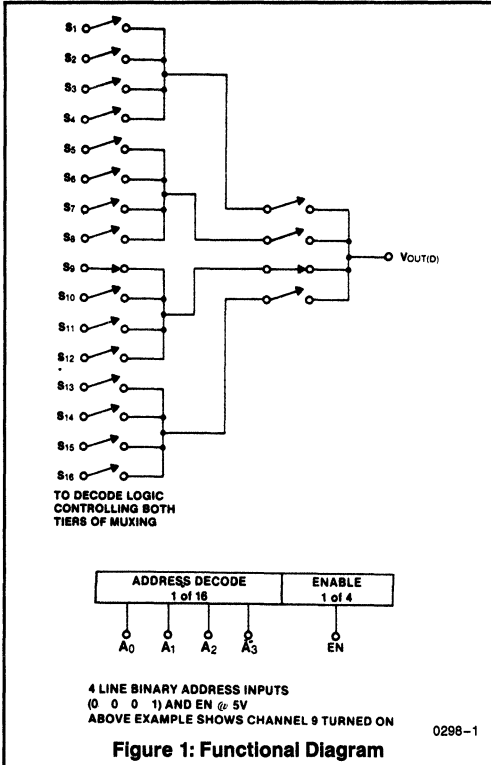


Figure 1: Functional Diagram

FEATURES

- Pin Compatible With DG506A, HI-506 & AD7506
- Ultra Low Leakage — $I_{D(off)} \leq 100\text{pA}$ Typical
- ± 11 Analog Signal Range
- $r_{DS(on)} < 700$ Ohms Over Full Signal and Temperature Range
- Break-Before-Make Switching
- TTL and CMOS Compatible Address Control
- Binary Address Control (4 Address Inputs Control 16 Channels)
- Two Tier Submultiplexing to Facilitate Expandability
- Power Supply Quiescent Current Less Than $100\mu\text{A}$
- No SCR Latchup
- Internal Diode In Series With V^+ For Fault Protection

DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$ Logic "0" = $V_{AL} \leq 0.8V$

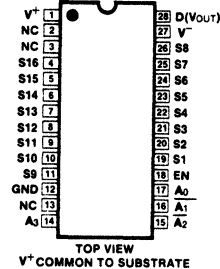


Figure 2: Pin Configuration

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NOTE: All typical values have been characterized but are not tested.

9

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground -15V to 15V
V_S or V_D to $V+$ 0, -36V
V_S or V_D to $V-$ 0, 36V
$V+$ to Ground 16V
$V-$ to Ground -16V
Current (Any Terminal) 30mA

Current (Analog Source or Drain) 20mA
Operating Temperature -55 to 125°C
Storage Temperature -65 to 150°C
Lead Temperature (Soldering, 10sec) 300°C
Power Dissipation (Package)* 1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

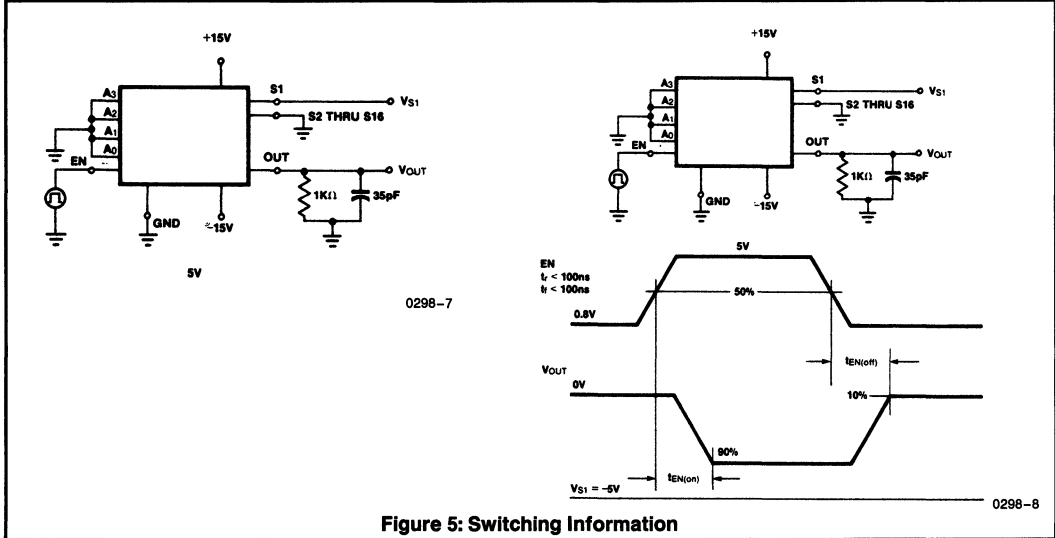
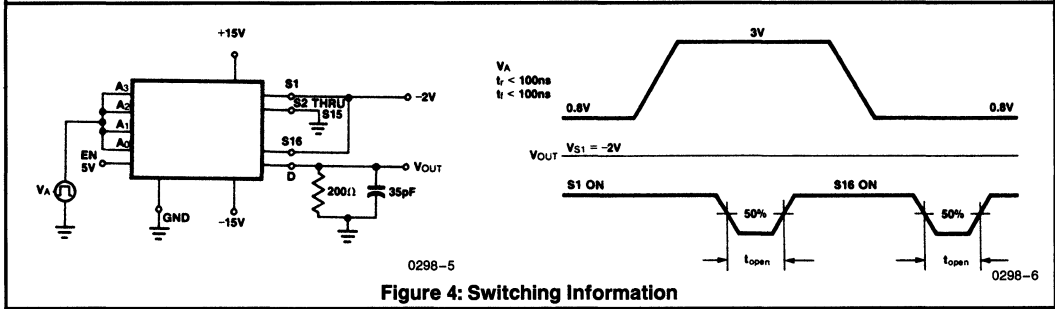
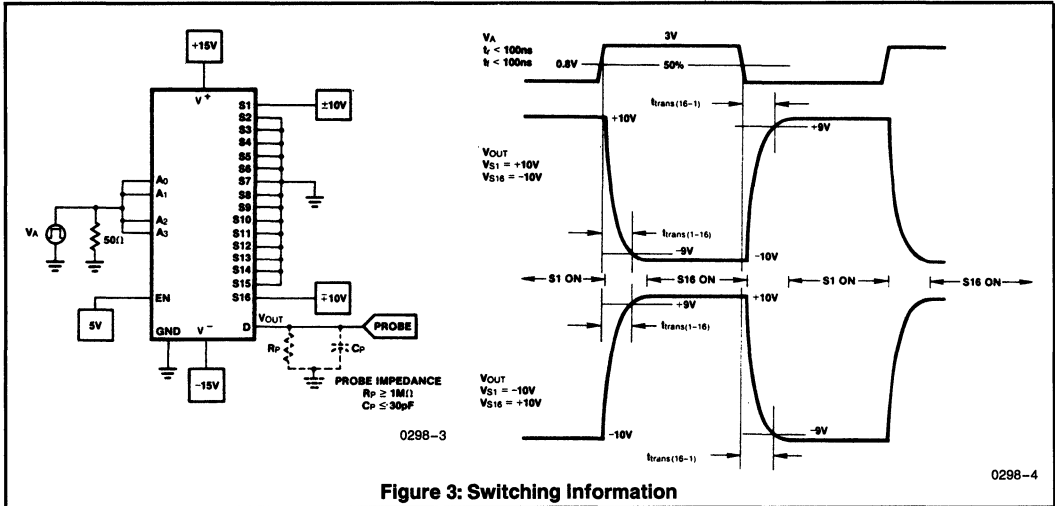
$V+ = 15V$, $V- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	0°C	25°C	70°C		
SWITCH												
$r_{DS(ON)}$	S to D	16	480	$V_D = 10V, I_S = -1mA$ $V_D = -10V, I_S = 1mA$	Sequence each switch on $V_{AL} = 0.8V, V_{AH} = 3V$	600	600	700	650	650	750	Ω
		16	300			600	600	700	650	650	750	
$\Delta r_{DS(ON)}$			20	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg}}$, $V_S = \pm 10V$								%
$I_{S(OFF)}$	S	16	0.01	$V_S = 10V, V_D = -10V$	$V_{EN} = 0.8V$		$\pm .5$	50		± 1	50	nA
		16	0.01	$V_S = -10V, V_D = 10V$			$\pm .5$	50		± 1	50	
$I_{D(OFF)}$	D	1	0.1	$V_D = 10V, V_S = -10V$	$V_{EN} = 0.8V$		± 1	100		± 5	100	nA
		1	0.1	$V_D = -10V, V_S = 10V$			± 2	100		± 5	100	
$I_{D(ON)}$	D	16	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on $V_{AL} = 0.8V, V_{AH} = 3V$		± 2	100		± 5	100	nA
		16	0.1	$V_{S(ALL)} = V_D = -10V$			± 2	100		± 5	100	
INPUT												
$I_{A(on)}$ or $I_{A(off)}$		4	0.01	$V_A = 2.4V$	All $V_A = 0$		-10	-30		-10	-30	μA
		4	0.01	$V_A = 14V$			10	30		10	30	
I_A	$A_0 A_1$ $A_2 A_3$	4		$V_{EN} = 5V$	All $V_A = 0$		-10	-30		-10	-30	μA
	EN	1		$V_{EN} = 0$			-10	-30		-10	-30	
DYNAMIC												
t_{trans}	D		0.6	See Fig. 3								μs
t_{open}	D		0.2	See Fig. 4								
$t_{EN(on)}$	D		0.8	See Fig. 5			1.5					
$t_{EN(off)}$	D		0.3				1					
"OFF" Isolation	D		60	$V_{EN} = 0, R_L = 200\Omega, C_L = 3pF, V_S = 3V_{RMS}, f = 500kHz$								dB
$C_{S(OFF)}$	S		5	$V_S = 0$	$V_{EN} = 0, f = 140kHz$ to 1MHz							pF
$C_{D(OFF)}$	D		40	$V_D = 0$								
$C_{ds(OFF)}$	D to S		1	$V_S = 0, V_D = 0$								
SUPPLY												
Supply Current	+	$V+$	1	55	$V_{EN} = 5V$		200			1000		μA
	-	$V-$	1	2			100			1000		
Standby Current	+	$V+$	1	1	$V_{EN} = 0$		100			1000		μA
	-	$V-$	1	1			100			1000		

NOTE 1: See Section V. Enable Input Strobing Levels.

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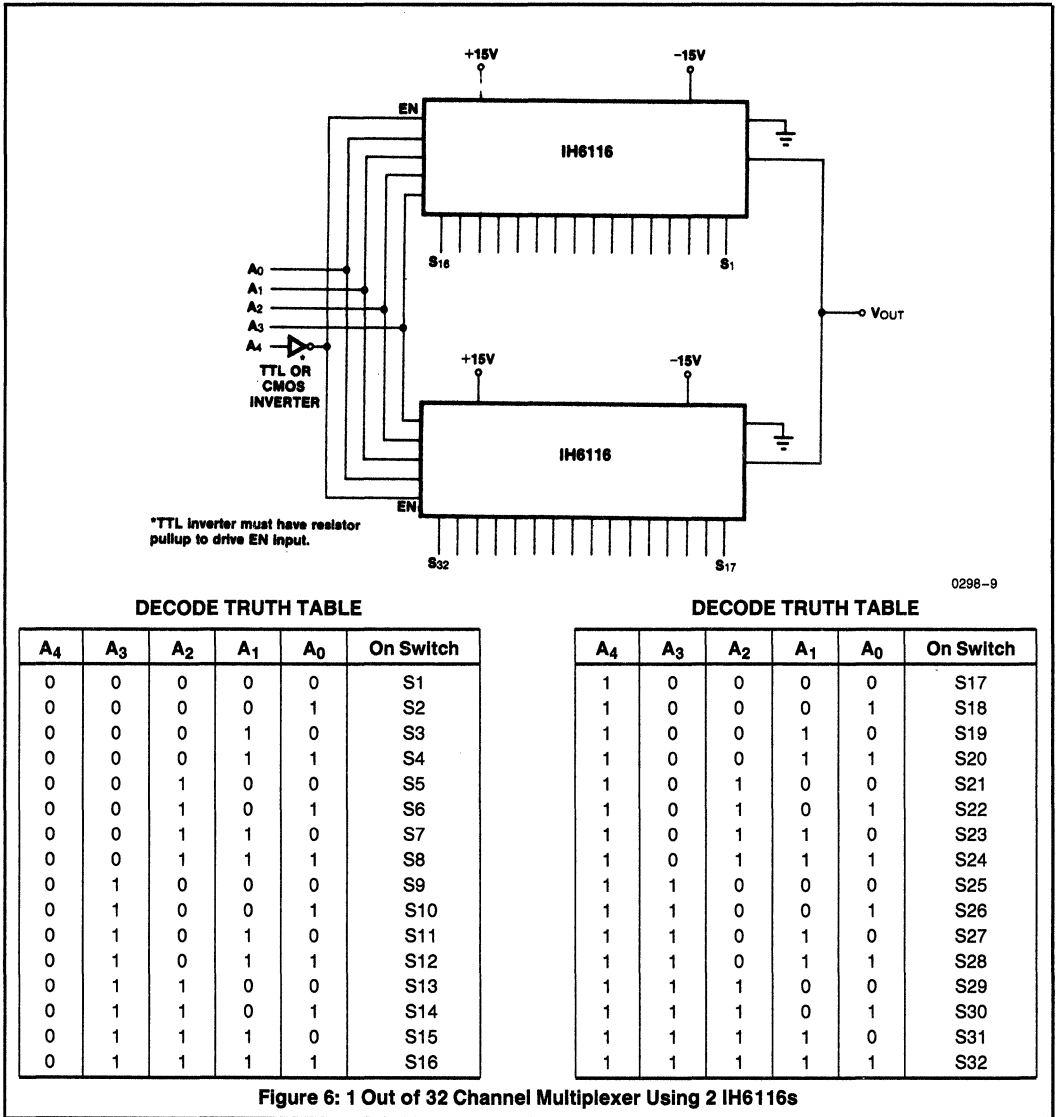
NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

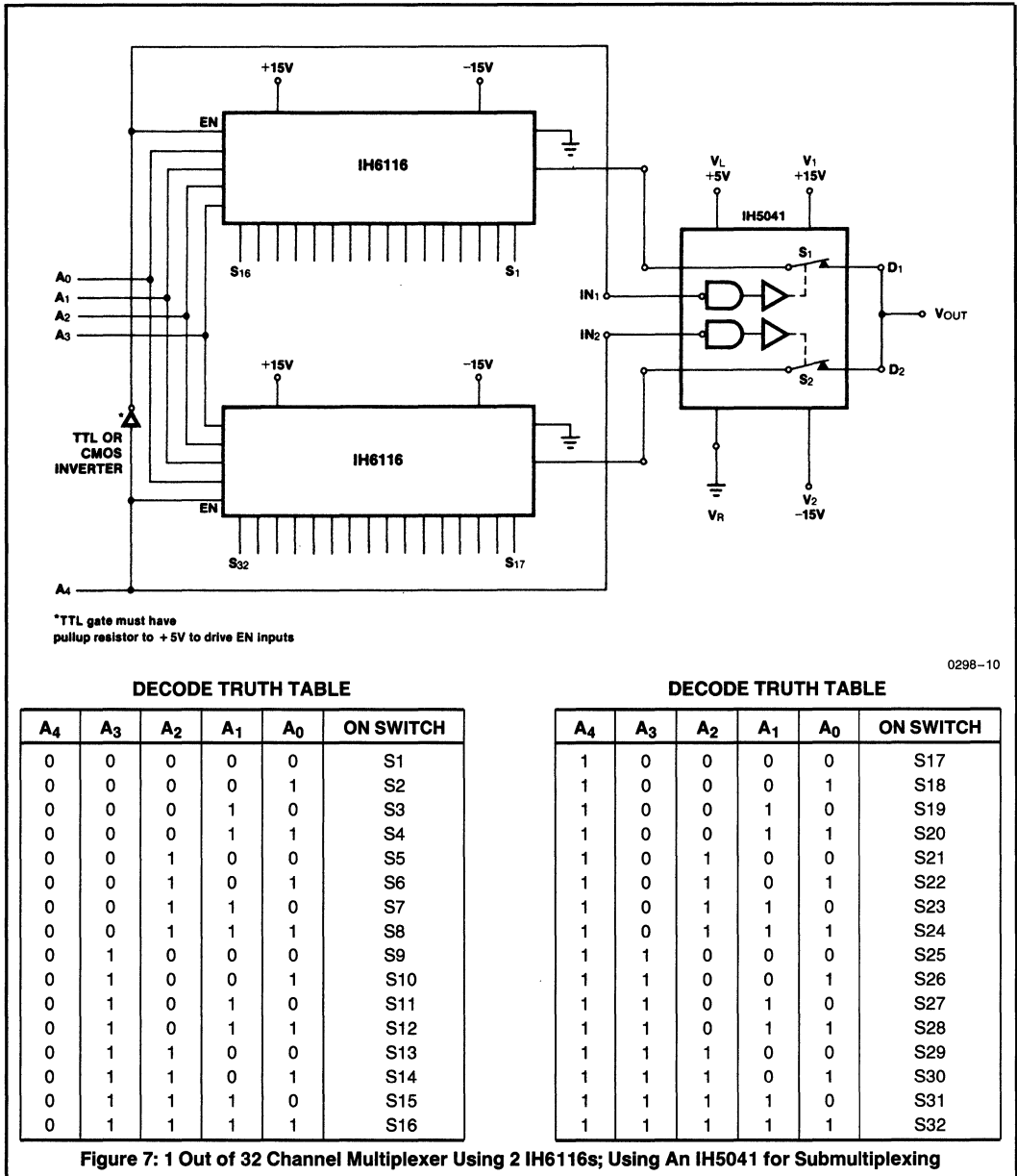
IH6116 APPLICATIONS



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NOTE: All typical values have been characterized but are not tested.

IH6116 APPLICATIONS (Continued)



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NOTE: All typical values have been characterized but are not tested.

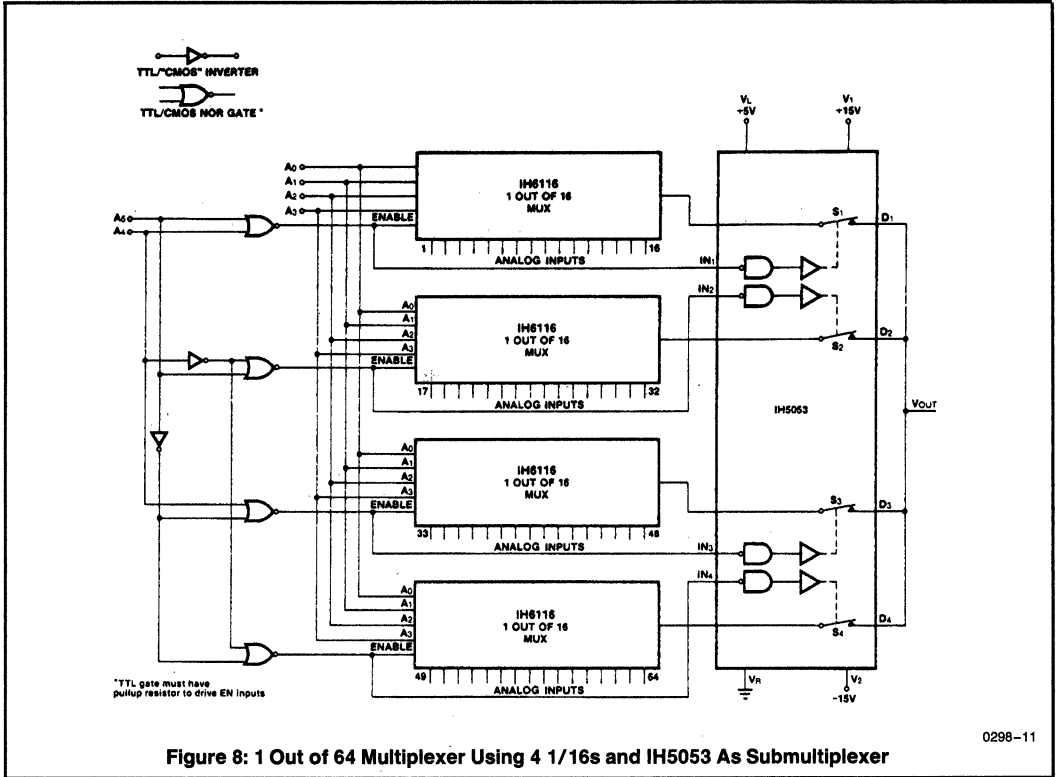


Figure 8: 1 Out of 64 Multiplexer Using 4 1/16s and IH5053 As Submultiplexer

0298-11

General note on expandability of IH6116

The IH6116 is a two tier multiplexer, where sixteen input channels are routed to a common output in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this is lower output capacitance and leakage than would be possible with a system using all 16 channels tied to one common output. Also the expandability into 32, 64, 128, channels etc. is facilitated. Figures 6, 7, and 8 show how the IH6116 can be expanded.

Figure 6 shows a 1 of 32 multiplexer, using 2 IH6116s. Since the 6116 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. The four output channels of each

6116 are tied together so that 8 channels are tied to the V_{OUT} common point. Since only one channel of information is on at a time, the common output will consist of 7 OFF channels and 1 ON channel. Thus the output leakage will correspond to 7 I_{D(off)} and 1 I_{D(on)}, or about 1.0nA of typical leakage at room temperature. Throughput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Throughput channel resistance will be in the 500Ω area.

Figure 7 shows the 1 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacitance. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thrupt channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

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NOTE: All typical values have been characterized but are not tested.

Figure 8 shows a 1 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5053 is used to get the third tier of MUXing. The V_{OUT} point will see 3 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.4 nA. Throughput channel resistance will be in the 550 ohm area with throughput switching speeds about 1.3 μ s for ON time and 0.8 μ s for OFF time.

The IH5053 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6116 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are on the order of 1-2 μ A, so that no excessive system power is dissipated. Note that the logic of the 5053 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra circuitry being required.

Enable input strobing levels

The enable input (EN) acts as an enabling or disabling pin for the IH6116 when used as a 16 channel MUX. However, when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A4 input.

For the system to function properly the EN input (pin 18) must go to 5V \pm 5% for the high state and less than 0.8V

for the low state. When using TTL logic, a pull-up resistor of 1k Ω or less should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6108 data sheet for details.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection"

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $t_{DS(ON)}$ of the switch is maintained at specified values.

IH6201

Dual CMOS

Driver/Voltage Translator



GENERAL DESCRIPTION

The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes low level TTL or CMOS logic signals and converts them to higher levels (i.e. to $\pm 15V$ swings). This translator is typically used in making solid state switches, or analog gates.

When used in conjunction with the Intersil IH401 family of Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time < t_{on} time). The combination has typical $t_{off} \approx 80ns$ and typ. $t_{on} \approx 200ns$ for signals up to 20Vpp in amplitude.

A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\bar{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\bar{\theta}$ goes to V^+ ; thus θ and $\bar{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive N and P channel MOSFETs, to make a complete CMOS analog gate.

The driver typically uses +5V and $\pm 15V$ power supplies, however a wide range of V^+ and V^- is also possible. It is necessary that $V^+ > 5V$ for the driver to work properly, however.

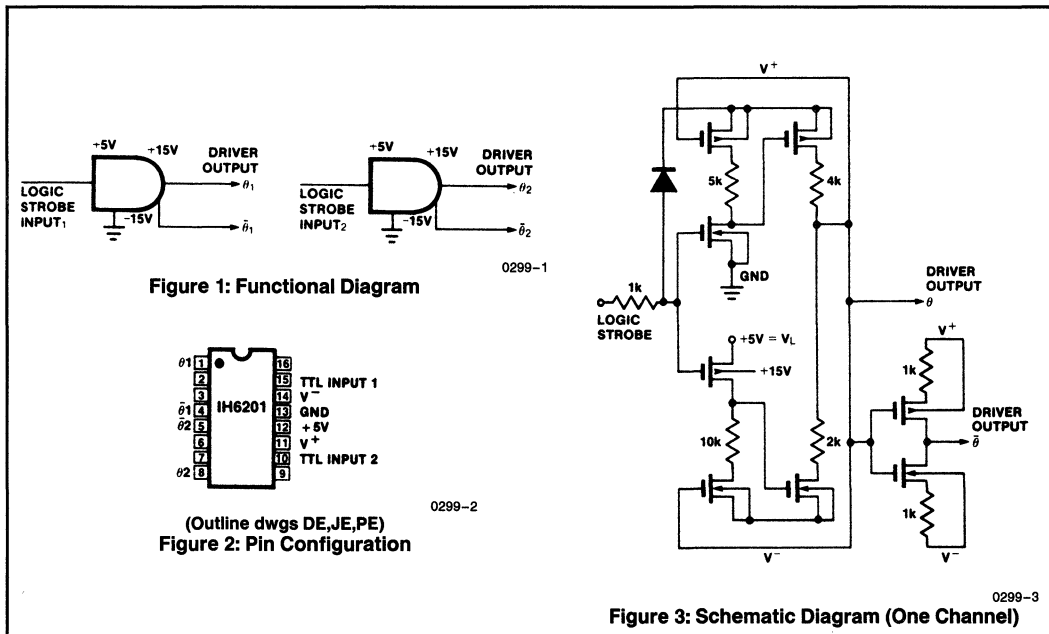
FEATURES

- Driven Direct From TTL or CMOS Logic
- Translates Logic Levels Up to 30V Levels
- Switches 20V_{ACPP} Signals When Used in Conjunction With Intersil IH401A Varafet (As An Analog Gate)
- $t_{ON} \leq 300ns$ & $t_{OFF} \leq 200ns$ for 30V Level Shifts
- Quiescent Supply Current $\leq 100\mu A$ for Any State (D.C.)
- Provides Both Normal & Inverted Outputs

ORDERING INFORMATION

Part Number	Temperature Range
*IH6201CDE	0°C to 70°C
*IH6201MDE	-55°C to +125°C
IH6201CJE	0°C to 70°C
IH6201MJE	-55°C to 125°C
IH6201CPE	0°C to 70°C

*Special Order Only



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V+ to V-	35V
V+	35V
V-	35V
V+ to V _{IN}	40V
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS V+ = +15V, V- = -15V, V_L = +5V

Item	Test Conditions	IH6201CDE			IH6201MDE			Units
		-25°C	+25°C	+85°C	-55°C	+25°C	+125°C	
θ or $\bar{\theta}$ driver output swing	V _{IN} = 0V \square \square +3V Fig. 5B		28			28		V _{pp}
V _{IN} strobe level ("1") for proper translation	$\theta \geq 14V$ $\bar{\theta} \geq -14V$	3.0	3.0	3.0		2.4		V _{D.C.}
V _{IN} strobe level ("0") for proper translation	$\theta \geq -14V$ $\bar{\theta} \geq 14V$	0.4	0.4	0.4		0.8		V _{D.C.}
I _{IN} input strobe current draw (for 0V - 5V range)	V _{IN} = 0V or +5V	± 1	± 1	10	± 1	± 1	10	μA
t _{on} time	V _{IN} = 0V \square \square C _L = 30pF switching turn-on time fig. 5B		400			300		ns
t _{off} time	V _{IN} = 0V \square \square C _L = 30pF switching turn-off time fig. 5B		300			200		ns
I+ (V+) power supply quiescent current	V _{IN} = 0V or +5V	100	100	100	100	100	100	μA
I- (V-) power supply quiescent current	V _{IN} = 0V or +5V	100	100	100	100	100	100	μA
I _L (V _L) power supply quiescent current	V _{IN} = 0V or +5V	100	100	100	100	100	100	μA

APPLICATIONS

Input Drive Capability

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V to 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1k Ω to 10k Ω range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to -15V) the circuit is unaffected as long as V+ to V_{IN} does not exceed absolute maximum rating.

Output Drive Capability

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel JFETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents a forward bias condition between the signal input and the +V_{CC} supply. The IH6201 will drive any JFET provided some sort of isolation is added.

You will notice in Figure 4 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for the inadequate charge area curve for isolation diode i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output JFET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100k Ω to 1M Ω range and is not too critical.

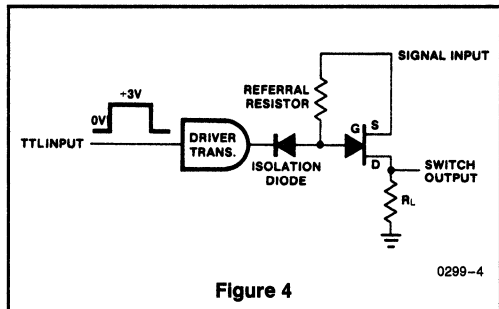


Figure 4

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NOTE: All typical values have been characterized but are not tested.

Making a Complete Solid State Switch That Can Handle 20Vpp Signals

The limitation on signal handling capability comes from the output gating device. When a JFET is used, the pinch-off of the JFET acting with the V^- supply does the limiting. In fact max. signal handling capability = $2(V_p + (V^-)) V_{pp}$ where V_p = pinch-off voltage of JFET chosen. i.e. $V_p = 7V$, $V^- = -15V$ \therefore max. signal handling = $2(7V + (-15V)) V_{pp} = 2(7V - 15V) V_{pp} = 2(-8V_{pp}) = 16V_{pp}$. Obviously to get $\geq 20V_{pp}$, $V_p \geq 5V$ with $V^- = -15V$. Another simple way to get 20Vpp with $V_p = 7V$, is to increase V^- to $-17V$. In fact using $V^+ = +12V$ or $+15V$ and setting $V^- = -18V$ allows one to switch 20Vpp with any member of IH401 family. The advantage of using the $V_p = 7V$ pinch-off (along with unsymmetrical supplies), over the $V_p = 5V$ pinch-off (and $\pm 15V$ supplies), is that you will have a much lower $R_{DS(ON)}$ for the $V_p = 7$ JFET (i.e. for the 2N4391).

$$r_{DS(ON)} \approx 22\Omega, \quad r_{DS(ON)} \approx 35\Omega$$

$$V_p = 7V, \quad V_p = 5V$$

The IH6201 is a dual translator, each containing 4 CMOS FET pairs. The schematic of one-half of an IH6201, driving one-quarter of an IH401, is shown in Figure 5A.

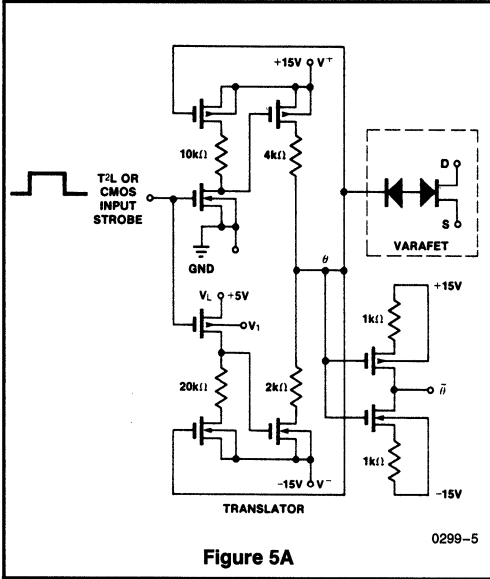


Figure 5A

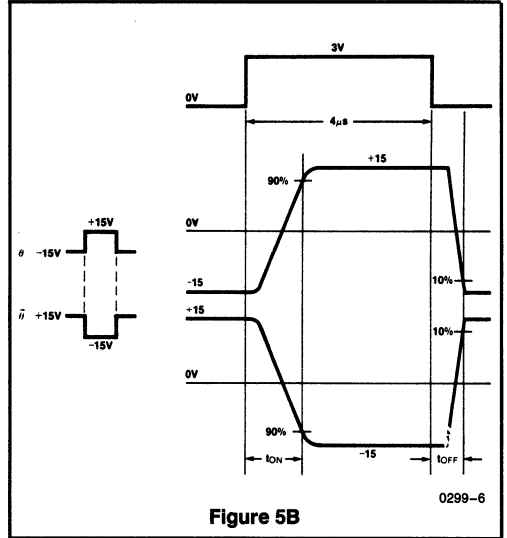


Figure 5B

NOTE: Each translator output has a θ and $\bar{\theta}$ output. θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See Figure 6)

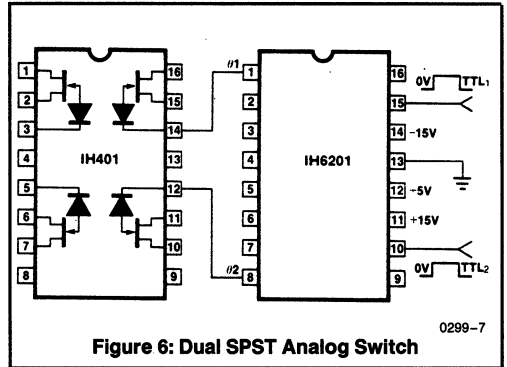


Figure 6: Dual SPST Analog Switch

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

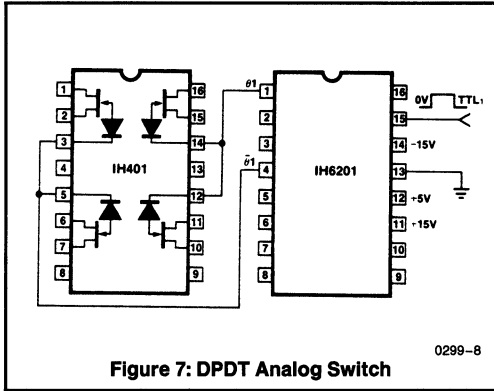


Figure 7: DPDT Analog Switch

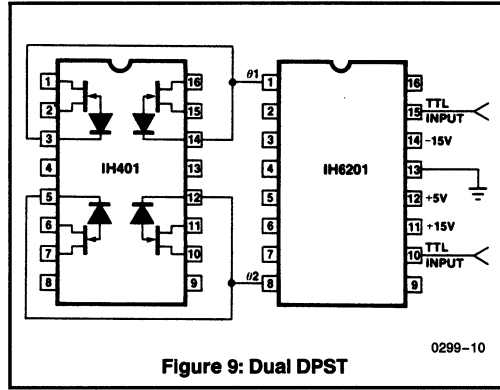


Figure 9: Dual DPST

NOTE: Either switch is turned on when strobe input goes high.

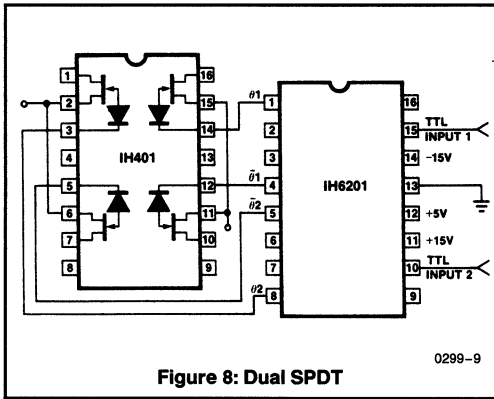


Figure 8: Dual SPDT

IH6208

4-Channel Differential CMOS Analog Multiplexer



GENERAL DESCRIPTION

The IH6208 is a 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

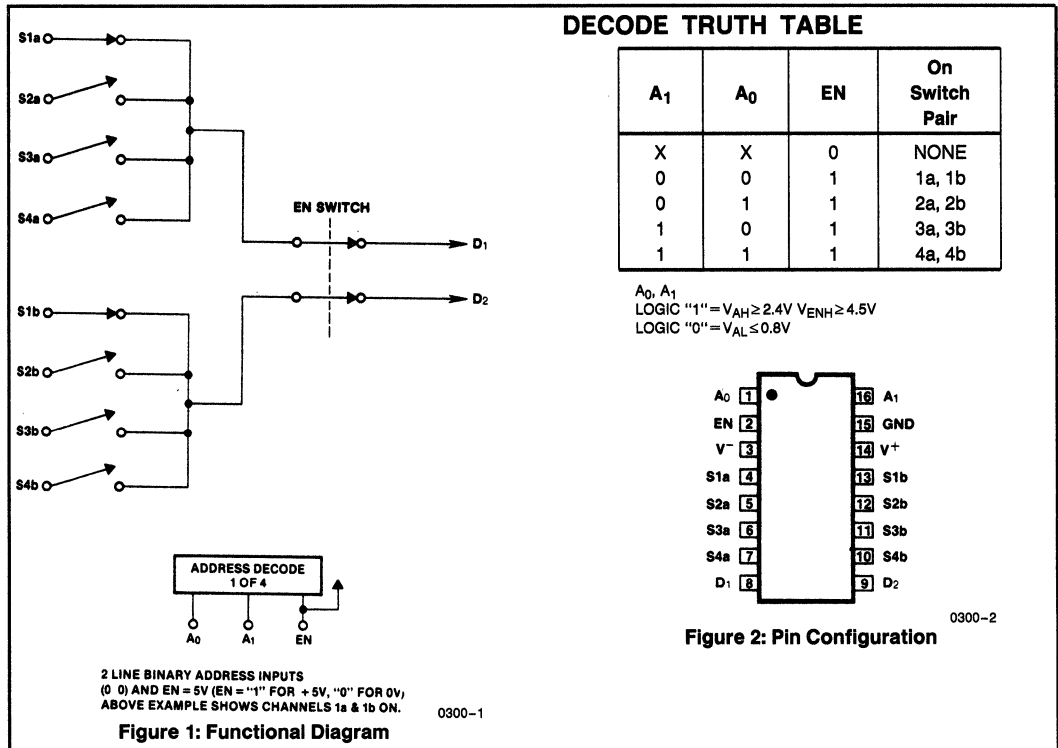
ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6208MJE	-55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

Ceramic package available as special order only (IH6208MDE/CDE)

FEATURES

- Ultra Low Leakage — $I_{D(off)} \leq 100\text{pA}$ Typical
- $r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range
- Power Supply Quiescent Current Less Than $100\mu\text{A}$
- $\pm 14\text{V}$ Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- Binary Address Control (2 Address Inputs Control 2 Out of 8 Channels)
- TTL and CMOS Compatible Address Control
- Pin Compatible With HI509, DG509A & AD7509
- Internal Diode In Series With V^+ For Fault Protection



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V _{IN} (A, EN) to Ground -15V, V _I
V _S or V _D to V ⁺ 0, -36V
V _S or V _D to V ⁻ 0, 36V
V ⁺ to Ground 16V
V ⁻ to Ground -16V
Current (Any Terminal) 30mA

Current (Analog Source or Drain) 20mA
Operating Temperature -55 to 125°C
Storage Temperature -65 to 150°C
Lead Temp (Soldering, 10sec) 300°C
Power Dissipation (Package)* 1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V⁺ = 15V, V⁻ = -15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

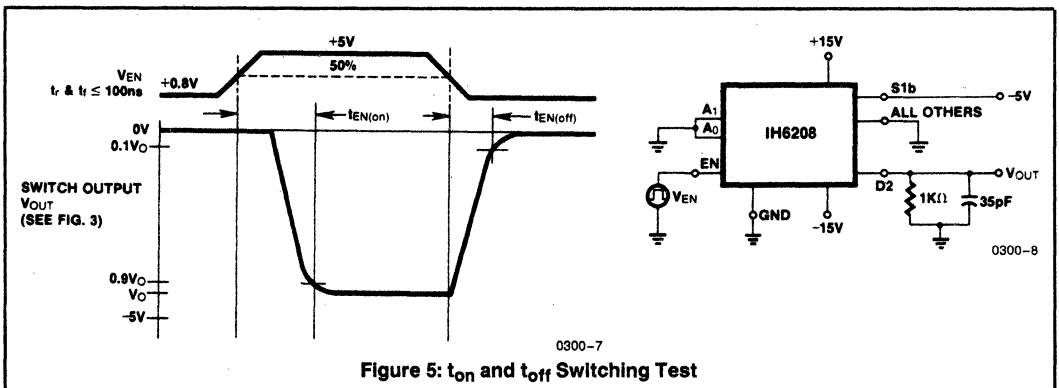
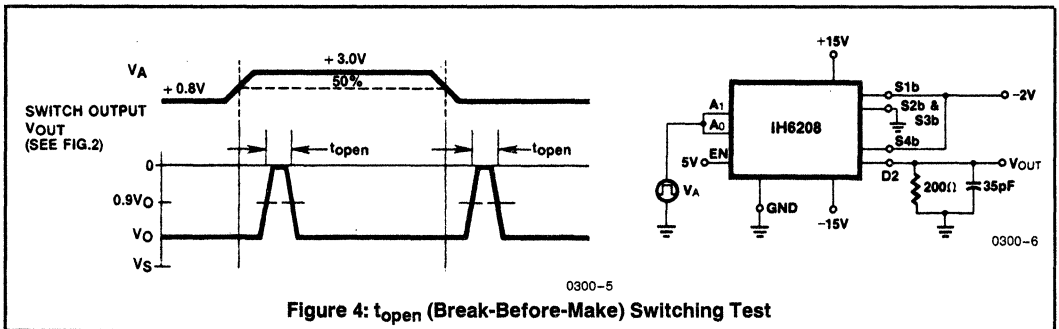
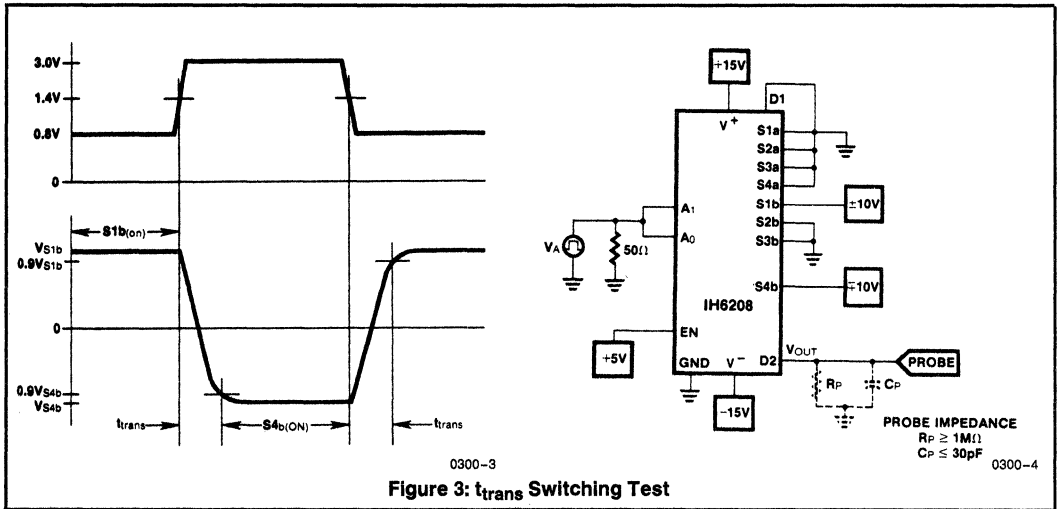
Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions	Max Limits						Units		
					M Suffix			C Suffix					
					-55°C	25°C	125°C	0°C	25°C	70°C			
SWITCH													
r _{DS(ON)}	S to D	8	180	V _D = -10V, I _S = -1.0mA	Sequence each switch on V _{AL} = 0.8V, V _{AH} = 2.4V	300	300	400	350	350	450	Ω	
		8	150	V _D = -10V, I _S = -1.0mA		300	300	400	350	350	450		
Δr _{DS(ON)}			20	Δr _{DS(ON)} = $\frac{r_{DS(ON)max} - r_{DS(ON)min}}{r_{DS(ON)avg}}$, V _S = ±10V								%	
I _{S(OFF)}	S	8	0.002	V _S = 10V, V _D = -10V	V _{EN} = 0.8V		±.5	50		±1	50	nA	
		8	0.002	V _S = -10V, V _D = 10V			±.5	50		±1	50		
I _{D(OFF)}	D	2	0.03	V _D = 10V, V _S = -10V				±2	50		±5		100
		2	0.03	V _D = -10V, V _S = 10V				±2	50		±5		100
I _{D(ON)}	D	8	0.1	V _{S(ALL)} = V _D = 10V	Sequence each switch on		±2	50		±5	100		
		8	0.1	V _{S(ALL)} = -10V	V _{AL} = 0.8V, V _{AH} = 2.4V		±2	50		±5	100		
INPUT													
I _{A(ON)}		2	0.01	V _A = 2.4V or 0V			-10	-30		-10	-30	μA	
I _{A(OFF)}		2	0.01	V _A = 14V or 0V			10	30		10	30		
I _A	A ₀ , A ₁	2		V _{EN} = 5V	All V _A = 0 (Address Pins)		-10	-30		-10	-30		
	EN	1		V _{EN} = 0			-10	-30		-10	-30		
DYNAMIC													
t _{transition}	D		0.3	See Fig. 3		1						μs	
t _{open}	D		0.2	See Fig. 4									
t _{EN(ON)}	D		0.6	See Fig. 5		1.5							
t _{EN(OFF)}	D		0.4			1							
"OFF" Isolation	D		60	V _{EN} = 0, R _L = 200Ω, C _L = 3pF, V _S = 3VRMS, f = 500kHz								dB	
C _{s(off)}	S		5	V _S = 0								pF	
C _{d(off)}	D		12	V _D = 0	V _{EN} = 0V, f = 140kHz to 1MHz								
C _{ds(off)}	D to S		1	V _S = 0, V _D = 0									
SUPPLY													
Supply	+	V ⁺	1	40	All V _A = 0 or 5V		200			1000		μA	
Current	-	V ⁻	1	2		V _{EN} = 5V		100			1000		
Standby	+	V ⁺	1	1				100			1000		
Current	-	V ⁻	1	1		V _{EN} = 0		100			1000		

NOTE 1: See Section 1 Enable Input Strobing Levels.

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NOTE: All typical values have been characterized but are not tested.

IH6208
SWITCHING INFORMATION



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NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION

ENable Input Strobing Levels

The ENable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6).

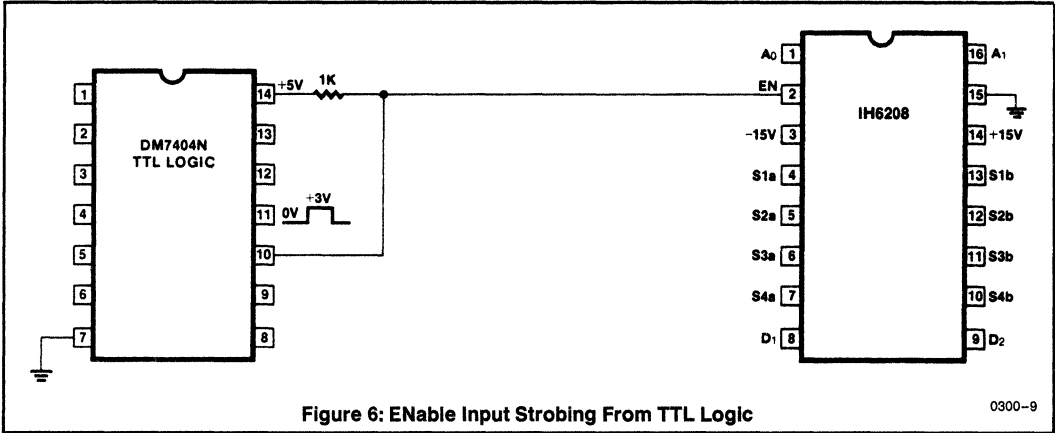


Figure 6: ENable Input Strobing From TTL Logic

0300-9

When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 7)

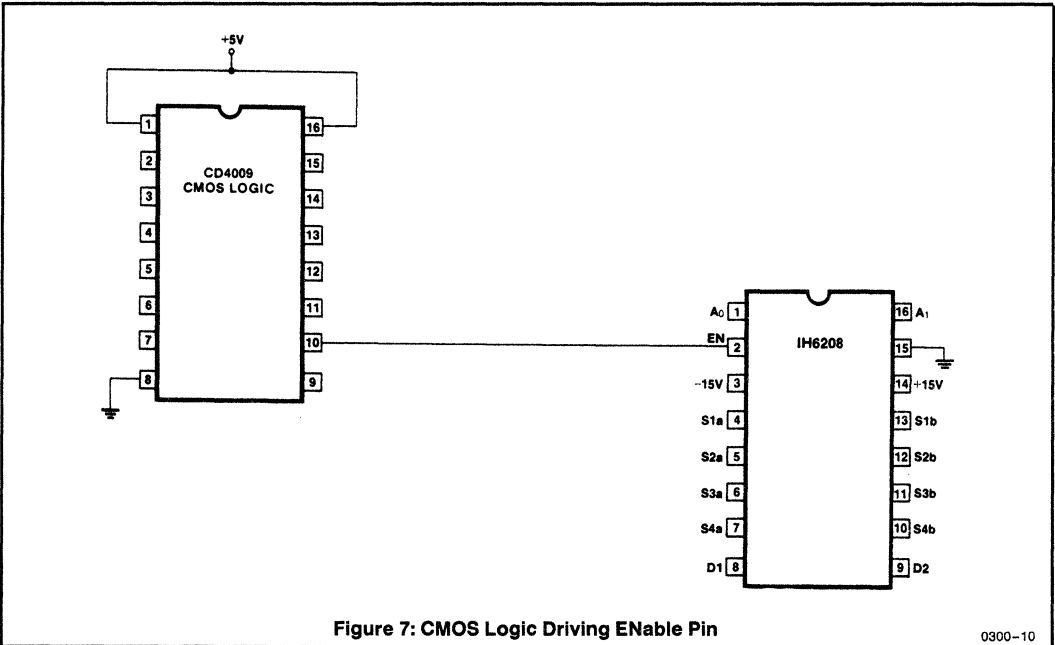


Figure 7: CMOS Logic Driving ENable Pin

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NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION (Continued)

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than four differential channels is required; in these cases the EN terminal acts as a third address input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

Using the IH6208 with supplies other than $\pm 15V$

The IH6208 can be used with power supplies ranging from $\pm 6V$ to $\pm 16V$. The switch $r_{DS(on)}$ will increase as the

supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the Address Input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 14) via a silicon diode as shown in Figure 8. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V, which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN (See Figure 9). A $1\mu F$ capacitor can be placed across the diode to minimize switching glitches.

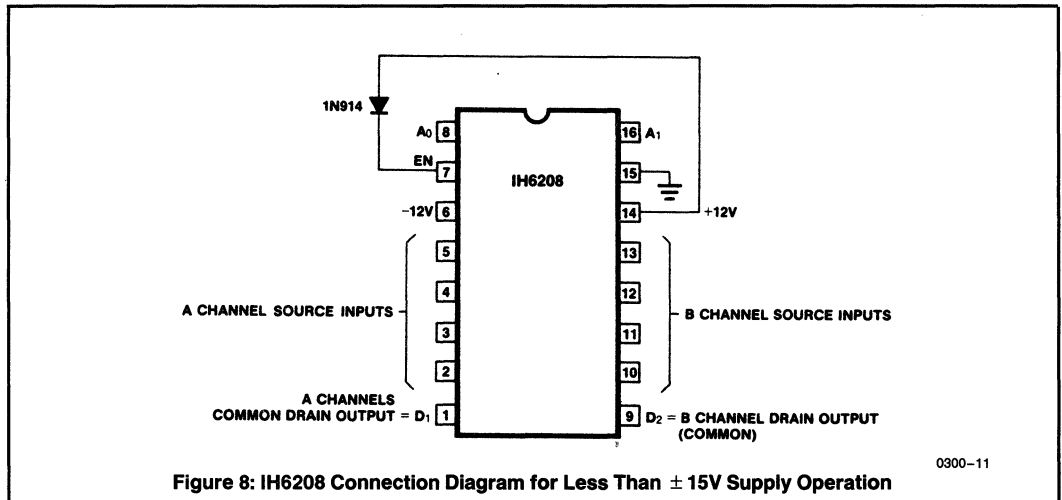
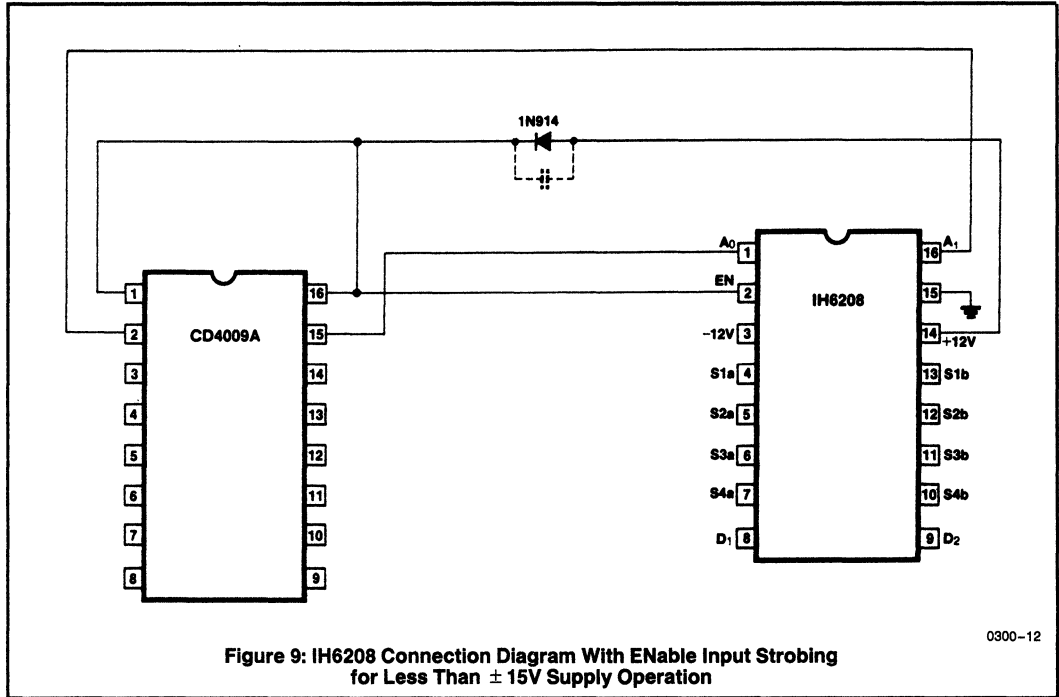


Figure 8: IH6208 Connection Diagram for Less Than $\pm 15V$ Supply Operation

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NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION (Continued)



Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to $\pm 14V$ (actually $-15V$ to $+14.3V$ because of the input protection diode) when using $\pm 15V$ supplies.

The electrical specifications of the IH6208 are guaranteed for $\pm 10V$ signals, but the specifications have very minor changes for $\pm 14V$ signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

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NOTE: All typical values have been characterized but are not tested.

IH6216

8-Channel Differential CMOS Analog Multiplexer



GENERAL DESCRIPTION

The IH6216 is a CMOS 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V), all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6216MJI	-55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

Ceramic package available as special order only (IH6216MDI/CDI)

FEATURES

- Pin Compatible With HI507, DG507A & AD7507
- ± 11V Analog Signal Range
- $r_{DS(on)} < 700$ Ohms Over Full Signal and Temperature Range
- Break-Before-Make Switching
- TTL and CMOS Compatible Address Control
- Binary Address Control (3 Address Inputs Control 2 Out of 16 Channels)
- Two Tier Submultiplexing to Facilitate Expandability
- Power Supply Quiescent Current Less Than 100µA
- No SCR Latchup
- Very Low Leakage $I_{D(OFF)} \leq 100pA$
- Internal Diode In Series With V^+ for Fault Protection

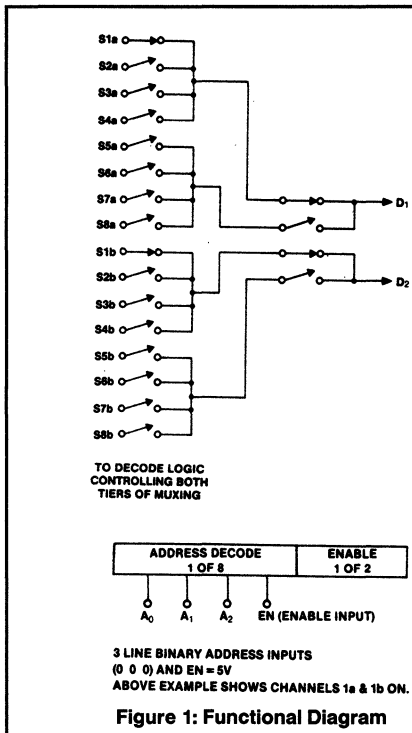


Figure 1: Functional Diagram

DECODE TRUTH TABLE

A ₂	A ₁	A ₀	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = $V_{AH} > 3V$ $V_{ENH} > 4.5V$
 LOGIC "0" = $V_{AL} < 0.8V$

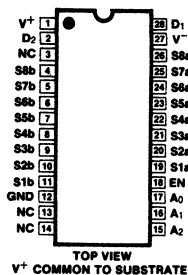


Figure 2: Pin Configuration

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V _{IN} (A, EN) to Ground	-15V ₀ -V ₁
V _S or V _D to V ⁺	0, -36V
V _S or V _D to V ⁻	0, 36V
V ⁺ to Ground	16V
V ⁻ to Ground	-16V
Current (Any Terminal)	30mA

Current (Analog Source or Drain)	20mA
Operating Temperature	-55 to 125°C
Storage Temperature	-65 to 150°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation (Package)*	1200mW

* All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

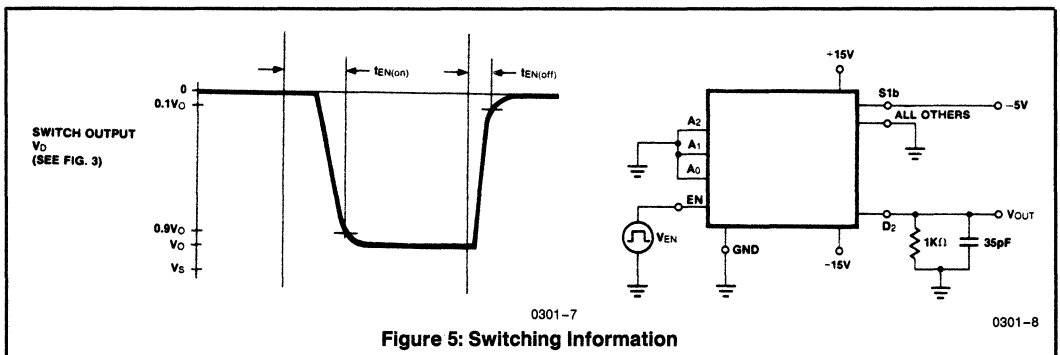
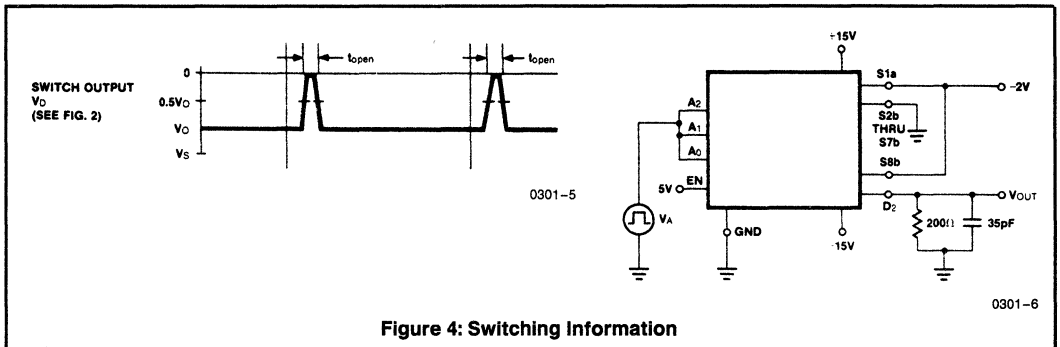
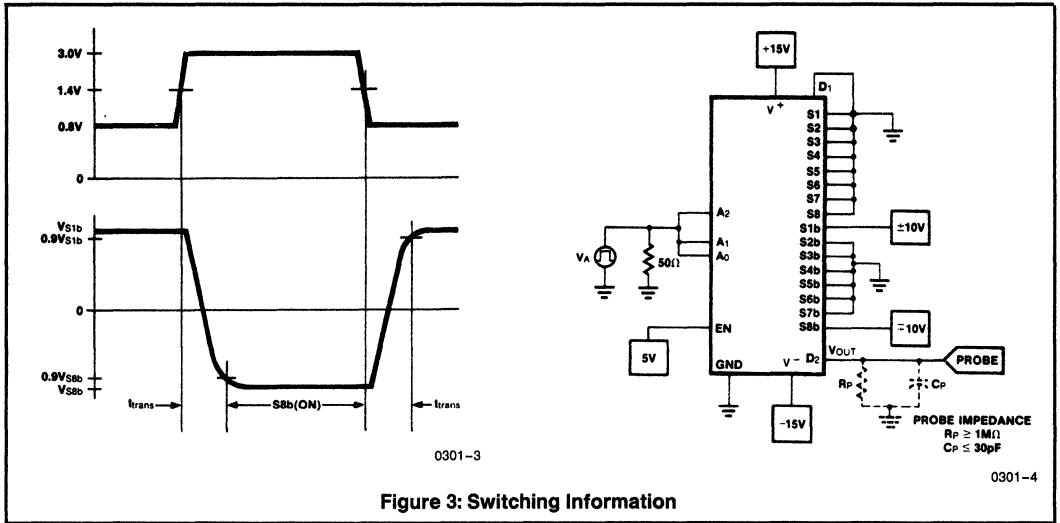
V⁺ = 15V, V⁻ = -15V, V_{EN} = +5V (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	0°C	25°C	70°C		
SWITCH												
r _{DS(ON)}	S to D	16	480	V _D = -10V, I _S = -1mA	Sequence each switch on V _{AL} = 0.8V, V _{AH} = 3V	600	600	700	650	650	750	Ω
		16	300	V _D = -10V, I _S = -1mA		600	600	700	650	650	750	
Δr _{DS(ON)}			20	Δr _{DS(ON)} = $\frac{r_{DS(ON)max} - r_{DS(ON)min}}{r_{DS(ON)avg}}$, V _S = ±10V								%
I _{S(OFF)}	S	16	0.01	V _S = 10V, V _D = -10V	V _{EN} = 0.8V		±.5	50		±1	50	nA
		16	0.01	V _S = -10V, V _D = 10V			±.5	50		±1	50	
I _{D(OFF)}	D	2	0.1	V _D = 10V, V _S = -10V	V _{EN} = 0.8V		±2	100		±5	100	nA
		2	0.1	V _D = -10V, V _S = 10V			±2	100		±5	100	
I _{D(ON)}	D	16	0.1	V _{S(ALL)} = V _D = 10V	Sequence each switch on V _{AL} = 0.8V, V _{AH} = 3V		±2	100		±5	100	nA
		16	0.1	V _{S(ALL)} = V _D = -10V			±2	100		±5	100	
INPUT												
I _{A(on)} OR		3	0.01	V _A = 3.0V	All V _A = 0		-10	-30		-10	-30	μA
I _{A(off)}		3	0.01	V _A = 14V			10	30		10	30	
I _A	A ₀ A ₁ A ₂ A ₃	3		V _{EN} = 5V			-10	-30		-10	-30	
	EN	1		V _{EN} = 0		-10	-30		-10	-30		
DYNAMIC												
t _{trans}	D		0.6	See Fig. 3		1						μs
t _{open}	D		0.2	See Fig. 4								
t _{on(EN)}	D		0.8	See Fig. 5		1.5						
t _{off(EN)}	D		0.3			1						
"OFF" Isolation	D		60	V _{EN} = 0, R _L = 200Ω, C _L = 3pF, V _S = 3V _{RMS} , f = 500kHz								dB
C _s	S		5	V _S = 0	V _{EN} = 0, f = 140kHz to 1MHz							pF
C _{d(off)}	D		20	V _D = 0								
C _{ds}	D to S		1	V _S = 0, V _D = 0								
SUPPLY												
Supply	+	V ⁺	1	55	V _{EN} = 5V		200			1000		μA
Current	-	V ⁻	1	2			100			1000		
Standby	+	V ⁺	1	1	V _{EN} = 0		100			1000		
Current	-	V ⁻	1	1			100			1000		

NOTE 1: See Enable Input Strobing Levels, Section 1.

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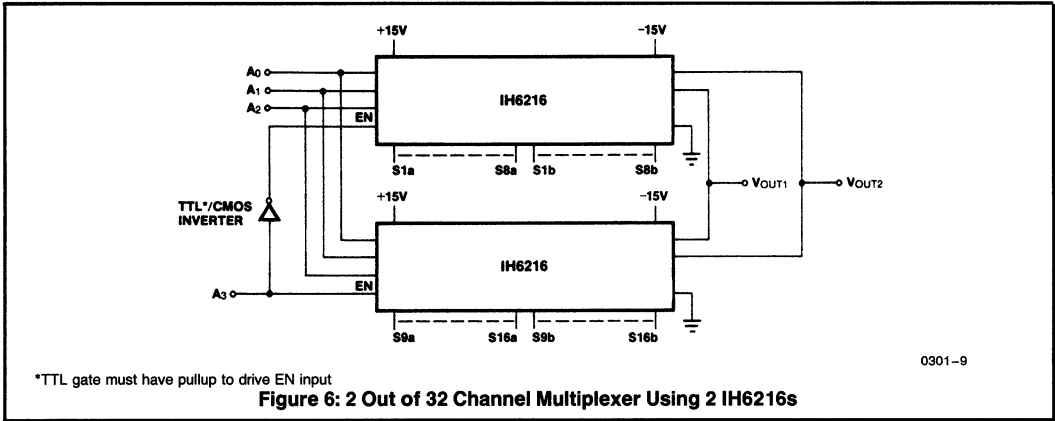
NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

IH6216 APPLICATIONS



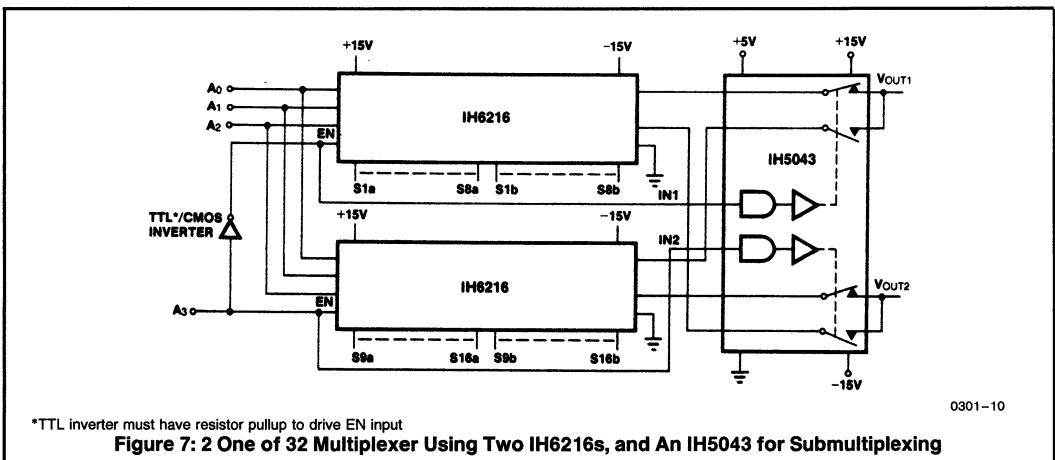
DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	On Switch	
0	0	0	0	S1a	V _{OUT1}
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	On Switch	
0	0	0	0	S1b	V _{OUT2}
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

9



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NOTE: All typical values have been characterized but are not tested.

General note on expandability of IH6216

The IH6216 is a two tier multiplexer, where 8 pairs of input channels are routed to a pair of outputs in blocks of 4. Each block of 4 input channels is routed to one common output channel, and thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs with the 4 outputs tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantages of this are lower output capacitance and leakage than would be possible using a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 6, 7, and 8 show how the IH6216 is expanded.

Figure 6 shows a 2 of 32 multiplexer, using 2 IH6216s. Since the 6216 is itself a 2 tier MUX, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the ENable input strobe is used as the A₃ input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 3 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 I_{D(on)} plus 3 I_{D(off)} or about 0.4nA at room temperature. Throughput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}, with throughput channel resistance in the 500Ω area.

DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	On Switch	
0	0	0	0	S1a	V _{OUT1}
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	On Switch	
0	0	0	0	S1b	V _{OUT2}
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

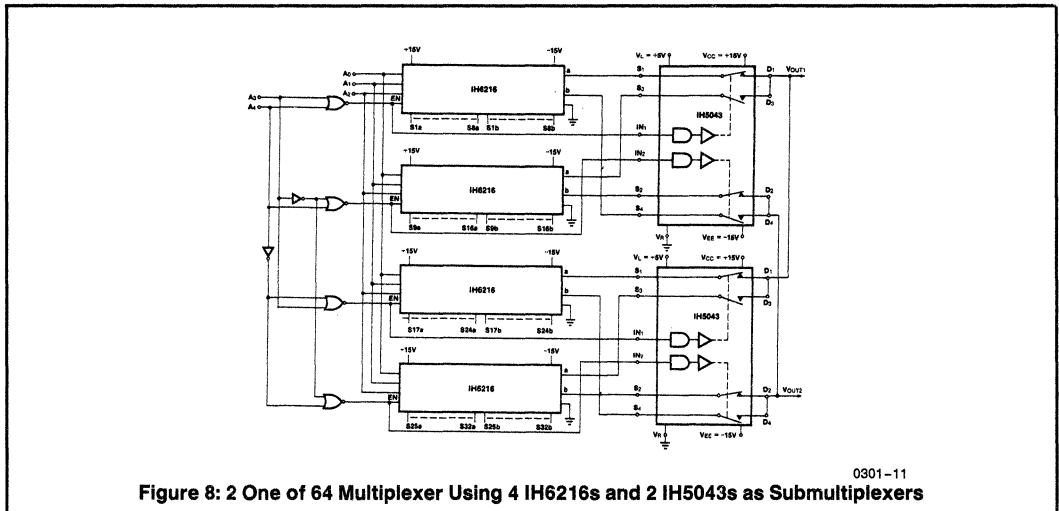


Figure 8: 2 One of 64 Multiplexer Using 4 IH6216s and 2 IH5043s as Submultiplexers

0301-11

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NOTE: All typical values have been characterized but are not tested.

Figure 7 shows the 2 of 32 MUX of Figure 6, with a third tier of submultiplexing added to further reduce leakage and output capacitance. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases throughput channel resistance from the 500 ohms of Figure 6 to about 550 ohms for Figure 7. Throughput channel speed is a little slower by about $0.5\mu\text{s}$ for both ON and OFF time, and output leakage is about 0.2nA .

Figure 8 shows a 2 of 64 MUX using 3 tier MUXing (similar to Figure 7). The Intersil IH5043 is used for the third tier of MUXing. Each V_{out} point will see 3 OFF channels and 1 ON channel at anytime, so that the typical leakages will be about 0.4nA . Throughput channel resistance will be in the 550Ω area and throughput switching speeds about $1.3\mu\text{s}$ for ON time and $0.8\mu\text{s}$ for OFF time.

The IH5043 was chosen as the third tier of the MUX because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically $1\text{--}2\mu\text{A}$ so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 6 and 7 show the EN pin used as the A_3 input.

For the system to function properly the EN input (pin 18) must go to $5\text{V} \pm 5\%$ for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up of $1\text{k}\Omega$ or less resistor should be used to pull the output voltage up to 5V. When using CMOS logic, the high state goes to the power supply so no pull-up is required.

If used on high voltage logic supplies, EN should be at least 0.7V below V^+ at all times. See IH6208 data sheet for details.

APPLICATION NOTES

Further information may be found in:

- A003** "Understanding and Applying the Analog Switch"
- A006** "A New CMOS Analog Gate Technology"
- A020** "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"
- R009** "Reduce CMOS Multiplexer Troubles Through Proper Device Selection"

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of this fact, the $r_{\text{DS(ON)}}$ of the switch is maintained at specified values.

IH9108

8-Channel High-Voltage Multiplexer with Latches



GENERAL DESCRIPTION

The IH9108 is an 8-channel multiplexer with latches designed for high voltage ($\pm 50V$) applications in microprocessor based instrumentation and process control systems. The multiplexer features true bi-directional switch action over the full analog signal range. Interfacing with microprocessors is simplified by on-board data latches and control pins.

The IH9108 utilizes D/CMOS junction isolation technology providing high breakdown voltage ($> 120V$). In addition, the IH9108 features low ON resistance (35Ω typ) and extremely low leakages (0.5 nA typ). The multiplexer provides 8-channel single-ended multiplexing and demultiplexing. Individual channels are selected by addressing appropriate data latches with binary coded inputs (A_0 , A_1 and A_2). Switch state inputs are stored or cleared via write \overline{WR} and device reset \overline{RS} respectively. During system power-up or reset, switch turn-off is simplified by \overline{RS} . The IH9108 is available over the commercial ($0^\circ C$ to $70^\circ C$), Industrial ($-25^\circ C$ to $85^\circ C$) and Military ($-55^\circ C$ to $125^\circ C$) temperature range in 18 pin sidebrazed package.

FEATURES

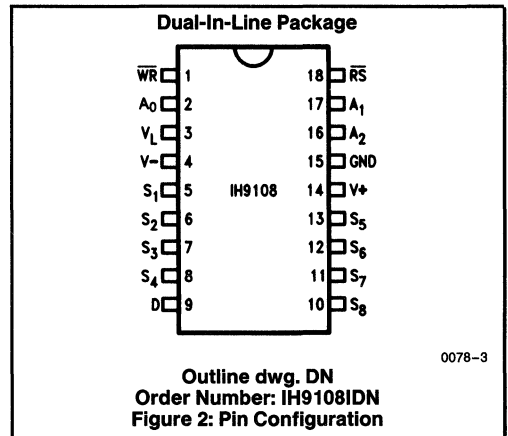
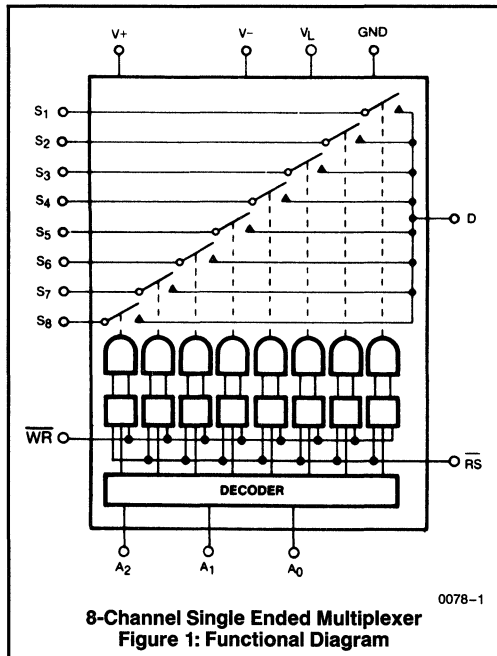
- Low Leakage Current
- $\pm 50V$ Analog Signal Range
- Low ON Resistance
- Latchable Logic Inputs
- Direct Reset (\overline{RS})

APPLICATIONS

- Automatic Test Equipment
- Ultrasound Medical Equipment
- Microprocessor Controlled Systems
- Communications Systems
- Data Acquisition

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH9108CDN	$0^\circ C$ to $70^\circ C$	Sidebrazed 18-pin
IH9108IDN	$-25^\circ C$ to $85^\circ C$	Sidebrazed 18-pin
IH9108MDN	$-55^\circ C$ to $125^\circ C$	Sidebrazed 18-pin



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V+	+62V
V-	-62V
Digital Inputs	-0.3V to V _L +0.3V
Continuous Current S or D30 mA
Peak Current, S or D (Note 1)	100 mA
Operating Temperature		
(C Version)	0°C to 70°C
(I Version)	-25°C to 85°C
(M Version)	-55°C to 125°C

Storage Temperature -55°C to 125°C
 Power Dissipation (Package*) 250 mW

*All leads soldered or welded to PC board.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Commercial and Industrial Grade

Parameter	Symbol	Test Conditions (unless otherwise noted) V ⁺ = 60V, V ⁻ = -60V, GND = V _{WR} = 0 V _L = V _{RS} = 15V, T _A = 25°C		Limits			Units
				Min	Typ (Note 3)	Max	
MULTIPLEXER							
Analog Signal Range	V _{analog}			-50		+50	V
Drain-Source ON Resistance	r _{DS(ON)}	V _D = -50V, I _S = 10 mA -10V ≤ V _D ≤ +10V, I _S = 10 mA V _D = +50V, I _S = 10 mA			25 35 95	35 50 120	Ω
Source OFF Leakage Current	I _{S(OFF)}	See Fig. 5 V _D = -50V, V _S = +50V			0.5	5	nA
Drain OFF Leakage Current	I _{D(OFF)}	See Fig. 6 V _S = -50V, V _D = +50V			5	25	
Drain ON Leakage Current	I _{D(ON)}	See Fig. 7 V _S = -50V, V _D = +50V			5	20	
INPUT							
Input Current/Input Low	I _{INL}	V _{IN} = 0V (Note 2)			0.1	2	μA
Input Current/Input High	I _{INH}	V _{IN} = 15V (Note 2)			0.1	2	
DYNAMIC							
Turn-ON Time	t _{ON}	R _L = 5K, C _L = 10 pF	See Fig. 3		1	2	μS
Turn-OFF Time	t _{OFF}	V _S = ±50V	See Fig. 3		0.5	1	
Break-Before-Make Interval	t _{OPEN}	Fig. 8	See Fig. 4		25		ns
Address Access Time	t _A	See Fig. 3			100		ns
Address Hold Time	t _H	See Fig. 3 t _{WR} = 500 ns			300		
Reset Pulse Width	t _{RS}	See Fig. 3			100		
Write Pulse Width	t _{WR}	See Fig. 3			300		
Source OFF Capacitance	C _{S(OFF)}	V _S = 0V	f = 50 kHz		14		pF
Drain OFF Capacitance	C _{D(OFF)}	V _D = 0V			85		
Channel ON Capacitance	C _{D+S(ON)}	V _S = 0V			110		
OFF Isolation	OIRR	V _{RS} = 0V, R _L = 2k, C _L = 3 pF V _{analog} = 10 V _{p-p} , f = 100 kHz			65		dB
SUPPLY							
Positive Supply Current	I ⁺	V _{IN(all)} = 0 or 15V (Note 2)			0.002	2	μA
Negative Supply Current	I ⁻				0.003	2	
Logic Supply Current	I _L				0.002	2	

NOTE 1: Pulsed at 1 mS, 10% duty cycle.

2: Inputs are digital inputs (A₀, A₁, A₂, RS and WR).

3: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS Military Grade

Parameter	Symbol	Test Conditions (unless otherwise noted) $V^+ = 60V, V^- = -60V, GND = \overline{V_{WR}} = 0$ $V_L = \overline{V_{RS}} = 15V, T_A = 25^\circ C$	Limits			Units
			Min	Typ (Note 3)	Max	
MULTIPLEXER						
Analog Signal Range	V_{analog}		-50		+50	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$V_D = -50V, I_S = 10\text{ mA}$ $-10V \leq V_D \leq +10V, I_S = 10\text{ mA}$ $V_D = +50V, I_S = 10\text{ mA}$		25 35 75	35 50 120	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	See Fig. 5 $V_D = -50V, V_S = +50V$		0.5	2	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	See Fig. 6 $V_S = -50V, V_D = +50V$		5	15	
Drain ON Leakage Current	$I_{D(ON)}$	See Fig. 7 $V_S = -50V, V_D = +50V$		5	15	
INPUT						
Input Current/Input Low	I_{INL}	$V_{IN} = 0V$ (Note 2)		0.1	1	μA
Input Current/Input High	I_{INH}	$V_{IN} = 15V$ (Note 2)		0.1	1	
DYNAMIC						
Turn-ON Time	t_{ON}	$R_L = 5K, C_L = 10\text{ pF}$	See Fig. 3	1	2	μS
Turn-OFF Time	t_{OFF}	$V_S = \pm 50V$	See Fig. 3	0.5	1	μS
Break-Before-Make Interval	t_{OPEN}	Fig. 8	See Fig. 4	25		ns
Address Access Time	t_A	See Fig. 3		100		
Address Hold Time	t_H	See Fig. 3 $t_{\overline{WR}} = 500\text{ ns}$		300		
Reset Pulse Width	$t_{\overline{RS}}$	See Fig. 3		100		ns
Write Pulse Width	$t_{\overline{WR}}$	See Fig. 3		300		
Source OFF Capacitance	$C_{S(OFF)}$	$V_S = 0V$	$f = 50\text{ kHz}$	14		pF
Drain OFF Capacitance	$C_{D(OFF)}$	$V_D = 0V$		85		
Channel ON Capacitance	$C_{D+S(ON)}$	$V_S = 0V$		110		
OFF Isolation	OIRR	$\overline{V_{RS}} = 0V, R_L = 2k, C_L = 3\text{ pF}$ $V_{analog} = 10\text{ V}_{p-p}, f = 100\text{ kHz}$		65		dB
SUPPLY						
Positive Supply Current	I^+	$V_{IN(all)} = 0\text{ or }15V$ (Note 2)		0.002	1	μA
Negative Supply Current	I^-			0.003	1	
Logic Supply Current	I_L			0.002	1	

NOTE 1: Pulsed at 1 mS, 10% duty cycle.

2: Inputs are digital inputs ($A_0, A_1, A_2, \overline{RS}$ and \overline{WR}).

3: Typical values are not 100% tested, and are for design aid only.

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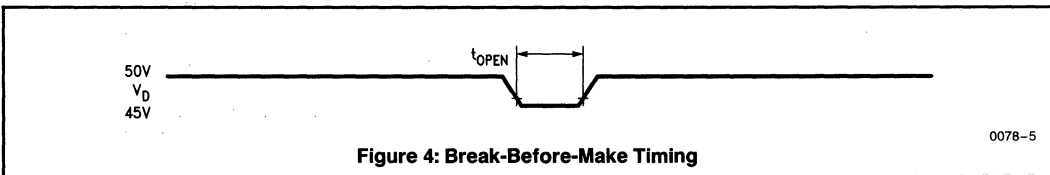
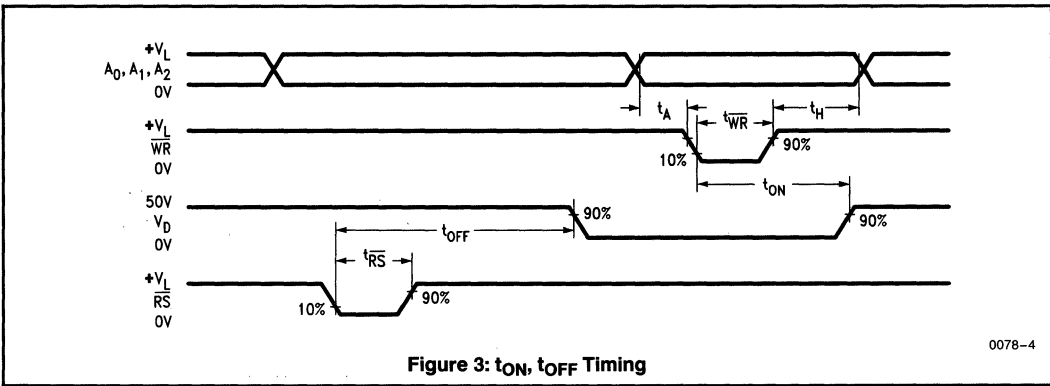
NOTE: All typical values have been characterized but are not tested.

TRUTH TABLE

A ₂	A ₁	A ₀	WR	RS	ON Switch	Latch Condition
X	X	X	X	0	None	
X	X	X		1	Maintains previous switch condition	Latches Address
X	X	X	1		None	Latches Reset
X	X	X		1	One of eight switches	Unlatches Reset
X	X	X				Not Allowed
0	0	0	0	1	1	
0	0	1	0	1	2	
0	1	0	0	1	3	
0	1	1	0	1	4	
1	0	0	0	1	5	
1	0	1	0	1	6	
1	1	0	0	1	7	
1	1	1	0	1	8	

Logic "1": $V_{IN} \geq 0.7 (V_L)$ Logic "0": $V_{IN} \leq 1.0V$ 0078-10

TIMING DIAGRAMS



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NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS

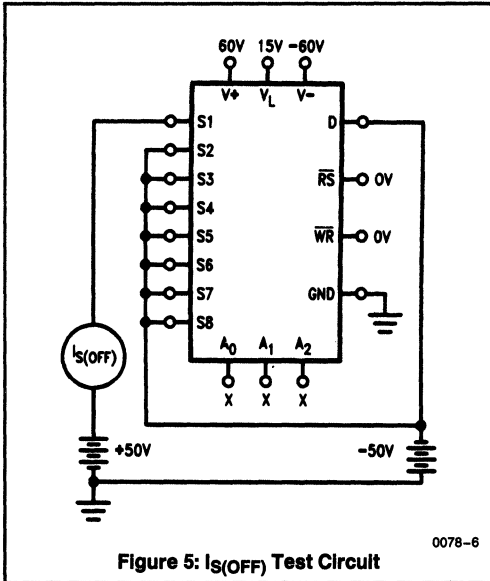


Figure 5: $I_{S(OFF)}$ Test Circuit

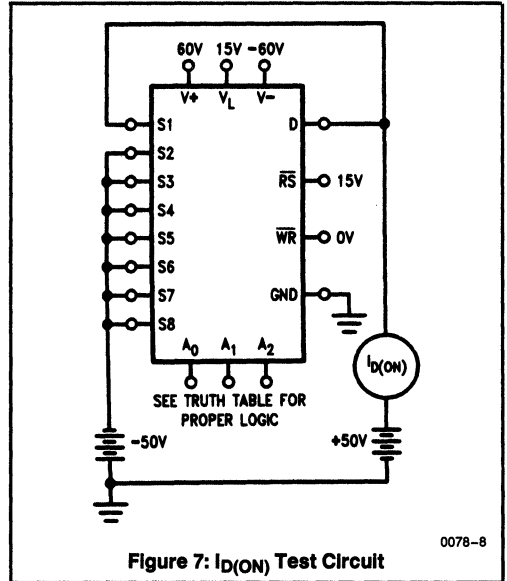


Figure 7: $I_{D(ON)}$ Test Circuit

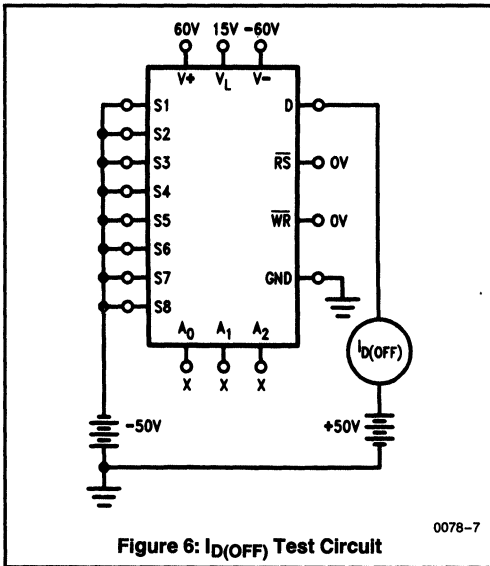


Figure 6: $I_{D(OFF)}$ Test Circuit

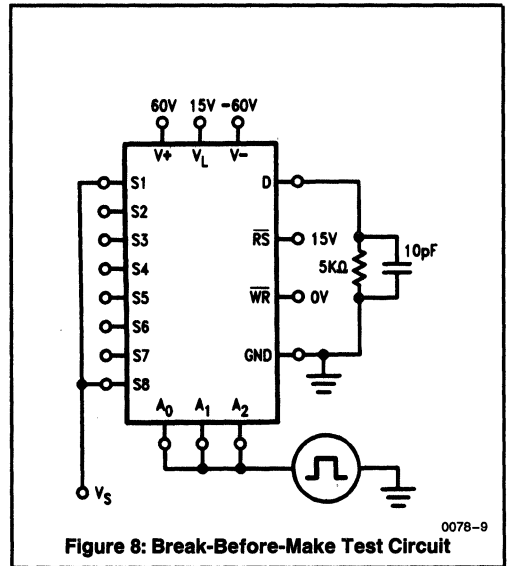


Figure 8: Break-Before-Make Test Circuit

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NOTE: All typical values have been characterized but are not tested.

Section 10 — Discretes

2N2607	10-1	2N4879	10-16	2N4859	10-30
2N2608	10-1	2N4880	10-16	2N4859JAN,JTX,JTXV	10-30
2N2609	10-1	2N4091JANTX	10-19	2N4860	10-30
2N2609JAN	10-1	2N4091	10-19	2N4860JAN,JTX,JTXV	10-30
2N3684	10-2	2N4092JANTX	10-19	2N4861	10-30
2N3685	10-2	2N4092	10-19	2N4861JAN,JTX,JTXV	10-30
2N3686	10-2	2N4093JANTX	10-19	2N4867/A	10-32
2N3687	10-2	2N4093	10-19	2N4868/A	10-32
2N3810/A	10-3	ITE4091	10-19	2N4869/A	10-32
2N3811/A	10-3	ITE4092	10-19	2N5018	10-33
2N3821	10-5	ITE4093	10-19	2N5019	10-33
2N3821JAN	10-5	2N4117	10-21	2N5114	10-35
2N3821JTX	10-5	2N4117A	10-21	2N5114JAN,JTX,JTXV	10-35
2N3821JTXV	10-5	2N4118	10-21	2N5115	10-35
2N3822	10-5	2N4118A	10-21	2N5115JAN,JTX,JTXV	10-35
2N3822JAN	10-5	2N4119	10-21	2N5116	10-35
2N3822JTX	10-5	2N4119A	10-21	2N5116JAN,JTX,JTXV	10-35
2N3822JTXV	10-5	2N4220	10-22	2N5117	10-37
2N3823	10-7	2N4221	10-22	2N5118	10-37
2N3823JAN	10-7	2N4222	10-22	2N5119	10-37
2N3823JTX	10-7	2N4223	10-23	2N5196	10-39
2N3823JTXV	10-7	2N4224	10-23	2N5197	10-39
2N3824	10-8	2N4338	10-24	2N5198	10-39
2N3921	10-9	2N4339	10-24	2N5199	10-39
2N3922	10-9	2N4340	10-24	2N5397	10-41
2N3954	10-11	2N4341	10-24	2N5398	10-41
2N3954A	10-11	2N4351	10-25	2N5432	10-43
2N3955	10-11	2N4391	10-26	2N5433	10-43
2N3955A	10-11	2N4392	10-26	2N5434	10-43
2N3956	10-11	2N4393	10-26	2N5452	10-45
2N3957	10-11	ITE4391	10-26	2N5453	10-45
2N3958	10-11	ITE4392	10-26	2N5454	10-45
2N3970	10-13	ITE4393	10-26	2N5457	10-47
2N3971	10-13	2N4416/A	10-28	2N5458	10-47
2N3972	10-13	ITE4416	10-28	2N5459	10-47
2N3993	10-15	2N4856	10-30	2N5460	10-48
2N3994	10-15	2N4856JAN,JTX,JTXV	10-30	2N5461	10-48
2N4044	10-16	2N4857	10-30	2N5462	10-48
2N4045	10-16	2N4857JAN,JTX,JTXV	10-30	2N5463	10-48
2N4100	10-16	2N4858	10-30	2N5464	10-48
2N4878	10-16	2N4858JAN,JTX,JTXV	10-30	2N5465	10-48

Section 10 — Discretes (Continued)

2N5484	10-50	3N189	10-71	J176	10-92
2N5485	10-50	3N190	10-71	J177	10-92
2N5486	10-50	3N191	10-71	J201	10-94
2N5515	10-52	ID100	10-73	J202	10-94
2N5516	10-52	ID101	10-73	J203	10-94
2N5517	10-52	IT100	10-75	J204	10-94
2N5518	10-52	IT101	10-75	J308	10-95
2N5519	10-52	IT120	10-76	J309	10-95
2N5520	10-52	IT120A	10-76	J310	10-95
2N5521	10-52	IT121	10-76	LM114/H	10-97
2N5522	10-52	IT122	10-76	LM114A/AH	10-97
2N5523	10-52	IT126	10-78	M116	10-99
2N5524	10-52	IT127	10-78	U200	10-100
2N5638	10-54	IT128	10-78	U201	10-100
2N5639	10-54	IT129	10-78	U202	10-100
2N5640	10-54	IT130	10-80	U231	10-101
2N5902	10-56	IT130A	10-80	U232	10-101
2N5903	10-56	IT131	10-80	U233	10-101
2N5904	10-56	IT132	10-80	U234	10-101
2N5905	10-56	IT136	10-82	U235	10-101
2N5906	10-56	IT137	10-82	U257	10-103
2N5907	10-56	IT138	10-82	U304	10-104
2N5908	10-56	IT139	10-82	U305	10-104
2N5909	10-56	IT500	10-84	U306	10-104
2N5911	10-58	IT501	10-84	U308	10-106
2N5912	10-58	IT502	10-84	U309	10-106
IT5911	10-58	IT503	10-84	U310	10-106
IT5912	10-58	IT504	10-84	U401	10-108
ITC5911	10-58	IT505	10-84	U402	10-108
ITC5912	10-58	IT1700	10-87	U403	10-108
2N6483	10-60	IT1750	10-88	U404	10-108
2N6484	10-60	J105	10-89	U405	10-108
2N6485	10-60	J106	10-89	U406	10-108
3N161	10-62	J107	10-89	U1897	10-110
3N163	10-63	J108	10-90	U1898	10-110
3N164	10-63	J109	10-90	U1899	10-110
3N165	10-65	J110	10-90	VCR2N	10-112
3N166	10-65	J111	10-91	VCR3P	10-112
3N170	10-67	J112	10-91	VCR4N	10-112
3N171	10-67	J113	10-91	VCR5P	10-112
3N172	10-69	J174	10-92	VCR7N	10-112
3N173	10-69	J175	10-92	VCR11B	10-115
3N188	10-71				

2N2607-2N2609

P-Channel JFET

General Purpose Amplifier

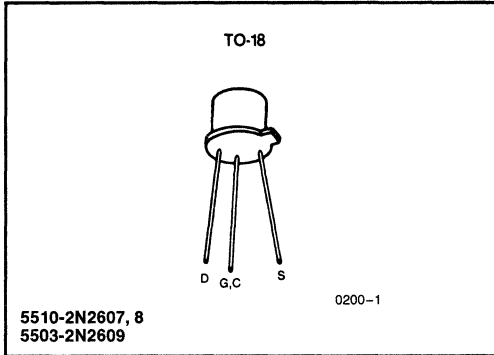


2N2607-2N2609

APPLICATIONS

- Low-Level Choppers
- Data Switches
- Commutators

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source Voltage 30V
Gate-Drain Voltage 30V
Gate Current 50mA
Storage Temperature Range -65°C to $+200^\circ\text{C}$
Operating Temperature Range -55°C to $+175^\circ\text{C}$
Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$
Power Dissipation 300mW
Derate above 25°C $2\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
2N2607
2N2608
2N2609

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N2607		2N2608		2N2609		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = 30\text{V}, V_{DS} = 0$		3		10		30	nA
		$V_{GS} = 5\text{V}, V_{DS} = 0, T_A = 150^\circ\text{C}$		3		10		30	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu\text{A}, V_{DS} = 0$	30		30		30		V
V_P	Gate-Source Pinch-Off Voltage	$V_{DS} = -5\text{V}, I_D = -1\mu\text{A}$	1	4	1	4	1	4	V
I_{DSS}	Drain Current at Zero Gate Voltage	$V_{DS} = -5\text{V}, V_{GS} = 0$	-0.30	-1.50	-0.90	-4.50	-2	-10	mA
g_{fs}	Small-Signal Common-Source Forward Transconductance	$V_{DS} = -5\text{V}, V_{GS} = 0, f = 1\text{kHz}$	330		1000		2500		μS
C_{iss}	Common-Source Input Capacitance	$V_{DS} = -5\text{V}, V_{GS} = 1\text{V}, f = 1\text{MHz}$ (Note 1)		10		17		30	pF
NF	Noise Figure (Note 1)	$V_{DS} = -5\text{V}, V_{GS} = 0, f = 1\text{kHz}$		3					dB
		$R_G = 10\text{M}\Omega$							
		$R_G = 1\text{M}\Omega$				3		3	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3684-2N3687

N-Channel JFET

Low Noise Amplifier



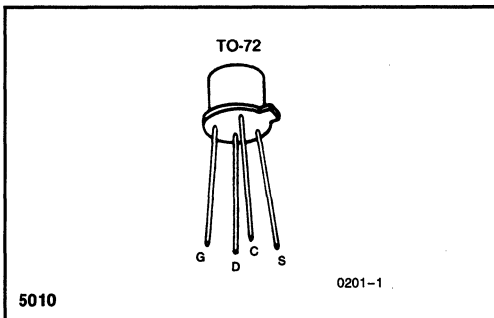
FEATURES

- Low Noise
- High Input Impedance
- Low Capacitance

APPLICATIONS

- Low Level Choppers
- Data Switches
- Multiplexers
- Low Noise Amplifiers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N3684
2N3685
2N3686
2N3687

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	2N3684		2N3685		2N3686		2N3687		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
BV _{GSS}	Gate to Source Breakdown Voltage	V _{DS} = 0, I _G = 1.0μA	-50		-50		-50		-50		V
V _P	Pinch-Off Voltage	V _{DS} = 20V, I _D = 0.001μA	-2.0	-5.0	-1.0	-3.5	-0.6	-2.0	-0.3	-1.2	
I _{GSS}	Gate Leakage Current	V _{GS} = -30V, V _{DS} = 0		-0.1		-0.1		-0.1		-0.1	nA
		T _A = 150°C		-0.5		-0.5		-0.5		-0.5	μA
I _{DSS}	Saturation Current, Drain-to-Source	V _{GS} = 0, V _{DS} = 20V	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA
Y _{fs}	Forward Transadmittance	V _{DS} = 20V, V _{GS} = 0	2000	3000	1500	2500	1000	2000	500	1500	μS
G _{os}	Common Source Output Conductance	f = 1kHz		50		25		10		5	μS
C _{iss}	Common Source Input Capacitance	V _{DS} = 20V, V _{GS} = 0		4.0		4.0		4.0		4.0	pF
C _{rss}	Common Source Short Circuit Reverse Transfer Capacitance	f = 1MHz (Note 1)		1.2		1.2		1.2		1.2	pF
r _{DS(on)}	On Resistance	V _{DS} = 0, V _{GS} = 0		600		800		1200		2400	ohms
NF	Noise Figure (Note 1)	f = 100Hz, R _G = 10MΩ, NBW = 6Hz, V _{DS} = 10V, V _{GS} = 0V		0.5		0.5		0.5		0.5	dB

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3810/A, 2N3811/A

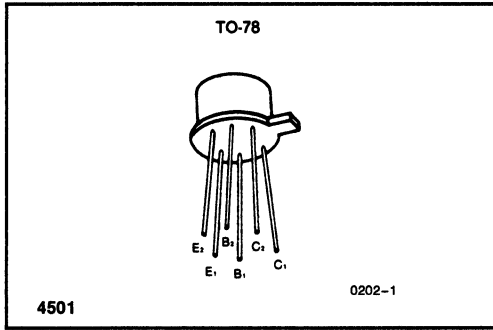
Monolithic Dual Matched PNP

General Purpose Amplifier



2N3810/A, 2N3811/A

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Emitter-Base Voltage (Note 1) -5V
 Collector-Base or Collector-Emitter Voltage
 (Note 1) -60V
 Collector Current (Note 1) 50mA
 Storage Temperature Range -65°C to $+175^\circ\text{C}$
 Operating Temperature Range -55°C to $+175^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation ..	500mW	600mW
Derate above 25°C	$3.3\text{mW}/^\circ\text{C}$	$4.0\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-78
2N3810
2N3810A
2N3811
2N3811A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3810/A		2N3811/A		Units
			Min	Max	Min	Max	
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = -10\mu\text{A}, I_E = 0$	-60		-60		V
BV_{CEO}	Collector-Emitter Breakdown Voltage (Note 2)	$I_C = -10\text{mA}, I_B = 0$	-60		-60		
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -10\mu\text{A}, I_C = 0$	-5		-5		
$I_{C(off)}$	Collector Cutoff Current	$V_{CB} = -50\text{V}, I_E = 0$		-10	-10	nA	
			$T_A = +150^\circ\text{C}$		-10	-10	μA
$I_{E(off)}$	Emitter Cutoff Current	$V_{BE} = 4\text{V}, I_C = 0$		-20	-20	nA	
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -5\text{V}$	$I_C = -10\mu\text{A}$	100		225	
			$I_C = -100\mu\text{A}$ to -1mA	150	450	300	900
			$I_C = 10\text{mA}$ (Note 2)	125		250	
			$I_C = 100\mu\text{A}, T_A = -55^\circ\text{C}$	75		150	

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NOTE: All typical values have been characterized but are not tested.

2N3810/A, 2N3811/A



ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3810/A		2N3811/A		Units	
			Min	Max	Min	Max		
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = -100\mu\text{A}, I_B = -10\mu\text{A}$		-0.7		-0.7	V	
		$I_C = -1.0\text{mA}, I_B = -100\mu\text{A}$		-0.8		-0.8		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 2)	$I_B = -10\mu\text{A}, I_C = -100\mu\text{A}$		-0.2		-0.2	V	
		$I_B = -100\mu\text{A}, I_C = -1\text{mA}$		-0.25		-0.25		
h_{ie}	Input Impedance (Note 4)	$V_{CE} = -10\text{V}$	3	30	10	40	$k\Omega$	
h_{fe}	Forward Current Transfer Ratio (Note 4)	$I_C = -1\text{mA}$	150	600	300	900		
h_{re}	Reverse Voltage Transfer Ratio (Note 4)	$f = 1\text{kHz}$		0.25		0.25		
h_{oe}	Output Admittance (Note 4)		5	60	5	60		μs
$ h_{fe} $	Magnitude of small signal current gain (Note 4)	$V_{CE} = -5\text{V}$	$I_C = -1\text{mA}, f = 100\text{MHz}$	1	5	1	5	
			$I_C = -500\mu\text{A}, f = 30\text{MHz}$	1		1		
C_{obo}	Output Capacitance (Note 4)	$V_{CB} = -5\text{V}, I_E = 0, f = 1\text{MHz}$		4		4	pF	
C_{ibo}	Input Capacitance (Note 4)	$V_{CB} = -0.5\text{V}, I_C = 0, f = 1\text{MHz}$		8		8		
h_{FE1}/h_{FE2}	DC Current Gain Ratio	$V_{CE} = -5\text{V}, I_C = 100\mu\text{A}$		0.9	1.0	0.9	1.0	
			A devices	0.95	1.0	0.95	1.0	
$ V_{BE1} - V_{BE2} $	Base-Emitter Voltage Differential	$V_{CE} = -5\text{V}$	$I_C = 10\mu\text{A}$ to 10mA		-5		-5	mV
				A devices		-2.5		
			$I_C = 100\mu\text{A}$		-3		-3	
				A devices		-1.5		
$\frac{\Delta V_{BE1} - V_{BE2}}{\Delta T}$	Base-Emitter Voltage Differential Gradient	$V_{CE} = -5, I_C = 100\mu\text{A}$		10		10	$\mu\text{V}/^\circ\text{C}$	
			A devices		5			5
NF	Spot Noise Figure (Note 4)	$V_{CE} = -10\text{V}, I_C = -100\mu\text{A}, R_G = 3k\Omega, f = 100\text{Hz}, \text{Noise Bandwidth} = 20\text{Hz}$		7		4	dB	
		$V_{CE} = -10\text{V}, I_C = -100\mu\text{A}, R_G = 3k\Omega, f = 1\text{kHz}, \text{Noise Bandwidth} = 200\text{kHz}$		3		1.5		
		$V_{CE} = -10\text{V}, I_C = -100\mu\text{A}, R_G = 3k\Omega, f = 10\text{kHz}, \text{Noise Bandwidth} = 2\text{kHz}$		2.5		1.5		
		$V_{CE} = -10\text{V}, I_C = -100\mu\text{A}, R_G = 3k\Omega, \text{Noise Bandwidth} = 15.7\text{kHz}$ (Note 3)		3.5		2.5		

- NOTES: 1. Per transistor.
 2. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2.0\%$.
 3. 3dB down at 10Hz and 10kHz.
 4. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3821, 2N3822, JAN, JTX, JTXV

N-Channel JFET High Frequency Amplifier

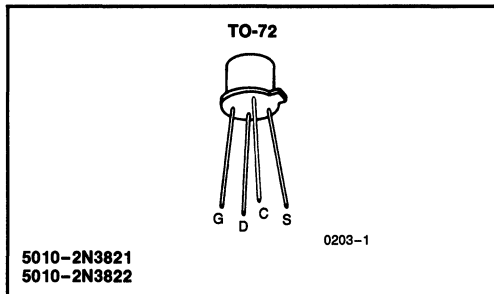


2N3821, 2N3822, JAN, JTX, JTXV

FEATURES

- Low Capacitance
- Up to 6500 μ s Transconductance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source Voltage	-50V
Gate-Drain Voltage	-50V
Gate Current	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N3821
2N3822

† add JAN, JTX, JTXV to basic part number to specify these devices.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3821		2N3822		Units
			Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-0.1		-0.1	nA
				-0.1		-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-50		-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.5\text{nA}$		-4		-6	
V_{GS}	Gate-Source Voltage	$V_{DS} = 15V, I_D = 50\mu\text{A}$	-0.5	-2			
		$V_{DS} = 15V, I_D = 200\mu\text{A}$			-1	-4	
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	0.5	2.5	2	10	mA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3821		2N3822		Units	
			Min	Max	Min	Max		
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	f = 1kHz	1500	4500	3000	6500	μs
$ y_{fs} $	Common-Source Forward Transadmittance (Note 2)			f = 100MHz	1500		3000	
g_{os}	Common-Source Output Conductance (Note 1)		f = 1kHz		10		20	
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz		6		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				3		3	
NF	Noise Figure (Note 2)	$V_{DS} = 15V, V_{GS} = 0,$ $R_{gen} = 1\text{meg}, BW = 5\text{Hz}$	f = 10Hz		5		5	dB
\bar{e}_n	Equivalent Input Noise Voltage (Note 2)	$V_{DS} = 15V, V_{GS} = 0,$ $BW = 5\text{Hz}$			200		200	$\frac{nV}{\sqrt{Hz}}$

NOTES: 1. These parameters are measured during a 2ms interval 100ms after DC power is applied.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3823, JAN, JTX, JTXV

N-Channel JFET

High Frequency Amplifier

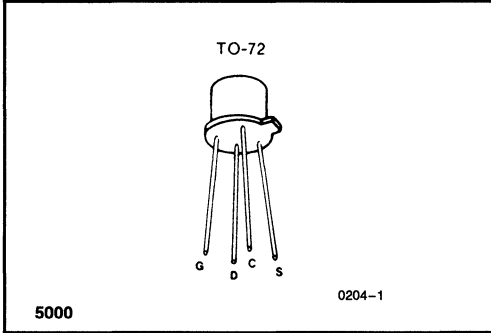


2N3823, JAN, JTX, JTXV

FEATURES

- Low Noise
- Low Capacitance
- Transconductance Up to 6500 μ s

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N3823

† add JAN, JTX, JTXV to basic part number to specify these devices.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units	
I_{GSS}	Gate Reverse Current	$V_{GS} = -20V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-0.5	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-30		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.5nA$		-8		
V_{GS}	Gate-Source Voltage	$V_{DS} = 15V, I_D = 400\mu A$	-1.0	-7.5		
I_{DSS}	Saturation Drain Current	$V_{DS} = 15V, V_{GS} = 0$	4	20	mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	$f = 1\text{kHz}$	3,500	6,500	μ s
$ Y_{fs} $	Common-Source Forward Transadmittance (Note 2)		$f = 100\text{MHz}$	3,200		
g_{os}	Common-Source Output Conductance (Note 1)		$f = 1\text{kHz}$		35	
g_{iss}	Common-Source Input Conductance (Note 2)		$f = 200\text{MHz}$		800	
g_{oss}	Common-Source Output Conductance (Note 2)				200	pF
C_{iss}	Common-Source Input Capacitance (Note 2)		$f = 1\text{MHz}$		6	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)				2	
NF	Noise Figure (Note 2)		$V_{DS} = 15V, V_{GS} = 0$ $R_G = 1k\Omega$	$f = 100\text{MHz}$	2.5	dB

NOTES: 1. These parameters are measured during a 2ms interval 100ms after DC power is applied.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

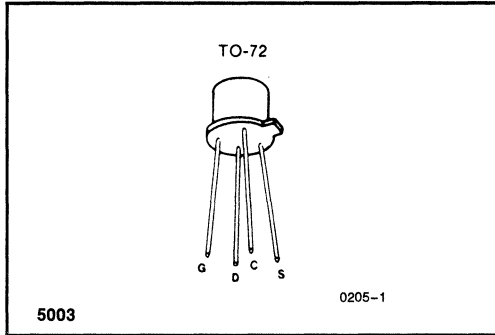
2N3824 N-Channel JFET Switch



FEATURES

- $r_{ds} < 250 \text{ Ohms}$
- $I_{D(off)} < 0.1 \text{ nA}$

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Load Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N3824

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-0.1	nA
				-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1 \mu\text{A}, V_{DS} = 0$	-50		V
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 15V, V_{GS} = -8V$ $T_A = 150^\circ\text{C}$		0.1	nA
				0.1	μA
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0V, I_D = 0$ $f = 1 \text{ kHz}$		250	Ω
C_{iss}	Common-Source Input Capacitance (Note 1)	$V_{DS} = 15V, V_{GS} = 0$ $f = 1 \text{ MHz}$		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)			3	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3921, 2N3922

Monolithic Dual N-Channel JFET

General Purpose Amplifier

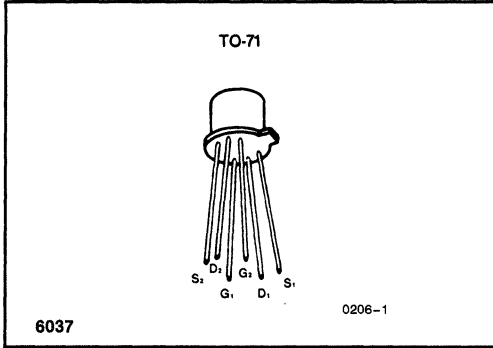


2N3921, 2N3922

FEATURES

- Low Drain Current
- High Output Impedance
- Matched V_{GS} , ΔV_{GS} , and g_{fs}

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate Current (Note 1)	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +200°C
Load Temperature (Soldering, 10sec)	+300°C
Total Power Dissipation	300mW
Derate above 25°C	1.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
2N3921
2N3922

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units	
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$		-1	nA	
		$T_A = 100^\circ\text{C}$		-1	μA	
BV_{DGO}	Drain-Gate Breakdown Voltage	$I_D = 1\mu\text{A}, I_S = 0$	50		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10V, I_D = 1\text{nA}$		-3		
V_{GS}	Gate-Source Voltage	$V_{DS} = 10V, I_D = 100\mu\text{A}$	-0.2	-2.7		
I_G	Gate Operating Current	$V_{DG} = 10V, I_D = 700\mu\text{A}$		-250	pA	
		$T_A = 100^\circ\text{C}$		-25	nA	
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 10V, V_{GS} = 0$	1	10	mA	
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 10V, V_{GS} = 0$	f = 1kHz	1500	7500	μs
g_{os}	Common-Source Output Conductance				35	
C_{iss}	Common-Source Input Capacitance (Note 3)	$V_{DS} = 10V, V_{GS} = 0$	f = 1MHz		18	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)				6	
g_{fs}	Common-Source Forward Transconductance	$V_{DG} = 10V, I_D = 700\mu\text{A}$	f = 1kHz	1500		μs
g_{oss}	Common-Source Output Conductance				20	
NF	Spot Noise Figure (Note 3)	$V_{DS} = 10V, V_{GS} = 0$	f = 1kHz, $R_G = 1\text{meg}\Omega$		2	dB

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NOTE: All typical values have been characterized but are not tested.

MATCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3921		2N3922		Units	
			Min	Max	Min	Max		
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 10\text{V}$, $I_D = 700\mu\text{A}$		5		5	mV	
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		$T_A = 0^\circ\text{C}$ $T_B = 100^\circ\text{C}$		10		25	$\mu\text{V}/^\circ\text{C}$
g_{fs1}/g_{fs2}	Transconductance Ratio		$f = 1\text{kHz}$	0.95	1.0	0.95	1.0	

NOTES: 1. Per transistor.

2. Pulse test duration = 2 ms.

3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3954-2N3958

2N3954A/2N3955A

Monolithic Dual N-Channel JFET

General Purpose Amplifier

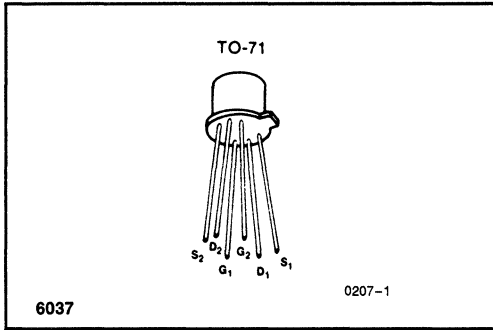


2N3954-2N3958 2N3954A/2N3955A

FEATURES

- Low Offset and Drift
- Low Capacitance
- Low Noise
- Superior Tracking Ability
- Low Output Conductance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	- 50V
Gate-to-Gate Voltage	$\pm 50\text{V}$
Gate Current	50mA
Total Device Dissipation 85°C (Each Side)	250mW
Case Temperature (Both Sides)	500mW
Power Derating (Each Side)	2.86mW/ $^\circ\text{C}$
(Both Sides)	4.3mW/ $^\circ\text{C}$
Storage Temperature Range	- 65°C to + 200°C
Lead Temperature ($1/16"$ from case for 10 seconds)	300 $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
2N3954
2N3954A
2N3955
2N3955A
2N3956
2N3957
2N3958

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -30\text{V}$, $V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-100		-100		-100		-100		-100		-100		-100	pA
				-500		-500		-500		-500		-500		-500		-500	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0$ $I_G = -1\mu\text{A}$	-50		-50		-50		-50		-50		-50		-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20\text{V}$, $I_D = 1\text{nA}$	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	
$V_{GS(f)}$	Gate-Source Forward Voltage	$V_{DS} = 0$ $I_G = 1\text{mA}$		2.0		2.0		2.0		2.0		2.0		2.0		2.0	
V_{GS}	Gate-Source Voltage	$V_{DS} = 20\text{V}$ $I_D = 50\mu\text{A}$		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2		-4.2	
			$I_D = 200\mu\text{A}$	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.4	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0
I_G	Gate Operating Current	$V_{DS} = 20\text{V}$, $I_D = 200\mu\text{A}$ $T_A = 125^\circ\text{C}$		-50		-50		-50		-50		-50		-50		-50	pA
				-250		-250		-250		-250		-250		-250		-250	nA

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NOTE: All typical values have been characterized but are not tested.

2N3954-2N3958 2N3954A/2N3955A



ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I_{DSS}	Saturation Drain Current	$V_{DS} = 20\text{V}$, $V_{GS} = 0$	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA
g_{fs}	Common-Source Forward Transconductance	$f = 1\text{kHz}$ (Note 2) $f = 200\text{MHz}$	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	μS
g_{os}	Common-Source Output Conductance	$V_{DS} = 20\text{V}$, $f = 1\text{kHz}$		35		35		35		35		35		35		35	
C_{iss}	Common-Source Input Capacitance (Note 2)	$V_{GS} = 0$, $f = 1\text{MHz}$		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF
C_{rss}	Common Source Reverse Transfer Capacitance (Note 2)			1.2		1.2		1.2		1.2		1.2		1.2		1.2	
C_{dgo}	Drain-Gate Capacitance (Note 2)	$V_{DG} = 10\text{V}$, $I_S = 0$		1.5		1.5		1.5		1.5		1.5		1.5		1.5	
NF	Common-Source Spot Noise Figure (Note 2)	$V_{DS} = 20\text{V}$, $V_{GS} = 0$, $R_G = 10\text{M}\Omega$, $f = 100\text{Hz}$		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB
$ I_{G1} - I_{G2} $	Differential Gate Current	$V_{DS} = 20\text{V}$, $I_D = 200\mu\text{A}$, $T = 125^\circ\text{C}$		10		10		10		10		10		10		10	nA
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	$V_{DS} = 20\text{V}$, $V_{GS} = 0$	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage			5.0		5.0		10.0		5.0		15		20		25	
	Gate-Source Differential	$T = 25^\circ\text{C}$ to -55°C		0.8		0.4		2.0		1.2		4.0		6.0		8.0	mV
$\Delta V_{GS1} - V_{GS2} $	Voltage Change With Temperature	$V_{DS} = 20\text{V}$, $I_D = 200\mu\text{A}$, $T = 25^\circ\text{C}$ to 125°C		1.0		0.5		2.5		1.5		5.0		7.5		10.0	
g_{fs1}/g_{fs2}	Transconductance Ratio	$f = 1\text{kHz}$	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0	

NOTES: 1. Per Transistor.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N3970-2N3972

N-Channel JFET Switch

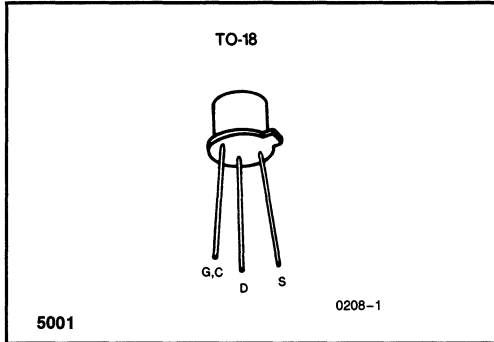


2N3970-2N3972

FEATURES

- Low $r_{DS(on)}$
- $I_{D(OFF)} < 250\text{pA}$
- Fast Switching

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +200°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation @ 25°C Case Temp.	1.8W
Derate above 25°C	10mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
2N3970
2N3971
2N3972

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N3970		2N3971		2N3972		Units	
			Min	Max	Min	Max	Min	Max		
BV_{GSS}	Gate Reverse Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-40		-40		-40		V	
I_{DGO}	Drain Reverse Current	$V_{DG} = 20\text{V}, I_S = 0$		250		250		250	pA	
$I_{D(off)}$	Drain Cutoff Current	$V_{DG} = 20\text{V}, V_{GS} = -12\text{V}$ $T_A = 150^\circ\text{C}$		500		500		500	nA	
				250		250		250	pA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$ $T_A = 150^\circ\text{C}$		500		500		500	nA	
				-4	-10	-2	-5	-0.5	-3	V
I_{DSS}	Saturation Drain Current (Pulse width 300 μs , duty cycle $\leq 3\%$)	$V_{DS} = 20\text{V}, V_{GS} = 0$	50	150	25	75	5	30	mA	
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0$	$I_D = 5\text{mA}$						2	V
			$I_D = 10\text{mA}$				1.5			
			$I_D = 20\text{mA}$		1					
$r_{DS(on)}$	Static Drain-Source ON Resistance	$V_{GS} = 0, I_D = 1\text{mA}$		30		60		100	Ω	
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0, I_D = 0$		30		60		100		
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0$ (Note 1)		25		25		25	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance	$V_{DS} = 0, V_{GS} = -12\text{V}$ (Note 1)		6		6		6		
t_d	Turn-On Delay Time (Note 1)	$V_{DD} = 10\text{V}, V_{GS(on)} = 0$ $I_{D(on)} \quad V_{GS(off)} \quad R_L$		10		15		40	ns	
t_r	Rise Time (Note 1)	2N3970 20mA -10V 450 Ω		10		15		40		
t_{off}	Turn-Off Time (Note 1)	2N3971 10mA -5V 850 Ω 2N3972 5mA -3V 1.6K Ω		30		60		100		

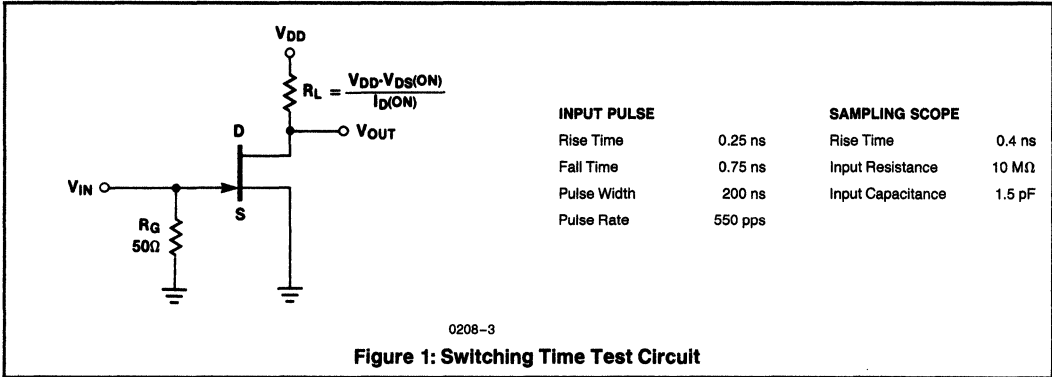
NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)



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NOTE: All typical values have been characterized but are not tested.

2N3993, 2N3994

P-Channel JFET

General Purpose Amplifier/Switch

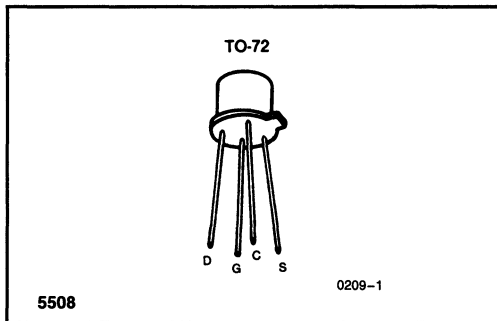


2N3993, 2N3994

FEATURES

- Low $r_{DS(on)}$
- High Y_{fs}/C_{iss} Ratio (High-Frequency Figure-of-Merit)

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N3993
2N3994

APPLICATIONS

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ± 10 VAC. Can be driven direct from TTL or CMOS logic.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions (Note 3)	2N3993		2N3994		Units
			Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu\text{A}$, $V_{DS} = 0$	25		25		V
I_{DGO}	Drain Reverse Current	$V_{DG} = -15\text{V}$, $I_S = 0$		-1.2		-1.2	nA
		$V_{DG} = -15\text{V}$, $I_S = 0$, $\theta_A = 150^\circ$		-1.2		-1.2	μA
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = -10\text{V}$, $V_{GS} = 0$, (See Note 1)	-10		-2		mA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = -10\text{V}$, $V_{GS} = 6\text{V}$				-1.2	nA
		$V_{DS} = -10\text{V}$, $V_{GS} = 6\text{V}$, $T_A = 150^\circ\text{C}$				-1	μA
		$V_{DS} = -10\text{V}$, $V_{GS} = 10\text{V}$		-1.2			nA
		$V_{DS} = -10\text{V}$, $V_{GS} = 10\text{V}$, $T_A = 150^\circ\text{C}$		-1			μA
$V_{GS(off)}$	Gate-Source Voltage	$V_{DS} = -10\text{V}$, $I_D = -1\mu\text{A}$	4	9.5	1	5.5	V
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	$V_{GS} = 0$, $I_D = 0$, $f = 1\text{kHz}$		150		300	Ω
$ Y_{fs} $	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = -10\text{V}$, $V_{GS} = 0$, $f = 1\text{kHz}$, (See Note 1)	6	12	4	10	μs
C_{iss}	Common-Source Short-Circuit Input Capacitance (Note 3)	$V_{DS} = -10\text{V}$, $V_{GS} = 0$, $f = 1\text{MHz}$, (See Note 2)		16		16	pF
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance (Note 3)	$V_{DS} = 0$, $V_{GS} = 6\text{V}$, $f = 1\text{MHz}$				5	pF
		$V_{DS} = 0$, $V_{GS} = 10\text{V}$, $f = 1\text{MHz}$		4.5			pF

- NOTES:** 1. These parameters must be measured using pulse techniques, $t_p = 100\text{ms}$, duty cycle $\leq 10\%$.
 2. This parameter must be measured with bias voltage applied for less than 5 seconds to avoid overheating.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

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2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

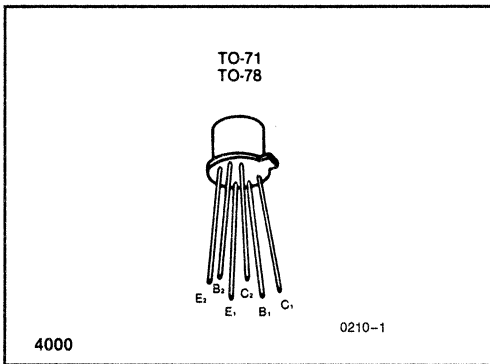
Dielectrically Isolated Monolithic Dual NPN General Purpose Amplifier



FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)	2N4044, 2N4878	60V
	2N4100, 2N4879	55V
	2N4045, 2N4880	45V
Collector-Collector Voltage		100V
Emitter Base Voltage (Note 2)		7V
Collector Current (Note 1)		10mA
Storage Temperature Range		-65°C to $+175^\circ\text{C}$
Operating Temperature Range		-55°C to $+175^\circ\text{C}$
Lead Temperature (Soldering, 10sec)		$+300^\circ\text{C}$

	TO-71		TO-78	
	One Side	Both Sides	One Side	Both Sides
Power Dissipation	200mW	400mW	250mW	500mW
Derate above 25°C (mW/ $^\circ\text{C}$)	1.3	2.7	1.7	3.3

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-78	TO-71
2N4044	2N4878
2N4045	2N4879
2N4100	2N4880

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		Units
			Min	Max	Min	Max	Min	Max	
h_{FE}	DC Current Gain	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$	200	600	150	600	80	800	
		$I_C = 1.0\text{mA}, V_{CE} = 5\text{V}$	225		175		100		
		$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$ $T_A = -55^\circ\text{C}$	75		50		30		
$V_{BE(on)}$	Emitter-Base On Voltage			0.7		0.7		0.7	V
$V_{CE(sat)}$	Collector Saturation Voltage	$I_C = 1.0\text{mA}, I_B = 0.1\text{mA}$		0.35		0.35		0.35	
I_{CBO}	Collector Cutoff Current	$I_E = 0, V_{CB} = 45\text{V}, 30\text{V}$		0.1		0.1		0.1	nA
		$T_A = 150^\circ\text{C}$		0.1		0.1		0.1	μA
I_{EBO}	Emitter Cutoff Current	$I_C = 0, V_{EB} = 5\text{V}$		0.1		0.1		0.1	nA
C_{obo}	Output Capacitance (Note 4)	$I_E = 0, V_{CB} = 5\text{V}, f = 1\text{MHz}$		0.8		0.8		0.8	pF

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NOTE: All typical values have been characterized but are not tested.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880



2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		Units
			Min	Max	Min	Max	Min	Max	
C_{te}	Emitter Transition Capacitance (Note 4)	$I_C = 0, V_{EB} = 0.5V, f = 1\text{MHz}$		1		1		1	pF
C_{C1}, C_{C2}	Collector to Collector Capacitance (Note 4)	$V_{CC} = 0, f = 1\text{MHz}$		0.8		0.8		0.8	pF
I_{C1}, I_{C2}	Collector to Collector Leakage Current	$V_{CC} = \pm 100V$		5		5		5	pA
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	$I_C = 1\text{mA}, I_B = 0$	60		55		45		V
f_t	Current Gain Bandwidth Product (Note 4)	$I_C = 1\text{mA}, V_{CE} = 10V$	200		150		150		MHz
f_t	Current Gain Bandwidth Product (Note 4)	$I_C = 10\mu\text{A}, V_{CE} = 10V$	20		15		15		MHz
NF	Narrow Band Noise Figure (Note 4)	$I_C = 10\mu\text{A}, V_{CE} = 5V$ $R_G = 10k\Omega$ $f = 1\text{kHz}$ $BW = 200\text{Hz}$		2		3		3	dB
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu\text{A}, I_E = 0$	60		55		45		V
BV_{EBO}	Emitter Base Breakdown Voltage (Note 2)	$I_E = 10\mu\text{A}, I_C = 0$	7		7		7		V

MATCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

h_{FE1}/h_{FE2}	DC Current Gain Ratio (Note 3)	$I_C = 10\mu\text{A}$ to 1mA , $V_{CE} = 5V$	0.9	1	0.85	1	0.8	1	
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential	$I_C = 10\mu\text{A}, V_{CE} = 5V$		3		5		5	mV
$ I_{B1} - I_{B2} $	Base Current Differential	$I_C = 10\mu\text{A}, V_{CE} = 5V$		5		10		25	nA
$ \Delta(V_{BE1} - V_{BE2}) /\Delta T$	Base Emitter Voltage Differential Change with Temperature	$I_C = 10\mu\text{A}$, $V_{CE} = 5V$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		3		5		10	$\mu\text{V}/^\circ\text{C}$
$ \Delta(I_{B1} - I_{B2}) /\Delta T$	Base Current Differential Change with Temperature			0.3		0.5		1	$\text{nA}/^\circ\text{C}$

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NOTE: All typical values have been characterized but are not tested.

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880



SMALL SIGNAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Typical Value	Units
h_{ib}	Input Resistance	$I_C = 1\text{mA}, V_{CB} = 5\text{V}$ (Note 4)	28	Ω
h_{rb}	Voltage Feedback Ratio		43	$\times 10^{-3}$
h_{fe}	Small Signal Current Gain	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$ (Note 4)	250	
h_{ob}	Output Conductance		60	μS
h_{ie}	Input Resistance		9.6	$\text{k}\Omega$
h_{re}	Voltage Feedback Ratio		42	$\times 10^{-3}$
h_{oe}	Output Conductance		12	μS

- NOTES: 1. Per transistor.
 2. The reverse base-emitter voltage must never exceed 7.0 volts and the reverse base-emitter current must never exceed $10\mu\text{A}$.
 3. The lowest of two h_{FE} readings is taken as h_{FE1} for purposes of this ratio.
 4. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N4091-2N4093 JAN, JANTX*, JTXV ITE4091-ITE4093 N-Channel JFET Switch

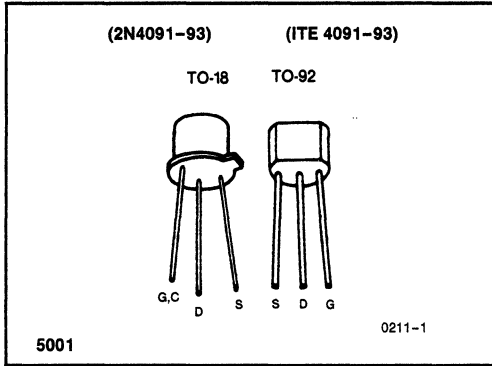


2N4091-2N4093 JAN, JANTX*, JTXV, ITE4091-ITE4093

FEATURES

- Low $r_{DS(on)}$
- $I_{D(OFF)} < 100\text{pA}$ (JAN TX Types)
- Fast Switching

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V	
Gate Current	10mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +200°C	
Lead Temperature (Soldering, 10sec)	+300°C	

	TO-18	TO-92
Power Dissipation	1.8W	360mW
Derate above 25°C	10mW/°C	3.3mW/°C

Plastic

Storage	-55°C to +150°C
Operating	-55°C to +135°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92	TO-18†
ITE 4091	2N4091
ITE 4092	2N4092
ITE 4093	2N4093

† add JANTX to these part numbers if JANTX processing is desired.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N/ITE 4091		2N/ITE 4092		2N/ITE 4093		Units
			Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-40		-40		-40		V
I_{DGO}	Drain Reverse Current (Not JANTX Specified)	$V_{DG} = 20\text{V}, I_S = 0$		200		200		200	pA
		$T_A = 150^\circ\text{C}$		400		400		400	nA
I_{GSS}	Gate Reverse Current (JANTX, ITE devices only)	$V_{GS} = -20\text{V}, V_{DS} = 0$		-100		-100		-100	pA
		$T_A = 150^\circ\text{C}$		-200		-200		-200	nA

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NOTE: All typical values have been characterized but are not tested.

2N4091-2N4093 JAN, JANTX*, JTXV, ITE4091-ITE4093



ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Test Conditions			2N/ITE 4091		2N/ITE 4092		2N/ITE 4093		Units
						Min	Max	Min	Max	Min	Max	
I _{D(OFF)}	Drain Cutoff Current	JANTX	V _{DS} = 20V	V _{GS} = -12V(4091) V _{GS} = -8V(4092) V _{GS} = -6V(4093)	T _A = 25°C		100		100		100	pA
		JAN, JTXV					200		200		200	
		JANTX			T _A = 150°C		200		200		200	
		JAN, JTXV					400		400		400	
V _P	Gate-Source Pinch-Off Voltage	V _{DS} = 20V, I _D = 1nA				-5	-10	-2	-7	-1	-5	V
I _{DSS}	Drain Current at Zero Gate Voltage	V _{DS} = 20V, V _{GS} = 0, Pulse Test Duration = 2ms				30		15		8		mA
V _{DS(ON)}	Drain-Source ON Voltage	V _{GS} = 0	I _D = 2.5mA								0.2	V
			I _D = 4mA						0.2			
			I _D = 6.6mA			0.2						
r _{DS(on)}	Static Drain-Source ON Resistance	V _{GS} = 0, I _D = 1mA					30		50		80	Ω
r _{ds(on)}	Static Drain Source ON Resistance	V _{GS} = 0, I _D = 0, f = 1kHz					30		50		80	
C _{iss}	Common-Source Input Capacitance	V _{DS} = 20V, V _{GS} = 0, f = 1MHz					16		16		16	pF
C _{rss}	JANTX Only	(Note 1)					5		5		5	
	Common-Source Reverse Transfer Capacitance	V _{DS} = 0, V _{GS} = -20V, f = 1MHz (Note 1)					5		5		5	
t _{d(ON)}	Turn-ON Delay Time (Note 1)	V _{DD} = 3V, V _{GD(ON)} = 0					15		15		20	ns
t _r	Rise Time (Note 1)		I _{D(on)}	V _{GS(off)}	R ₁		10		20		40	
t _{off}	Turn-OFF Time (Note 1)	4091	6.6mA	-12V	425Ω		40		60		80	
		4092	4mA	-8V	700Ω							
		4093	2.5mA	-6V	1120Ω							

NOTE 1. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N4117-2N4119, 2N4117A-2N4119A

N-Channel JFET General Purpose Amplifier

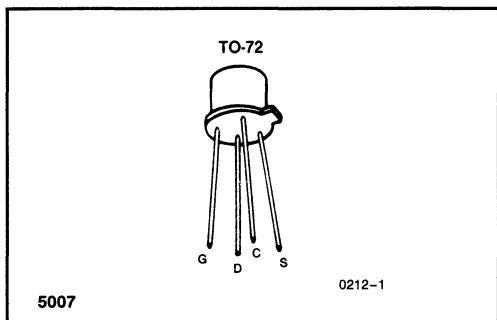


2N4117-2N4119, 2N4117A-2N4119A

FEATURES

- Low Leakage
- Low Capacitance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N4117
2N4117A
2N4118
2N4118A
2N4119
2N4119A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		Units	
			Min	Max	Min	Max	Min	Max		
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-40		-40		-40		V	
I _{GSS}	Gate Reverse Current	V _{GS} = -20V, V _{DS} = 0 T _A = +150°C		-10		-10		-10	pA	
			A devices		-1		-1		-1	nA
			A devices		-25		-25		-25	nA
			-2.5		-2.5		-2.5	nA		
V _{GS(off)}	Gate-Source Pinch-Off Voltage	V _{DS} = 10V, I _D = 1nA	-0.6	-1.8	-1	-3	-2	-6	V	
I _{DSS}	Drain Current at Zero Gate Voltage (Note 1)	V _{DS} = 10V V _{GS} = 0	0.02	0.09	0.08	0.24	0.20	0.60	mA	
g _{fs}	Common-Source Forward Transconductance (Note 1)	V _{DS} = 10V f = 1kHz	70	210	80	250	100	330	μs	
g _{fs}	Common-Source Forward Transconductance (Note 2)	V _{GS} = 0, f = 30MHz	60		70		90			
g _{os}	Common-Source Output Conductance	V _{DS} = 10V, V _{GS} = 0, f = 1kHz		3		5		10		
C _{iss}	Common-Source Input Capacitance (Note 2)	V _{DS} = 10V, V _{GS} = 0, f = 1MHz		3		3		3	pF	
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V _{DS} = 10V, V _{GS} = 0, f = 1MHz		1.5		1.5		1.5		

NOTES: 1. Pulse test: Pulse duration of 2ms used during test.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N4220-2N4222

N-Channel JFET

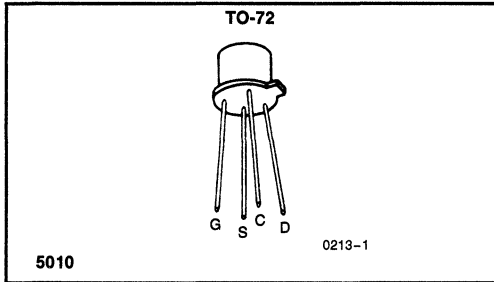
General Purpose Amplifier/Switch



FEATURES

- $C_{rss} < 2pF$
- Moderately High Forward Transconductance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N4220
2N4221
2N4222

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4220		2N4221		2N4222		Units	
			Min	Max	Min	Max	Min	Max		
I_{GSS}	Gate Reverse Current	$V_{GS} = -15V, V_{DS} = 0$		-0.1		-0.1		-0.1	nA	
		$T_A = 150^\circ C$		-0.1		-0.1		-0.1	μA	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -10\mu A, V_{DS} = 0$	-30		-30		-30		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.1nA$		-4		-6		-8		
V_{GS}	Gate-Source Voltage	$V_{DS} = 15V$ $I_D = 50\mu A$ (2N4220) $I_D = 200\mu A$ (2N4221) $I_D = 500\mu A$ (2N4222)	-0.5	-2.5	-1	-5	-2	-6	V	
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	0.5	3	2	6	5	15	mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	f = 1kHz		1000	4000	2000	5000	2500	6000
$ y_{fs} $	Common-Source Forward Transadmittance (Note 2)		f = 100MHz		750		750		750	
g_{os}	Common-Source Output Conductance (Note 1)		f = 1kHz			10		20		40
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz			6		6		6
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)		f = 1MHz			2		2		2

- NOTES:**
1. Pulse test duration 2ms.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N4223, 2N4224

N-Channel JFET

High Frequency Amplifier

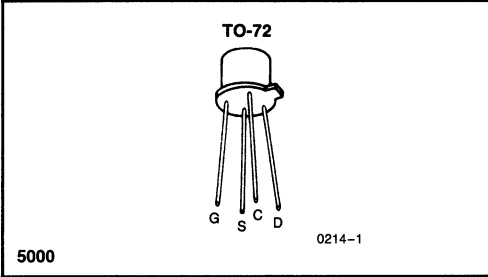


2N4223, 2N4224

FEATURES

- NF = 3dB Typical at 200MHz
- $C_{rss} < 2\text{pF}$

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-30V
Gate Current	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N4223
2N4224

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4223		2N4224		Units		
			Min	Max	Min	Max			
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\text{V}, V_{DS} = 0$		-0.25		-0.5	nA		
			$T_A = +150^\circ\text{C}$	-0.25		-0.5	μA		
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -10\mu\text{A}, V_{DS} = 0$	-30		-30				
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15\text{V}$	$I_D = 0.25\text{nA}$ (2N4223)	-0.1	-8	-0.1	-8	V	
			$I_D = 0.5\text{nA}$ (2N4224)						
V_{GS}	Gate-Source Voltage		$I_D = 0.3\text{mA}$ (2N4223)	-1.0	-7.0	-1.0	-7.5		
			$I_D = 0.2\text{mA}$ (2N4224)						
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15\text{V}, V_{GS} = 0$	3	18	2	20	mA		
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 15\text{V}, V_{GS} = 0$	f = 1kHz		3000	7000	2000	7500	μs
C_{iss}	Common-Source Input Capacitance (Output Shorted)	$V_{DS} = 15\text{V}, V_{GS} = 0$	f = 1MHz			6		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance	(Note 2)				2		2	
$ y_{fs} $	Common-Source Forward Transadmittance	$V_{DS} = 15\text{V}, V_{GS} = 0$ (Note 2)	f = 200MHz		2700		1700		μS
g_{iss}	Common-Source Input Conductance (Output Shorted)					800		800	
g_{oss}	Common-Source Output Conductance (Input Shorted)					200		200	
G_{ps}	Small Signal Power Gain				10				
NF	Noise Figure (Note 2)	$V_{DS} = 15\text{V}, V_{GS} = 0,$ $R_{gen} = 1\text{k}\Omega$				5			dB

- NOTES:** 1. Pulse test, duration 2ms.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N4338-2N4341

N-Channel JFET

Low Noise Amplifier



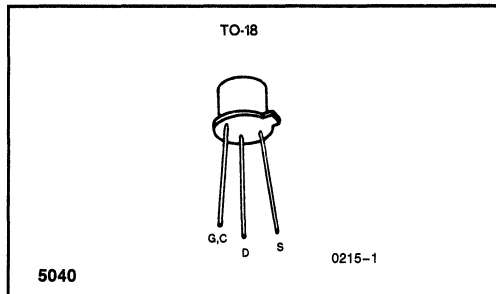
FEATURES

- Exceptionally High Figure of Merit
- Radiation Immunity
- Extremely Low Noise and Capacitance
- High Input Impedance

APPLICATIONS

- Low-level Choppers
- Data Switches
- Multiplexers and Low Noise Amplifiers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-50V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
2N4338
2N4339
2N4340
2N4341

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4338		2N4339		2N4340		2N4341		Units	
			Min	Max	Min	Max	Min	Max	Min	Max		
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-0.1		-0.1		-0.1		-0.1	nA	
				-0.1		-0.1		-0.1		-0.1	μA	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-50		-50		-50		-50		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.1\mu\text{A}$	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 15V, V_{GS} = ()$		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	
I_{DSS}	Saturation Drain Current (Note 2)	$V_{DS} = 15V, V_{GS} = 0$	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 15V, V_{GS} = 0$	f = 1kHz	600	1800	800	2400	1300	3000	2000	4000	μs
g_{os}	Common-Source Output Conductance				5		15		30		60	
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{DS} = 0, I_{DS} = 0$		2500		1700		1500		800	ohm	
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 15V, V_{GS} = 0$ (Note 1)	f = 1MHz	7		7		7		7	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance				3		3		3			3
NF	Noise Figure (Note 1)	$V_{DS} = 15V, V_{GS} = 0$ $R_{gen} = 1\text{meg}, BW = 200\text{Hz}$	f = 1kHz	1		1		1		1	dB	

NOTE 1: For design reference only, not 100% tested.
NOTE 2: Pulse test duration 2 ms (non-JEDEC Condition).

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NOTE: All typical values have been characterized but are not tested.

2N4351

N-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch

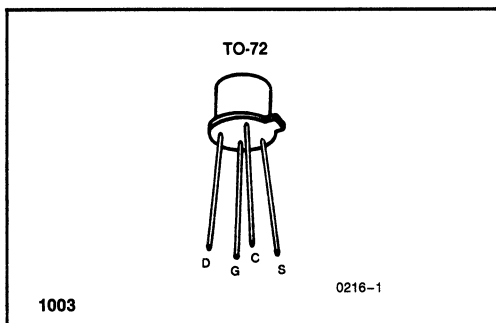


2N4351

FEATURES

- Low ON Resistance
- Low Capacitance
- High Gain
- High Gate Breakdown Voltage
- Low Threshold Voltage

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Source Voltage or Drain-Body Voltage 25V
Peak Gate-Source Voltage (Note 1) ± 125V
Drain Current 100mA
Storage Temperature Range -65°C to +200°C
Operating Temperature Range -55°C to +150°C
Lead Temperature (Soldering, 10sec) +300°C
Power Dissipation 375mW
Derate above 25°C 3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N4351

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Substrate connected to source.

Symbol	Parameter	Test Conditions	Min	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	I _D = 10μA, V _{GS} = 0	25		V
I _{GSS}	Gate Leakage Current	V _{GS} = ± 30V, V _{DS} = 0		10	pA
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} = 10V, V _{GS} = 0		10	nA
V _{GS(th)}	Gate-Source Threshold Voltage	V _{DS} = 10V, I _D = 10μA	1	5	V
I _{D(on)}	'ON' Drain Current	V _{GS} = 10V, V _{DS} = 10V	3		mA
V _{DS(on)}	Drain-Source "ON" Voltage	I _D = 2mA, V _{GS} = 10V		1	V
r _{DS(on)}	Drain-Source Resistance	V _{GS} = 10V, I _D = 0, f = 1kHz		300	ohms
y _{fs}	Forward Transfer Admittance	V _{DS} = 10V, I _D = 2mA, f = 1kHz	1000		μs
C _{rSS}	Reverse Transfer Capacitance (Note 2)	V _{DS} = 0, V _{GS} = 0, f = 1MHz		1.3	pF
C _{iSS}	Input Capacitance (Note 2)	V _{DS} = 10V, V _{GS} = 0, f = 1MHz		5.0	
C _{d(sub)}	Drain-Substrate Capacitance (Note 2)	V _{D(SUB)} = 10V, f = 1MHz		5.0	
t _{d(on)}	Turn-On Delay (Note 2)			45	ns
t _r	Rise Time (Note 2)			65	
t _{d(off)}	Turn-Off Delay (Note 2)			60	
t _f	Fall Time (Note 2)			100	

- NOTES:** 1. Device must not be tested at ± 125V more than once or longer than 300ms.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

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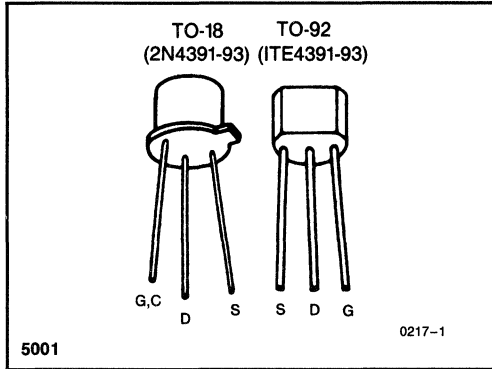
2N4391-2N4393, ITE4391-ITE4393 N-Channel JFET Switch



FEATURES

- $r_{ds(on)} < 300$ Ohms (2N4391)
- $I_{D(OFF)} < 100$ pA
- Switches ± 10 VAC With ± 15 V Supplies (2N4392, 2N4393)

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V	
Gate Current	10mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +200°C	
Lead Temperature (Soldering, 10sec)	+300°C	

	TO-18	TO-92
Power Dissipation	1.8W	360mW
Derate above 25°C	10mW/°C	3.3mW/°C

Plastic

Storage	-55°C to +150°C
Operating	-55°C to +135°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION*

TO-92	TO-18
ITE 4391	2N4391
ITE 4392	2N4392
ITE 4393	2N4393

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	4391		4392		4393		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -20V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-100		-100		-100	pA
				-200		-200		-200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-40		-40		-40		V
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 20V$ $V_{GS} = -5V$ (4393) $V_{GS} = -7V$ (4392) $V_{GS} = -12V$ (4391) $T_A = 150^\circ\text{C}$		100		100		100	pA
				200		200		200	nA
$V_{GS(f)}$	Gate-Source Forward Voltage	$I_G = 1mA, V_{DS} = 0$		1		1		1	V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1nA$	-4	-10	-2	-5	-0.5	-3	
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 20V, V_{GS} = 0$	50	150	25	75	5	30	mA

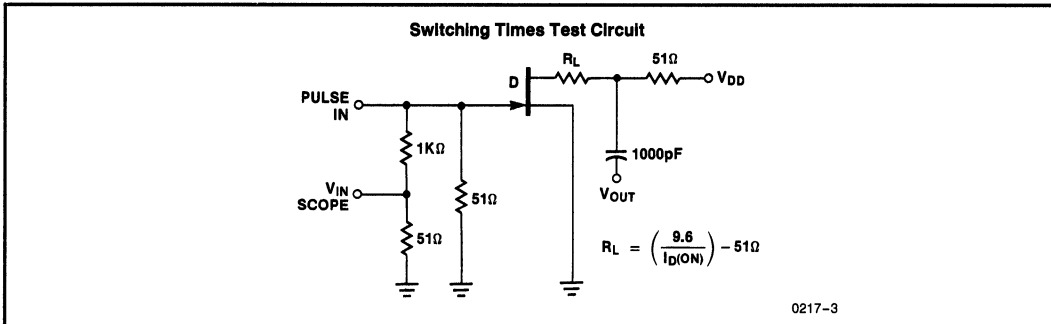
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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	4391		4392		4393		Units	
			Min	Max	Min	Max	Min	Max		
V _{DS(on)}	Drain-Source ON Voltage	V _{GS} = 0 I _D = 3mA (4393) I _D = 6mA (4392) I _D = 12mA (4391)		0.4		0.4		0.4	V	
r _{DS(on)}	Static Drain-Source ON Resistance	V _{GS} = 0, I _D = 1mA		30		60		100	Ω	
r _{ds(on)}	Drain-Source ON Resistance	V _{GS} = 0, I _D = 0 f = 1kHz		30		60		100		
C _{iss}	Common-Source Input Capacitance (Note 2)	V _{DS} = 20V, V _{GS} = 0		14		14		14	pF	
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V _{DS} = 0, V _{GS} = -5V						3.5		
		V _{GS} = -7V f = 1MHz				3.5				
		V _{GS} = -12V		3.5						
t _d	Turn-ON Delay Time (Note 2)	V _{DD} = 10V, V _{GS(on)} = 0 I _{D(on)} V _{GS(off)}		15		15		15	ns	
t _r	Rise Time (Note 2)			5		5		5		
t _{off}	Turn-OFF Delay Time (Note 2)		4391 12mA -12V		20		35			50
t _f	Fall Time (Note 2)		4392 6 -7		15		20			30
		4393 3 -5								

NOTES: 1. Pulse test required, pulse width = 300μs, duty cycle ≤ 3%.
 2. For design reference only, not 100% tested.



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NOTE: All typical values have been characterized but are not tested.

2N4416/A, ITE4416

N-Channel JFET

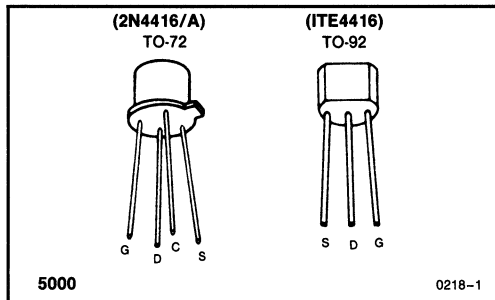
High Frequency Amplifier



FEATURES

- Low Noise
- Low Feedback Capacitance
- Low Output Capacitance
- High Transconductance
- High Power Gain

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	
2N4416, ITE4416	-30V
2N4416A	-35V
Gate Current	10mA
Storage Temperature Range	
2N4416/2N4416A	-65°C to +200°C
ITE4416	-55°C to +150°C
Operating Temperature Range	
2N4416/2N4416A	-65°C to +200°C
ITE4416	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	
2N4416/2N4416A	1.7mW/°C
ITE4416	2.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92	TO-72
ITE 4416	2N4416
—	2N4416A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
I _{GSS}	Gate Reverse Current	V _{GS} = -20V, V _{DS} = 0 T _A = 150°C		-0.1	nA
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-30		V
			-35		
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 15V, I _D = 1nA		-6	V
			-2.5	-6	
V _{GS(f)}	Gate-Source Forward Voltage	I _G = 1mA, V _{DS} = 0		1	V
I _{DSS}	Drain Current at Zero Gate Voltage	V _{DS} = 15V, V _{GS} = 0	5	15	mA
g _{fs}	Common-Source Forward Transconductance	f = 1kHz	4500	7500	
g _{os}	Common-Source Output Conductance			50	μS
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 1)	f = 1MHz		0.8	pF
C _{iss}	Common-Source Input Capacitance (Note 1)			4	pF
C _{oss}	Common-Source Output Capacitance (Note 1)			2	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	100MHz		400MHz		Units
			Min	Max	Min	Max	
g_{iss}	Common-Source Input Conductance	$V_{DS} = 15V, V_{GS} = 0$ (Note 1)		100		1000	μS
b_{iss}	Common-Source Input Susceptance			2500		10,000	
g_{oss}	Common-Source Output Conductance			75		100	
b_{oss}	Common-Source Output Susceptance			1000		4000	
g_{fs}	Common-Source Forward Transconductance				4000		
G_{ps}	Common-Source Power Gain	$V_{DS} = 15V, I_D = 5mA$ (Note 1)	18		10		dB
NF	Noise Figure (Note 1)	$V_{DS} = 15V, I_D = 5mA, R_G = 1k\Omega$		2		4	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

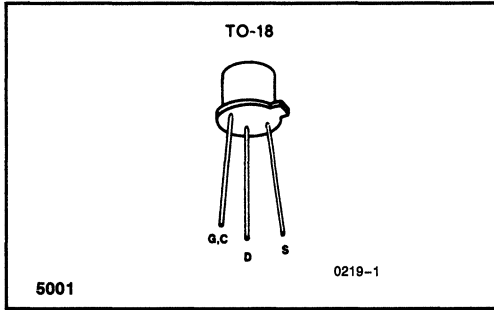
2N4856-2N4861, JAN, JTX, JTXV N-Channel JFET Switch



FEATURES

- Low $r_{DS(on)}$
- $I_{D(off)} < 250\text{pA}$
- Switches $\pm 10\text{V}$ Signals With $\pm 15\text{V}$ Supplies (2N4858, 2N4861)

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage

2N4856-58 -40V

2N4859-61 -30V

Gate Current 50mA

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Operating Temperature Range -55°C to $+200^\circ\text{C}$

Led Temperature (Soldering, 10sec) $+300^\circ\text{C}$

Power Dissipation 1.8W

Derate above 25°C 10mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
2N4856†
2N4857†
2N4858†
2N4859
2N4860
2N4861

†add JAN, JTX, JTXV, to basic part number to specify these devices.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4856		2N4857		2N4858		2N4859		2N4860		2N4861		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-40		-40		-40		-40		-40		-40		V
			-30		-30		-30		-30		-30		-30		
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\text{V}, V_{DS} = 0$		-0.25		-0.25		-0.25							nA
		$V_{GS} = -20\text{V}, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-0.5		-0.5		-0.5							μA
		$V_{GS} = -15\text{V}, V_{DS} = 0$							-0.25		-0.25		-0.25		nA
		$V_{GS} = -15\text{V}, V_{DS} = 0$ $T_A = 150^\circ\text{C}$							-0.5		-0.5		-0.5		nA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 15\text{V}, V_{GS} = -10\text{V}$	250		250		250		250		250		250		pA
		$T_A = 150^\circ\text{C}$	500		500		500		500		500		500		nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15\text{V}, I_D = 0.5\text{nA}$	-4	-10	-2	-6	-0.8	-4	-4	-10	-2	-6	-0.8	-4	V
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15\text{V}, V_{GS} = 0$	50		20	100	8	80	50		20	100	8	80	mA

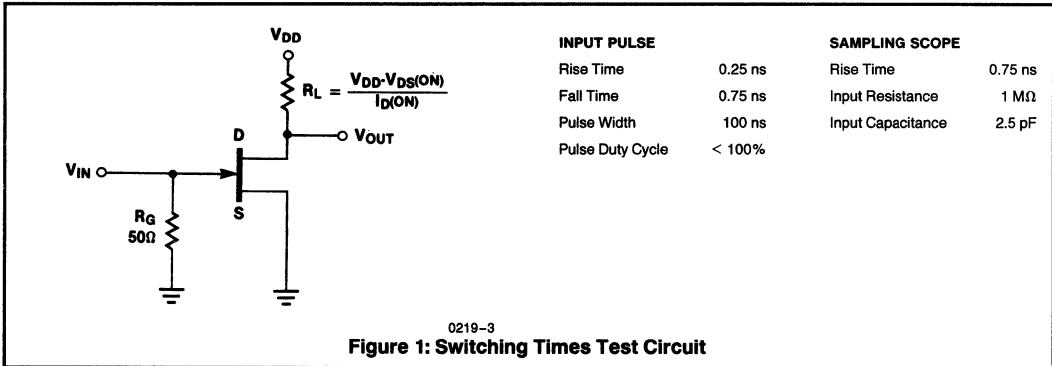
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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4856		2N4857		2N4858		2N4859		2N4860		2N4861		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS}=0, I_D=()$		0.75 (20)		0.50 (10)		0.50 (5)		0.75 (20)		0.50 (10)		0.50 (5)	V (mA)
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS}=0, I_D=0$	f = 1kHz		25	40	60	25	40	60	ohm				
C_{iss}	Common-Source Input Capacitance	$V_{DS}=0, V_{GS}=-10\text{V}$	f = 1MHz		18	18	18	18	18	18	pF				
C_{rss}	Common-Source Reverse Transfer Capacitance	(Note 2)	8	8	8	8	8	8	8	8					
t_{d1}	Turn-ON Delay Time (Note 2)	$V_{DD}=10\text{V}, R_L=464\Omega$ (2N4856,59) 953Ω (2N4857,60)	6	6	10	6	6	10	6	10	ns				
t_r	Rise Time (Note 2)	$V_{GS(on)}=0$ 1910Ω (2N4858,61) $V_{GS(off)}=-10\text{V}, I_D=20\text{mA}$ (2N4856,9) $V_{GS(off)}=-6\text{V}, I_D=10\text{mA}$ (2N4857,60)	3	4	10	3	4	10	3	4					
t_{off}	Turn-OFF Time (Note 2)	$V_{GS(off)}=-4\text{V}, I_D=5\text{mA}$ (2N4858,61)	25	50	100	25	50	100	25	50					

NOTES: 1. Pulse test required, pulse width = 100 μs , duty cycle $\leq 10\%$.
2. For design reference only, not 100% tested.



2N4867/A-2N4869/A

N-Channel JFET

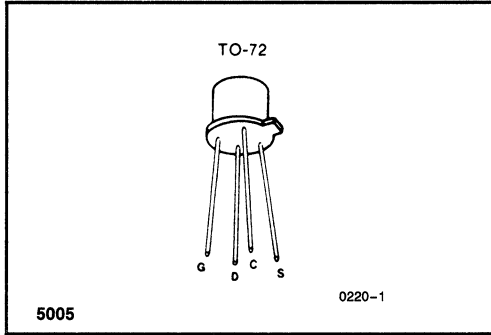
Low Noise Amplifier



FEATURES

- Low Noise Voltage
- Low Leakage
- High Gain

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +200°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	1.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N4867
2N4867A
2N4868
2N4868A
2N4869
2N4869A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		Units			
			Min	Max	Min	Max	Min	Max				
I _{GSS}	Gate Reverse Current	V _{GS} = -30V, V _{DS} = 0		-0.25		-0.25		-0.25	nA			
		T _A = 150°C		-0.25		-0.25		-0.25	μA			
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-40		-40		-40		V			
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 20V, I _D = 1μA	-0.7	-2	-1	-3	-1.8	-5				
I _{DSS}	Saturation Drain Current (Note 1)	V _{DS} = 20V, V _{GS} = 0	0.4	1.2	1	3	2.5	7.5	mA			
g _{fs}	Common-Source Forward Transconductance (Note 1)	V _{DS} = 20V, V _{GS} = 0	f = 1kHz	700	2000	1000	3000	1300	4000	μS		
g _{os}	Common-Source Output Conductance				1.5		4		10			
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 2)			f = 1MHz		5		5			5	pF
C _{iss}	Common-Source Input Capacitance (Note 2)					25		25			25	
e _n	Short Circuit Equivalent Input Noise Voltage (Note 2)	V _{DS} = 10V, V _{GS} = 0	f = 10Hz		20		20		20	nV/√Hz		
				A devices	f = 1kHz		10		10		10	
					f = 10Hz		10		10		10	
					f = 1kHz		5		5		5	
NF	Spot Noise Figure (Note 2)	V _{DS} = 10V, V _{GS} = 0 R _{gen} = 20K, (2N4867 Series) R _{gen} = 5K, (2N4867A Series)	f = 1kHz		1		1		1	dB		

- NOTES:** 1. Pulse test duration = 2ms.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N5018, 2N5019

P-Channel JFET Switch

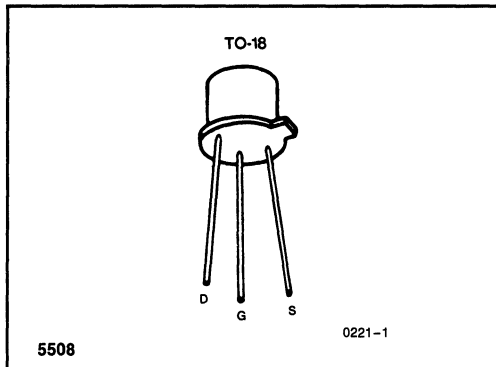


2N5018, 2N5019

FEATURES

- Low Insertion Loss
- No Offset or Error Voltages Generated By Closed Switch
- Purely Resistive

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Commutators
- Choppers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	30V
Gate Current	50mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+200^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	500mW
Derate above 25°C	$3\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION*

TO-18
2N5018
2N5019

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5018		2N5019		Units
			Min	Max	Min	Max	
BV_{GS}	Gate-Source Breakdown Voltage	$I_G = 1\mu\text{A}, V_{DS} = 0$	30		30		V
I_{GSS}	Gate Reverse Current	$V_{GS} = 15\text{V}, V_{DS} = 0$		2		2	nA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = -15\text{V}, V_{GS} = 12\text{V}$ (2N5018) $V_{GS} = 7\text{V}$ (2N5019) $T_A = 150^\circ\text{C}$		-10		-10	μA
I_{DGO}	Drain Reverse Current	$V_{DG} = -15\text{V}, I_S = 0$ $T_A = 150^\circ\text{C}$		-2		-2	nA
				-3		-3	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = -15\text{V}, I_D = -1\mu\text{A}$		10		5	V
I_{DSS}	Saturation Drain Current	$V_{DS} = -20\text{V}, V_{GS} = 0$	-10		-5		mA
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0, I_D = -6\text{mA}$ (2N5018), $I_D = -3\text{mA}$ (2N5019)		-0.5		-0.5	V
$r_{ds(on)}$	Static Drain-Source ON Resistance	$I_D = -1\text{mA}, V_{GS} = 0$		75		150	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	$I_D = 0, V_{GS} = 0$ $f = 1\text{kHz}$		75		150	
C_{iss}	Common-Source Input Capacitance (Note 1)	$V_{DS} = -15\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$		45		45	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)	$V_{DS} = 0, V_{GS} = 12\text{V}$ (2N5018), $V_{GS} = 7\text{V}$ (2N5019)		10		10	

10

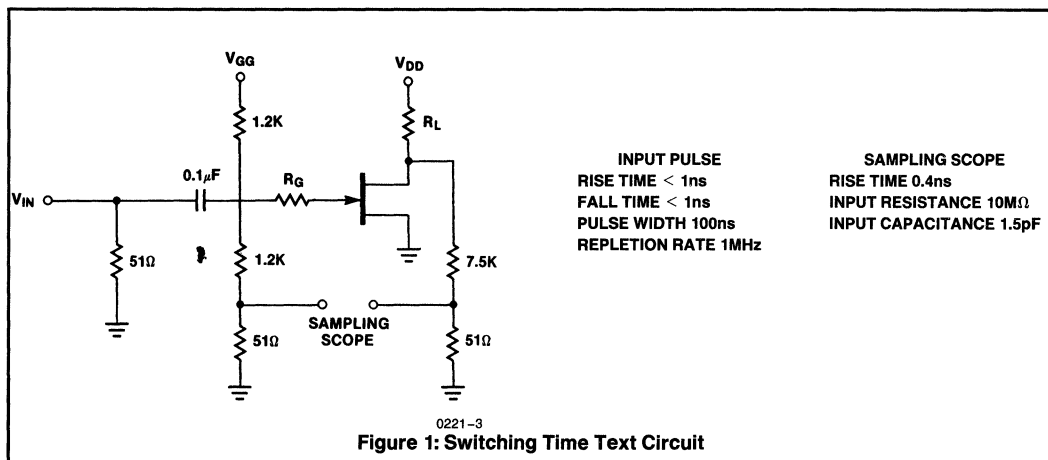
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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5018		2N5019		Units	
			Min	Max	Min	Max		
$t_{d(on)}$	Turn-ON Delay Time (Note 1)	$V_{DD} = -6\text{V}, V_{GS(on)} = 0$		15		15	ns	
t_r	Rise Time (Note 1)			20		75		
$t_{d(off)}$	Turn-off Delay Time (Note 1)	2N5018	12V	-6mA	910 Ω	15		25
t_f	Fall Time (Note 1)	2N5019	7V	-3mA	1.8k Ω	50		100

NOTES: 1. For design reference only, not 100% tested.



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NOTE: All typical values have been characterized but are not tested.

2N5114-2N5116, JAN, JTX, JTXV P-Channel JFET Switch



2N5114-2N5116, JAN, JTX, JTXV

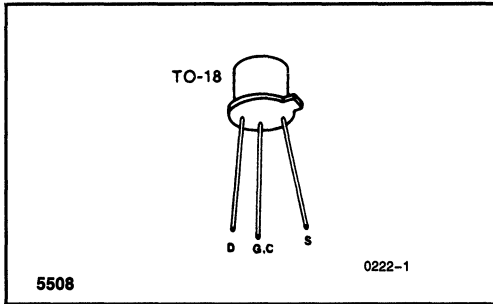
GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and ± 10 VAC signals can be handled using only +5V logic (TTL or CMOS).

FEATURES

- Low ON Resistance
- $I_{D(off)} < 500$ pA
- Switches directly from TTL Logic

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	30V
Gate Current	50mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+200^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	500mW
Derate above 25°C	3mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO18†
2N5114
2N5115
2N5116

†add JAN, JTX, JTXV to basic part number to specify these devices.

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	2N5114	2N5115	2N5116	JAN TX 2N5114	JAN TX 2N55115	JAN TX 2N5116	Units
		Max	Max	Max	Max	Max	Max	
t_d	Turn-ON Delay Time	6	10	12	6	10	25	ns
t_r	Rise Time (Note 2)	10	20	30	10	20	35	
t_{off}	Turn-OFF Delay Time (Note 2)	6	8	10	6	8	20	
t_f	Fall Time (Note 2)	15	30	50	15	30	60	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5114		2N5115		2N5116		Units
			Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu\text{A}, V_{DS} = 0$	30		30		30		V
I_{GSS}	Gate Reverse Current	$V_{GS} = 20\text{V}, V_{DS} = 0$		500		500		500	pA
		$T_A = 150^\circ\text{C}$		1.0		1.0		1.0	μA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = -15\text{V}$ $V_{GS} = 12\text{V}$ (2N5114) $V_{GS} = 7\text{V}$ (2N5115) $V_{GS} = 5\text{V}$ (2N5116)		-500		-500		-500	pA
				-1.0		-1.0		-1.0	μA
V_p	Gate-Source Pinch-Off Voltage	$V_{DS} = -15\text{V}, I_D = -1\text{nA}$	5	10	3	6	1	4	V

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NOTE: All typical values have been characterized but are not tested.

2N5114-2N5116, JAN, JTX, JTXV



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	2N5114		2N5115		2N5116		Units
			Min	Max	Min	Max	Min	Max	
I _{DSS}	Drain Current at Zero Gate Voltage (Note 1)	V _{GS} = 0 V _{DS} = -18V (2N5114) V _{DS} = -15V (2N5115) V _{DS} = -15V (2N5116)	-30	-90	-15	-60	-5	-25	mA
V _{GS(f)}	Forward Gate-Source Voltage	I _G = -1mA, V _{DS} = 0		-1		-1		-1	V
V _{DS(on)}	Drain-Source ON Voltage	V _{GS} = 0 I _D = -15 mA (2N5114) I _D = -7 mA (2N5115) I _D = -3 mA (2N5116)		-1.3		-0.8		-0.6	
r _{DS(on)}	Static Drain-Source ON Resistance	V _{GS} = 0, I _D = -1mA		75		100		150	Ω
r _{ds(on)}	Small-Signal Drain-Source ON Resistance	V _{GS} = 0, I _D = 0, f = 1kHz		75		100		150	
C _{iss}	Common-Source Input Capacitance (Note 2)	V _{DS} = -15 V, V _{GS} = 0, f = 1mHz	Jan TX only						
					25	25	25	25	
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V _{DS} = 0 V _{GS} = 12V (2N5114) V _{GS} = 7V (2N5115) V _{GS} = 5V (2N5116) f = 1mHz		7		7		pF	

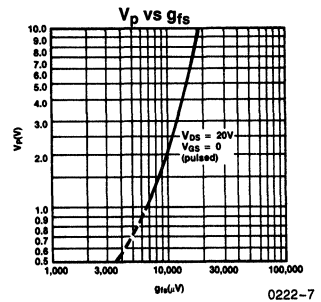
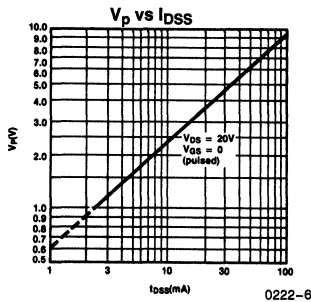
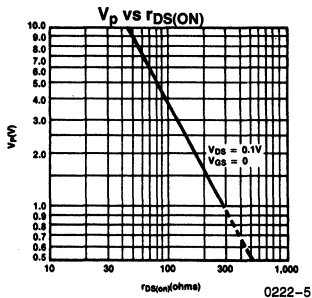
- NOTES: 1. Pulse test; duration = 2ms.
2. For design reference only, not 100% tested.

Test Conditions			
	2N5114	2N5115	2N5116
V _{DD}	-10V	-6V	-6V
V _{GG}	20V	12V	8V
R _L	430Ω	910Ω	2KΩ
R _G	100Ω	220Ω	390Ω
I _{D(ON)}	-15mA	-7mA	-3mA
V _{IN}	-12V	-7V	-5V

0222-3

0222-4

TYPICAL PERFORMANCE CHARACTERISTICS



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NOTE: All typical values have been characterized but are not tested.

2N5117-2N5119

Dielectrically Isolated Dual PNP General Purpose Amplifier

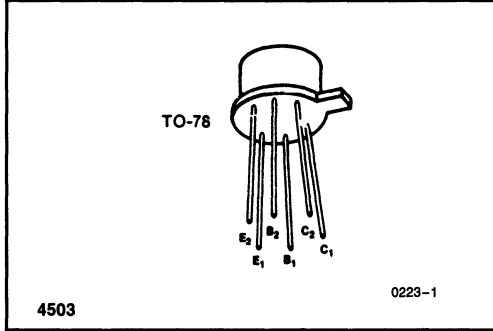


2N5117-2N5119

FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Good h_{FE} Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base or Collector-Emitter Voltage (Note 1)	-45V
Emitter-Base Voltage (Notes 1 and 2)	-7V
Collector-Collector Voltage	100V
Collector Current (Note 1)	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +175°C
Lead Temperature (Soldering, 10sec)	+300°C

	ONE SIDE	BOTH SIDES
Power Dissipation	250mW	500mW
Derate above 25°C	1.67mW/°C	3.33mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-78
2N5117
2N5118
2N5119

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol		Test Conditions	2N5117 2N5118		2N5119		Units
			Min	Max	Min	Max	
h_{FE}	DC Current Gain	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$	100	300	50		
		$I_C = 500\mu\text{A}, V_{CE} = 5.0\text{V}$	100		50		
		$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}, T_A = -55^\circ\text{C}$	30		20		
I_{CBO}	Collector Cutoff-Current	$I_E = 0, V_{CB} = 30\text{V}$		0.1	0.1		nA
		$T_A = 150^\circ\text{C}$		0.1	0.1		μA
I_{EBO}	Emitter Cutoff Current	$I_C = 0, V_{EB} = 5.0\text{V}$		0.1	0.1		nA
I_{C1-C2}	Collector-Collector Leakage	$V_{CC} = 100\text{V}$		5.0	5.0		pA
GBW	Current Gain Bandwidth Product (Note 4)	$I_C = 500\mu\text{A}, V_{CE} = 10\text{V}$	100		100		MHz
C_{ob}	Output Capacitance (Note 4)	$I_E = 0, V_{CB} = 5.0\text{V}, f = 1\text{MHz}$		0.8	0.8		pF
C_{ie}	Emitter Transition Capacitance (Note 4)	$I_C = 0, V_{EB} = 0.5\text{V}, f = 1\text{MHz}$		1.0	1.0		
C_{C1-C2}	Collector-Collector Capacitance (Note 4)	$V_{CC} = 0, f = 1\text{MHz}$		0.8	0.8		
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	$I_C = 1.0\text{mA}, I_B = 0$	45		45		V
NF	Narrow Band Noise Figure (Note 4)	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$ $BW = 200\text{Hz}$		4.0	4.0		dB
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu\text{A}, I_E = 0$	45		45		V
BV_{EBO}	Emitter Base Breakdown Voltage	$I_E = 10\mu\text{A}, I_C = 0$	7.0		7.0		V

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NOTE: All typical values have been characterized but are not tested.

MATCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5117		2N5118		2N5119		Units	
			Min	Max	Min	Max	Min	Max		
h_{FE1}/h_{FE2}	DC Current Gain Ratio (Note 3)	$I_C = 10\mu\text{A to } 500\mu\text{A}, V_{CE} = 5\text{V}$	0.9	1.0						
		$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$			0.85	1.0	0.8	1.0		
$V_{BE1}-V_{BE2}$	Base-Emitter Voltage Differential	$I_C = 10\mu\text{A to } 500\mu\text{A}, V_{CE} = 5\text{V}$ $I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$		3.0					mV	
						5.0	5.0			
$I_{B1}-I_{B2}$	Base Current Differential			10.0		15		40	nA	
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base Voltage Differential Change with Temperature		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			3.0		5.0		$\mu\text{V}/^\circ\text{C}$
$\Delta(I_{B1}-I_{B2})/\Delta T$	Base-Current Differential Change with Temperature		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			0.3		0.5		1.0 nA/ $^\circ\text{C}$

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed $10\mu\text{A}$.

3. Lower of two h_{FE} readings is defined as h_{FE1} .

4. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N5196-2N5199

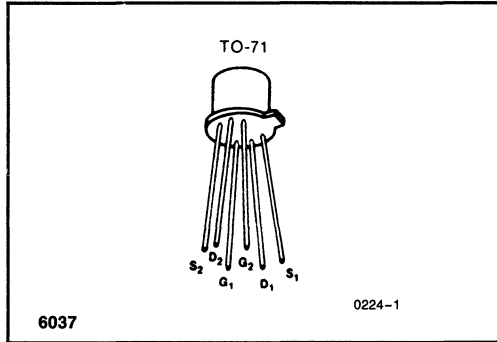
Dual N-Channel JFET

General Purpose Amplifier



2N5196-2N5199

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1) -50V	
Gate Current (Note 1) 50mA	
Storage Temperature Range -65°C to +200°C	
Operating Temperature Range -55°C to +150°C	
Lead Temperature (Soldering, 10sec) +300°C	
	One Side	Both Sides
Power Dissipation ($T_A = 85^\circ\text{C}$)	... 250mW	500mW
Derating 2.6mW/°C	4.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
2N5196
2N5197
2N5198
2N5199

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-25	pA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1nA$	-0.7	-4	
V_{GS}	Gate-Source Voltage	$V_{DG} = 20V, I_D = 200\mu A$	-0.2	-3.8	pA
I_G	Gate Operating Current	$T_A = 125^\circ\text{C}$		-15	
I_{DSS}	Saturation Drain Current (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	0.7	7	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	1000	4000	μs
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DG} = 20V, I_D = 200\mu A$	700	1600	
g_{os}	Common-Source Output Conductance (Note 2)	$V_{DS} = 20V, V_{GS} = 0$		50	
g_{os}	Common-Source Output Conductance (Note 2)	$V_{DG} = 20V, I_D = 200\mu A$		4	
C_{iss}	Common-Source Input Capacitance (Note 4)	$V_{DS} = 20V, V_{GS} = 0$		6	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 4)			2	
NF	Spot Noise Figure (Note 4)	$f = 100\text{Hz}, R_G = 10M\Omega$		0.5	dB
\bar{e}_n	Equivalent Input Noise Voltage (Note 4)	$f = 1\text{kHz}$		20	$\frac{nV}{\sqrt{Hz}}$

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	2N5196		2N5197		2N5198		2N5199		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
$ I_{G1}-I_{G2} $	Differential Gate Current	$V_{DG} = 20\text{V}$, $I_D = 200\mu\text{A}$ $T_A = 125^\circ\text{C}$		5		5		5		5	nA
I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 2)	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$	0.95	1	0.95	1	0.95	1	0.95	1	
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	$f = 1\text{kHz}$	0.97	1	0.97	1	0.95	1	0.95	1	
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage			5		5		10		15	mV
$\Delta V_{GS1} = V_{GS2} $ ΔT	Gate-Source Differential Voltage Change with Temperature (Note 3)	$V_{DG} = 20\text{V}$, $T_A = 25^\circ\text{C}$ $I_D = 200\mu\text{A}$, $T_B = 125^\circ\text{C}$		5		10		20		40	$\mu\text{V}/^\circ\text{C}$
		$T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$		5		10		20		40	
$ g_{os1}-g_{os2} $	Differential Output Conductance	$f = 1\text{kHz}$		1		1		1		1	μS

NOTES: 1. Per transistor.

2. Pulse test required, pulsewidth = $300\mu\text{s}$, duty cycle < 3%.

3. Measured at endpoints T_A and T_B .

4. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N5397, 2N5398

N-Channel JFET

High Frequency Amplifier

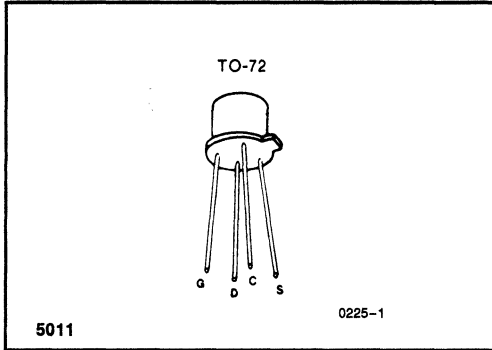


2N5397, 2N5398

FEATURES

- $G_{ps} = 15\text{dB}$ Minimum (Common Gate) at 450MHz
- Low Noise
- Low Capacitance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	25V
Drain-Source Voltage	25V
Continuous Forward Gate Current	10mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	300mW
Derate above 25°C	$2.4\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N5397
2N5398

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5397		2N5398		Units	
			Min	Max	Min	Max		
I_{GSS}	Gate Reverse Current	$V_{GS} = -15\text{V}, V_{DS} = 0$		-0.1		0.1	nA	
			$T_A = 150^\circ\text{C}$		-0.1		-0.1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0, I_G = -1\mu\text{A}$	-25		-25		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10\text{V}, I_D = 1\text{nA}$	-1.0	-6.0	-1.0	-6.0		
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 10\text{V}, V_{GS} = 0$	10.	30	5	40	mA	
$V_{GS(f)}$	Gate-Source Forward Voltage	$V_{DS} = 0, I_G = 1\text{mA}$		1		1	V	
g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DS} = 10\text{V}, I_D = 10\text{mA}$	f = 1kHz	6000	10,000			μS
						5500	10,000	
g_{oss}	Common-Source Output Conductance	$V_{DS} = 10\text{V}, I_D = 10\text{mA}$	f = 1kHz		200			μS
							400	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	$V_{DS} = 10\text{V}, I_D = 10\text{mA}$	f = 1MHz		1.2			pF
							1.3	
C_{iss}	Common-Source Input Capacitance (Note 2)	$V_{DG} = 10\text{V}, I_D = 10\text{mA}$	f = 1MHz		5.0			pF
							5.5	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5397		2N5398		Units	
			Min	Max	Min	Max		
g_{iss}	Common-Source Input Conductance (Note 2)	$V_{DG} = 10\text{V}, I_D = 10\text{mA}$		2000			μs	
		$V_{DG} = 10\text{V}, V_{GS} = 0$				3000		
g_{oss}	Common-Source Output Conductance (Note 2)	$V_{DG} = 10\text{V}, I_D = 10\text{mA}$		400				
		$V_{DS} = 10\text{V}, V_{GS} = 0$				500		
g_{fs}	Common-Source Forward Transconductance (Note 1, 2)	$V_{DG} = 10\text{V}, I_D = 10\text{mA}$	$f = 450\text{MHz}$	5500	9000			
		$V_{DS} = 10\text{V}, V_{GS} = 0$				5000		10,000
G_{ps}	Common-Source Power Gain (neutralized)	$V_{DG} = 10\text{V}, I_D = 10\text{mA}$		15			dB	
NF	Common-Source, Spot Noise Figure (neutralized)	(Note 2)		3.5				

NOTES: 1. Pulse test duration = 2ms
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N5432-2N5434

N-Channel JFET Switch

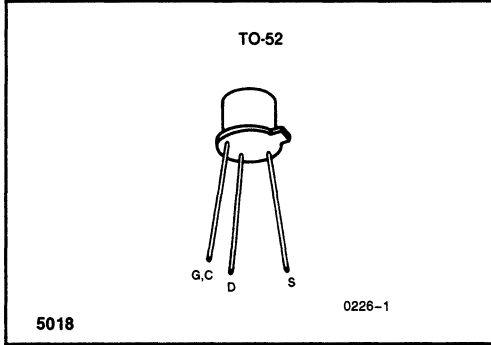


2N5432-2N5434

FEATURES

- Low $r_{ds(on)}$
- Excellent Switching
- Low Cutoff Current

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source Voltage	-25V
Gate-Drain Voltage	-25V
Gate Current	100mA
Drain Current	400mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-52
2N5432
2N5433
2N5434

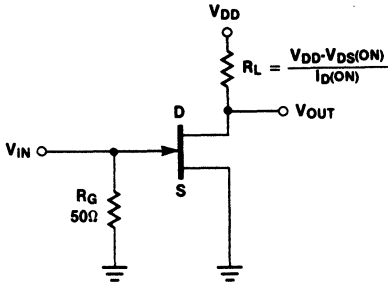
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5432		2N5433		2N5434		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -15V, V_{DS} = 0$		-200		-200		-200	pA
		$T_A = 150^\circ\text{C}$		-200		-200		-200	nA
BV_{GSS}	Gate Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-25		-25		-25		V
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 5V, V_{GS} = -10V$		200		200		200	pA
		$T_A = 150^\circ\text{C}$		200		200		200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 5V, I_D = 3nA$	-4	-10	-3	-9	-1	-4	V
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15V, V_{GS} = 0$	150		100		30		mA
$r_{DS(on)}$	Static Drain-Source ON Resistance	$V_{GS} = 0, I_D = 10mA$	2	5	7		10		ohm
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100		mV
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0, I_D = 0$		5		7		10	ohm
C_{iss}	Common-Source Input Capacitance (Note 2)	$V_{DS} = 0, V_{GS} = -10V$	$f = 1kHz$	30		30		30	
				$f = 1MHz$	15		15		15
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)		15			15		15	pF
t_d	Turn-ON Delay Time (Note 2)	$V_{DD} = 1.5V,$		4		4		4	ns
t_r	Rise Time (Note 2)	$V_{GS(on)} = 0,$		1		1		1	
t_{off}	Turn-OFF Delay Time (Note 2)	$V_{GS(off)} = -12V$		6		6		6	
t_f	Fall Time (Note 2)	$I_{D(on)} = 10mA$		30		30		30	

- NOTES:** 1. Pulse test required, pulsewidth 300 μs , duty cycle $\leq 3\%$.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.



Input Pulse		Sampling Scope	
Rise Time	0.25 ns	Rise Time	0.4 ns
Fall Time	0.75 ns	Input Resistance	10 MΩ
Pulse Width	200 ns	Input Capacitance	1.5 pF
Pulse Rate	550 pps		

0226-3

Figure 1: Switching Time, Test Circuit

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NOTE: All typical values have been characterized but are not tested.

2N5452-2N5454

Dual N-Channel JFET

General Purpose Amplifier

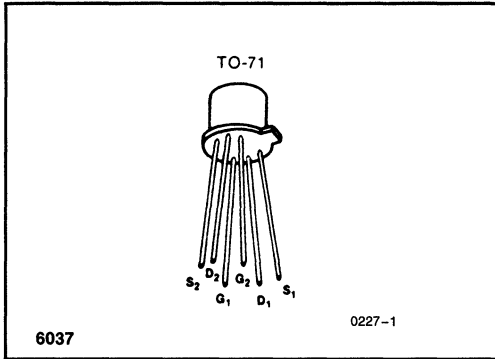


2N5452-2N5454

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

PIN CONFIGURATION



FEATURES

- Low Offset Voltage
- Low Drift
- Low Capacitance
- Low Output Conductance

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate Drain Voltage	
(Note 1)	−50V
Gate Current (Note 1)	50mA
Storage Temperature Range	−65°C to +200°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

One Side Both Sides

Power Dissipation ($T_C = 85^\circ\text{C}$)	250mW	500mW
Derate above 25°C	2.9mW/°C	4.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
2N5452
2N5453
2N5454

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5452		2N5453		2N5454		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		−100		−100		−100	pA
				−200		−200		−200	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0, I_G = -1\mu\text{A}$	−50		−50		−50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1\text{nA}$	−1	−4.5	−1	−4.5	−1	−4.5	
V_{GS}	Gate-Source Voltage	$V_{DS} = 20V, I_D = 50\mu\text{A}$	−0.2	−4.2	−0.2	−4.2	−0.2	−4.2	
$V_{GS(f)}$	Gate-Source Forward Voltage	$V_{DS} = 0, I_G = 1\text{mA}$		2		2		2	
I_{DSS}	Saturation Drain Current	$V_{DS} = 20V, V_{GS} = 0$	0.5	5.0	0.5	5.0	0.5	5.0	mA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5452		2N5453		2N5454		Units	
			Min	Max	Min	Max	Min	Max		
g _{fs}	Common-Source Forward Transconductance (Note 2)	V _{DS} = 20V, V _{GS} = 0	f = 1kHz	1000	3000	1000	3000	1000	3000	μS
			f = 100MHz	1000		1000		1000		
g _{os}	Common-Source Output Conductance	V _{DS} = 20V, I _D = 200μA	f = 1kHz		3.0		3.0		3.0	μS
					1.0		1.0		1.0	
C _{iss}	Common-Source Input Capacitance (Note 2)	V _{DS} = 20V, V _{GS} = 0		4.0		4.0		4.0	pF	
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	V _{DG} = 10V, I _S = 0	f = 1MHz		1.2		1.2	1.2		
C _{dgo}	Drain-Gate Capacitance (Note 2)				1.5		1.5	1.5		
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage	V _{DS} = 20V, V _{GS} = 0	f = 1kHz		20		20		20	nV/√Hz
NF	Common-Source Spot Noise Figure (Note 2)	V _{DS} = 20V, V _{GS} = 0 R _G = 10MΩ	f = 100Hz		0.5		0.5		0.5	dB
I _{DSS1} /I _{DSS2}	Drain Saturation Current Ratio	V _{DS} = 20V, V _{GS} = 0		0.95	1.0	0.95	1.0	0.95	1.0	
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage	V _{DS} = 20V, I _D = 200μA			5.0		10.0		15.0	mV
$\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Change with Temperature		T = 25°C to -55°C		0.4		0.8		2.0	
			T = 25°C to +125°C		0.5		1.0		2.5	
g _{fs1} /g _{fs2}	Transconductance Ratio		f = 1kHz	0.97	1.0	0.97	1.0	0.95	1.0	
g _{os1} -g _{os2}	Differential Output Conductance				0.25		0.25		0.25	μS

NOTES: 1. Per transistor.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N5457-2N5459

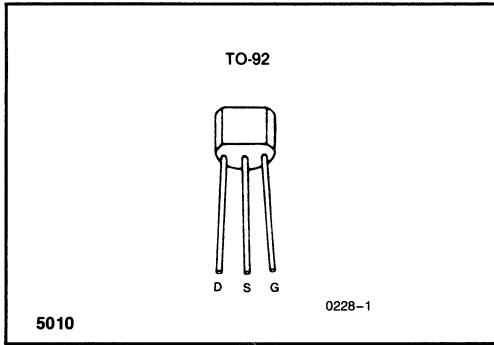
N-Channel JFET

General Purpose Amplifier/Switch



2N5457-2N5459

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage	25V
Drain-Source Voltage	25V
Continuous Forward Gate Current	10mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	310mW
Derate above 25°C	2.82mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
2N5457
2N5458
2N5459

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -10μA, V _{DS} = 0	-25		V
I _{GSS}	Gate Reverse Current	V _{GS} = -15V, V _{DS} = 0		-1.0	nA
		V _{GS} = -15V, V _{DS} = 0, T _A = 100°C		-200	
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 15V, I _D = 10nA	-0.5	-6.0	V
	2N5457		-1.0	-7.0	
	2N5458		-2.0	-8.0	
	2N5459				
V _{GS}	Gate-Source Voltage	V _{DS} = 15V, I _D = 100μA			V
	2N5458	V _{DS} = 15V, I _D = 200μA			
	2N5459	V _{DS} = 15V, I _D = 400μA			
I _{DSS}	Zero-Gate-Voltage Drain Current (Note 1)	V _{DS} = 15V, V _{GS} = 0	1.0	5.0	mA
	2N5457		2.0	9.0	
	2N5458		4.0	16	
	2N5459				
y _{fs}	Forward Transfer Admittance	V _{DS} = 15V, V _{GS} = 0, f = 1kHz	1000	5000	μS
	2N5457		1500	5500	
	2N5458		2000	6000	
	2N5459				
y _{os}	Output Admittance	V _{DS} = 15V, V _{GS} = 0, f = 1kHz		50	μS
C _{iss}	Input Capacitance (Note 2)	V _{DS} = 15V, V _{GS} = 0, f = 1MHz		7.0	pF
C _{rss}	Reverse Transfer Capacitance (Note 2)	V _{DS} = 15V, V _{GS} = 0, f = 1MHz		3.0	pF
NF	Noise Figure (Note 2)	V _{DS} = 15V, V _{GS} = 0, R _G = 1MHz BW = 1Hz, f = 1kHz		3.0	dB

- NOTES:** 1. Pulse test required. PW ≤ 630ms, duty cycle ≤ 10%
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

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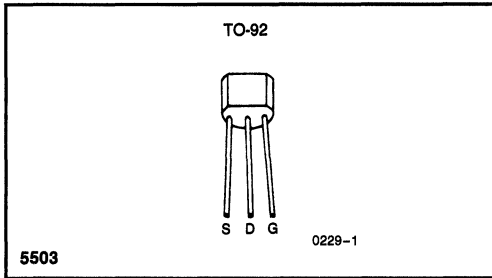
2N5460-2N5465

P-Channel JFET

Low Noise Amplifier



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate or Source-Gate Voltage	
2N5460 - 2N5462	-40V
2N5463 - 2N5465	-60V
Gate Current	10 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	310 mW
Derate above 25°C	2.82 mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
2N5460
2N5461
2N5462
2N5463
2N5464
2N5465

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units		
BV _{GSS}	Gate-Source Breakdown Voltage	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	I _G = 10 μA, V _{DS} = 0	40		V	
				60			
V _{GS(off)}	Gate-Source Cutoff Voltage	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	V _{DS} = -15V, I _D = 1.0 μA	0.75	6.0	V	
				1.0	7.5		
				1.8	9.0		
I _{GSS}	Gate Reverse Current	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	V _{DS} = 0	V _{GS} = 20V	5.0	nA	
				V _{GS} = 30V	5.0		
		2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	T _A = 100°C	V _{GS} = 20V	1.0	μA	
				V _{GS} = 30V	1.0		
I _{DSS}	Zero-Gate Voltage Drain Current	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	V _{DS} = -15V	V _{GS} = 0	-1.0	-5.0	mA
					-2.0	-9.0	
					-4.0	-16	
V _{GS}	Gate-Source Voltage	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465		I _D = 0.1mA	0.5	4.0	V
				I _D = -0.2mA	0.8	4.5	
				I _D = -0.4mA	1.5	6.0	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Test Conditions		Min	Max	Units
g_{fs}	Forward Transadmittance	2N5460, 2N5463	$V_{DS} = 15\text{V}$ $V_{GS} = 0\text{V}$	$f = 1.0\text{kHz}$	1000	4000	μS
		2N5461, 2N5464			1500	5000	
		2N5462, 2N5465			2000	6000	
g_{os}	Output Admittance					75	μS
C_{iss}	Input Capacitance (Note 1)				$f = 1\text{mHz}$	7	pF
C_{rss}	Reverse Transfer Capacitance (Note 1)					2.0	pF
NF	Common-Source Noise Figure (Note 1)			$f = 100\text{Hz}$ $BW = 1.0\text{Hz}$	$R_G = 1.0\text{M}\Omega$	2.5	dB
\bar{e}_n	Equivalent Short-Circuit Input Noise Voltage (Note 1)					115	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$

NOTE 1: For design reference only, not 100% tested.

2N5484-2N5486

2N5484-2N5486

N-Channel JFET

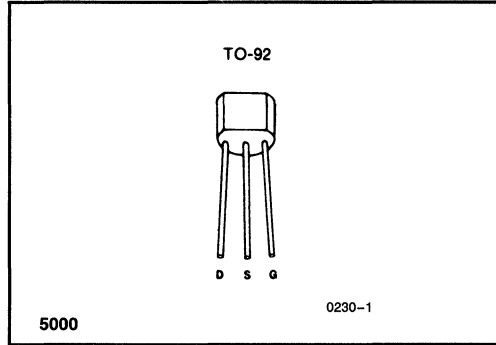
High Frequency Amplifier



FEATURES

- Up to 400MHz Operation
- Economy Packaging
- $C_{rss} < 1.0pF$

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise specified)

Drain-Gate Voltage	25V
Source Gate Voltage	25V
Drain Current	30mA
Forward Gate Current	10mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	310mW
Derate above 25°C	2.82mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
2N5484
2N5485
2N5486

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5484		2N5485		2N5486		Units		
			Min	Max	Min	Max	Min	Max			
I_{GSS}	Gate Reverse Current	$V_{GS} = -20V, V_{DS} = 0$ $T_A = 100^\circ C$		-1.0		-1.0		-1.0	nA		
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-25		-25		-25		V		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V, I_D = 10nA$	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0			
I_{DSS}	Saturation Drain Current	$V_{DS} = 15V, V_{GS} = 0$ (Note 1)	1.0	5.0	4.0	10	8.0	20	mA		
g_{fs}	Common-Source Forward Transconductance	$V_{DS} = 15V, V_{GS} = 0$	f = 1kHz		3000	6000	3500	7000	4000	8000	μS
g_{os}	Common-Source Output Conductance				50		60		75		
$Re_{(yfs)}$	Common-Source Forward Transconductance (Note 2)		f = 100MHz		2500						
			f = 400MHz				3000		3500		
$Re_{(yos)}$	Common-Source Output Conductance (Note 2)		f = 100MHz			75					
			f = 400MHz					100	100		
$Re_{(yis)}$	Common-Source Input Conductance (Note 2)		f = 100MHz			100					
			f = 400MHz					1000	1000		
C_{iss}	Common-Source Input Capacitance (Note 2)		f = 1MHz			5.0		5.0	5.0	pF	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)					1.0		1.0	1.0		
C_{oss}	Common-Source Output Capacitance (Note 2)				2.0		2.0	2.0			

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions		2N5484		2N5485		2N5486		Units
				Min	Max	Min	Max	Min	Max	
NF	Noise Figure (Note 2)	V _{DS} = 15V, V _{GS} = 0, R _G = 1MΩ	f = 1kHz		2.5		2.5		2.5	dB
			f = 100MHz		3.0					
		V _{DS} = 15V, I _D = 4mA, R _G = 1kΩ		f = 400MHz				2.0	2.0	
							4.0	4.0		
G _{ps}	Common-Source Power Gain (Note 2)	V _{DS} = 15V, I _D = 1mA	f = 100MHz	16	25					
						18	30	18	30	
		V _{DS} = 15V, I _D = 4mA	f = 400MHz			10	20	10	20	

NOTES: 1. Pulse test required. Pulse width = 300μs, duty cycle ≤ 3%.
 2. For design reference only, not 100% tested.

2N5515-2N5524

Dual N-Channel JFET

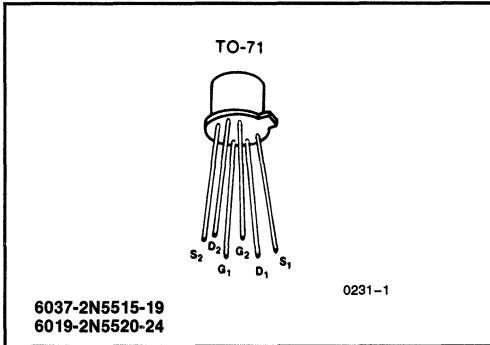
Low Noise Amplifier



FEATURES

- Tight Temperature Tracking
- Tight Matching
- High Common Mode Rejection
- Low Noise

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Source or Gate-Drain Voltage	-40V	
Gate Current (Note 1)	50mA	
Storage Temperature Range	-65°C to +200°C	
Operating Temperature Range	-55°C to +150°C	
Lead Temperature (Soldering, 10sec)	+300°C	

	One Side	Both Sides
Power Dissipation (T _A = 85°C)	250mW	375mW
Derate above 25°C	2.0mW/°C	3.0mW/°C

NOTE: Per transistor.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
2N5515
2N5516
2N5517
2N5518
2N5519
2N5520
2N5521
2N5522
2N5523
2N5524

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units	
I _{GSS}	Gate Reverse Current	V _{GS} = -30V, V _{DS} = 0		-250	pA	
		T _A = 150°C		-250	nA	
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1 μA, V _{DS} = 0	-40		V	
V _P	Gate-Source Pinch-Off Voltage	V _{DS} = 20V, I _D = 1nA	-0.7	-4		
I _{DSS}	Drain Current at Zero Gate Voltage (Note 1)	V _{DS} = 20V, V _{GS} = 0		0.5	7.5	mA
g _{fs}	Common-Source Forward Transconductance (Note 1)		f = 1kHz	1000	4000	
g _{oss}	Common-Source Output Conductance				10	
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 3)		f = 1MHz		5	pF
C _{iss}	Common-Source Input Capacitance (Note 3)				25	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Max	Units	
\bar{e}_n	Equivalent Input Noise Voltage (Note 3)	2N5515-19	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$	f = 10Hz	30	nV/ $\sqrt{\text{Hz}}$	
		2N5520-24			15		
		2N5515-24		f = 1kHz	10		
I_G	Gate Current				-100	pA	
V_{GS}	Gate Source Voltage				-100	nA	
g_{fs}	Common-Source Forward Transconductance (Note 1)				-0.2	-3.8	V
g_{oss}	Common-Source Output Conductance			f = 1kHz	500	1000	μs
						1	μs

MATCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I_{DSS1}/I_{DSS2}	Drain Current Ratio at Zero Gate Voltage (Note 1)	$V_{DS} = 20\text{V}, V_{GS} = 0$	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	
$ I_{G1} - I_{G2} $	Differential Gate Current (+125°C)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		10		10		10		10		10	nA
g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	
$ g_{oss1} - g_{oss2} $	Differential Output Conductance	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$		0.1		0.1		0.1		0.1		0.1	μs
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		5		5		10		15		15	mV
$\Delta V_{GS1} - V_{GS2} $	Gate-Source Voltage Differential Drift ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		5		10		20		40		80	$\frac{\mu\text{V}}{^\circ\text{C}}$
CMRR	Common Mode Rejection Ratio (Note 2, 3)	$V_{DD} = 10$ to $20\text{V}, I_D = 200\mu\text{A}$	100		100		90						dB

- NOTES: 1. Pulse duration of 28ms used during test.
 2. CMRR = $20 \log_{10} \Delta V_{DD} / \Delta |V_{GS1} - V_{GS2}|$, ($\Delta V_{DD} = 10\text{V}$)
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

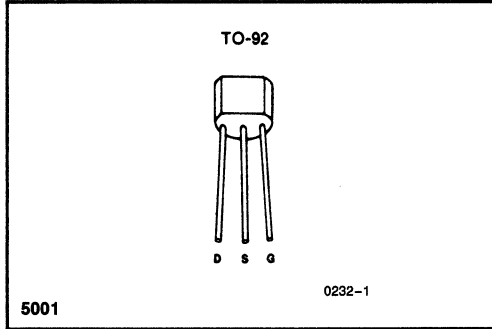
2N5638-2N5640 N-Channel JFET Switch



FEATURES

- Economy Packaging
- Fast Switching
- Low Drain-Source 'ON' Resistance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain-Source Voltage	30V
Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Forward Gate Current	10mA
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+135^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	310mW
Derate above 25°C	2.82mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
2N5638
2N5639
2N5640

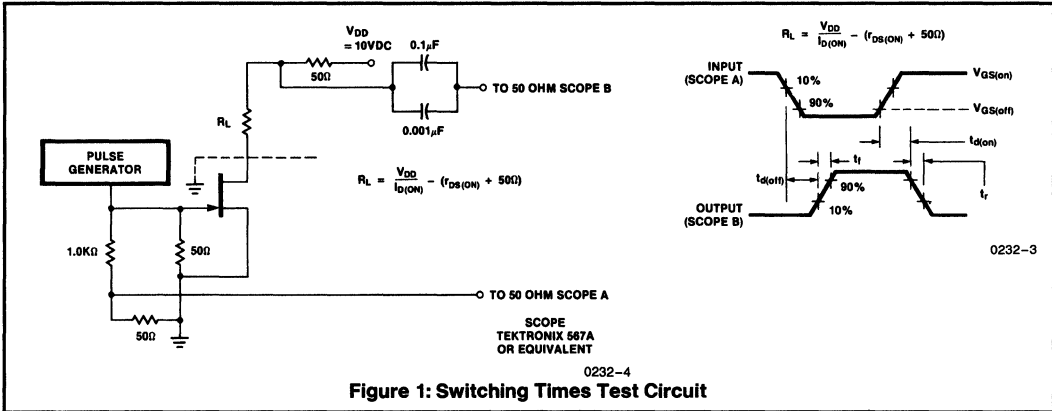
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5638		2N5639		2N5640		Units
			Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate Reverse Breakdown Voltage	$I_G = -10\mu\text{A}, V_{DS} = 0$	-30		-30		-30		V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15\text{V}, V_{DS} = 0$		-1.0		-1.0		-1.0	nA
		$T_A = 100^\circ\text{C}$		-1.0		-1.0		-1.0	μA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 15\text{V}, V_{GS} = -12\text{V}$ (2N5638), $V_{GS} = -8\text{V}$ (2N5639), $V_{GS} = -6\text{V}$ (2N5640)		1.0		1.0		1.0	nA
		$T_A = 100^\circ\text{C}$		1.0		1.0		1.0	μA
I_{DSS}	Saturation Drain Current	$V_{DS} = 20\text{V}, V_{GS} = 0$ (Note 1)	50		25		5.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0, I_D = 12\text{mA}$ (2N5638), $I_D = 6\text{mA}$ (2N5639), $I_D = 3\text{mA}$ (2N5640)		0.5		0.5		0.5	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	$I_D = 1\text{mA}, V_{GS} = 0$		30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0, I_D = 0$		30		60		100	
		$f = 1\text{kHz}$		30		60		100	
C_{iss}	Common-Source Input Capacitance (Note 2)	$V_{GS} = -12\text{V}, V_{DS} = 0$		10		10		10	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	$f = 1\text{MHz}$		4.0		4.0		4.0	
$t_{d(on)}$	Turn-On Delay Time (Note 2)	$V_{DD} = 10\text{V}$ $V_{GS(on)} = 0$ $V_{GS(off)} = -10\text{V}$ $R_G = 50\Omega$		4.0		6.0		8.0	ns
t_r	Rise Time (Note 2)	$I_{D(on)} = 12\text{mA}$ (2N5638) $I_{D(on)} = 6\text{mA}$ (2N5639)		5.0		8.0		10	
t_d	Turn-OFF Delay Time (Note 2)	$I_{D(on)} = 3\text{mA}$ (2N5640)		5.0		10		15	
t_f	Fall Time (Note 2)	(Note 2)		10		20		30	

- NOTES: 1. Pulse test; $PW \leq 300\mu\text{s}$, duty cycle $\leq 3.0\%$.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

2N5902-2N5909

Monolithic Dual N-Channel JFET

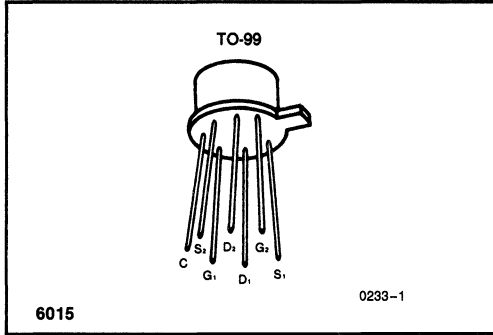
General Purpose Amplifier



FEATURES

- Tight Tracking
- Good Matching

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Gate-Drain or Gate-Source

Voltage (Note 1)	-40V
Gate Current (Note 1)	10mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

One Side Both Sides

Power Dissipation	367mW	500mW
Derate above 25°C	3mW/°C	4mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-99
2N5902
2N5903
2N5904
2N5905
2N5906
2N5907
2N5908
2N5909

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5902-6		2N5903-7		2N5904-8		2N5905-9		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
$ I_{G1} - I_{G2} $	Differential Gate Current	$V_{DG} = 10V$, $I_D = 30\mu A$, $T_A = 125^\circ\text{C}$	2N5902-5	2.0	2.0	2.0	2.0	2.0	2.0	2.0	nA
			2N5906-9	0.2	0.2	0.2	0.2	0.2	0.2		
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	$V_{DS} = 10V$, $V_{GS} = 0$	0.95	1	0.95	1	0.95	1	0.95	1	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	$f = 1\text{kHz}$	0.97	1	0.97	1	0.95	1	0.95	1	
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage			5		5		10		15	mV
$\Delta V_{GS1} - V_{GS2} $	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)	$V_{DG} = 10V$, $I_D = 30\mu A$		5		10		20		40	$\mu\text{V}/^\circ\text{C}$
ΔT		$T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$		5		10		20		40	
		$T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$		5		10		20		40	
$ g_{os1} - g_{os2} $	Differential Output Conductance	$f = 1\text{kHz}$		0.2		0.2		0.2		0.2	μS

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5902-5		2N5906-9		Units	
			Min	Max	Min	Max		
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\text{V}, V_{DS} = 0$ $T_A = 125^\circ\text{C}$		-5		-2	pA	
				-10		-5	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-40		-40		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10\text{V}, I_D = 1\text{nA}$	-0.6	-4.5	-0.6	-4.5		
V_{GS}	Gate Source Voltage	$V_{DG} = 10\text{V}, I_D = 30\mu\text{A}$		-4		-4		
I_G	Gate Operating Current	$T_A = 125^\circ\text{C}$		-3		-1	pA	
				-3		-1	nA	
I_{DSS}	Saturation Drain Current	$V_{DS} = 10\text{V}, V_{GS} = 0$	f = 1kHz	30	500	30	500	μA
g_{fs}	Common-Source Forward Transconductance			70	250	70	250	μS
g_{os}	Common-Source Output Conductance				5		5	
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0$ (Note 1)	f = 1MHz		3		3	pF
C_{rss}	Common-Source Reverse Transfer Capacitance				1.5		1.5	
g_{fs}	Common-Source Forward Transconductance	$V_{DG} = 10\text{V}, I_D = 30\mu\text{A}$	f = 1kHz	50	150	50	150	μS
g_{os}	Common-Source Output Conductance				1		1	
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage (Note 1)			$V_{DS} = 10\text{V}, V_{GS} = 0$		0.2		0.1
NF	Spot Noise Figure (Note 1)		f = 100Hz $R_G = 10\text{M}\Omega$		3		1	dB

NOTE 1: For design reference only, not 100% tested.

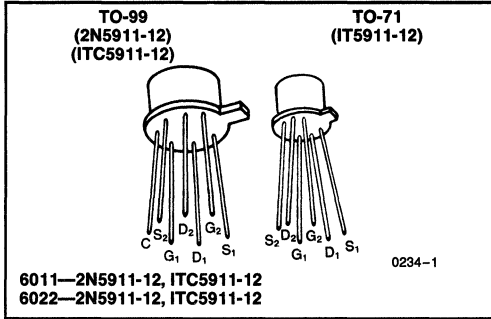
2N5911, 2N5912, ITC5911, ITC5912, IT5911, IT5912 Dual N-Channel JFET High Frequency Amplifier



FEATURES

- Tight Tracking
- Low Insertion Loss
- Good Matching

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Drain or Gate-Source Voltage -25V
 Gate Current 50mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$

	TO-71		TO-99	
	One Side	Both Sides	One Side	Both Sides

Power

Dissipation 200mW 400mW 367mW 500mW

Derate above

25°C 1.6mW/ $^\circ\text{C}$ 3.2mW/ $^\circ\text{C}$ 3.0mW/ $^\circ\text{C}$ 4.0mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71	TO-99	Wafer	Dice
IT5911	2N5911	2N5911/W	2N5911/D
IT5912	2N5912	2N5912/W	2N5912/D

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units	
I_{GSS}	Gate Reverse Current	$V_{GS} = -15V, V_{DS} = 0$		-100	pA	
		$T_A = 150^\circ\text{C}$		-250	nA	
BV_{GSS}	Gate Reverse Breakdown Voltage	$I_G = -1\mu A, V_{DS} = 0$	-25		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10V, I_D = 1nA$	-1	-5		
V_{GS}	Gate-Source Voltage	$V_{DG} = 10V, I_D = 5mA$	-0.3	-4	pA	
I_G	Gate Operating Current	$T_A = 150^\circ\text{C}$		-100		
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μ s, duty cycle $\leq 3\%$)	$V_{DS} = 10V, V_{GS} = 0V$	7	40	mA	
g_{fs}	Common-Source Forward Transconductance	$V_{DG} = 10V, I_D = 5mA$	$f = 1kHz$	5000	10,000	μ s
g_{fs}	Common-Source Forward Transconductance (Note 1)		$f = 100MHz$	5000	10,000	
g_{os}	Common-Source Output Conductance		$f = 1kHz$		100	
g_{oss}	Common-Source Output Conductance (Note 1)		$f = 100MHz$		150	
C_{iss}	Common-Source Input Capacitance (Note 1)		$f = 1MHz$		5	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)				1.2	
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage (Note 1)	$f = 10kHz$		20	$\frac{nV}{\sqrt{Hz}}$	
NF	Spot Noise Figure (Note 1)	$f = 10kHz$ $R_G = 100k\Omega$		1	dB	

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NOTE: All typical values have been characterized but are not tested.

2N5911, 2N5912, ITC5911, ITC5912, IT5911, IT5912



2N5911, 2N5912, ITC5911, ITC5912, IT5911, IT5912

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions		IT, 2N5911		IT, 2N5912		Units				
				Min	Max	Min	Max					
$ I_{G1}-I_{G2} $	Differential Gate Current	$V_{DG} = 10\text{V}$	$I_D = 5\text{mA}$	$T_A = 125^\circ\text{C}$			20	20	nA			
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	$V_{DS} = 10\text{V}$		$V_{GS} = 0$		(Pulsewidth $300\mu\text{s}$, duty cycle $\leq 3\%$)		0.95	1	0.95	1	
$ V_{GS1}-V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 10\text{V}$		$I_D = 5\text{mA}$			10		15	mV		
$\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)					$T_A = 25^\circ\text{C}$	$T_B = 125^\circ\text{C}$		20		40	$\mu\text{V}/^\circ\text{C}$
						$T_A = -55^\circ\text{C}$	$T_B = 25^\circ\text{C}$		20		40	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio					$f = 1\text{kHz}$	0.95	1	0.95	1		

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

2N6483-2N6485

Dual N-Channel JFET

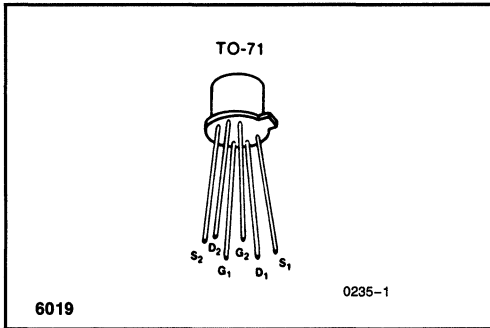
Low Noise Amplifier



FEATURES

- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate-Gate Voltage	$\pm 50\text{V}$
Gate Current (Note 1)	50mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+175^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation	250mW	400mW
Derate above 25°C	1.7mW/ $^\circ\text{C}$	2.7mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
2N6483
2N6484
2N6485

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{GSS}	Gate Reverse Current	$V_{GS} = -30\text{V}, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-200	pA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-50	-200	nA
V_p	Gate-Source Pinch Off Voltage	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$	-0.7	-4.0	V
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	$V_{DS} = 20\text{V}, V_{GS} = 0$	0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{kHz}$ (Note 6)	1000	4000	μs
g_{oss}	Common-Source Output Conductance				
C_{iss}	Common-Source Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0, f = 1\text{MHz}$ (Note 6)		20	pF
C_{rss}	Common-Source Reverse Transfer Capacitance			3.5	
I_G	Gate Current	$V_{GD} = 20\text{V}, I_D = 200\mu\text{A}$ (Note 6) $T_A = 150^\circ\text{C}$		100	pA
				100	nA
V_{GS}	Gate Source Voltage	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$	0.2	3.8	V
g_{fs}	Common-Source Forward Transconductance	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$	500	1500	μs
g_{os}	Common-Source Output Conductance	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		1	
\bar{e}_n	Equivalent Input Noise Voltage (Note 6)	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 10\text{Hz}$ $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$		10	nV/ $\sqrt{\text{Hz}}$
				5	

- NOTES:**
1. Per transistor.
 2. Pulse test required; pulse width = 2ms.

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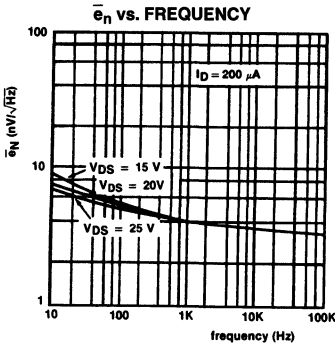
NOTE: All typical values have been characterized but are not tested.

MATCHING CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

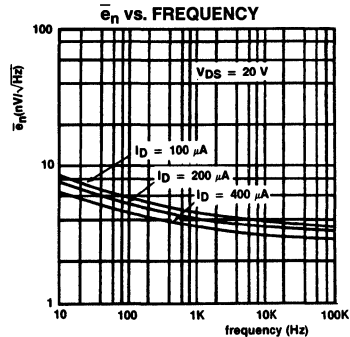
Symbol	Parameter	Test Conditions	2N6483		2N6484		2N6485		Units
			Min	Max	Min	Max	Min	Max	
I_{DSS1} I_{DSS2}	Drain Current Ratio at Zero Gate Voltage	$V_{DS} = 20\text{V}, V_{GS} = 0$ (Note 4)	0.95	1	0.95	1	0.95	1	
$ I_{G1} - I_{G2} $	Differential Gate Current	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$ $T_A = +125^\circ\text{C}$		10		10		10	nA
g_{fs1} g_{fs2}	Transconductance Ratio	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$, $f = 1\text{kHz}$ (Note 4)	0.97	1	0.97	1	0.95	1	
$ g_{os1} - g_{os2} $	Differential Output Conductance (Note 6)	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$, $f = 1\text{kHz}$		0.1		0.1		0.1	μs
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$		5		10		15	mV
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift	$V_{DG} = 20\text{V}, I_D = 200\mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		5		10		25	$\mu\text{V}/^\circ\text{C}$
CMRR	Common Mode Rejection Ratio (Note 6)	$V_{DD} = 10$ to 20V , $I_D = 200\mu\text{A}$ (Note 5)	100		100		90		dB

- NOTES: 3. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
 4. Pulse duration of 2ms used during test.
 5. $\text{CMRR} = 20\text{Log}_{10} \Delta V_{DD} / \Delta |V_{GS1} - V_{GS2}|$, ($\Delta V_{DD} = 10\text{V}$), not included in JEDEC registration.
 6. For design reference only, not 100% tested.

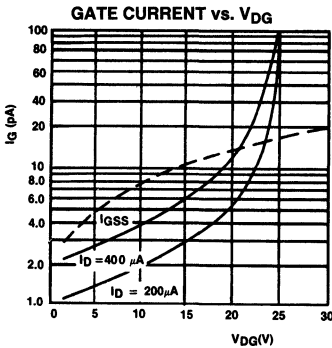
TYPICAL PERFORMANCE CHARACTERISTICS



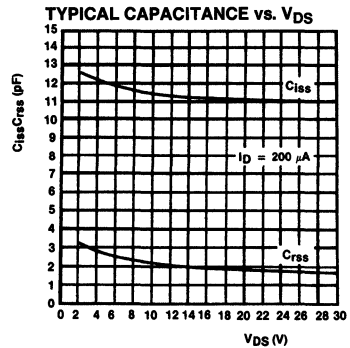
0235-3



0235-4



0235-5



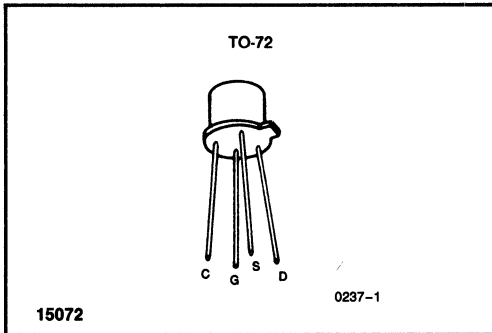
0235-6

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NOTE: All typical values have been characterized but are not tested.

3N161**Diode Protected P-Channel
Enhancement Mode MOSFET
General Purpose Amplifier/Switch****FEATURES**

- Channel Cut Off With Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate From Damage Due to Overvoltage

PIN CONFIGURATION**ABSOLUTE MAXIMUM RATINGS**(T_A = 25°C unless otherwise noted)

Drain-Source or Drain-Gate Voltage	40V
Drain Current	50mA
Gate Forward Current	10μA
Gate Reverse Current	1mA
Storage Temperature	-65°C to +200°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	375mW
Derate above 25°C	3.0mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
3N161

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{BS} = 0 unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units	
I _{GSSF}	Forward Gate-Terminal Current	V _{GS} = -25V, V _{DS} = 0 T _A = +100°C		-100 -10	pA nA	
BV _{GSS}	Forward Gate-Source Break-down Voltage	I _G = -0.1mA, V _{DS} = 0	-25		V	
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} = -15V, V _{GS} = 0 V _{DS} = -25V, V _{GS} = 0		-10 -10	nA μA	
V _{GS(th)}	Gate-Source Threshold Voltage	V _{DS} = -15V, I _D = -10μA	-1.5	-5	V	
V _{GS}	Gate-Source Voltage	V _{DS} = -15V, I _D = -8mA	-4.5	-8		
I _{D(on)}	On-State Drain Current (Note 2)	V _{DS} = -15V, V _{GS} = -15V	-40	-120	mA	
Y _{fs}	Small-Signal Common-Source Forward Transfer Admittance	V _{DS} = -15V, I _D = -8mA	f = 1kHz	3500	6500	μs
Y _{os}	Small-Signal Common-Source Output Admittance				250	
C _{iss}	Common-Source Short-Circuit Input Capacitance (Note 1)		f = 1MHz		10	pF
C _{rss}	Common-Source Short Circuit Reverse Transfer Capacitance (Note 1)				4	

NOTE 1: For design reference only, not 100% tested.

2: Pulse test duration 300 μs; duty cycle ≤ 3%

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NOTE: All typical values have been characterized but are not tested.

3N163, 3N164

P-Channel Enhancement Mode MOSFET General Purpose Amplifier Switch

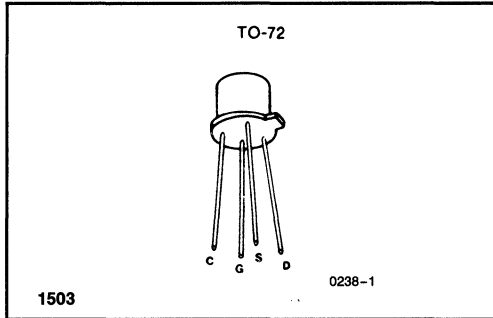


3N163, 3N164

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage	
3N163	-40V
3N164	-30V
Static Gate-Source Voltage	
3N163	$\pm 40\text{V}$
3N164	$\pm 30\text{V}$
Transient Gate-Source Voltage (Note 2)	$\pm 125\text{V}$
Drain Current	50mA
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	375mW
Derate above $+25^\circ\text{C}$	3.0mW/ $^\circ\text{C}$

- NOTES:**
1. See handling precautions on 3N170 data sheet.
 2. Devices must not be tested at $\pm 125\text{V}$ more than once, nor for longer than 300ms.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
3N163
3N164

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	3N163		3N164		Units
			Min	Max	Min	Max	
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = -40\text{V}, V_{DS} = 0$ (3N163) $V_{GS} = -30\text{V}, V_{DS} = 0$ (3N164) $T_A = +125^\circ\text{C}$		-10		-10	pA
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -10\mu\text{A}, V_{GS} = 0$	-40		-30		V
BV_{SDS}	Source-Drain Breakdown Voltage	$I_S = -10\mu\text{A}, V_{GD} = 0, V_{BD} = 0$	-40		-30		
$V_{GS(th)}$	Threshold Voltage	$V_{DS} = V_{GS}, I_D = -10\mu\text{A}$	-2.0	-5.0	-2.0	-5.0	
$V_{GS(th)}$	Threshold Voltage	$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$	-2.0	-5.0	-2.0	-5.0	
V_{GS}	Gate Source Voltage	$V_{DS} = -15\text{V}, I_D = -0.5\text{mA}$	-2.5	-6.5	-2.5	-6.5	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -15\text{V}, V_{GS} = 0$		200		400	pA
I_{SDS}	Source Drain Current	$V_{SD} = 15\text{V}, V_{GS} = V_{DB} = 0$		400		800	
$r_{DS(on)}$	Drain-Source on Resistance	$V_{GS} = -20\text{V}, I_D = -100\mu\text{A}$		250		300	ohms
$I_{D(on)}$	On Drain Current	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$	-5.0	-30.0	-3.0	-30.0	mA

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NOTE: All typical values have been characterized but are not tested.

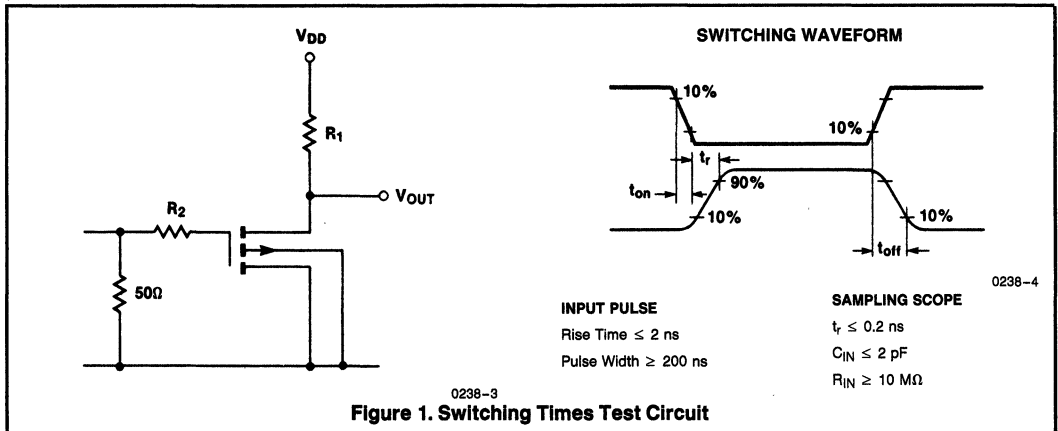
ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	3N163		3N164		Units
			Min	Max	Min	Max	
g_{fs}	Forward Transconductance	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 1\text{kHz}$	2000	4000	1000	4000	μs
g_{os}	Output Admittance			250		250	
C_{iss}	Input Capacitance—Output Shorted	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 1\text{MHz}$ (Note 1)		2.5		2.5	pF
C_{rss}	Reverse Transfer Capacitance			0.7		0.7	
C_{oss}	Output Capacitance Input Shorted			3.0		3.0	

NOTE 1: For design reference only, not 100% tested.

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	3N163		3N164		Units
			Min	Max	Min	Max	
t_{on}	Turn-On Delay Time	$V_{DD} = -15\text{V}$ $I_{D(on)} = -10\text{mA}$ (Note 1) $R_G = R_L = 1.4\text{k}\Omega$		12		12	ns
t_r	Rise Time			24		24	
t_{off}	Turn-Off Time			50		50	



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NOTE: All typical values have been characterized but are not tested.

3N165, 3N166

Monolithic Dual P-Channel Enhancement Mode MOSFET General Purpose Amplifier

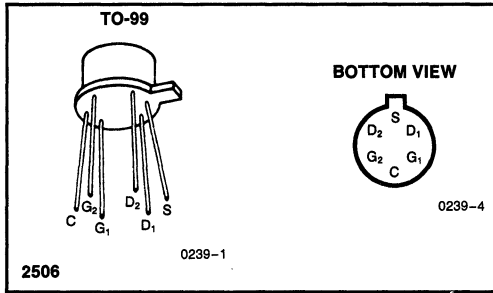


3N165, 3N166

FEATURES

- Very High Impedance
- High Gate Breakdown
- Low Capacitance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain-Source or Drain-Gate Voltage (Note 2)

3N165	40V
3N166	30V

Transient Gate-Source Voltage (Note 3) ± 125

Gate-Gate Voltage $\pm 80\text{V}$

Drain Current (Note 2) 50mA

Storage Temperature -65°C to $+200^\circ\text{C}$

Operating Temperature -55°C to $+150^\circ\text{C}$

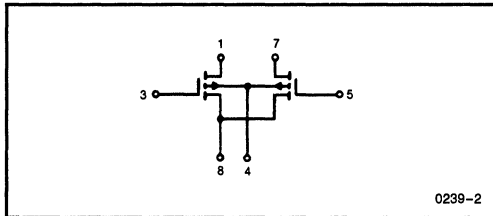
Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$

Power Dissipation

One Side	300mW
Both Sides	525mW
Total Derating above 25°C	4.2mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DEVICE SCHEMATIC



ORDERING INFORMATION

TO-99
3N165
3N166

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{GSSR}	Gate Reverse Leakage Current	$V_{GS} = 40\text{V}$		10	pA
I_{GSSF}	Gate Forward Leakage Current	$V_{GS} = -40\text{V}$		-10	
		$T_A = +125^\circ\text{C}$		-25	
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = -20\text{V}$		-200	
I_{SDS}	Source to Drain Leakage Current	$V_{SD} = -20, V_{DB} = 0$		-400	
$I_{D(on)}$	On Drain Current	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$	-5	-30	mA
$V_{GS(th)}$	Gate Source Threshold Voltage	$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$	-2	-5	V
$V_{GS(th)}$	Gate Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -10\mu\text{A}$	-2	-5	
$r_{DS(on)}$	Drain Source ON Resistance	$V_{GS} = -20\text{V}, I_D = -100\mu\text{A}$		300	ohms

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ and $V_{BS}=0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
g_{fs}	Forward Transconductance	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 1\text{kHz}$	1500	3000	μs
g_{os}	Output Admittance			300	
C_{iss}	Input Capacitance	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 1\text{MHz}$ (Note 4)		3.0	pF
C_{rSS}	Reverse Transfer Capacitance			0.7	
C_{oss}	Output Capacitance			3.0	
$R_E(Y_{fs})$	Common Source Forward Transconductance	$V_{DS} = -15\text{V}, I_D = -10\text{mA}, f = 100\text{MHz}$ (Note 4)	1200		μs

MATCHING CHARACTERISTICS 3N165

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}, f = 1\text{kHz}$	0.90	1.0	
V_{GS1-2}	Gate Source Threshold Voltage Differential	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$		100	mV
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature	$V_{DS} = -15\text{V}, I_A = -500\mu\text{A}$ $T_A = -55^\circ\text{C}$ to $+25^\circ\text{C}$		100	$\mu\text{V}/^\circ\text{C}$

- NOTES 1. See handling precautions on 3N170 data sheet.
 2. Per transistor.
 3. Devices must not be tested at $\pm 125\text{V}$ more than once, nor for longer than 300ms.
 4. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

3N170, 3N171

N-Channel Enhancement Mode MOSFET Switch

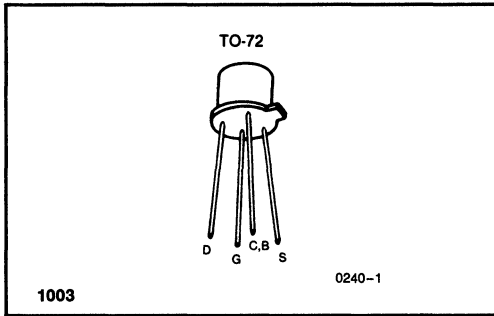


3N170, 3N171

FEATURES

- Low Switching Voltages
- Fast Switching Times
- Low Drain-Source Resistance
- Low Reverse Transfer Capacitance

PIN CONFIGURATION



ORDERING INFORMATION

TO-72
3N170
3N171

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	±35V
Drain-Source Voltage	25V
Gate-Source Voltage	±35V
Drain Current	30mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.4mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

Symbol	Parameter	Test Conditions	Limits		Units	
			Min	Max		
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 10\mu\text{A}, V_{GS} = 0$	25		V	
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 35\text{V}, V_{DS} = 0$		±10	pA	
		$V_{GS} = 35\text{V}, V_{DS} = 0, T_A = 125^\circ\text{C}$		100		
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = 10\text{V}, V_{GS} = 0$		10	nA	
		$T_A = 125^\circ\text{C}$		1.0	μA	
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{DS} = 10\text{V}, I_D = 10\mu\text{A}$	3N170	1.0	2.0	V
			3N171	1.5	3.0	
$I_{D(on)}$	"ON" Drain Current	$V_{GS} = 10\text{V}, V_{DS} = 10\text{V}$	10		mA	
$V_{DS(on)}$	Drain-Source "ON" Voltage	$I_D = 10\text{mA}, V_{GS} = 10\text{V}$		2.0	V	
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 10\text{V}, I_D = 0, f = 1.0\text{kHz}$		200	Ω	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified) Substrate connected to source.

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$ Y_{fs} $	Forward Transfer Admittance	$V_{DS} = 10\text{V}$, $I_D = 2.0\text{mA}$, $f = 1.0\text{kHz}$	1000		μS
C_{rss}	Reverse Transfer Capacitance (Note 1)	$V_{DS} = 0$, $V_{GS} = 0$, $f = 1.0\text{MHz}$		1.3	pF
C_{iss}	Input Capacitance (Note 1)	$V_{DS} = 10\text{V}$, $V_{GS} = 0$, $f = 1.0\text{MHz}$		5.0	
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 1)	$V_{D(SUB)} = 10\text{V}$, $f = 1.0\text{MHz}$		5.0	
$t_{d(on)}$	Turn-On Delay Time (Note 1)	$V_{DD} = 10\text{V}$, $I_{D(on)} = 10\text{mA}$, $V_{GS(on)} = 10\text{V}$, $V_{GS(off)} = 0$, $R_G = 50\Omega$		3.0	ns
t_r	Rise Time (Note 1)			10	
$t_{d(off)}$	Turn-Off Delay Time (Note 1)			3.0	
t_f	Fall Time (Note 1)			15	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

3N172, 3N173

Diode Protected P-Channel Enhancement Mode MOSFET General Purpose Amplifier/Switch

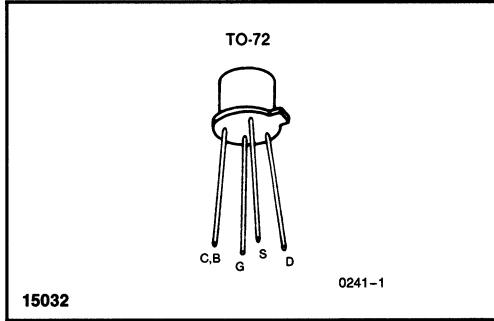


3N172, 3N173

FEATURES

- High Input Impedance
- Diode Protected Gate

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage

3N172	40V
3N173	30V

Drain Current 50mA

Gate Forward Current 10 μA

Gate Reverse Current 1mA

Storage Temperature -65°C to $+200^\circ\text{C}$

Operating Temperature -55°C to $+150^\circ\text{C}$

Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$

Power Dissipation 375mW

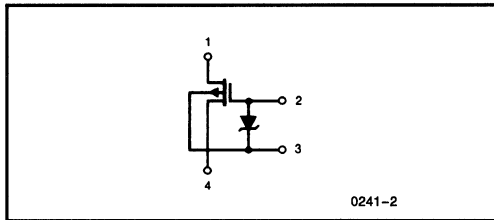
Derate above 25°C 3.0mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION*

TO-72
3N172
3N173

DEVICE SCHEMATIC



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	3N172		3N173		Units
			Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\text{V}$		-200		-500	pA
		$T_A = +125^\circ\text{C}$		-0.5		-1.0	μA
BV_{GSS}	Gate Breakdown Voltage	$I_D = -10\mu\text{A}$	-40	-125	-30	-125	V
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -10\mu\text{A}$	-40		-30		
BV_{SDS}	Source-Drain Breakdown Voltage	$I_S = -10\mu\text{A}, V_{DB} = 0$	-40		-30		
$V_{GS(th)}$	Threshold Voltage	$V_{DS} = V_{GS}, I_D = -10\mu\text{A}$	-2.0	-5.0	-2.0	-5.0	
		$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$	-2.0	-5.0	-2.0	-5.0	
V_{GS}	Gate Source Voltage	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$	-3.0	-6.5	-2.5	-6.5	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -15\text{V}, V_{GS} = 0$		-0.4		-10	nA
I_{SDS}	Zero Gate Voltage Source Current	$V_{SD} = -15\text{V}, V_{DB} = 0, V_{GD} = 0$		-0.4		-10	
$r_{DS(on)}$	Drain Source On Resistance	$V_{GS} = -20\text{V}, I_D = -100\mu\text{A}$		250		350	ohms
$I_{D(on)}$	On Drain Current	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$	-5.0	-30	-5.0	-30	mA

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NOTE: All typical values have been characterized but are not tested.

3N172, 3N173



Small-Signal Electrical Characteristics $T_A = 25^\circ\text{C}$ and Bulk (substrate) Lead Connected to Source

Symbol	Parameter	Test Conditions	3N172		3N173		Units
			Min	Max	Min	Max	
$ y_{fs} $	Magnitude of Small-Signal, Common-Source, Short-Circuit, Forward Transadmittance*	$V_{DS} = -15\text{V}$, $I_D = -10\text{mA}$, $f = 1\text{kHz}$	1500	4000	1000	4000	μmhos
$ y_{os} $	Magnitude of Small-Signal, Common-Source, Short-Circuit, Output Admittance*	$V_{DS} = -15\text{V}$, $I_D = -10\text{mA}$, $f = 1\text{kHz}$		250		250	μmhos
C_{iss}	Small-Signal, Common-Source, Short-Circuit, Input Capacitance*	$V_{DS} = -15\text{V}$, $I_D = -10\text{mA}$, $f = 1\text{MHz}$		3.5		3.5	pF
C_{rss}	Small-Signal, Common-Source, Short-Circuit, Reverse Transfer Capacitance*	$V_{DS} = -15\text{V}$, $I_D = -10\text{mA}$, $f = 1\text{MHz}$		1.0		1.0	pF
C_{oss}	Small-Signal, Common-Source, Short-Circuit, Output Capacitance*	$V_{DS} = -15\text{V}$, $I_D = -10\text{mA}$, $f = 1\text{MHz}$		3.0		3.0	pF

Noise Characteristics

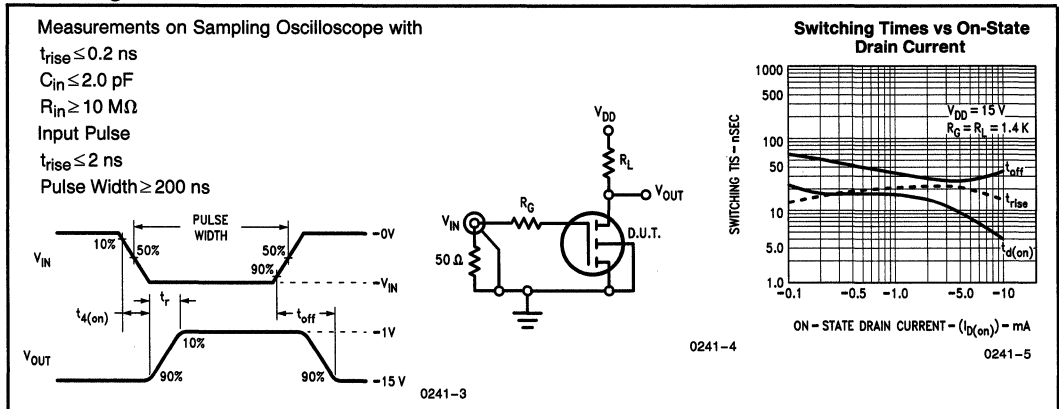
Symbol	Parameter	Test Conditions	Typical	Units
NF	Common-Source Spot Noise Figure	$V_{DS} = -15\text{V}$, $I_D = -1\text{mA}$, $f = 1\text{kHz}$, $R_G = 1\text{M}\Omega$	1.0	dB

Switching Characteristics $T_A = 25^\circ\text{C}$ Bulk (substrate) Lead Connected to Source

Symbol	Parameter	Test Conditions	3N172		3N173		Units
			Min	Max	Min	Max	
$t_{d(on)}$	Turn-On Delay Time*	$V_{DD} = -15\text{V}$, $I_{D(on)} = -10\text{mA}$		12		12	ns
t_r	Rise Time*	$R_G = R_L = 1.4\text{k}\Omega$		24		24	ns
t_{off}	Turn-Off Time*	See Test Circuit Below		50		50	ns

*Registered JEDEC Data

Switching Time Detail



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NOTE: All typical values have been characterized but are not tested.

3N188-3N191

Dual P-Channel Enhancement Mode MOSFET General Purpose Amplifier

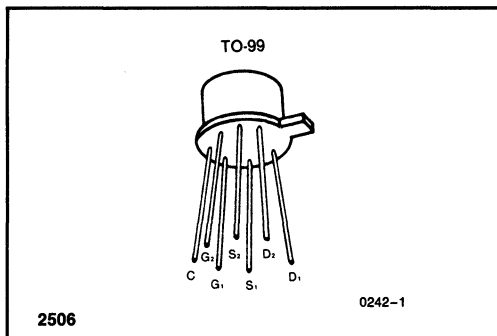


3N188-3N191

FEATURES

- Very High Input Impedance
- High Gate Breakdown 3N190-3N191
- Zener Protected Gate 3N188-3N189
- Low Capacitance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source or Drain-Gate Voltage (Note 1)	40V
3N188, 3N189	30V
3N190, 3N191	$\pm 125\text{V}$
Transient Gate-Source Voltage (Notes 1 and 2)	$\pm 80\text{V}$
Gate-Gate Voltage	50mA
Drain Current (Note 1)	-65°C to $+200^\circ\text{C}$
Storage Temperature	-55°C to $+150^\circ\text{C}$
Operating Temperature	$+300^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	Power Dissipation
	One Side
	Both Sides
Total Derating above 25°C	300mW
	525mW
	4.2mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-99
3N188
3N189
3N190
3N191

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	3N188 3N189		3N190 3N191		Units
			Min	Max	Min	Max	
I_{GSSR}	Gate Reverse Current	$V_{GS} = 40\text{V}$				10	pA
I_{GSSF}	Gate Forward Current	$V_{GS} = -40\text{V}$		-200		-10	
		$T_A = 125^\circ\text{C}$		-200		-25	
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -10\mu\text{A}$	-40		-40		V
BV_{SDS}	Source-Drain Breakdown Voltage	$I_S = -10\mu\text{A}, V_{BD} = 0$	-40		-40		
$V_{GS(th)}$	Threshold Voltage	$V_{DS} = -15\text{V}, I_D = -10\mu\text{A}$	-2.0	-5.0	-2.0	-5.0	V
		$V_{DS} = V_{GS}, I_D = -10\mu\text{A}$	-2.0	-5.0	-2.0	-5.0	
V_{GS}	Gate Source Voltage	$V_{DS} = -15\text{V}, I_D = -500\mu\text{A}$	-3.0	-6.5	-3.0	-6.5	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -15\text{V}$		-200		-200	pA
I_{SDS}	Source Drain Current	$V_{SD} = -15\text{V}, V_{DB} = 0$		-400		-400	
$r_{DS(on)}$	Drain-Source on Resistance	$V_{DS} = -20\text{V}, I_D = -100\mu\text{A}$		300		300	ohms
$I_{D(on)}$	On Drain Current	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}$	-5.0	-30.0	-5.0	-30.0	mA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	3N188 3N189		3N190 3N191		Units
			Min	Max	Min	Max	
g_{fs}	Forward Transconductance (Note 3)	$V_{DS} = -15\text{V}$, $I_D = -10\text{mA}$	1500	4000	1500	4000	μs
Y_{OS}	Output Admittance						
C_{ISS}	Input Capacitance Output Shorted (Note 5)	$f = 1\text{MHz}$		4.5		4.5	pF
C_{RSS}	Reverse Transfer Capacitance (Note 5)			1.5		1.0	
C_{OSS}	Output Capacitance Input Shorted (Note 5)			3.0		3.0	

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$t_{d(on)}$	Turn On Delay Time	$V_{DD} = -15\text{V}$, $I_D = -10\text{mA}$ $R_G = R_L = 1.4\text{k}\Omega$ (Note 5)		15	ns
t_r	Rise Time			30	
t_{off}	Turn Off Time			50	

MATCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified) 3N188 and 3N190

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	$V_{DS} = -15\text{V}$, $I_D = -500\mu\text{A}$, $f = 1\text{kHz}$	0.85	1.0	
V_{GS1-2}	Gate Source Threshold Voltage Differential	$V_{DS} = -15\text{V}$, $I_D = -500\mu\text{A}$		100	mV
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	$V_{DS} = -15\text{V}$, $I_D = -500\mu\text{A}$, $T = -55^\circ\text{C}$ to $+25^\circ\text{C}$		100	$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature (Note 4)	$V_{DS} = -15\text{V}$, $I_D = -500\mu\text{A}$, $T = +25^\circ\text{C}$ to $+125^\circ\text{C}$		100	$\mu\text{V}/^\circ\text{C}$

- NOTES: 1. Per transistor.
 2. Approximately doubles for every 10°C increase in T_A .
 3. Pulse test duration = $300\mu\text{s}$; duty cycle $\leq 3\%$.
 4. Measured at end points, T_A and T_B .
 5. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

ID100, ID101

Dual Low Leakage Diode

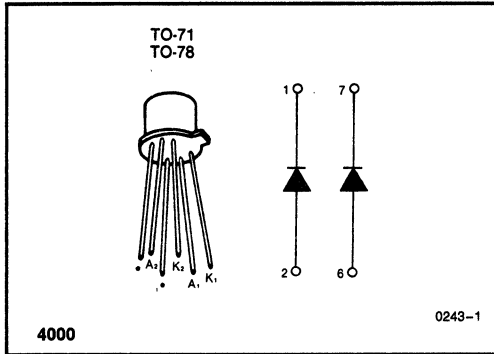


ID100, ID101

GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

PIN CONFIGURATIONS



FEATURES

- $I_R = 0.1\text{pA}$ (Typical)
- $BV_R > 30\text{V}$
- $C_{rss} = 0.75\text{pF}$ (Typical)

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Diode Reverse Voltage	30V
Diode to Diode Voltage	$\pm 50\text{V}$
Forward Current	20mA
Reverse Current	100 μA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	300mW
Derate above 25°C	2.4mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO78	TO71
ID100	ID101

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	ID100, ID101			Units
			Min	Typ	Max	
V_F	Forward Voltage Drop	$I_F = 10\text{mA}$	0.8		1.1	V
BV_R	Reverse Breakdown Voltage	$I_R = 1\mu\text{A}$	30			V
I_R	Reverse Leakage Current	$V_R = 1\text{V}$		0.1		pA
		$V_R = 10\text{V}$		2.0	10	
		$T_A = 125^\circ\text{C}$				10
$ I_{R1} - I_{R2} $	Differential Leakage Current	$V_R = 10\text{V}$			3	pA
C_{rss}	Total Reverse Capacitance	$V_R = 10\text{V}, f = 1\text{Hz}$ (Note 1)		0.75	1	pF

NOTE 1: For design reference only, not 100% tested.

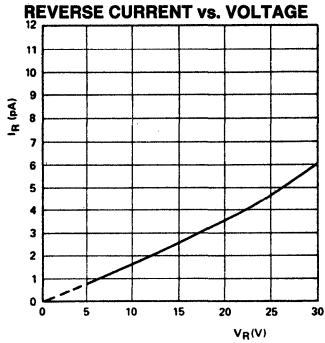
2: Pins 3 and 5 should not be connected together nor connected to the circuit in any way.

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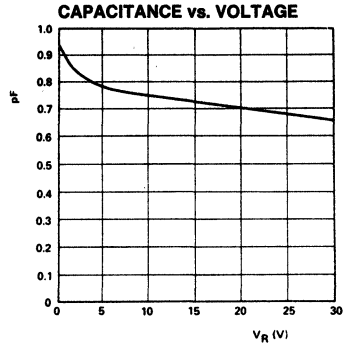
NOTE: All typical values have been characterized but are not tested.

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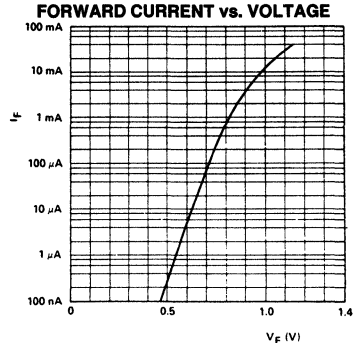
TYPICAL PERFORMANCE CHARACTERISTICS



0243-3



0243-4



0243-5

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NOTE: All typical values have been characterized but are not tested.

IT100, IT101

P-Channel JFET Switch

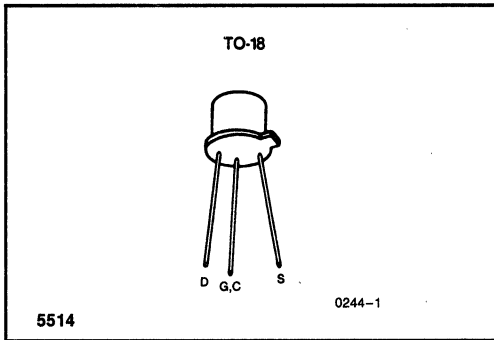


IT100, IT101

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with TTL logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of $\pm 15V$ can be switched. The FET is OFF for hi level inputs ($+5V$ or $+15V$) and ON for low level inputs ($<0.5 V$ for IT100, $<1.5V$ for IT101).

PIN CONFIGURATION



FEATURES

- Interfaces Directly w/TTL Logic Elements
- $r_{DS(on)} < 75\Omega$ for 5V Logic Drive
- $I_{D(off)} < 100pA$

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise noted)

Gate-Source Voltage	35V
Gate-Drain Voltage	35V
Gate Current	50mA
Storage Temperature Range	$-65^\circ C$ to $+200^\circ C$
Operating Temperature Range	$-55^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10sec)	$+300^\circ C$
Power Dissipation	300mW
Derate above $25^\circ C$	2.4mW/ $^\circ C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
IT100
IT101

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT100		IT101		Units
			Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = 20V, V_{DS} = 0$		200		200	pA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu A, V_{DS} = 0$	35		35		V
V_P	Pinch Off Voltage	$I_D = 1nA, V_{DS} = -15V$	2	4.5	4	10	
I_{DSS}	Drain Current	$V_{GS} = 0, V_{DS} = -15V$	-10		-20		mA
g_{fs}	Transconductance	$V_{GS} = 0, V_{DS} = -15V$	8		8		mS
g_{os}	Output Conductance			1		1	
$I_{D(off)}$	Drain (OFF) Leakage	$V_{DS} = -10V, V_{GS} = 15V$		-100		-100	pA
$r_{DS(on)}$	Drain-Source "ON" Resistance	$V_{GS} = 0, V_{DS} = -0.1V$		75		60	Ω
C_{iss}	Input Capacitance	$V_{DG} = -20V, V_{GS} = 0$ (Note 1)		35		35	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DG} = -10V, I_S = 0$ (Note 1)		12		12	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

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IT120, IT122

Dual NPN

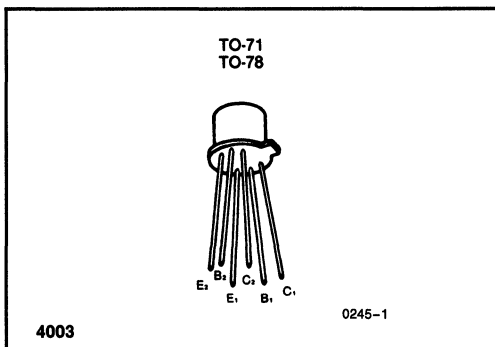
General Purpose Amplifier



FEATURES

- High h_{FE} at Low Current
- Low Output Capacitance
- Good Matching
- Tight V_{BE} Tracking

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base Voltage (Note 1)	45V
Collector-Emitter Voltage (Note 1)	45V
Emitter Base Voltage (Notes 1 and 2)	7V
Collector Current (Note 1)	50mA
Collector-Collector Voltage	60V
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$

	TO-78		TO-71	
	One Side	Both Sides	One Side	Both Sides
Power Dissipation	250mW	500mW	200mW	400mW
Derate Above				
25°C	1.7mW/°C	3.3mW/°C	1.3mW/°C	2.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-78	TO-71
IT120	IT120-TO71
IT121	IT121-TO71
IT122	IT122-TO71

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT120A		IT120		IT121		IT122		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
h_{FE}	DC Current Gain	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$	200		200		80		80		
		$I_C = 1.0\text{mA}, V_{CE} = 5.0\text{V}$	225		225		100		100		
		$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$ $T_A = -55^\circ\text{C}$	75		75		30		30		
$V_{BE(ON)}$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7		V
$V_{CE(SAT)}$	Collector Saturation Voltage	$I_C = 0.5\text{mA}, I_B = 0.05\text{mA}$	0.5		0.5		0.5		0.5		
I_{CBO}	Collector Cutoff Current	$I_E = 0, V_{CB} = 45\text{V}$	1.0		1.0		1.0		1.0		nA
		$T_A = +150^\circ\text{C}$	10		10		10		10		μA
I_{EBO}	Emitter Cutoff Current	$I_C = 0, V_{EB} = 5.0\text{V}$	1.0		1.0		1.0		1.0		nA
C_{obo}	Output Capacitance	$I_E = 0, V_{CB} = 5.0\text{V}$ $f = 1\text{MHz}$	2.0		2.0		2.0		2.0		pF
C_{te}	Emitter Transition Capacitance	$I_C = 0, V_{EB} = 0.5\text{V}$ (Note 3)	2.5		2.5		2.5		2.5		
$C_{C1, C2}$	Collector to Collector Capacitance	$V_{CC} = 0$	4.0		4.0		4.0		4.0		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	IT120A		IT120		IT121		IT122		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I _{C1,C2}	Collector to Collector Leakage Current	V _{CC} = ±60V (Note 3)		10		10		10		10	nA
V _{CEO(SUST)}	Collector to Emitter Sustaining Voltage	I _C = 1.0mA, I _B = 0	45		45		45		45		V
GBW	Current Gain Bandwidth Product (Note 3)	I _C = 10μA, V _{CE} = 5V	10		10		7		7		MHz
		I _C = 1mA, V _{CE} = 5V	220		220		180		180		
V _{BE1} - V _{BE2}	Base Emitter Voltage Differential	I _C = 10μA, V _{CE} = 5.0V		1		2		3		5	mV
I _{B1} - I _{B2}	Base Current Differential			2.5		5		25		25	nA
$\frac{\Delta(V_{BE1} - V_{BE2})}{\Delta T}$	Base-Emitter Voltage Differential Change with Temperature	(Note 3) T _A = -55°C to +125°C I _C = 10μA, V _{CE} = 5.0V		3		5		10		20	μV/°C

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μA.

3. For design reference only, not 100% tested.

IT126-IT129

Monolithic Dual NPN

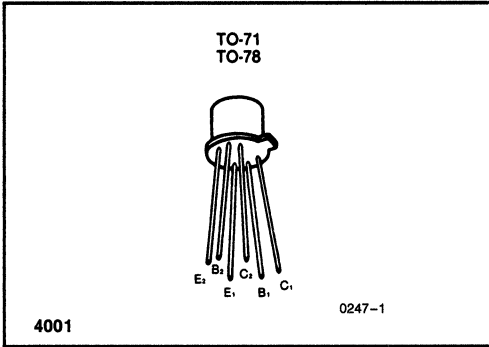
General Purpose Amplifier



FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Collector-Base Voltage (Note 1)	IT126, IT127	60V
	IT128	55V
	IT129	45V
Collector-Emitter Voltage (Note 1)	IT126, IT127	60V
	IT128	55V
	IT129	45V
Emitter-Base Voltage (Notes 1 and 2)		7.0V
Collector Current (Note 1)		100mA
Collector-Collector Voltage		70V
Storage Temperature Range		-65°C to $+175^\circ\text{C}$
Operating Temperature Range		-55°C to $+175^\circ\text{C}$
Lead Temperature (Soldering, 10sec)		$+300^\circ\text{C}$

	TO71		TO78	
	One Side	Both Sides	One Side	Both Sides
Power Dissipation				
Total Dissipation at 25°C	200mW	400mW	250mW	500mW
	1.3	2.7	1.7	3.3
Derating Factor	mW/ $^\circ\text{C}$		mW/ $^\circ\text{C}$	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO78	TO-71
IT126	IT126-TO71
IT127	IT127-TO71
IT128	IT128-TO71
IT129	IT129-TO71

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT126		IT127		IT128		IT129		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
h_{FE}	DC Current Gain	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$	150		150		100		70		
		$I_C = 1.0\text{mA}, V_{CE} = 5\text{V}$	200	800	200	800	150	800	100		
		$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	230		230		170		115		
		$I_C = 50\text{mA}, V_{CE} = 5\text{V}$	100		100		75		50		
		$I_C = 1\text{mA}, V_{CE} = 5\text{V}, T_A = -55^\circ\text{C}$	75		75		60		40		
$V_{BE(on)}$	Emitter-Base On Voltage	$I_C = 10\text{mA}, V_{CE} = 5\text{V}$		0.9		0.9		0.9		0.9	V
		$I_C = 50\text{mA}, V_{CE} = 5\text{V}$		1.0		1.0		1.0		1.0	
$V_{CE(sat)}$	Collector Saturation Voltage	$I_C = 10\text{mA}, I_B = 1\text{mA}$		0.3		0.3		0.3		0.3	
		$I_C = 50\text{mA}, I_B = 5\text{mA}$		1.0		1.0		1.0		1.0	
I_{CBO}	Collector Cutoff Current	$I_E = 0, V_{CB} = 45\text{V}$		0.1		0.1		0.1		0.1*	nA
		$V_{CB} = 30\text{V}^* (\text{IT129}), T_A = +150^\circ\text{C}$		0.1		0.1		0.1		0.1*	μA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT126		IT127		IT128		IT129		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{EBO}	Emitter Cutoff Current	$I_C = 0, V_{EB} = 5V$		0.1		0.1		0.1		0.1	nA
C_{obo}	Output Capacitance (Note 3)	$I_E = 0, V_{CB} = 20V$		3		3		3		3	pF
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	$I_C = \pm 1\mu A$	± 100		± 100		± 100		± 100		V
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	$I_C = 1mA, I_B = 0$	60		60		55		45		
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu A, I_E = 0$	60		60		55		45		
BV_{EBO}	Emitter Base Breakdown Voltage	$I_E = 10\mu A, I_C = 0$	7		7		7		7		

MATCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	IT126		IT127		IT128		IT129		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential	$I_C = 1mA, V_{CE} = 5V$		1		2		3		5	mV
$\frac{\Delta(V_{BE1} - V_{BE2})}{\Delta T}$	Base Emitter Voltage Differential Change with Temperature (Note 3)	$I_C = 1mA, V_{CE} = 5V$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		3		5		10		20	$\mu\text{V}/^\circ\text{C}$
$ I_{B1} - I_{B2} $	Base Current Differential	$I_C = 10\mu A, V_{CE} = 5V$		2.5		5		10		20	nA
		$I_C = 1mA, V_{CE} = 5V$		0.25		0.5		1.0		2.0	μA

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed $10\mu\text{A}$.

3. For design reference only, not 100% tested.

IT130-IT132

Monolithic Dual PNP

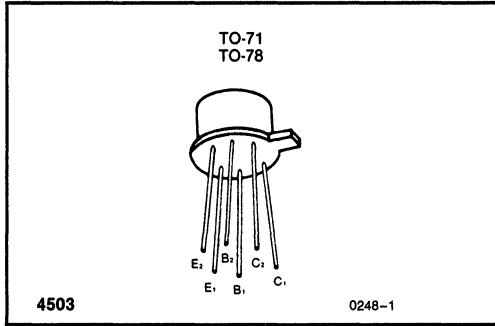
General Purpose Amplifier



FEATURES

- High h_{FE} at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Collector-Base Voltage (Note 1) 45V
 Collector-Emitter Voltage (Note 1) 45V
 Emitter Base Voltage (Notes 1 and 2) 7V
 Collector Current (Note 1) 50mA
 Collector-Collector Voltage 60V
 Storage Temperature Range -65°C to $+175^\circ\text{C}$
 Operating Temperature Range -55°C to $+175^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$

TO-71		TO-78	
One Side	Both Sides	One Side	Both Sides
200mW	400mW	250mW	500mW

Power

Dissipation 1.3mW/ $^\circ\text{C}$ 2.7mW/ $^\circ\text{C}$ 1.7mW/ $^\circ\text{C}$ 3.3mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-78	TO-71
IT130A	IT130A-TO71
IT130	IT130-TO71
IT131	IT131-TO71
IT132	IT132-TO71

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT130A		IT130		IT131		IT132		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
h_{FE}	DC Current Gain	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$	200		200		80		80		
		$I_C = 1.0\text{mA}, V_{CE} = 5.0\text{V}$	225		225		100		100		
		$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}, T_A = -55^\circ\text{C}$	75		75		30		30		
$V_{BE(ON)}$	Emitter-Base On Voltage	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$		0.7		0.7		0.7		0.7	V
$V_{CE(SAT)}$	Collector Saturation Voltage	$I_C = 0.5\text{mA}, I_B = 0.05\text{mA}$		0.5		0.5		0.5		0.5	
I_{CBO}	Collector Cutoff Current	$I_E = 0, V_{CB} = 45\text{V}, T_A = +150^\circ\text{C}$		-1.0		-1.0		-1.0		-1.0	nA
				-10		-10		-10		-10	μA
I_{EBO}	Emitter Cutoff Current	$I_C = 0, V_{EB} = 5.0\text{V}$		-1.0		-1.0		-1.0		-1.0	nA
C_{ob} (Note 3)	Output Capacitance	$I_E = 0, V_{CB} = 5.0\text{V}$		2.0		2.0		2.0		2.0	pF
C_{te} (Note 3)	Emitter Transition Capacitance	$I_C = 0, V_{EB} = 0.5\text{V}$		2.5		2.5		2.5		2.5	
C_{C1-C2} (Note 3)	Collector to Collector Capacitance	$V_{CC} = 0$		4.0		4.0		4.0		4.0	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT130A		IT130		IT131		IT132		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{C1-C2}	Collector to Collector Leakage Current	$V_{CC} = \pm 60\text{V}$		10		10		10		10	nA
$V_{CEO(\text{SUST})}$	Collector to Emitter Sustaining Voltage	$I_C = 1.0\text{mA}, I_B = 0$	-45		-45		-45		-45		V
GBW	Current Gain Bandwidth Product (Note 3)	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$	5		5		4		4		MHz
		$I_C = 1\text{mA}, V_{CE} = 5\text{V}$	110		110		90		90		
$ V_{BE1} - V_{BE2} $	Base Emitter Voltage Differential	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$		1		2		3		5	mV
$ I_{B1} - I_{B2} $	Base Current Differential	$I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$		2.5		5		25		25	nA
$\Delta(V_{BE1} - V_{BE2})/\Delta T$	Base-Emitter Voltage Differential Change with Temperature (Note 3)	$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $I_C = 10\mu\text{A}, V_{CE} = 5.0\text{V}$		3		5		10		20	$\mu\text{V}/^\circ\text{C}$

NOTES: 1. Per transistor.

2. The reverse base-to-emitter voltage must never exceed 7.0V, and the reverse base-to-emitter current must never exceed $10\mu\text{A}$.

3. For design reference only, not 100% tested.

IT136-IT139

Monolithic Dual PNP

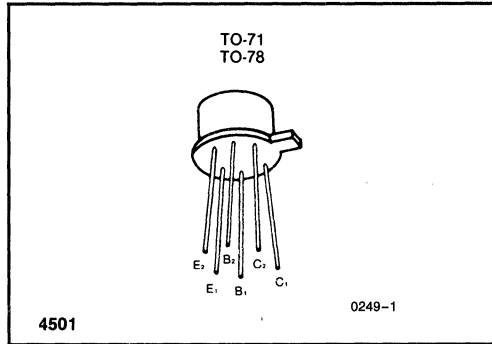
General Purpose Amplifier



FEATURES

- High Gain at Low Current
- Low Output Capacitance
- Tight I_B Match
- Tight V_{BE} Tracking
- Dielectrically Isolated Matched Pairs for Differential Amplifiers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Collector-Base Voltage (Note 1)	IT136, IT137	60V
	IT138	55V
	IT139	45V
Collector-Emitter Voltage (Note 1)	IT136, IT137	60V
	IT138	55V
	IT139	45V
Emitter Base Voltage (Notes 1 and 2)		7V
Collector Current (Note 1)		100mA
Collector-Collector Voltage		70V
Storage Temperature Range		-65°C to $+175^\circ\text{C}$
Operating Temperature Range		-55°C to $+175^\circ\text{C}$
Lead Temperature (Soldering, 10sec)		$+300^\circ\text{C}$

	TO-71		TO-78	
	One Side	Both Sides	One Side	Both Sides
Power Dissipation ...	200mW	400mW	250mW	500mW
Derate above 25°C ..	1.3mW/ $^\circ\text{C}$	2.7mW/ $^\circ\text{C}$	1.7mW/ $^\circ\text{C}$	3.3mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-78	TO-71
IT136	IT136-TO71
IT137	IT137-TO71
IT138	IT138-TO71
IT139	IT139-TO71

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT136		IT137		IT138		IT139		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
h_{FE}	DC Current Gain	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$	150		150		100		70		
		$I_C = 1.0\text{mA}, V_{CE} = 5\text{V}$	150	800	150	800	100	800	70	800	
		$I_C = 10\text{mA}, V_{CE} = 5\text{V}$	125		125		80		50		
		$I_C = 50\text{mA}, V_{CE} = 5\text{V}$	65		60		40		25		
		$I_C = 1\text{mA}, V_{CE} = 5\text{V}$ $T_A = 55^\circ\text{C}$	75		75		60		40		
$V_{BE(on)}$	Emitter-Base On Voltage	$I_C = 10\text{mA}, V_{CE} = 5\text{V}$.9		.9		.9		.9		V
		$I_C = 50\text{mA}, V_{CE} = 5\text{V}$		1.0		1.0		1.0		1.0	
$V_{CE(sat)}$	Collector Saturation Voltage	$I_C = 1\text{mA}, I_B = .1\text{mA}$.3		.3		.3		.3	
		$I_C = 10\text{mA}, I_B = 1\text{mA}$.6		.6		.6		.6	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	IT136		IT137		IT138		IT139		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CBO}	Collector Cutoff Current	$I_E = 0, V_{CB} = 45V, V_{CD} = 30V^* (IT139), T_A = +150^\circ\text{C}$		0.1		0.1		0.1		0.1*	nA
				0.1		0.1		0.1		0.1*	μA
I_{EBO}	Emitter Cutoff Current	$I_C = 0, V_{EB} = 5V$		0.1		0.1		0.1		0.1	nA
C_{obo}	Output Capacitance (Note 3)	$I_E = 0, V_{CB} = 20V, f = 1\text{MHz}$		3		3		3		3	pF
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	$I_C = \pm 1\mu\text{A}$	± 100		± 100		± 100		± 100		V
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	$I_C = 1\text{mA}, I_B = 0$	60		60		55		45		
BV_{CBO}	Collector Base Breakdown Voltage	$I_C = 10\mu\text{A}, I_E = 0$	60		60		55		45		
BV_{EBO}	Emitter Base Breakdown Voltage	$I_E = 10\mu\text{A}, I_C = 0$	7		7		7		7		
$ V_{BE_1} - V_{BE_2} $	Base Emitter Voltage Differential	$I_C = 1\text{mA}, V_{CE} = 5V$		1		2		3		5	mV
$\frac{\Delta V_{BE_1} - V_{BE_2} }{\Delta T}$	Base Emitter Voltage Differential Change with Temperature (Note 3)	$I_C = 1\text{mA}, V_{CE} = 5V, T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		3		5		10		20	$\mu\text{V}/^\circ\text{C}$
$ I_{B_1} - I_{B_2} $	Base Current Differential	$I_C = 10\mu\text{A}, V_{CE} = 5V$		2.5		5		10		20	nA
		$I_C = 1\text{mA}, V_{CE} = 5V$.25		.5		1.0		2.0	μA

- NOTES: 1. Per transistor.
 2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed $10\mu\text{A}$.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

IT500-IT505

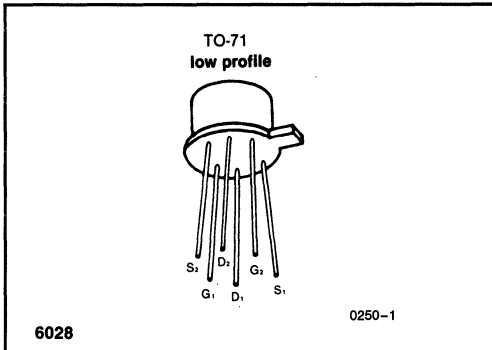
Monolithic Dual Cascoded N-Channel JFET General Purpose Amplifier



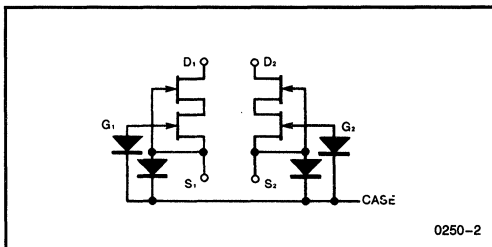
GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low I_G at high voltage levels, while giving high transconductance and very high common, mode rejection ratio.

PIN CONFIGURATION



SCHEMATIC DIAGRAM



FEATURES

- $C_{MRR} > 120\text{dB}$
- $I_G < 5\text{pA}$ @ 50V_{DG}
- $C_{rss} < 0.5\text{pF}$
- $\theta_{os} > .025\mu\text{s}$

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain-Source and Drain-Gate Voltages (Note 1)	60V
Drain Current (Note 1)	50mA
Gate-Gate Voltage	$\pm 60\text{V}$
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation (Note 3)	250mW	500mW
Derate above 25°C	$3.8\text{mW}/^\circ\text{C}$	$7.7\text{mW}/^\circ\text{C}$

NOTE 1. Per transistor.

NOTE 2. Due to the non-symmetrical structure of these devices, the drain and source ARE NOT interchangeable.

NOTE 3. @ 85°C free air temp.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
IT500
IT501
IT502
IT503
IT504
IT505

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Characteristics	Test Conditions	Limits		Units	
			Min	Max		
I _{GSS}	Gate Reverse Current	V _{GS} = -20V, V _{DS} = 0, T _A = 125°C		-100	pA	
				-5	nA	
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-50		V	
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 20V, I _D = 1nA	-0.7	-4		
V _{GS}	Gate-Source Voltage	V _{DS} = 35V, I _D = 200μA, T _A = 125°C	-0.2	-3.8		
I _G	Gate Operating Current			-5	pA	
				-5	nA	
I _{DSS}	Saturation Drain Current (Note 1)	V _{DS} = 20V, V _{GS} = 0	0.7	7	mA	
g _{fs}	Common-Source Forward Transconductance (Note 1)	V _{DS} = 20V, V _{GS} = 0	1000	4000	μs	
g _{fs}	Common-Source Forward Transconductance (Note 1)	V _{DS} = 20V, I _D = 200μA	500	1600		
g _{os}	Common-Source Output Conductance	V _{DS} = 20V, V _{GS} = 0		1		
g _{os}	Common-Source Output Conductance	V _{DS} = 20V, I _D = 200μA		0.025		
C _{g1g2}	Gate to Gate Capacitance (Note 4)	V _{G1} = V _{G2} = 10V		3.5		pF
C _{iss}	Common-Source Input Capacitance (Note 4)	V _{DS} = 20V, V _{GS} = 0	f = 1MHz	7	pF	
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 3, 4)			0.5		
NF	Spot Noise Figure (Note 4)			f = 100Hz, R _G = 10MΩ	0.5	dB
e _n	Equivalent Input Noise Voltage (Note 4)			f = 10Hz	50	μV
		f = 1kHz	15	√Hz		

Symbol	Characteristics	Test Conditions	IT500		IT501		IT502		IT503		IT504		IT505		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I _{G1} -I _{G2}	Differential Gate Current	V _{DG} = 20V, I _D = 200μA, T _A = 125°C		5		5		5		5		10		15	nA
I _{DSS1} I _{DSS2}	Saturation Drain Current Ratio (Note 1)	V _{DS} = 20V, V _{GS} = 0V	0.95	1	0.95	1	0.95	1	0.95	1	0.9	1	0.85	1	
g _{fs1} /g _{fs2}	Transconductance Ratio (Note 1)		f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	0.85	1

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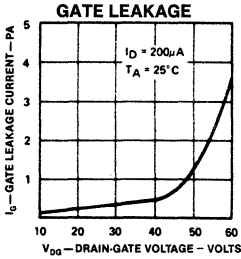
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

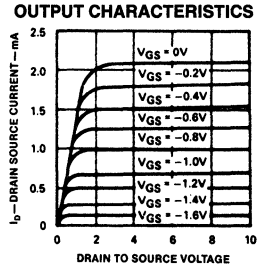
Symbol	Characteristics	Test Conditions	IT500		IT501		IT502		IT503		IT504		IT505		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{GS1}-V_{GS2}$	Differential Gate-Source Voltage	$V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$		5		5		10		15		25		50	mV
$\frac{\Delta V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Differential Voltage Change with Temp. (Note 2, 4)	$T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$		5		10		20		40		100		200	$\mu\text{V}/^\circ\text{C}$
C_{MRR} (Note 5)	Common Mode Rejection Ratio (Note 4)	$\Delta V_{DD} = 10\text{V}$, $I_D = 200\mu\text{A}$	120		120		120		120		120		120		dB

- NOTES:** 1. Pulse test required, pulsewidth = 300 μs , duty cycle $\leq 3\%$.
 2. Measured at end points, T_A and T_B .
 3. With case guarded C_{RSS} is typically $< 0.15\text{pF}$.
 4. For design reference only, not 100% tested.
 5. $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{GS1}-V_{GS2}]$, $\Delta V_{DD} = 10/-20\text{V}$

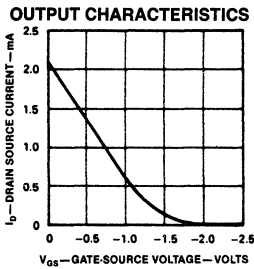
TYPICAL PERFORMANCE CHARACTERISTICS



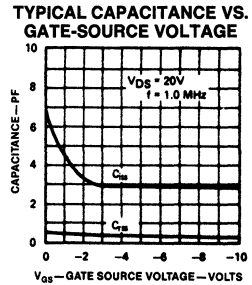
0250-4



0250-5



0250-6



0250-7

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NOTE: All typical values have been characterized but are not tested.

IT1700

P-Channel

Enhancement Mode MOSFET

General Purpose Amplifier

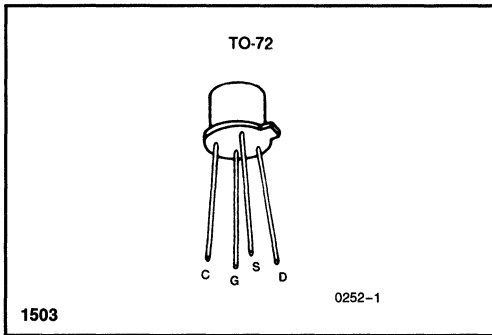


IT1700

FEATURES

- Low ON-Resistance
- High Gain
- Low Noise Voltage
- High Input Impedance
- Low Leakage

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source and Gate-Source Voltage	-40V
Peak Gate-Source Voltage (Note 1)	$\pm 125\text{V}$
Drain Current	50mA
Storage Temperature	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	375mW
Derate above 25°C	3mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
IT1700

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0, I_D = -10\mu\text{A}$	-40		V
BV_{SDS}	Source to Drain Breakdown Voltage	$V_{GS} = 0, I_D = -10\mu\text{A}$	-40		V
I_{GSS}	Gate Leakage Current		(See note 2)		
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0, V_{DS} = -20\text{V}$		200	pA
$I_{DSS}(150^\circ\text{C})$	Drain to Source Leakage Current			0.4	μA
I_{SDS}	Source to Drain Leakage Current			400	pA
$I_{SDS}(150^\circ\text{C})$	Source to Drain Leakage Current			0.8	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -10\mu\text{A}$	-2	-5	V
$r_{DS(on)}$	Static Drain to Source "on" Resistance	$V_{GS} = -10\text{V}, V_{DS} = 0$		400	ohms
$I_{DS(on)}$	Drain to Source "on" Current	$V_{GS} = -10\text{V}, V_{DS} = -15\text{V}$	2		mA
g_{fs}	Forward Transconductance Common Source	$V_{DS} = -15\text{V}, I_D = -10\text{mA}$ $f = 1\text{kHz}$	2000	4000	μs
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance	$V_{DS} = -15\text{V}, I_D = -10\text{mA}$ $f = 1\text{MHz}$ (Note 3)		5	pF
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance	$V_{DG} = -15\text{V}, I_D = 0$ $f = 1\text{MHz}$ (Note 3)		1.2	pF
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance	$V_{DS} = -15\text{V}, I_D = -10\text{mA}$ $f = 1\text{MHz}$ (Note 3)		3.5	pF

- NOTES:**
1. Device must not be tested at $\pm 125\text{V}$ more than once nor longer than 300ms.
 2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of $< 10\text{pA}$. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.
 3. For design reference only, not 100% tested.

INTERASIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

IT1750

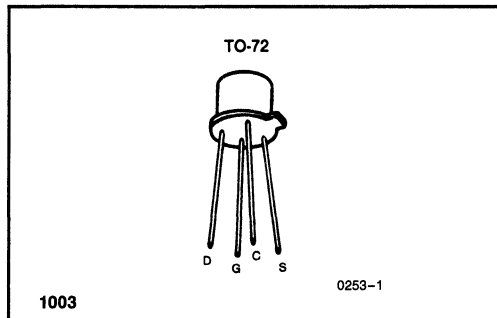
N-Channel Enhancement Mode MOSFET General Purpose Amplifier Switch



FEATURES

- Low ON Resistance
- Low C_{dg}
- High Gain
- Low Threshold Voltage

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Source and Gate-Source Voltage	25V
Peak Gate-Source Voltage (Note 1)	$\pm 125\text{V}$
Drain Current	100mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	375mW
Derate above 25°C	$3\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
IT1750

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, Body connected to Source and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 10\mu\text{A}$	0.50	3.0	V
I_{DSS}	Drain Leakage Current	$V_{DS} = 10\text{V}$, $V_{GS} = 0$		10	nA
I_{GSS}	Gate Leakage Current		See note 2.		
BV_{DSS}	Drain Breakdown Voltage	$I_D = 10\mu\text{A}$, $V_{GS} = 0$	25		V
$r_{DS(on)}$	Drain To Source on Resistance	$V_{GS} = 20\text{V}$		50	ohms
$I_{D(on)}$	Drain Current	$V_{DS} = V_{GS} = 10\text{V}$	10		mA
Y_{fs}	Forward Transadmittance	$V_{DS} = 10\text{V}$, $I_D = 10\text{mA}$, $f = 1\text{kHz}$	3,000		μs
C_{iss}	Total Gate Input Capacitance	$I_D = 10\text{mA}$, $V_{DS} = 10\text{V}$, $f = 1\text{MHz}$ (Note 3)		6.0	pF
C_{dg}	Gate to Drain Capacitance	$V_{DG} = 10\text{V}$, $f = 1\text{MHz}$ (Note 3)		1.6	pF

NOTES: 1. Devices must not be tested at $\pm 125\text{V}$ more than once nor longer than 300ms.

2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of $<10\text{pA}$. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

J105-J107

N-Channel JFET Switch

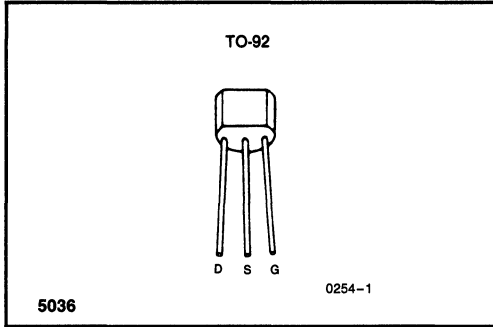


J105-J107

FEATURES

- Low $r_{DS(on)}$

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	50mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	360mW
Derate above 25°C	3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO92
J105
J106
J107

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	J105			J106			J107			Units	
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{GSS}	Gate-Reverse Current (Note 1)	$V_{DS} = 0V, V_{GS} = -15V$			-3			-3			-3	nA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 5V, I_D = 1\mu A$	-4.5		-10	-2		-6	-0.5		-4.5	V	
BV_{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu A$	-25			-25			-25				
I_{DSS}	Drain Saturation Current (Note 2)	$V_{DS} = 15V, V_{GS} = 0V$	500			200			100			mA	
$I_{D(off)}$	Drain Cutoff Current (Note 1)	$V_{DS} = 5V, V_{GS} = -10V$			3			3			3	nA	
$r_{DS(on)}$	Drain source ON Resistance	$V_{DS} \leq 0.1V, V_{GS} = 0V$			3			6			8	Ω	
$C_{dg(off)}$	Drain Gate OFF Capacitance	$V_{DS} = 0V, V_{GS} = -10V$			35			35			35	pF	
$C_{sg(off)}$	Source Gate OFF Capacitance	(Note 3)			35			35			35		
$C_{dg(on)} + C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance	(Note 3) $V_{DS} = V_{GS} = 0V$			160			160			160		
$t_d(on)$	Turn On Delay Time	Switching Time-Test Conditions (Note 3)			15			15			15	ns	
t_r	Rise Time				20			20			20		
$t_d(off)$	Turn Off Delay Time		V_{DD} 1.5V 1.5V 1.5V $V_{GS(off)}$ -12V -7V -5V R_L 50 Ω 50 Ω 50 Ω			15			15				15
t_f	Fall Time				20			20			20		

- NOTES:**
1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse test duration = 300 μ s; duty cycle \leq 3%.
 3. For design reference only, not 100% tested.

INTERSil's SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

10

J108-J110 N-Channel JFET Switch



FEATURES

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
- Purely Resistive High Isolation Resistance from Driver
- Fast Switching
- Low Noise

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

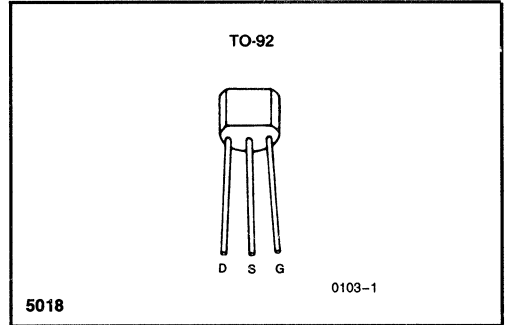
Gate-Drain or Gate-Source Voltage -25V
Gate Current 50mA
Storage Temperature Range -55°C to +150°C
Operating Temperature Range -55°C to +135°C
Lead Temperature (Soldering, 10sec) +300°C
Power Dissipation 360mW
Derate above 25°C 3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

APPLICATIONS

- Analog Switches
- Choppers
- Commutators
- Low-Noise Audio Amplifiers

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	J108			J109			J110			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{GSS}	Gate Reverse Current (Note 1)	V _{DS} = 0V, V _{GS} = -15V			-3			-3			-3	nA
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 5V, I _D = 1μA	-3		-10	-2		-6	-0.5		-4	V
BV _{GSS}	Gate-Source Breakdown Voltage	V _{DS} = 0V, I _G = -1μA	-25			-25			-25			
I _{DSS}	Drain Saturation Current (Note 2)	V _{DS} = 15V, V _{GS} = 0V	80			40			10			mA
I _{D(off)}	Drain Cutoff Current (Note 1)	V _{DS} = 5V, V _{GS} = -10V			3			3			3	nA
r _{DS(on)}	Drain-Source ON Resistance	V _{DS} ≤ 0.1V, V _{GS} = 0V			8			12			18	Ω
C _{dg(off)}	Drain-Gate OFF Capacitance	V _{DS} = 0V, V _{GS} = -10V (Note 3) f = 1MHz			15			15			15	pF
C _{sg(off)}	Source-Gate OFF Capacitance				15			15			15	
C _{dg(on)} + C _{sg(on)}	Drain-Gate Plus Source-Gate ON Capacitance		V _{DS} = V _{GS} = 0 (Note 3)			85			85			
t _{d(on)}	Turn ON Delay Time	Switching Time Test Conditions (Note 3)			4		4		4			ns
t _r	Rise Time	V _{DD}	1.5V	1.5V	1.5V		1		1			
t _{d(off)}	Turn OFF Delay Time	V _{GS(off)}	-12V	-7V	-5V	6		6		6		
t _f	Fall Time	R _L	150Ω	150Ω	150Ω	30		30		30		

NOTE 1: Approximately doubles for every 10°C increase in T_A.

2: Pulse test duration = 300μs; duty cycle ≤ 3%.

3: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

J111-J113

N-Channel JFET Switch

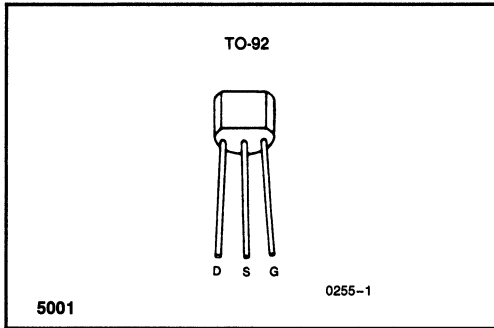


J111-J113

FEATURES

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltage Generated By Closed Switch
 - Purely Resistive
 - High Isolation Resistance From Driver
- Fast Switching
- Short Sample and Hold Aperture Time

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-35V
Gate Current	50mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	360mW
Derate Above 25°C	3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
J111
J112
J113

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	J111			J112			J113			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{GSSR}	Gate Reverse Current (Note 1)	$V_{DS} = 0V, V_{GS} = -15V$			-1			-1			-1	nA
$V_{GS(off)}$	Gate Source Cutoff Voltage	$V_{DS} = 5V, I_D = 1\mu A$	-3		-10	-1		-5			-3	V
BV_{GSS}	Gate Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu A$	-35			-35					-35	V
I_{DSS}	Drain Saturation Current (Note 2)	$V_{DS} = 15V, V_{GS} = 0V$	20			5					2	mA
$I_{D(off)}$	Drain Cutoff Current (Note 1)	$V_{DS} = 5V, V_{GS} = -10V$			1			1			1	nA
$r_{DS(on)}$	Drain Source ON Resistance	$V_{DS} = 0.1V, V_{GS} = 0V$			30			50			100	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	$V_{DS} = 0V, V_{GS} = -10V$ (Note 3)	$f = 1\text{MHz}$			5		5			5	pF
$C_{sg(off)}$	Source Gate OFF Capacitance					5		5		5		
$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance							28		28		
$t_{d(on)}$	Turn On Delay Time	Switching Time-Test Conditions (Note 3)			7		7		7		ns	
t_r	Rise Time		J111	J112	J113		6		6			
$t_{d(off)}$	Turn Off Delay Time	V_{DD}	10V	10V	10V		20		20			
t_f	Fall Time	$V_{GS(off)}$	-12V	-7V	-5V							
		R_L	0.8k Ω	1.6k Ω	3.2k Ω		15		15			

- NOTES:**
1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse Test duration 300 μs ; duty cycle $\leq 3\%$.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

10

J174-J177

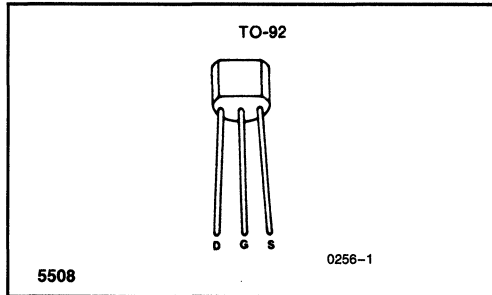
P-Channel JFET Switch



FEATURES

- Low Insertion Loss
- No Offset or Error Generated By Closed Switch
 - Purely Resistive
 - High Isolation Resistance From Driver
- Short Sample and Hold Aperture Time
- Fast Switching

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	30V
Gate Current	50mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	350mW
Derate above 25°C	3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
J17X

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	J174			J175			J176			J177			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{GSS}	Gate Reverse Current (Note 1)	V _{DS} = 0, V _{GS} = 20V			1			1			1			1	nA
V _{GS(off)}	Gate Source Cutoff Voltage	V _{DS} = -15V, I _D = -10nA	5		10	3		6	1		4	0.8		2.25	V
BV _{GSS}	Gate Source Breakdown Voltage	V _{DS} = 0, I _G = 1μA	30			30			30			30			
I _{DSS}	Drain Saturation Current (Note 2)	V _{DS} = -15V, V _{GS} = 0	-20		-135	-7		-70	-2		-35	-1.5		-20	mA
I _{D(off)}	Drain Cutoff Current (Note 1)	V _{DS} = -15V, V _{GS} = 10V			-1			-1			-1			-1	nA
r _{DS(on)}	Drain-Source ON Resistance	V _{GS} = 0, V _{DS} = -0.1V			85			125			250			300	Ω

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions				J174			J175			J176			J177			Units				
						Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max					
$C_{dg(off)}$	Drain-Gate OFF Capacitance	$V_{DS} = 0,$	f = 1MHz (Note 3)				5.5			5.5			5.5			5.5			pF			
$C_{sg(off)}$	Source-Gate OFF Capacitance	$V_{GS} = 10V$					5.5			5.5			5.5			5.5				5.5		
$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance	$V_{DS} = V_{GS} = 0$					32			32			32			32				32		
$t_{d(on)}$	Turn On Delay Time	Switching Time Test Conditions				2			5			15			20			ns				
		(Note 3)	J174	J175	J176	J177																
t_r	Rise Time	V_{DD}	-10V	-6V	-6V	-6V	5			10			20			25						
$t_{d(off)}$	Turn Off Delay Time	$V_{GS(off)}$	12V	8V	3V	3V	5			10			15			20						
t_f	Fall Time	R_L	560Ω	12kΩ	5.6kΩ	10kΩ																
		$V_{GS(on)}$	0V	0V	0V	0V	10			20			20			25						

- NOTES:** 1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse test duration – 300μs; duty cycle ≤ 3%.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

J201-J204

N-Channel JFET

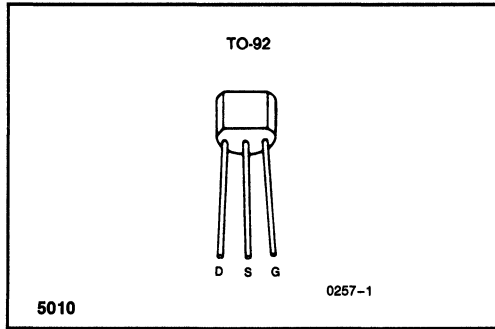
General Purpose Amplifier



FEATURES

- High Input Impedance
- Low I_{GSS}

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage	-40V
Gate Current	50mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	360mW
Derate above 25°C	3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92
J201
J202
J203
J204

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	J201			J202			J203			J204			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{GSS}	Gate Reverse Current (Note 1)	$V_{DS} = 0, V_{GS} = -20V$			-100			-100			-100			-100	pA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 10nA$	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	-0.3		-2.0	V
BV_{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0, I_G = 1\mu A$	-40			-40			-40			-25			
I_{DSS}	Saturation Drain Current (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	0.2		1.0	0.9		4.5	4.0		20	0.2	1.2	3.0	mA
I_G	Gate Current (Note 1)	$V_{DG} = 20V, I_D = I_{DSS(min)}$		-10			-10			-10			-10		pA
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 20V, V_{GS} = 0, f = 1kHz$	500			1,000			1,500			500	1,500		μS
g_{os}	Common Source Output Conductance	$V_{GS} = 0, f = 1MHz$		1			3.5			10			2.5		μS
C_{iss}	Common-Source Input Capacitance	(Note 3)		4			4			4			4		pF
C_{rss}	Common-Source Reverse Transfer Capacitance	(Note 3)		1			1			1			1		pF
\bar{e}_n	Equivalent Short-Circuit Input Noise Voltage	$V_{DS} = 10V, V_{GS} = 0, f = 1kHz$ (Note 3)		5			5			5			10		$\frac{nV}{\sqrt{Hz}}$

- NOTES:**
1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse test duration = 2ms.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

J308-J310

N-Channel JFET

High Frequency Amplifier

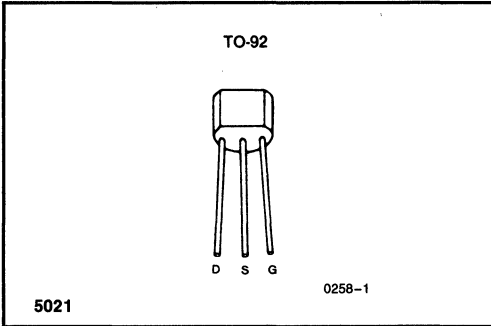


J308-J310

FEATURES

- Industry Standard Part in Low Cost Plastic Package
- High Power Gain
- Low Noise
- Dynamic Range Greater Than 100dB
- Easily Matched to 75Ω Input

PIN CONFIGURATION



APPLICATIONS

- VHF/UHF Amplifiers
- Oscillators
- Mixers

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-Gate Voltage	-25V
Drain-Source Voltage	-25V
Continuous Forward Gate Current	-10mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	360mW
Derate above 25°C	3.27mW/°C

ORDERING INFORMATION

TO-92
J3XX

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	J308			J309			J310			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1 μA, V _{DS} = 0	-25			-25			-25			V
I _{GSS}	Gate Reverse Current	V _{GS} = -15V, V _{DS} = 0, T _A = 125°C			-1.0			-1.0			-1.0	nA
					-1.0			-1.0			-1.0	μA
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 10V, I _D = 1nA	-1.0		-6.5	-1.0		-4.0	-2.0		-6.5	V
I _{DSS}	Saturation Drain Current (Note 1)	V _{DS} = 10V, V _{GS} = 0	12		60	12		30	24		60	mA
V _{GS(f)}	Gate-Source Forward Voltage	V _{DS} = 0, I _G = 1mA			1.0			1.0			1.0	V
g _{fs}	Common-Source Forward Transconductance	V _{DS} = 10V, f = 1kHz, I _D = 10mA (Note 2)	8,000	17,000		10,000	17,000		8,000	17,000		μS
g _{os}	Common-Source Output Conductance				250			250			250	
g _{fg}	Common-Gate Forward Transconductance			13,000			13,000			12,000		
g _{og}	Common Gate Output Conductance			150			150			150		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions		J308			J309			J310			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C_{gd}	Gate-Drain Capacitance	$V_{DS} = 10\text{V}$, $V_{GS} = -10\text{V}$	$f = 1\text{MHz}$ (Note 2)		1.8	2.5		1.8	2.5		1.8	2.5	pF
C_{gs}	Gate-Source Capacitance				4.3	5.0		4.3	5.0		4.3	5.0	
e_n	Equivalent Short-Circuit Input Noise Voltage	$V_{DS} = 10\text{V}$, $I_D = 10\text{mA}$	$f = 100\text{Hz}$ (Note 2)		10			10			10		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$Re_{(V_{fs})}$	Common-Source Forward Transconductance	$V_{DS} = 10\text{V}$, $I_D = 10\text{mA}$ (Note 2)	$f = 105\text{MHz}$		12			12			12		μS
$Re_{(V_{fg})}$	Common-Gate Input Conductance				14			14			14		
$Re_{(V_{is})}$	Common-Source Input Conductance				0.4			0.4			0.4		
$Re_{(V_{os})}$	Common-Source Output Conductance				0.15			0.15			0.15		
G_{pg}	Common-Gate Power Gain at Noise Match				16			16			16		
NF	Noise Figure				1.5			1.5			1.5		
G_{pg}	Common-Gate Power Gain at Noise Match			11			11			11			
NF	Noise Figure		2.7			2.7			2.7		dB		

- NOTES: 1. Pulse test PW 300 μs , duty cycle $\leq 3\%$.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

LM114/H, LM114A/AH Monolithic Dual NPN General Purpose Amplifier



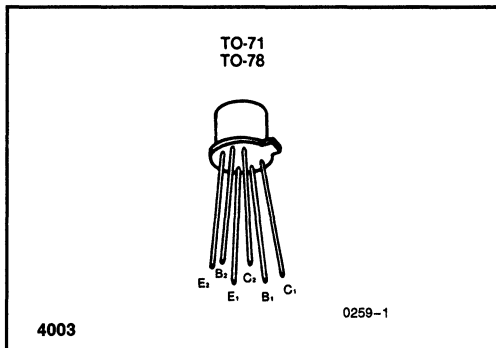
LM114/H, LM114A/AH

GENERAL DESCRIPTION

These devices contain a pair of junction-isolated NPN transistors fabricated on a single silicon substrate. This monolithic structure makes possible extremely tight parameter matching at low cost. Further, advanced processing techniques yield exceptionally high current gains at low collector currents, virtual elimination of "popcorn noise," low leakages and improved long-term stability.

Although designed primarily for high breakdown voltage and exceptional DC characteristics, these transistors have surprisingly good high-frequency performance. The gain-bandwidth product is 300MHz with 1mA collector current and 5V collector-base voltage and 22MHz with 10 μ A collector current. Typical collector-base capacitance is only 1.6 pF at 5V.

PIN CONFIGURATION



FEATURES

- Low Offset Voltage
- Low Drift
- High Current Gain
- Tight Beta Match
- High Breakdown Voltage
- Matching Guaranteed Over A 0V to 45V Collector-Base Voltage Range
- CMRR > 100dB

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Collector-Base Voltage (1)	45V
Collector-Emitter Voltage (1)	45V
Collector-Collector Voltage	45V
Emitter-Base Voltage (1)	6V
Collector Current (1)	20mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (T _C = 25°C)	800mW
Derate above 25°C	14mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71	TO-78
LM114	LM114H
LM114A	LM114AH

ELECTRICAL CHARACTERISTICS (NOTE 2)

Symbol	Parameter	Test Conditions	Maximum Limits		Units
			LM114A, AH	LM114, H	
V _{BE1-2}	Offset Voltage	1 μ A ≤ I _C ≤ 100 μ A	0.5	2.0	mV
I _{B1-2}	Offset Current	I _C = 10 μ A	2.0	10	nA
	Bias Current	I _C = 1 μ A	0.5	40	nA
		I _C = 10 μ A	20		
		I _C = 1 μ A	3.0		
ΔV _{BE} /V	Offset Voltage Change	0V ≤ V _{CB} ≤ V _{MAX} , I _C = 10 μ A	0.2	1.5	mV
ΔI _B /V	Offset Current Change		1.0	4.0	nA

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Maximum Limits		Units
			LM114A, AH	LM114, H	
$\Delta V_{BE}/\Delta T$	Offset Voltage Drift	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $I_C = 10\mu\text{A}$	2.0	10	$\mu\text{V}/^\circ\text{C}$
$\Delta I_{B1-2}/\Delta T$	Offset Current		12	50	nA
$\Delta I_B/\Delta T$	Bias Current		60	150	
I_{CBO}	Collector-Base Leakage Current	$V_{CB} = V_{MAX}$	10	50	pA
		$T_A = 125^\circ\text{C}$ (Note 3)	10	50	nA
I_{CEO}	Collector-Emitter Leakage Current	$V_{CE} = V_{MAX}$, $V_{EB} = 0\text{V}$	50	200	pA
		$T_A = 125^\circ\text{C}$ (Note 3)	50	200	nA
I_{C1-C2}	Collector-Collector Leakage Current	$V_{CC} = V_{MAX}$	100	300	pA
		$T_A = 125^\circ\text{C}$ (Note 3)	100	300	nA

NOTES: 1. Per transistor.

2. These specifications apply for $T_A = +25^\circ\text{C}$ and $0\text{V} \leq V_{CB} \leq V_{MAX}$, unless otherwise specified. For the LM114 and LM114A, $V_{MAX} = 30\text{V}$.

3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

M116

Diode Protected N-Channel Enhancement Mode MOSFET General Purpose Amplifier

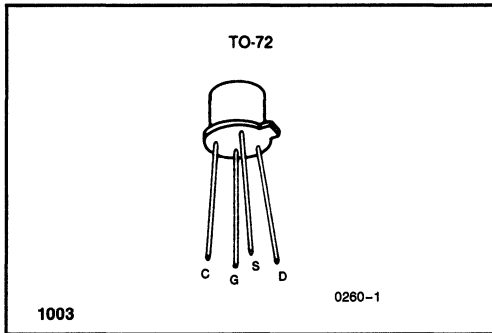


M116

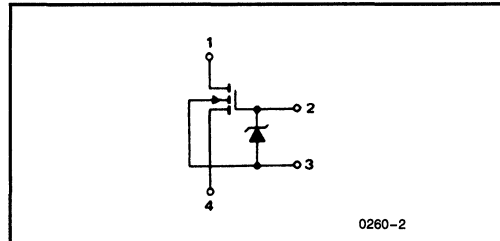
FEATURES

- Low I_{GSS}
- Integrated Zener Clamp for Gate Protection

PIN CONFIGURATION



DEVICE SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain to Source Voltage	30V
Gate to Drain Voltage	30V
Drain Current	50mA
Gate Zener Current	$\pm 0.1\text{mA}$
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	225mW
Derate above 25°C	$2.2\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-72
M116

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

Symbol	Parameter	Test Conditions	M116		Units
			Min	Max	
$r_{DS(on)}$	Drain Source ON Resistance	$V_{GS} = 20\text{V}, I_D = 100\mu\text{A}$		100	Ω
		$V_{GS} = 10\text{V}, I_D = 100\mu\text{A}$		200	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 10\mu\text{A}$	1	5	V
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 1\mu\text{A}, V_{GS} = 0$	30		
BV_{SDS}	Source-Drain Breakdown Voltage	$I_S = 1\mu\text{A}, V_{GD} = V_{BD} = 0$	30		
BV_{GBS}	Gate-Body Breakdown Voltage	$I_G = 10\mu\text{A}, V_{SB} = V_{DB} = 0$	30	60	
$I_{D(OFF)}$	Drain Cutoff Current	$V_{DS} = 20\text{V}, V_{GS} = 0$		10	nA
$I_{S(OFF)}$	Source Cutoff Current	$V_{SD} = 20\text{V}, V_{GD} = V_{BD} = 0$		10	
I_{GSS}	Gate-Body Leakage	$V_{GS} = 20\text{V}, V_{DS} = 0$		100	pA
C_{gs}	Gate-Source (Note 1)	$V_{GB} = V_{DB} = V_{SB} = 0, f = 1\text{MHz}$ Body Guarded		2.5	pF
C_{gd}	Gate-Drain Capacitance (Note 1)			2.5	
C_{db}	Drain-Body Capacitance (Note 1)	$V_{GB} = 0, V_{DB} = 10\text{V}, f = 1\text{MHz}$		7	
C_{iss}	Input Capacitance (Note 1)	$V_{GB} = 0, V_{DB} = 10\text{V}, V_{BS} = 0, f = 1\text{MHz}$		10	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

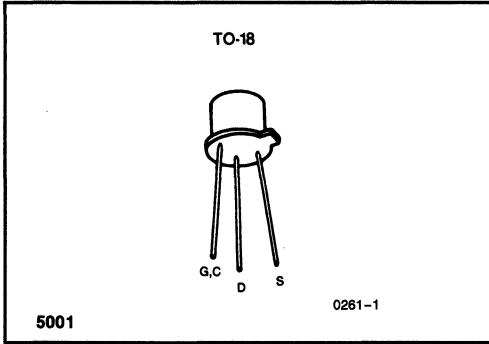
U200-U202 N-Channel JFET Switch



FEATURES

- Low Insertion Loss
- Good OFF Isolation

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Commutators
- Choppers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-30V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Total Device Dissipation ($T_C = 25^\circ\text{C}$)	1.8W
Derate above 25°C	10mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
U200
U201
U202

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	U200		U201		U202		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = -20V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$	-	-1	-	-1	-	-1	nA
			-	-1	-	-1	-	-1	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-30	-	-30	-	-30	-	V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 10\text{nA}$	-0.5	-3	-1.5	-5	-3.5	-10	
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 10V, V_{GS} = -12V$ $T_A = 150^\circ\text{C}$	-	1	-	1	-	1	nA
			-	1	-	1	-	1	μA
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 20V, V_{GS} = 0$	3	25	15	75	30	150	mA
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 0, I_D = 0$ $f = 1\text{kHz}$	-	150	-	75	-	50	ohm
C_{iss}	Common-Source Input Capacitance (Note 2)	$V_{DS} = 20V, V_{GS} = 0$ $f = 1\text{MHz}$	-	30	-	30	-	30	pF
			-	8	-	8	-	8	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)	$V_{DS} = 0, V_{GS} = -12V$	-	8	-	8	-	8	

NOTES: 1. Pulse test required, pulsewidth = 300 μs , duty cycle $\leq 3\%$.
2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

U231-U235

Dual N-Channel JFET

General Purpose Amplifier

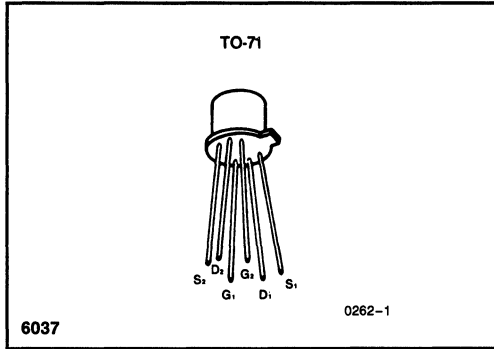


U231-U235

FEATURES

- Good Matching Characteristics

PIN CONFIGURATION



APPLICATIONS

- Differential Amplifiers
- Low and Medium Frequency Amplifiers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage (Note 1)	-50V
Gate Current (Note 1)	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +200°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	1.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
U23X

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units	
			Min	Max		
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$ $T_A = 150^\circ\text{C}$		-100	pA	
				-500	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu A, V_{DS} = 0$	-50		V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DG} = 20V, I_D = 1nA$	-0.5	-4.5		
V_{GS}	Gate-Source Voltage		-0.3	-4.0		
I_G	Gate Operating Current	$V_{DG} = 20V, I_D = 200\mu A$ $T_A = 125^\circ\text{C}$		-50	pA	
				-250	nA	
I_{DSS}	Saturation Drain Current (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	0.5	5.0	mA	
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	$f = 1\text{kHz}$	1000	5000	μS
			$f = 100\text{MHz}$ (Note 4)	1000		
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DG} = 20V, I_D = 200\mu A$	$f = 1\text{kHz}$	600	1600	
g_{os}	Common-Source Output Capacitance	$V_{DS} = 20V, V_{GS} = 0$		10		
g_{os}	Common-Source Output Conductance	$V_{DG} = 20V, I_D = 200\mu A$				
C_{iss}	Common-Source Input Capacitance (Note 4)	$V_{DS} = 20V, V_{GS} = 0$	$f = 1\text{MHz}$		6	pF
					2	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 4)					
\bar{e}_n	Equivalent Short Circuit Input Noise Voltage	$f = 100\text{Hz}$		80	$\frac{nV}{\sqrt{Hz}}$	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Matching Characteristics	Test Conditions	U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Units	
$ I_{G1} - I_{G2} $	Differential Gate Current (Note 4)	$V_{DG} = 20\text{V}$, $I_D = 200\mu\text{A}$, $T_A = 125^\circ\text{C}$	10	10	10	10	10	nA	
$\frac{ I_{DSS1} - I_{DSS2} }{I_{DSS1}}$	Saturation Drain Current Match (Note 2, 4)	$V_{DS} = 20\text{V}$, $V_{GS} = 0$	5	5	5	10	15	%	
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 20\text{V}$, $I_D = 200\mu\text{A}$	$T_A = 25^\circ\text{C}$	5	10	15	20	25	mV
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		$T_A = 25^\circ\text{C}$						$\mu\text{V}/^\circ\text{C}$
			$T_B = 125^\circ\text{C}$	10	25	50	75	100	
$\frac{ g_{fs1} - g_{fs2} }{g_{fs1}}$	Transconductance Match (Notes 2, 4)		$T_A = -55^\circ\text{C}$						%
			$T_B = 25^\circ\text{C}$	10	25	50	75	100	
$ g_{os1} - g_{os2} $	Differential Output Conductance	$f = 1\text{kHz}$	3	5	5	10	15	%	
			5	5	5	5	5	μs	

NOTES: 1. Per transistor.

2. Pulse test required, pulse width = $300\mu\text{s}$, duty cycle $\leq 3\%$.

3. Measured at end points, T_A and T_B .

4. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

U257

Dual N-Channel JFET

High Frequency Amplifier

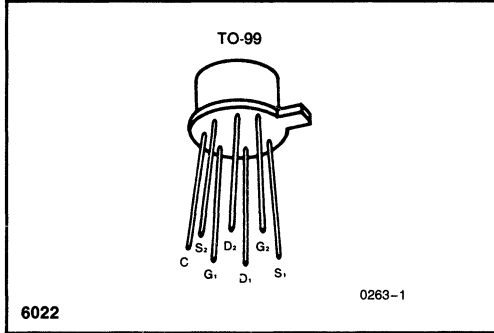


U257

FEATURES

- $g_{fs} > 4500 \mu S$ From DC to 100MHz
- Matched V_{GS} , g_{fs} and g_{os}

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ C$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) -25V

Gate Current (Note 1) 50mA

Storage Temperature Range $-65^\circ C$ to $+200^\circ C$

Operating Temperature Range $-55^\circ C$ to $+150^\circ C$

Lead Temperature (Soldering, 10sec) $+300^\circ C$

	One Side	Both Sides
Power Dissipation	250mW	500mW
($T_A = 85^\circ C$)		
Derate above $25^\circ C$	3.8mW/ $^\circ C$	7.7mW/ $^\circ C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-99
U257

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units			
I_{GSS}	Gate Reverse Current	$V_{GS} = 15V, V_{DS} = 0$		-100	pA			
		$T_A = 150^\circ C$		-250	nA			
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1 \mu A, V_{DS} = 0$	-25		V			
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 10V, I_D = 1nA$	-1	-5				
I_{DSS}	Saturation Drain Current (Note 2)	$V_{DS} = 10V, V_{GS} = 0$	5	40	mA			
g_{fs}	Common-Source Forward Transconductance	$V_{DS} = 10V, I_D = 5mA$ $f = 1kHz$	4500	10,000	μS			
g_{fs}	Common-Source Forward Transconductance	$V_{DG} = 10V, I_D = 5mA$ $f = 100MHz$ (Note 3)	4500	10,000				
g_{os}	Common-Source Output Conductance	$V_{DS} = 10V, I_D = 5mA$ $f = 1kHz$		200				
g_{oss}	Common-Source Output Conductance	$V_{DG} = 10V, I_D = 5mA$		200	pF			
C_{iss}	Common-Source Input Capacitance					$f = 1MHz$	5	
C_{rss}	Common-Source Reverse Transfer Capacitance			1.2				
e_n	Equivalent Input Noise Voltage	(Note 3) $f = 10kHz$		30	$\frac{nV}{\sqrt{Hz}}$			
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 2)	$V_{DS} = 10V, V_{GS} = 0$	0.85	1				
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 10V, I_D = 5mA$		100	mV			
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio					$f = 1kHz$	0.85	1
$ g_{os1} - g_{os2} $	Differential Output Conductance							20

- NOTES:** 1. Per transistor.
 2. Pulse test required, pulse width = 300 μs , duty cycle $\leq 3\%$.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

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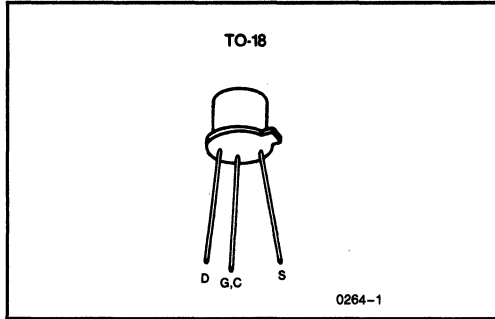
U304-U306 P-Channel JFET Switch



FEATURES

- Low ON Resistance
- $I_{D(off)} < 500\text{pA}$
- Switches directly from TTL Logic (U306)

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Commutators
- Choppers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) 30V

Gate Current 50mA

Storage Temperature Range -65°C to $+200^\circ\text{C}$

Operating Temperature Range -55°C to $+150^\circ\text{C}$

Lead Temperature (Soldering, 10sec) 300°C

Power Dissipation 350mW

Derate above 25°C $2.8\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-18
U304
U305
U306

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	U304		U305		U306		Units
			Min	Max	Min	Max	Min	Max	
I_{GSS}	Gate Reverse Current	$V_{GS} = 20\text{V}, V_{DS} = 0$		500		500		500	pA
		$T_A = 150^\circ\text{C}$		1.0		1.0		1.0	μA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\mu\text{A}, V_{DS} = 0$	30		30		30		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = -15\text{V}, I_D = -1\mu\text{A}$	5	10	3	6	1	4	
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0, I_D = -15\text{mA}$ (U304), $I_D = -7\text{mA}$ (U305), $I_D = -3\text{mA}$ (U306)		-1.3		-0.8		-0.6	
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = -15\text{V}, V_{GS} = 0$	-30	-90	-15	-60	-5	-25	mA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = -15\text{V}, V_{GS} = 12\text{V}$ (U304) $V_{GS} = 7\text{V}$ (U305) $V_{GS} = 5\text{V}$ (U306)		-500		-500		-500	pA
		$T_A = 150^\circ\text{C}$		-1.0		-1.0		-1.0	μA
$r_{DS(on)}$	Static Drain-Source ON Resistance	$V_{GS} = 0\text{V}, I_D = -1\text{mA}$		85		110		175	Ω
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{GS} = 0\text{V}, I_D = 0$ $f = 1\text{kHz}$		85		110		175	Ω

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions				U304		U305		U306		Units
						Min	Max	Min	Max	Min	Max	
C_{iss}	Common-Source Input Capacitance (Note 2)	$V_{DS} = -15\text{V}$, $V_{GS} = 0$	$f = 1\text{MHz}$				27		27		27	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)					$V_{DS} = 0$, $V_{GS} = 12\text{V}$ (U304) $V_{GS} = 7\text{V}$ (U305), $V_{GS} = 5\text{V}$ (U306)		7		7		
$t_{d(on)}$	Turn-ON Delay Time (Note 2)	V_{DD}	U304	U305	U306		20		25		25	ns
t_r			Rise Time (Note 2)	$V_{GS(off)}$	12V	7V	5V		15		25	
$t_{d(off)}$	Turn-OFF Delay Time (Note 2)	R_L	580 Ω	743 Ω	1800 Ω		10		15		20	
t_f	Fall Time (Note 2)	$V_{GS(on)}$	0	0	0		25		40		60	
		$I_{D(on)}$	-15mA	-7mA	-3mA							

NOTES: 1. Pulse test pulsewidth = 300 μs , duty cycle $\leq 3\%$.
 2. For design reference only, not 100% tested.

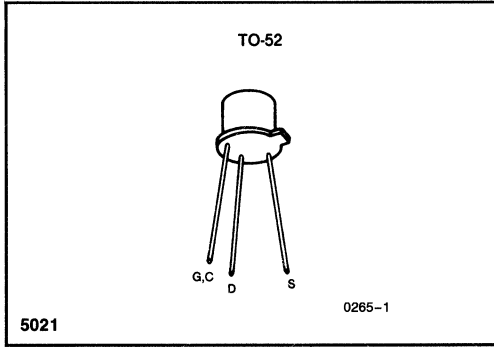
U308-U310 N-Channel JFET High Frequency Amplifier



FEATURES

- High Power Gain
- Low Noise
- Dynamic Range Greater Than 100dB
- Easily Matched to 75Ω Input

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	20mA
Storage Temperature	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	500mW
Derate above 25°C	4mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-52
U308
U309
U310

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	U308			U309			U310			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{GSS}	Gate Reverse Current	V _{GS} = -15V			-150			-150			-150	pA
		V _{GS} = 0 T _A = 125°C			-150			-150			-150	nA
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-25			-25			-25			V
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 10V, I _D = 1nA	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0	
I _{DSS}	Saturation Drain Current (Note 1)	V _{DS} = 10V, V _{GS} = 0	12		60	12		30	24		60	mA
V _{GS(f)}	Gate-Source Forward Voltage	I _G = 10mA, V _{DS} = 0			1.0			1.0			1.0	V
g _{fg}	Common-Gate Forward Transconductance (Note 1)	V _{DS} = 10V, I _D = 10mA	10	17		10	17		10	17		μS
g _{ogs}	Common Gate Output Conductance				250			250			250	μS
C _{gd}	Drain-Gate Capacitance	V _{GS} = -10V, f = 1MHz			2.5			2.5			2.5	pF
C _{gs}	Gate-Source Capacitance	V _{DS} = 10V			5.0			5.0			5.0	
e _n	Equivalent Short Circuit Input Noise Voltage	V _{DS} = 10V, I _D = 10mA		10			10			10		nV/√Hz

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	U308			U309			U310			Units	
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
g _{fg}	Common-Gate Forward Transconductance	V _{DS} = 10V, I _D = 10mA	f = 100MHz		15			15			15	μS	
			f = 450MHz		14			14			14		
g _{ogs}	Common-Gate Output Conductance		f = 100MHz		0.18			0.18			0.18		
			f = 450MHz		0.32			0.32			0.32		
G _{pg}	Common-Gate Power Gain		(Note 2)	f = 100MHz	14	16		14	16		14	16	dB
				f = 450MHz	10	11		10	11		10	11	
NF	Noise Figure	f = 100MHz			1.5	2.0		1.5	2.0		1.5	2.0	
		f = 450MHz			2.7	3.5		2.7	3.5		2.7	3.5	

- NOTES: 1. Pulse test duration = 2ms.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

U401-U406

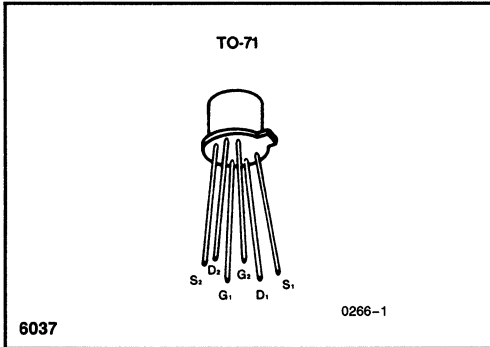
Dual N-Channel JFET Switch



FEATURES

- Minimum System Error and Calibration
- Low Drift With Temperature
- Operates From Low Power Supply Voltages
- High Output Impedance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 50V

Gate Current (Note 1) 10mA

Storage Temperature Range -65°C to +200°C

Operating Temperature Range -55°C to +150°C

Lead Temperature (Soldering, 10sec) +300°C

	One Side	Both Sides
Power Dissipation (T _A = 85°C)	300mW	500mW
Derate above 25°C	2.6mW/°C	5mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
U40X

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	U401		U402		U403		U404		U405		U406		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
BV _{GSS}	Gate-Source Breakdown Voltage	V _{DS} = 0, I _G = -1μA	-50		-50		-50		-50		-50		-50		V
I _{GSS}	Gate Reverse Current (Note 2)	V _{DS} = 0, V _{GS} = -30V		-25		-25		-25		-25		-25		-25	pA
V _{GS(off)}	Gate-Source Cutoff Voltage	V _{DS} = 15V, I _D = 1nA	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	V
V _{GS(on)}	Gate-Source Voltage (on)	V _{DG} = 15V, I _D = 200μA		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3	
I _{DSS}	Saturation Drain Current (Note 3)	V _{DS} = 10V, V _{GS} = 0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA
I _G	Operating Gate Current (Note 2)	V _{DG} = 15V, I _D = 200μA		-15		-15		-15		-15		-15		-15	pA
		T _A = 125°C			-10		-10		-10		-10		-10		nA
BV _{G1-G2}	Gate-Gate Breakdown Voltage	V _{DS} = 0, V _{GS} = 0, I _G = ±1μA	±50		±50		±50		±50		±50		±50		V
g _{fs}	Common-Source Forward Transconductance (Note 3)	V _{DS} = 10V, V _{GS} = 0	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μS
g _{os}	Common-Source Output Conductance														
g _{fs}	Common-Source Forward Transconductance	V _{DG} = 15V, I _D = 200μA	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	
g _{os}	Common-Source Output Conductance														
C _{iss}	Common-Source Input Capacitance (Note 6)	f = 1MHz		8.0		8.0		8.0		8.0		8.0		8.0	pF
C _{rss}	Common-Source Reverse Transfer Capacitance (Note 6)				3.0		3.0		3.0		3.0		3.0		

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	U401		U402		U403		U404		U405		U406		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
e_n	Equivalent Short-Circuit Input Noise Voltage	$V_{DS} = 15\text{V}$, $V_{GS} = 0$	$f = 10\text{Hz}$ (Note 6)			20		20		20		20		20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
CMRR	Common-Mode Rejection Ratio	$V_{DG} = 10$ to 20V , $I_D = 200\mu\text{A}$ (Note 5, 6)	95		95		95		95		90				dB
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	$V_{DG} = 10\text{V}$, $I_D = 200\mu\text{A}$		5		10		10		15		20		40	mV
$\frac{ \Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)	$V_{DG} = 10\text{V}$, $I_D = 200\mu\text{A}$		10		10		25		25		40		80	$\mu\text{V}/^\circ\text{C}$

NOTES: 1. Per transistor.

2. Approximately doubles for every 10°C increase in T_A .

3. Pulse test duration = $300\mu\text{s}$; duty cycle $\leq 3\%$.

4. Measured at end points, T_A , T_B , T_C .

5. $\text{CMRR} = 20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right]$, $\Delta V_{DD} = 10\text{V}$.

6. For design reference only, not 100% tested.

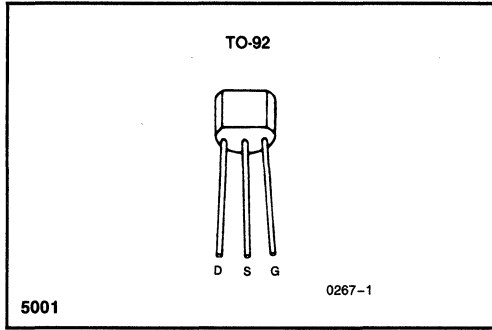
U1897-U1899 N-Channel JFET Switch



FEATURES

- Low Insertion Loss
- No Error or Offset Voltage Generated By Closed Switch

PIN CONFIGURATION



APPLICATIONS

- Analog Switches, Choppers

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-40V
Forward Gate Current	10mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	350mW
Derate above 25°C	3.2mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92	TO-92-18
U1897	U1897-18
U1898	U1898-18
U1899	U1899-18

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	U1897		U1898		U1899		Units
			Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-40		-40		-40		V
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\text{V}, V_{DS} = 0$		-400		-400		-400	pA
I_{DGO}	Drain-Gate Leakage Current	$V_{DG} = 20\text{V}, I_S = 0$		200		200		200	
I_{SGO}	Source-Gate Leakage Current	$V_{SG} = 20\text{V}, I_D = 0$		200		200		200	
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = 20\text{V},$ $V_{GS} = -12\text{V}$ (U1897) $V_{GS} = -8\text{V}$ (U1898) $V_{GS} = -6\text{V}$ (U1899) $T_A = 85^\circ\text{C}$		200		200		200	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$	-5.0	-10	-2.0	-7.0	-1.0	-5.0	V
I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 20\text{V}, V_{GS} = 0$	30		15		8.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 0, I_D = 6.6\text{mA}$ (U1897) $I_D = 4.0\text{mA}$ (U1898) $I_D = 2.5\text{mA}$ (U1899)		0.2		0.2		0.2	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	$I_D = 1\text{mA}, V_{GS} = 0$		30		50		80	Ω

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions			U1897		U1898		U1899		Units
					Min	Max	Min	Max	Min	Max	
C _{dg}	Drain-Gate Capacitance	V _{DG} = 20V, I _S = 0				5		5		5	pF
C _{sg}	Source-Gate Capacitance	V _{SG} = 20V, I _D = 0				5		5		5	
C _{iss}	Common-Source Input Capacitance	V _{DS} = 20V, V _{GS} = 0 f = 1MHz (Note 2)				16		16		16	
C _{rss}	Common-Source Reverse Transfer Capacitance					3.5		3.5		3.5	
t _{d(on)}	Turn ON Delay Time (Note 2)	Switching Time Test Conditions				15		15		20	ns
t _r	Rise Time (Note 2)	U1897 U1898 U1899				10		20		40	
t _{off}	Turn OFF Time (Note 2)	V _{DD}	3V	3V	3V	40	60	80	80		
		V _{GS(on)}	0	0	0						
		V _{GS(off)}	-12V	-8V	-6V						
		R _L	425Ω	770Ω	1120Ω						
		I _{D(on)}	6.6mA	4mA	2.5mA						

NOTES: 1. Pulse test pulsewidth = 300μs; duty cycle < 3%.
 2. For design reference only, not 100% tested.

VCR2N/3P/4N/5P/7N Voltage Controlled Resistors



APPLICATIONS

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

ORDERING INFORMATION

TO-18	TO-72	Wafer	Dice
VCR2N	—	VCR2N/W	VCR2N/D
VCR4N	—	VCR4N/W	VCR4N/D
—	VCR3P	VCR3P/W	VCR3P/D
—	VCR7N	VCR7N/W	VCR7N/D

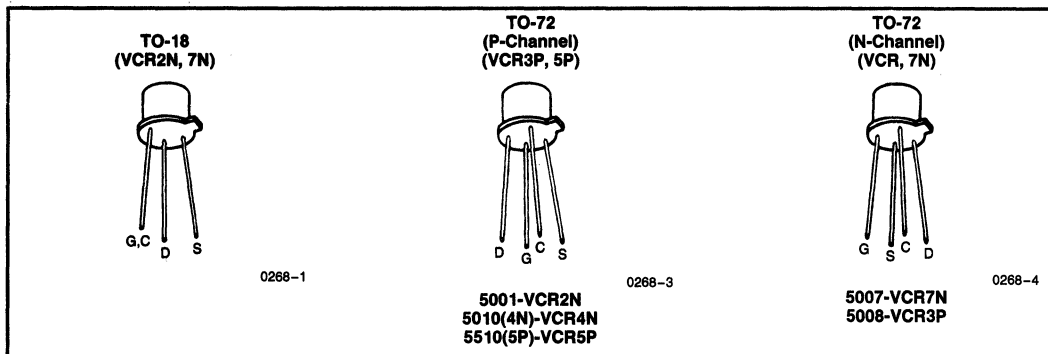
ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 15V
 Gate Current 10mA
 Storage Temperature Range -65°C to +200°C
 Operating Temperature Range -55°C to +175°C
 Lead Temperature (Soldering, 10sec) +300°C
 Power Dissipation 300mW
 Derate above 25°C 2mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

N Channel VCR FETS

Symbol	Parameter	Test Conditions	VCR2N		VCR4N		VCR7N		Units		
			Min	Max	Min	Max	Min	Max			
STATIC											
I _{GSS}	Gate Reverse Current	V _{GS} = -15V, V _{DS} = 0		-5		-0.2		-0.1	nA		
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0	-15		-15		-15		V		
V _{GS(off)}	Gate-Source Cutoff Voltage	I _D = 1μA, V _{DS} = 10V	1.0	3.5	-3.5	-7	-2.5	-5			
r _{ds(on)}	Drain source ON Resistance	V _{GS} = 0, I _D = 0	f = 1kHz		20	60	200	600	4,000	8,000	Ω
DYNAMIC (Note 1)											
C _{dgo}	Drain-Gate Capacitance	V _{GD} = -10V, I _S = 0	f = 1MHz			7.5		3		1.5	pF
C _{sgo}	Source-Gate Capacitance	V _{GS} = -10V, I _D = 0				7.5		3		1.5	

NOTE 1: For design reference only, not 100% tested.

P Channel VCR FETS

Symbol	Parameter	Test Conditions	VCR3P		VCR5P		Units		
			Min	Max	Min	Max			
STATIC									
I _{GSS}	Gate Reverse Current	V _{GS} = 15V, V _{DS} = 0			20		10	nA	
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = 1μA, V _{DS} = 0		15		15		V	
V _{GS(off)}	Gate-Source Cutoff Voltage	I _D = -1μA, V _{DS} = -10V		1.0	5	3.5	7		
r _{ds(on)}	Drain-Source ON Resistance	V _{GS} = 0, I _D = 0	f = 1kHz		70	200	300	900	Ω
DYNAMIC (Note 1)									
C _{dgo}	Drain-Gate Capacitance	V _{GD} = 10V, I _S = 0	f = 1MHz			6		3	pF
C _{sgo}	Source-Gate Capacitance	V _{GS} = 10V, I _D = 0	(Note 1)			6		3	

NOTE 1: For design reference only, not 100% tested.

JFETS AS VOLTAGE REGULATORS

The voltage controlled resistor is a junction field effect transistor whose drain to source ON resistance is controlled by gate to source voltage.

The gate control terminal is high impedance thereby allowing negligible control current. The gate voltage is zero for minimum resistance, and increases as the gate voltage approaches the pinch-off voltage.

This VCR is intended for use on applications using low level AC signals. Figure 1 shows the output characteristics, with an enlarged graph of V_{DS} = 0 for AC signals with no DC component. Operation is in the first and third quadrants; the device will operate in the first quadrant only if a constant

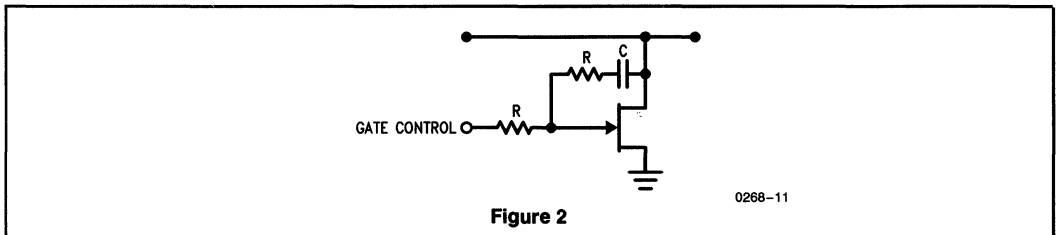
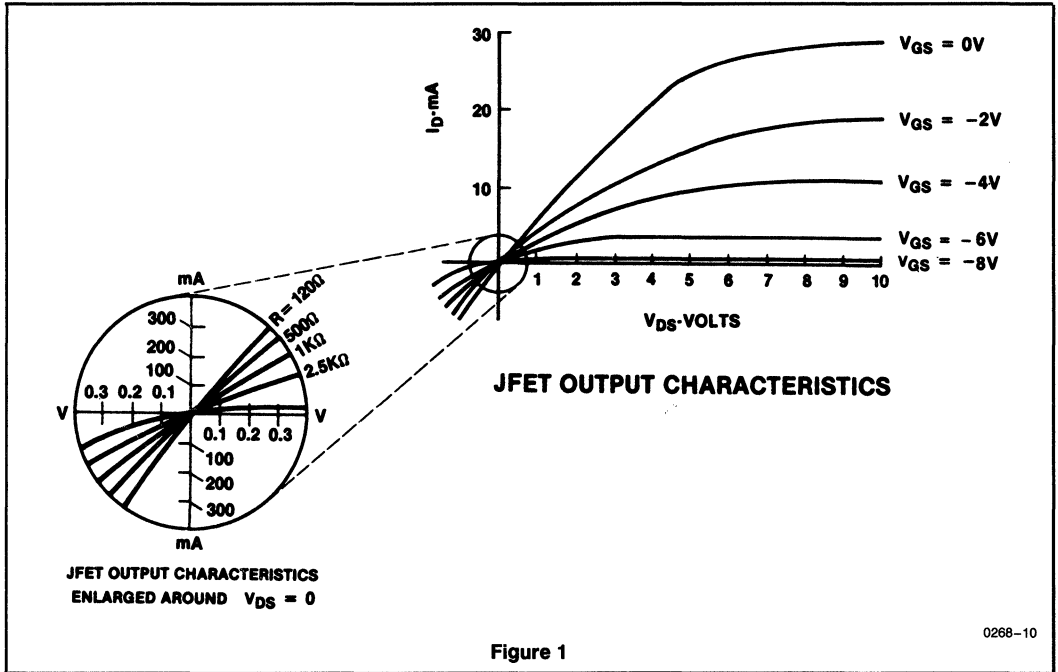
current is applied to the drain and the input signal level is kept low.

Figure 1 also shows that certain combinations of gate control voltage and signal levels will cause resistance modulation. This distortion may be improved by introducing local feedback as shown in figure 2 for best frequency response and impedance levels; eliminating the feedback capacitor will require the gate control voltage to be double for the same ON resistance. The resistor values should be equal, and about 100Ω.

Best gate control voltage for best linearity is up to about 0.8V_{PK}; ON resistance increases rapidly beyond this point.

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

VCR11N

Voltage Controlled Resistors

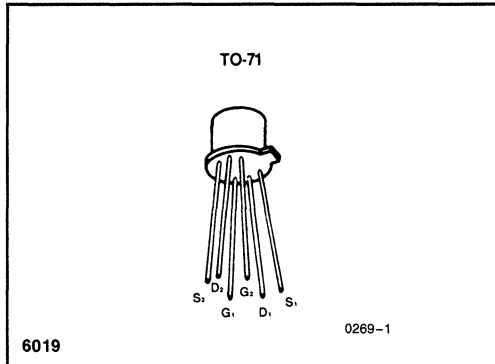


VCR11N

APPLICATIONS

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)
 Gate-Drain or Gate-Source Voltage 25V
 Gate Current 10mA
 Total Device Dissipation at T_A = 25°C
 (Derate at 2.0mW/°C to 175°C) 300mW
 Storage Temperature Range -55°C to +175°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
VCR11N

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Characteristic	Test Conditions		Min	Max	Units
I _{GSS}	Gate Reverse Current	V _{GS} = -15V, V _{DS} = 0			-0.2	nA
BV _{GSS}	Gate-Source Breakdown Voltage	I _G = -1μA, V _{DS} = 0		-25		V
V _{GS(off)}	Gate-Source Cutoff Voltage	I _D = 1μA, V _{DS} = 10V		-8	-12	
r _{ds(on)}	Drain Source ON Resistance	V _{GS} = 0, I _D = 0	f = 1kHz	100	200	Ω
C _{dgo}	Drain-Gate Capacitance (Note 2)	V _{GD} = -10V, I _S = 0	f = 1MHz		8	pF
C _{sgo}	Source-Gate Capacitance (Note 2)	V _{GS} = -10V, I _D = 0			8	
r _{DSmin}		V _{DS} = 100mV	r _{DS1} = 200Ω	.95	1	
r _{DSmax}		V _{GS1} = V _{GS2}	r _{DS1} = 2kΩ	.95	1	

NOTES: 1. V_{GS1} + Control Voltage necessary to force r_{DS} to 200Ω or 2kΩ.
 2. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

Section 11 — Data Communications

- IM26C9111-1
- IM4702/4712 11-19
- IM640211-26
- IM640311-26
- ICL232.....11-36



IM26C91

Universal Asynchronous Receiver/Transmitter (UART)



IM26C91

GENERAL DESCRIPTION

The IM26C91 is a high-performance Universal Asynchronous Receiver/Transmitter that provides full duplex operation. Operating speed can be selected from 18 fixed baud rates ranging from 50 to 38.4K baud, or from an internal programmable counter/timer (16 × clock speed), or from an external 1 × or 16 × clock. The ability to program the operating speed independently makes the UART particularly well suited for dual-speed channel applications, e.g. clustered terminal systems.

The quadruple buffered receiver minimizes potential receiver overrun and reduces overhead in interrupt driven systems. Handshaking capability disables a remote UART transmitter when the receiver buffer is full.

The IM26C91 UART is fabricated in 1.5 micron advanced VLSI CMOS technology which permits monolithic construction and encapsulation in a 0.3" wide 24-pin DIP. The device is TTL compatible and operates from a single +5V power supply.

PRELIMINARY
Subject To Change Without Notice

FEATURES

- **Programmable Data Format:**
 - 5 to 8 Data Bits Plus Parity
 - Odd, Even, no Parity or Force Parity
 - 1, 1.5 or 2 Stop Bits Programmable in 1/16 Bit Increments
- **Parity, Framing, and Overrun Error Detection**
- **False Start Bit Detection**
- **Line Break Detection and Generation**
- **Programmable Channel Mode**
 - Normal (Full-Duplex)
 - Automatic Echo
 - Local Loopback
 - Remote Loopback
- **Single Interrupt Output with Seven Maskable Interrupting Conditions**
- **On-Chip Crystal Oscillator**
- **300 mil 24 Pin DIP**

ORDER INFORMATION

V_{CC} = 5V ± 10%

Part Number	Temperature Range	Package
IM26C91CX24	0° to +70°C	24 Lead Plastic

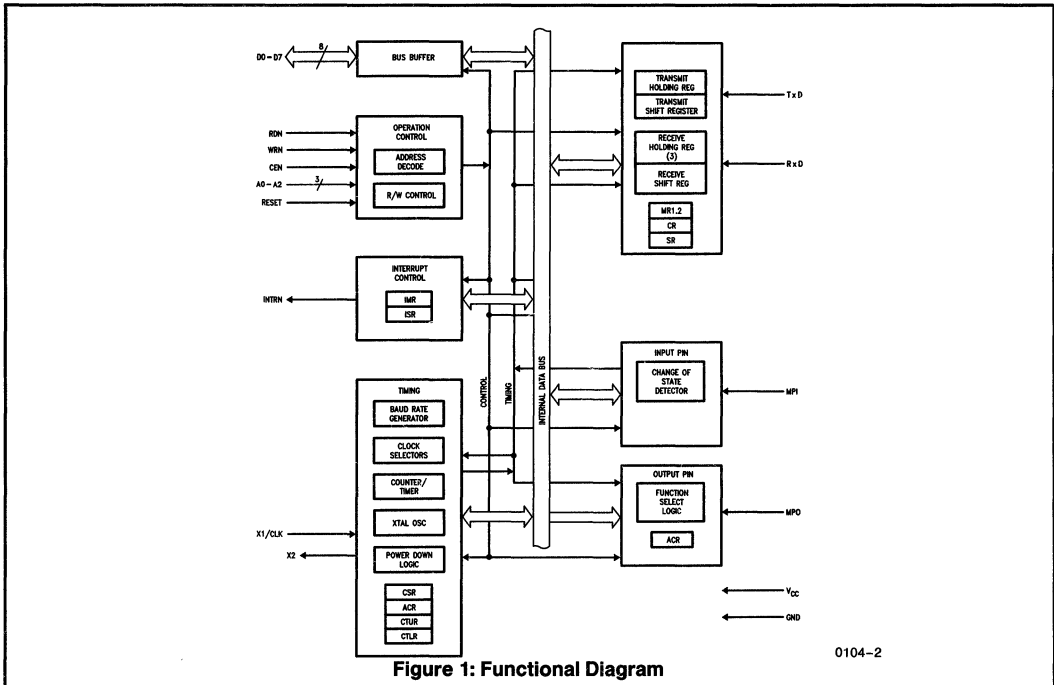


Figure 1: Functional Diagram

0104-2

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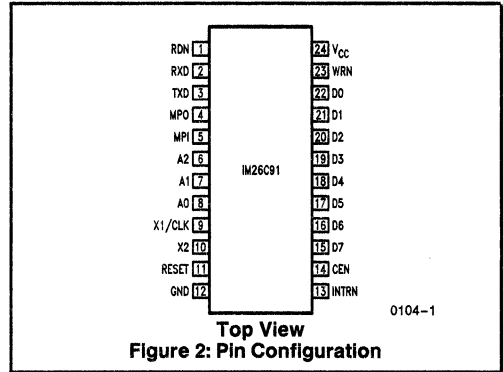
126091-002
March 1987

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Voltage from V_{CC} to GND (Note 1) -0.3 to +6.0V
 Voltage from any Pin to GND (Note 1) -0.3 to $V_{CC} \pm 10\% V$
 Power Dissipation 0.2W
 Operating Temperature Range (Note 2) 0°C to +70°C
 Storage Temperature Range -65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0104-1

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5.0\text{V} \pm 10\% \text{ 3, 4, 5}$

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage All Except X1/CLK X1/CLK		2.0 0.9 V_{CC}		V_{CC} V_{CC}	V V
V_{OL}	Output Low Voltage (Note 6)	$I_{OL} = 2.4 \text{ mA}$				
V_{OH}	Output High Voltage (Note 6) (Except Open Drain Outputs)	$I_{OH} = -400 \mu\text{A}$	2.4			V
I_{IL}	Input Leakage Current	$V_{IN} = 0 \text{ to } V_{CC}$	-10		10	μA
I_{ILL}	Data Bus 3-State Leakage Current	$V_O = 0.4 \text{ to } V_{CC}$	-10		10	μA
I_{OD}	Open Drain Output Leakage Current	$V_O = 0.4 \text{ to } V_{CC}$	-10		10	μA
I_{X1L}	X1/CLK Low Input Current	$V_{IN} = 0, X2 \text{ Floated}$	-100	-30	0.0	μA
I_{X1H}	X1/CLK High Input Current	$V_{IN} = V_{CC}, X2 \text{ Floated}$	0.0	+30	100	μA
OSCILLATOR IN POWER DOWN MODE:						
I_{X1H}	X1/CLK High Input Current	$V_{IN} = V_{CC}, X2 \text{ Floated}$			10	mA
I_{X2L}	X2 Low Output Current	$V_{OUT} = 0, X1/CLK = V_{CC}$			100	μA
I_{X2H}	X2 High Output Current	$V_{OUT} = V_{CC}, X1/CLK = 0\text{V}$			100	μA
I_{CC}	Power Supply Current Standby				20 500	mA μA

NOTES: 1: This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maximums.

- 2: For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
- 3: Parameters are valid over specified temperature range.
- 4: All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0.4V and 2.4V with a transition time of 20 ns maximum. For X1/CLK, this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
- 5: Typical values are at +25°C, typical supply voltages, and typical processing parameters.
- 6: Test condition for outputs: $C_L = 150 \text{ pF}$, except interrupt outputs. Test conditions for interrupt outputs: $C_L = 50 \text{ pF}, R_L = 2.7\text{K} \Omega \text{ to } V_{CC}$.
- 7: Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are OR'ed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
- 8: If CEN is used as the 'strobing' input, this parameter defines the minimum high time between one CEN and the next. The RDN signal must be negated for t_{RPD} to guarantee that any status register changes are valid.
- 9: Consecutive write operations to the same command require at least three edges of the X1 clock between writes.

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NOTE: All typical values have been characterized but are not tested.

AC ELECTRICAL CHARACTERISTICS $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}, V_{CC} = 5.0\text{V} \pm 10\% \text{ 3, 4, 5, 6}$

Symbol	Parameter	Tentative Limits			Units
		Min	Typ	Max	
RESET TIMING (Figure 3)					
t_{RES}	RESET Pulse Width	1.0			μs
BUS TIMING (Figure 4) (Note 7)					
t_{AS}	A0–A2 Set-Up Time to RDN, WRN Low	10			ns
t_{AH}	A0–A2 Hold Time from RDN, WRN High	0			ns
t_{CS}	CEN Set-Up Time to RDN, WRN Low	0			ns
t_{CH}	CEN Hold Time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN Pulse Width	225			ns
t_{DD}	Data Valid after RDN Low			175	ns
t_{DF}	Data Bus Floating after RDN High			100	ns
t_{DS}	Data Set-Up Time before WRN High	100			ns
t_{DH}	Data Hold Time after WRN High	10			ns
t_{RWD}	Time Between READs and/or WRITEs (Note 9)	200			ns
MPI AND MPO TIMING (Figure 5) (Note 7)					
t_{PS}	MPI Input Set-Up Time before RDN Low	0			ns
t_{PH}	MPI Input Hold Time after RDN High	0			ns
t_{PD}	MPO Output Valid after WRN High			370	ns
INTERRUPT TIMING (Figure 6)					
t_{IR}	INTRN Negated: Read RHR (RXRDY/FFULL Interrupt) Write THR (TXRDY/TXEMT Interrupt) Reset Command (Break Change Interrupt) Reset Command (MPI Change Interrupt) Stop C/T Command (Counter Interrupt) Write IMR (Clear of Interrupt Mask Bit)			370 370 370 370 370 270	ns ns ns ns ns ns
CLOCK TIMING (Figure 7) :					
t_{CLK}	X1/CLK High or Low Time	100			ns
f_{CLK}	X1/CLK Frequency	2.0	3.6864	4.0	MHz
t_{CTC}	Counter/Timer Clock High or Low Time	100			ns
f_{CTC}	Counter/Timer Clock Frequency	0		4.0	MHz
t_{RX}	RXC High or Low Time	220			ns
f_{RX}	RXC Frequency (16X) (1X)	0 0		2.0 1.0	MHz MHz
t_{TX}	TXC High or Low Time	220			ns
f_{TX}	TXC Frequency (16X) (1X)	0 0		2.0 1.0	MHz MHz
TRANSMITTER TIMING (Figure 8)					
t_{TXD}	TXD Output Delay from TXC Low			350	ns
t_{TCS}	TXC Output Delay from TXD Output Data	0		150	ns
RECEIVER TIMING (Figure 9)					
t_{RXS}	RXD Data Set-Up Time to RXC High	240			ns
t_{RXH}	RXD Data Hold Time from RXC High	200			ns

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NOTE: All typical values have been characterized but are not tested.

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

PIN DESCRIPTION

Mnemonic	DIP Pin No.	Type	Name and Function
D0-D7	22-15	I/O	Data Bus: Active high 8-bit bidirectional three-state data bus. Bit 0 is the LSB and bit 7 is the MSB. Handles all data, command, and status transfers between the CPU and the UART. Transfer direction is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the three-state condition.
CEN	14	I	Chip Enable: Active low input. When low, data transfers between the CPU and the UART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0-D7 are placed in the three-state condition.
WRN	23	I	Write Strobe: Active low input. A low on this pin while CEN is low, causes the contents of the data bus to be transferred to the register selected by A0-A2. The transfer occurs on the trailing (rising) edge of the signal.
RDN	1	I	Read Strobe: Active low input. A low input, while CEN is low, causes the contents of the register selected by A0-A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0-A2	8-6	I	Address Inputs: Active high address inputs select the UART registers for read/write operations.
INTRN	13	O	Interrupt Request: This active low output is asserted by one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s).
X1/CLK	9	I	Crystal 1: Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	10	O	Crystal 2: Connection for other side of crystal. If an external source is used instead of a crystal this connection should be open.
RXD	2	I	Receiver Serial Data Input: The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock.

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NOTE: All typical values have been characterized but are not tested.

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

PIN DESCRIPTION (Continued)

Mnemonic	DIP Pin No.	Type	Name and Function
TXD	3	0	Transmitter Serial Data Input: The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter clock is specified, the data is shifted on the falling edge of the transmitter clock.
MPO	4	0	Multi-Purpose Output: One of the following functions can be selected for this output pin by programming the auxiliary control register. RTSN —Request to send active low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. CXTO —The counter/timer output. TXC1X —The 1 × clock for the transmitter. TXC16X —The 16 × clock for the transmitter. RXC1X —The 1 × clock for the transmitter. RXC16X —The 16 × clock for the transmitter. TXRDY —The transmitter holding register empty signal. Active low interrupt. RXRDY/FFULL —The receiver FIFO not empty/full signal. Active low interrupt.
MPI	5	I	Multi-Purpose Input: This pin can be programmed to serve as an input for one of the following functions: GPI —General purpose input. The current state of the pin can be determined by reading the ISR. CTSN —Clear-to-Send active low input. CTCLK —Counter/Timer external clock input. RTCLK —Receiver and/or transmitter external clock input. This may be a 1 × or 16 × clock as programmed by CSR [3:0] or CSR [7:4].
V _{CC}	24	I	Power Supply: +5V supply input.
GND	12	I	Ground.

CIRCUIT DESCRIPTION

The IM26C91 UART is a full duplex asynchronous receiver/transmitter whose operating frequency can be selected from its internal baud rate generator or counter/timer, or from an external input.

The functional diagram of the IM26C91 UART is shown in Figure 1. It consists of the receiver and transmitter, a data bus buffer, an interrupt control, an operation control and a timing system. In addition, a multi-purpose input pin can be programmed to serve as an output for a variety of internal functions, including a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TXRDY output or RXRDY/FFULL output (see pin description table).

Registers associated with the communications channel are the Mode Registers, (MR1 and MR2), the Clock Select Register (CSR), the Command Register (CR), the Status Register (SR), the Transmit Holding Register (THR), and the Receiver Holding Register (RHR).

TRANSMITTER

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the Transmit Serial Data Output pin (TXD). It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first.

Following the transmission of the stop bits, if a new character is not available in the THR, the TXD output remains high and a TXEMT bit in the SR will be set to 1.

Transmission resumes and the TXEMT bit is cleared when the CPU loads a new character into the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous low condition) by issuing a **start break** command via the CR. The break is terminated by a **stop break** command.

If the transmitter is disabled, it continues operating until the character currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded into the THR while the transmitter is disabled.

RECEIVER

The receiver accepts serial data on the RXD pin, converts it to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU.

The receiver looks for a high-to-low (mark-to-space) transition of the start bit on the RXD input pin. If a transition is detected, the state of the RXD is sampled again each 16X clock for $7\frac{1}{2}$ clocks (16X clock mode) or at the next rising edge of the bit-time clock (1X clock mode). If RXD is sampled high, the start bit is invalid and the search for a valid start bit is resumed. If RXD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit-time intervals until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RHR and the RXRDY bit in the SR is set to a 1. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

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NOTE: All typical values have been characterized but are not tested.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RXD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point. The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RXRDY status bit is set.

If a break condition is detected, (RXD is low for the entire character including the stop bit) only one character consisting of all zeros will be loaded into the FIFO of the RHR and the received break bit in the SR is set to 1. The RXD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

Data entering the RHR is stored in a first-in-first-out (FIFO) queue with a capacity of three characters. Data is loaded from the Receive Shift Register into the top-most empty position of the FIFO.

The RXRDY bit in the Status Register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three queue positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped', thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the character mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the Receive Shift Register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR [4]) will be set upon receipt of the start bit of the new (overrunning) character.

Wake Up Mode-In addition to the normal transmitter and receiver operation described above, the UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multiprocessor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU (by setting RXRDY) only upon receipt of

RECEIVER (Continued)

a received address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]. A zero transmitted in the A/D bit position identifies the corresponding data bits as data; A one in the A/D bit position identifies the corresponding data bits as an address. The CPU should program the Mode Register prior to loading the corresponding data bits into the THR.

While in this mode, the receiver (whether enabled or disabled) continuously looks at the received data stream. If the receiver is disabled, it sets the RXRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

OPERATION CONTROL

The Operation Control logic receives operation commands from the CPU and generates appropriate signals to internal sections of the UART to control its operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Table 1. Register Addressing

A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	MR1, MR2	MR1, MR2
0	0	1	SR	CSR
0	1	0	Reserved*	CR
0	1	1	RHR	THR
1	0	0	Reserved*	ACR
1	0	1	ISR	IMR
1	1	0	CTU	CTUR
1	1	1	(CTL)	CTLR

*Reserved registers should never be read during normal operation since they are reserved for internal diagnostics.

- ACR — Auxiliary control register
- CR — Command register
- CSR — Clock select register
- CTL — Counter/timer lower
- CTLR — Counter/timer lower register
- CTU — Counter/timer upper
- CTUR — Counter/timer upper register
- MR — Mode Register A
- SR — Status register
- THR — Transmit holding register
- RHR — Receiver holding register

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. The pointer then remains at MR2 so the subsequent accesses are to MR2, unless the pointer is reset to MR1 as described above.

Interrupt Control

A single interrupt output (INTRN) is provided. It is asserted by any of the following internal events:

- Transmit holding register ready
- Transmit shift register empty
- Receive holding register ready or FIFO full
- Change in break received status
- Counter reached terminal count
- Change in MPI input
- High level at the MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain of the above conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupt conditions. However, the bits of the ISR are not masked by the IMR.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and two clock selectors.

The crystal oscillator operates directly from a 3.6864 MHz crystal connected across the X1/CLK and X2 inputs. An external clock of the appropriate frequency may be connected to X1/CLK. If an external clock is used instead of a crystal, X1/CLK is driven by a configuration similar to the one in Figure 5. However, the input-high voltage must be capable of attaining 4.4V. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock or any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection by the receiver and transmitter of any of these baud rates or an external timing signal.

The Counter/Timer operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can also be programmed by ACR[2:0], to be output on the MPO pin.

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OPERATION CONTROL (Continued)

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers (CTUR and CTLR). The **counter ready** bit in the ISR is set once each cycle of the square wave. If the value of CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the **stop counter** command (the command only resets the **counter ready** bit in the ISR). Receipt of a **start C/T** command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a **start C/T** command. Upon reaching terminal count, the **counter ready** bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MP0 is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and the **counter ready** bit is cleared when the counter is stopped by a **stop counter** command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next **start counter** command following a **stop counter** command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However a subsequent **start counter** command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Multi-Purpose Input Pin—The MPI can be programmed as input to one of several UART circuits. The function of the pin is selected by programming the appropriate control register (MR2[4], ACR[6:4], CSR[7:4], 3:0). Only one of the functions may be selected at any given time. If CTS or GPI is selected, a change-of-state detector provided with the pin is activated. A high-to-low or low-to-high transition of the inputs lasting longer than 25–50 μ sec sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input pin pulse detection circuitry uses a 38.4 kHz sampling clock derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25 μ sec (assuming a 3.6864 MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires that two successive samples at the new logic level be observed. Consequently, the minimum duration of the signal change is 25 μ sec if the transition occurs coincident with the first sample pulse. The 50 μ sec time refers to the condition where the change-of-state is just missed and the first change-of-state is not detected until after an additional 25 μ sec.

REGISTERS

The operation of UART is programmed by writing control words into the appropriate register. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is as described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Changing the contents of a register during operation may cause operation problems— e.g., changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. The contents of the MR, the CSR, and the ACR should only be changed while the receiver(s) and transmitter(s) are disabled, and certain changes to the ACR should only be made while the C/T is stopped.

The bit formats of the UART registers are depicted in Table 2 and described below.

MR1—Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a *set pointer* command applied via the CR. After reading or writing MR1, the pointers are set to MR2.

MR1[7]—Receiver Request-To-Send Control. This bit controls the deactivation of the RTSN output (MP0) by the receiver. This output is manually asserted and negated by commands applied via the Command Register. A “1” in MR1[7] causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. The feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6]—Receiver Interrupt Select. This bit selects either the receiver ready status (RXRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5]—Error Mode Select. This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis (the status applies only to the character at the top of the FIFO). In the block mode, the status provided in the SR for these bits is the accumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3]—Parity Mode Select. If “with parity” or “force parity” is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. If MR1[4:3] = 11, the channel operates in the special wake-up mode.

MR1[2]—Parity Type Select. This bit selects the parity type (odd or even) if the “with parity” mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the “force parity” mode is programmed. It has no effect if the “no parity” mode is programmed. In the special wake-up mode, it selects the polarity of the A/D bit.

MR1[1:0]—Bits-Per-Character Select. This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

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REGISTERS (Continued)**MR2—Mode Register 2**

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6]—Mode Select. The UART can operate in one of four modes: MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TXRDY and TXEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be selected. A local loopback mode is selected if MR2[7:6] = 10. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TXD output is held high.
4. The RXD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.

7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Similarly, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of auto echo or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated to be in auto-echo by assertion of RXRDY), and the transmitter is enabled, the transmitter will remain in auto echo mode until one full stop bit has been retransmitted.

MR2[5]—Transmitter Request-to-Send Control. This bit controls the deactivation of the RTSN output (MP0) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. If MR2[5] = 1, RTSN is reset automatically one bit time after the character in the transmit shift register and in the THR (if any) are completely transmitted; includes the programmed number of stop bits if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode (MR2[5] = 1).
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next-to-last character of the message is being sent by waiting until *transmitter ready* is asserted. Disable transmitter after the last character is loaded into the THR.
6. The last character will be transmitted and RTSN will be reset one bit-time after the last stop bit.

MR2[4]—Clear-to-Send Control. The state of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSN each time it is ready to send a character. If it is asserted (low), the character is transmitted. If it is negated (high), the TXD output remains in the marking state and the transmission is delayed until CTSN goes low. Changes in CTSN while a character is being transmitted does not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0]—Stop Bit Length Select. This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of $\frac{9}{16}$ to 1 and $1\frac{1}{16}$ to 2 bits, in increments of $\frac{1}{16}$ bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, $1\frac{1}{16}$ to 2 stop bits can be programmed in increments of $\frac{1}{16}$ bit. In all cases, the receiver only checks for a mark condition at the center of the first stop-bit position (one bit-time after the last data bit, or after the parity bit if parity is enabled). If an external $1 \times$ clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

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NOTE: All typical values have been characterized but are not tested.

Table 2. Register Bit Formats

MR1							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RXRTS CONTROL 0 = no 1 = yes	R/INT SELECT 0 = RXRDY 1 = FFULL	ERROR MODE 0 = char 1 = blobk	PARITY MODE 00 = with parity 01 = force parity 10 = no parity 11 = special mode		PARITY TYPE 0 = even 1 = odd	BITS PER CHAR 00 = 5 01 = 6 10 = 7 11 = 8	

MR2							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CHANNEL MODE 00 = Normal 01 = Auto Echo 10 = Lock Loop 11 = Remote Loop		Tx RTS CONTROL 0 = no 1 = yes	CTS ENABLE Tx 0 = no 1 = yes	STIP BIT LENGTH* 0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750 4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000 8 = 1.563 9 = 1.625 A = 1.688 B = 1.750 C = 1.813 D = 1.875 E = 1.938 F = 2.000			

*Add 0.5 to values shown for 0-7, if channel is programmed for 5 bits/char.

CSR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RECEIVER CLOCK SELECT See Text				TRANSMITTER CLOCK SELECT See Text			

CR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
MISCELLANEOUS COMMANDS See Text				DISABLE Tx 0 = no 1 = Yes	ENABLE Tx 0 = no 1 = yes	DISABLE Rx 0 = no 1 = yes	ENABLE Rx 0 = no 1 = yes

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Table 2. Register Bits Formats (Continued)

SR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RECEIVED BREAK 0 = no 1 = yes *	FRAMING ERROR 0 = no 1 = yes *	PARITY ERROR 0 = no 1 = yes *	OVERRUN ERROR 0 = no 1 = yes	TXEMT 0 = no 1 = yes	TXRDY 0 = no 1 = yes	FFULL 0 = no 1 = yes	RXRDY 0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode they are reset when the corresponding data character is read from the FIFO.

ACR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BRG SET SELECT 0 = Set 1 1 = Set 2	COUNTER/TIMER MODE AND SOURCE See Text			POWER DOWN MODE 0 = On 1 = off	000 = RTSN 001 = C/T0 010 = TXC(1X) 011 = TXC(16X)	MP0 PIN FUNCTION SELECT 100 = RXC (1X) 101 = RXC(16X) 110 = TXRDY 111 = RXRDY/FFULL	

ISR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
MPI PIN CHANGE 0 = no 1 = yes	MPI PIN CURRENT STATE 0 = low 1 = high	not used	COUNTER READY 0 = no 1 = yes	DELTA BREAK 0 = no 1 = yes	RXRDY/FFULL 0 = no 1 = yes	TXEMT 0 = no 1 = yes	TXRDY 0 = no 1 = yes

IMR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
MPI CHANGE INT 0 = off 1 = on	MPI LEVEL INT 0 = off 1 = on	not used	COUNTER READY INT 0 = off 1 = on	DELTA BREAK INT 0 = off 1 = on	RXRDY FFULL INT 0 = off 1 = on	TXEMT INT 0 = off 1 = on	TXRDY INT 0 = off 1 = on

CTUR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTLR							
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[4]	C/T[2]	C/T[1]	C/T[0]

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Table 3. Baud Rate

	CSR[3:0]/[7:4]			ACR[7] = 0		ACR[7] = 1	
0	0	0	0	50	75		
0	0	0	1	110	110		
0	0	1	0	134.5	134.5		
0	0	1	1	200	150		
0	1	0	0	300	300		
0	1	0	1	600	600		
0	1	1	0	1,200	1,200		
0	1	1	1	1,050	2,000		
1	0	0	0	2,400	2,400		
1	0	0	1	4,800	4,800		
1	0	1	0	7,200	1,800		
1	0	1	1	9,600	9,600		
1	1	0	0	38.4k	19.2k		
1	1	0	1	Timer	Timer		
1	1	1	0	MPI-16x	MPI-16X		
1	1	1	1	MPI-1X	MPI-1X		

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111

CSR—Select Register

CSR[7:4]—Receiver Clock Select. When using a 3.6864 MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

CSR[3:0]—Transmitter Clock Select. This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3.

CR—Command Register

CR is used to write commands to the UART. Multiple commands can be specified in a single write to CR as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

CR[7:4]—Miscellaneous Commands. The encoded value of this field may be used to specify a single command as follows:

- 0000 No command
- 0001 Reset MR pointer. Causes the MR pointer to point to MR1.
- 0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
- 0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.
- 0100 Reset error status. Clears the received break, parity error, framing error and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.
- 0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (SR[3]) to be cleared to zero.

- 0110 Start break. Forces the TXD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit-times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character (or any others loaded after it) has been transmitted (TXEMT must be true before break begins). The transmitter must be enabled to start a break.
- 0111 Stop break. The TXD line will go high (marking) within two bit times. TXD will remain high for one bit time before the next character, if any, is transmitted.
- 1000 Start C/T. In counter or timer modes, causes the contents of CTUR/CTLR to be preset into the counter/timer and starts the counting cycle. In timer mode, any counting cycle in progress when the command is issued is terminated. In counter mode, has no effect unless a stop C/T command was issued previously.
- 1001 Stop counter. In counter mode, stops operation of the counter/timer, resets the counter-ready bit in the ISR, and forces the MP0 output high if it is programmed to be the output of the C/T. In timer mode, resets the counter-ready bit in the ISR but has no affect on the counter/timer itself or on the MP0 output.
- 1010 Assert RTSN. Causes the RTSN output to be asserted (low).
- 1011 Negate RTSN. Causes the RTSN output to be negated (high).
- 1100 Reset MPI change interrupt. Causes the MPI change bit in the interrupt status register (SR[7]) to be cleared to zero.
- 1101 **Reserved.**
- 111x **Reserved.**

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REGISTERS (Continued)

CR[3]—Disabled Transmitter. This command terminates transmitter operation and resets the TXRDY and TXEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2]—Enable Transmitter. Enables operation of the channel A transmitter. The TXRDY status bit will be asserted.

CR[1]—Disable Receiver. This command terminates operation of the receiver immediately—a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wakeup mode is programmed, the receiver operates even if it is disabled (see Wakeup Mode).

CR[0]—Enable Receiver. Enables operation of the receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

SR—Channel Status Register

SR[7]—Receiver Break. This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RXD line returns to the marking state for at least one half bit-time (two successive edges of the internal or external 1X clock).

When this bit is set, the change in break bit in the ISR (SR[3]) is set. ISR[3] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character time in order for it to be detected.

SR[6]—Framing Error (FE). This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]—Parity Error (PE). This bit is set when the parity or force parity mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special wakeup mode, the parity error bit stores the received A/D bit.

SR[4]—Overrun Error (OE). This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character

when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a reset error status command.

SR[3]—Transmitter Empty (TXEMT). This bit will be set when the transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. However, this bit is not set until one character has been transmitted. It is set after transmission of the last stop bit of a character, if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

SR[2]—Transmitter Ready (TXRDY). This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TXRDY is reset when the transmitter is disabled and is set when transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1]—FIFO (FFULL). This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL will be reset by the CPU read and then set by the transfer of the character to the FIFO, which causes all three FIFO positions to be occupied.

SR[0]—Receiver Ready (RXRDY). This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

ACR—Auxiliary Control Register

ACR[7]—Baud Rate Generator Set. This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4]—Counter/Timer Mode and Clock Source Select. This field selects the operating mode of the counter/timer and its clock source as follows:

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REGISTERS (Continued)

ACR[6:4]			Mode	Clock Source
0	0	0	Counter	MPI Pin
0	0	1	Counter	MPI pin divided by 16
0	1	0	Counter	TXC—1 × clock of the transmitter
0	1	1	Counter	Crystal or external clock (× 1/CLK) divided by 16
1	0	0	Timer	MPI Pin
1	0	1	Timer	MPI Pin divided by 16
1	1	0	Timer	Crystal or external clock (× 1/CLK)
1	1	1	Timer	Crystal or external clock (× 1/CLK) divided by 16

ACR[3]—Power Down Mode Select. This bit, when set to zero, selects the power down mode. In this mode, the oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the UART in this mode. This bit must be set to a logic 1 after power up.

ACR[2:0]—MPO Output Select. This field programs the MPO output pin to provide one of the following:

- 000 Request to send active low output (RTSN). This output is asserted and negated via the command register. Mode RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.
- 001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.
- 010 The 1 × clock for the transmitter which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1 × clock is output.
- 011 The 16 × clock for the transmitter. This is the clock selected by CSR[3:0], and is a 1 × clock if CSR[3:0] = 1111.
- 100 The 1 × clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1 × clock is output.
- 101 The 16 × clock for the receiver. This is the clock selected by CSR[7:4], and is a 1 × clock if CSR[7:4] = 1111.
- 110 The transmitter register empty signal, which is the complement of SR[2]. Active low input.
- 111 The receiver ready or FIFO full signal (complement of ISR[2]). Active low output.

ISR—Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR—the true status is provided regardless of the contents of the IMR.

ISR[7]—MPI Change of State. This bit is set when a change of state occurs at the MPI input pin. It is reset by a reset MPI change interrupt command.

ISR[6]—MPI Current State. This bit provides the current state of the MPI pin. The information is unlatched and reflects the state of the pin at the time the ISR is read.

ISR[4]—Counter Ready. In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a *stop counter* command. The command, however, does not stop the C/T.

ISR[3]—Change in Break. This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[2]—Receiver Ready or FIFO Full. The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receive shift register. If there is a character waiting in the receiver shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[1]—Transmitter Empty. This bit is a duplicate of TXEMT (SR[3]).

ISR[0]—Transmitter Ready. This bit is a duplicate of TXRDY (SR[2]).

IMR—Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR—Counter/Timer Register

The CTUR and CTLR hold the eight MSB's and eight LSB's respectively, the value to be used by the counter/tim-

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NOTE: All typical values have been characterized but are not tested.

REGISTERS (Continued)

er in either the counter or timer modes of operation. The minimum value which may be loaded is 0002_{16} .

In the Timer (programmable divider) mode, the C/T generates a square wave whose period is twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be.

The counter ready status bit (SR[4]) is set once each cycle of the square wave. The bit is reset by a stop counter command. The command, however, does not stop the C/T. The generated square wave is output on MP0 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching the terminal count, the *counter-ready* interrupt bit (SR[4]) is set. The counter continues counting past the terminal count until

stopped by the CPU. If MP0 is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time it goes low.

The output returns to the high state and ISR[4] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next *start-counter* command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

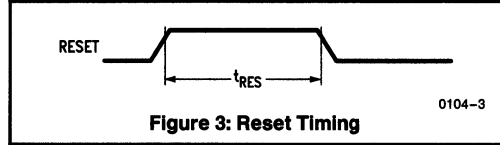


Figure 3: Reset Timing

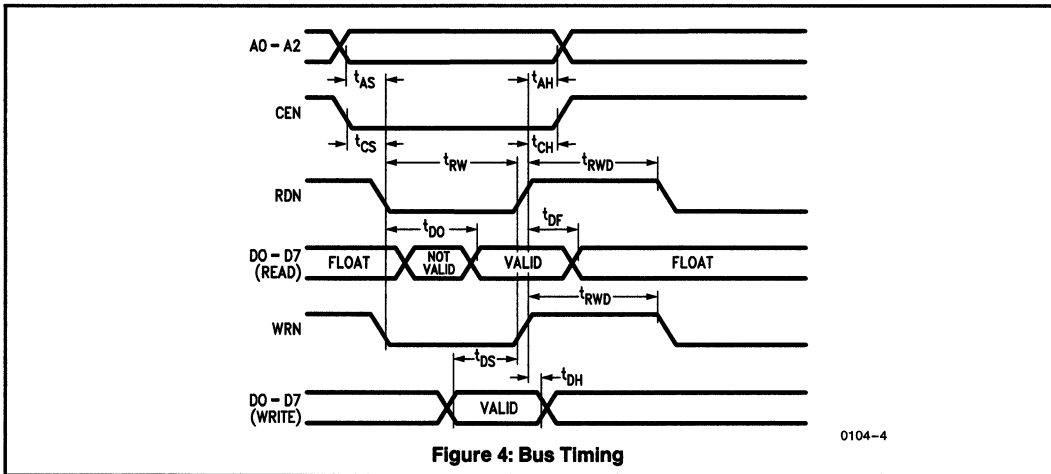


Figure 4: Bus Timing

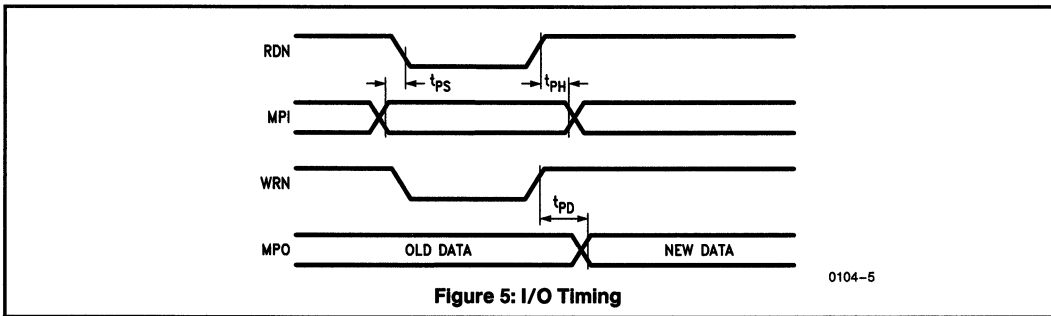
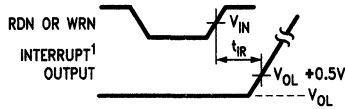


Figure 5: I/O Timing

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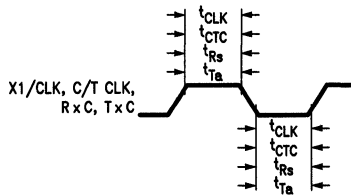


0104-6

NOTES:

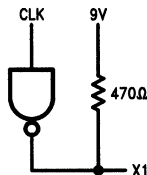
1. INTRN or MPO when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M , to a point 0.5V above V_{OL} . This point represents a noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6: Interrupt Timing



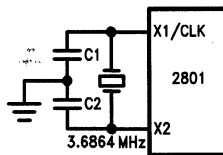
0104-7

DRIVING
FROM EXTERNAL SOURCE



0104-8

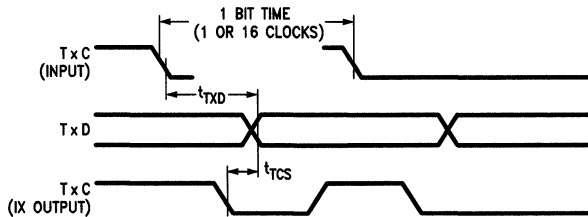
- C1: 10-15 pF + (STRAY < 5 pF)
- C2: 0-5 pF + (STRAY < 5 pF)



0104-9

CRYSTAL SERIES RESISTANCE SHOULD BE LESS THAN 130Ω

Figure 7: Clock Timing



0104-10

Figure 8: Transmit Timing

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NOTE: All typical values have been characterized but are not tested.

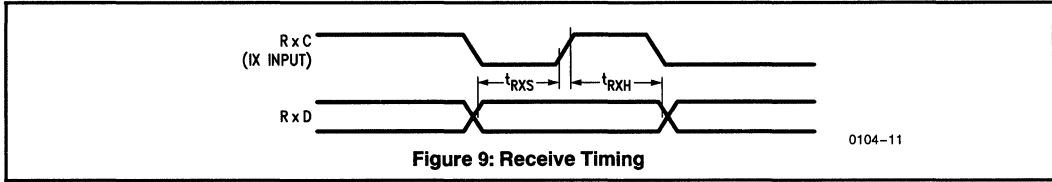
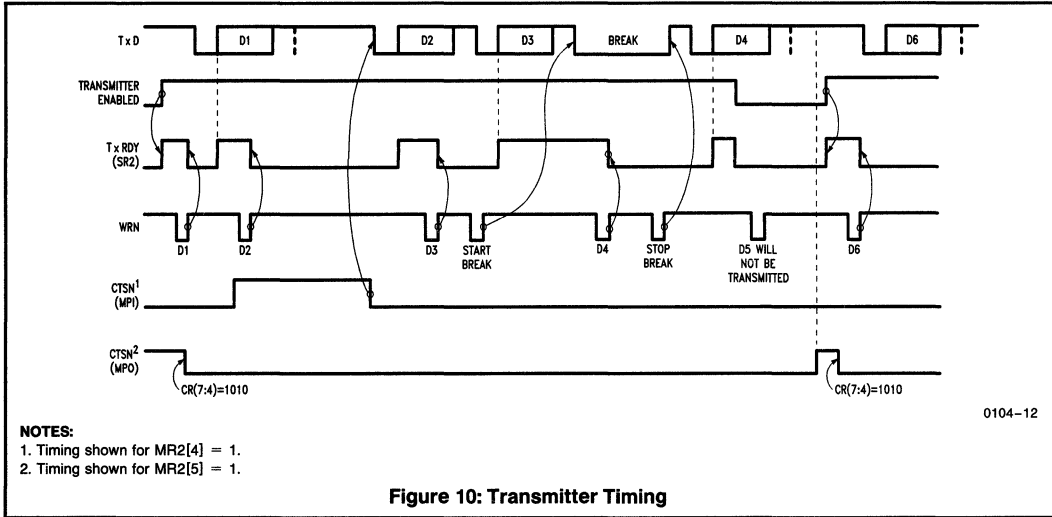


Figure 9: Receive Timing



- NOTES:**
1. Timing shown for MR2[4] = 1.
 2. Timing shown for MR2[5] = 1.

Figure 10: Transmitter Timing

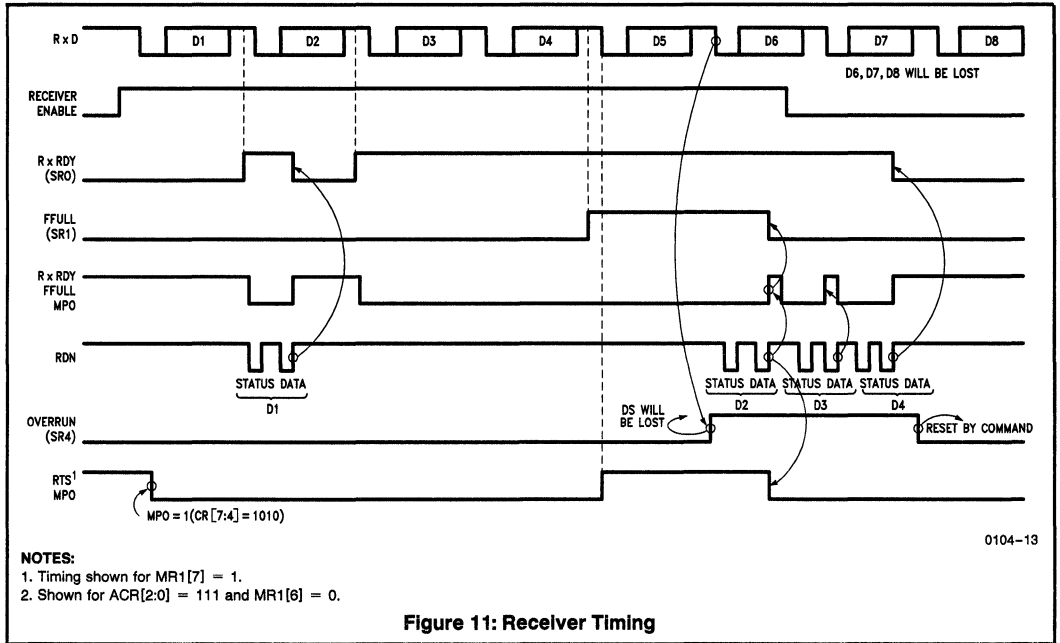


Figure 11: Receiver Timing

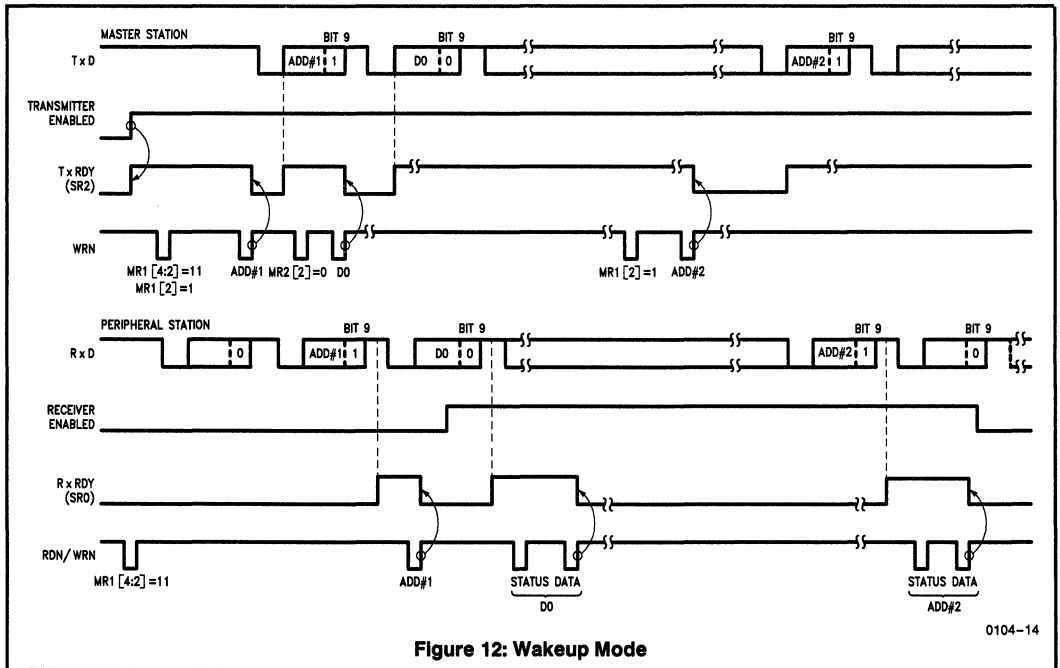


Figure 12: Wakeup Mode

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NOTE: All typical values have been characterized but are not tested.

IM4702/4712

Baud Rate Generator



IM4702/4712

GENERAL DESCRIPTION

The IM4702/12 Baud Rate Generators provide necessary clock signals for digital data transmission systems, such as UARTs, using a 2.4576MHz crystal oscillator as an input. They control up to 8 output channels and can be cascaded for output expansion.

Output rate is controlled by four digital input lines, and with the specified crystal, is selectable from "zero" through 9600 Baud. In addition, 19200 Baud is possible via hardwiring.

Multi-channel operation is facilitated by making the clock frequency and the $\div 8$ prescaler outputs available externally. This allows up to eight simultaneous Baud rates to be generated.

The IM4712 is identical to the IM4702 with the exception that the IM4712 integrates the oscillator feedback resistor and two load capacitors on-chip.

ORDERING INFORMATION

Order Number	Temperature Range	Package
IM4702IJE	-40°C to +85°C	16-pin CERDIP
IM4702IPE	-40°C to +85°C	16-pin PLASTIC
IM4712IJE	-40°C to +85°C	16-pin CERDIP
IM4712IPE	-40°C to +85°C	16-pin PLASTIC

FEATURES

- Provides 14 Most Commonly Used BAUD Rates
- On-Chip Oscillator Requires Only One External Part (IM4712)
- Controls Up to Eight Transmission Channels
- TTL Compatible Outputs Will Sink 1.6mA
- Uses Standard 2.4576MHz Crystal
- Low Power Consumption: 5.5mW Guaranteed Maximum Standby
- Pin and Function Compatible With 4702B and HD-4702
- Inputs Feature Active Pull-Ups

PIN DESCRIPTION

Signal	Pin	Description
Q ₀ –Q ₂	1,2,3	Prescaler Outputs
ECP	4	External Clock Enable Input
CP	5	External Clock Input
O _X	6	Crystal Output
I _X	7	Crystal Input
V _{SS}	8	Negative Supply
C ₀	9	Clock Output
Z	10	Baud Rate Output
S ₀ –S ₃	14-11	Baud Rate Select Inputs
I _M	15	Multiplexed Input
V _{DD}	16	Positive Supply

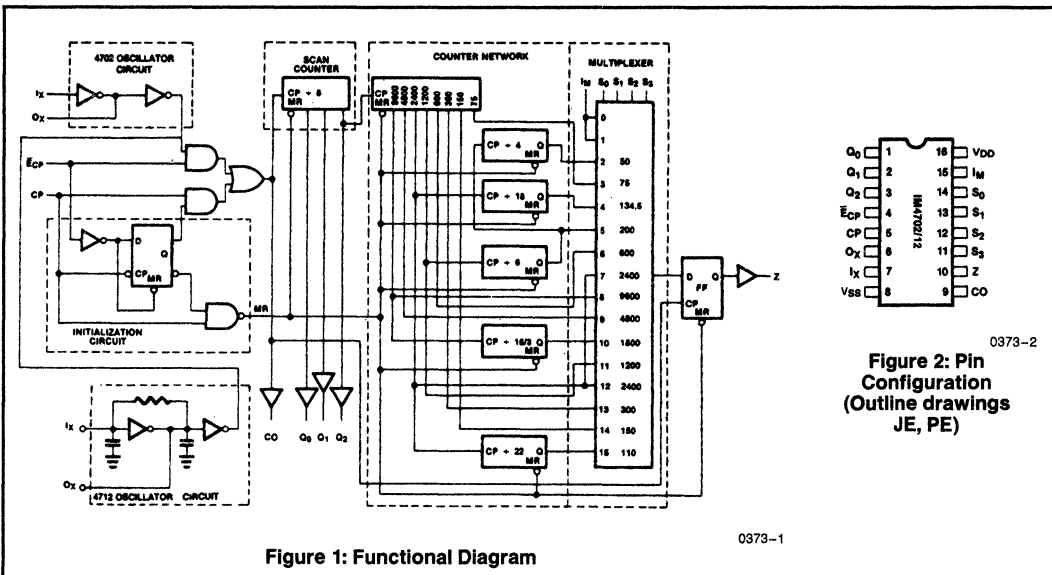


Figure 1: Functional Diagram

Figure 2: Pin Configuration (Outline drawings JE, PE)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$)	+ 8.0V
Input or Output Voltage	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS $V_{DD} = +5V \pm 10\%$ $V_{SS} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter		Test Conditions	Limits		Units
				Min	Max	
V_{IH}	Input Voltage High			70% V_{CC}		V
V_{IL}	Input Voltage Low				30% V_{CC}	
I_{IH}	Input Current High	Other Inputs	$V_{IN} = V_{DD}$ All other pins grounded		+ 1	
		I_x 4712			+ 10	
I_{IL}	Input Current Low	I_x 4702	Pin under test at ground All other Inputs at V_{DD}		- 1	μA
		I_x 4712			+ 10	
		Other Inputs		- 15	- 100	
V_{OH}	Output Voltage High		$I_{OH} < -1 \mu A$; Inputs at V_{SS} or V_{DD}	$V_{DD} - .05$		V
V_{OL}	Output Voltage Low		$I_{OL} < +1 \mu A$; Inputs at V_{SS} or V_{DD}		0.05	
I_{OH}	Output Current High	O_x	Inputs at V_{SS} or V_{DD} $V_0 = V_{DD} - .5$	- 0.1		mA
		All other Outputs		- 0.3		
I_{OL}	Output Current Low	O_x	$V_0 = +2.5V$	- 1.0		
		All other Outputs		$V_0 = 0.4$; Inputs at V_{SS} or V_{DD}	- 0.1	
I_{STBY}	Quiescent Supply Current		$\bar{E}_{CP} = V_{DD}$; $CP = V_{SS}$ All other Inputs = V_{SS} or V_{DD} . All outputs open		1.0	

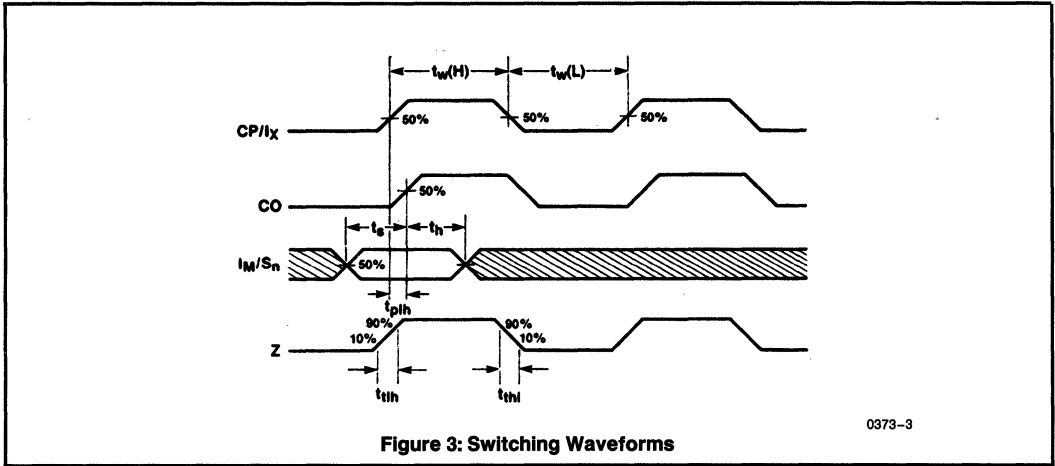
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NOTE: All typical values have been characterized but are not tested.

AC CHARACTERISTICS $V_{DD} = +5V$ $V_{SS} = 0V$, $T_A = 25^\circ C$

Symbol	Parameter		Test Conditions	Limits		Units
				Min	Max	
$t_{ph}(4702)$	Propagation delay(1), I_X to CO		C_L (except O_X) = 50pF $C_{L(O_X)}$ = 7pF $R_L = 200k\Omega$ Input Transition times $\leq 20ns$ Input low = 1.0V Input high = $V_{CC} - 1.0V$		350	ns
$t_{ph}(4702)$					275	
$t_{plh}(4712)$					350	
$t_{pll}(4712)$					275	
t_{plh}	Propagation delay(1), CP to CO				260	
t_{phl}					220	
t_{plh}	Propagation delay(1), CO to Q_n				(2)	
t_{phl}					(2)	
t_{plh}	Propagation delay(1), CO to Z				85	
t_{phl}					75	
t_{tlh}	Output Transition Time, (1) (except O_X)				160	
t_{thl}					75	
t_s	Set Up Time	Select to CO		350		
		I_M to CO		350		
t_h	Hold Time	Select to CO		0		
		I_M to CO		0		
$t_{wCP(L)}$	Clock pulse width(3)			120		
$t_{wCP(H)}$				120		
$t_{wI_X(L)}(4702)$	I_X Pulse Width			160		
$t_{wI_X(H)}(4702)$				160		
$t_{wI_X(L)}(4712)$				190		
$t_{wI_X(H)}(4712)$				190		

- NOTES:**
1. Propagation delays and output transition times will vary with output load capacitance.
 2. For multichannel operation, propagation delay (CO to Q_n) plus set-up time (Select to CO) is guaranteed to be less than 367ns for the IM4702/12.
 3. The first high level clock pulse after E_{cp} goes low must be at least 200ns wide to ensure resetting of all counters.
 4. For design reference only, not 100% tested.



0373-3

Figure 3: Switching Waveforms

FUNCTIONAL DESCRIPTION

Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud (for electromechanical devices) to 9600 baud (for high speed modems). Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the receiver requires a clock rate which is a multiple of the incoming bit rate. Popular MOSLSI UART circuits use a clock that is 16 times the transmitted bit rate. The IM4702/12 can generate 14 standard clock rates from one common high frequency input.

The IM4702/12 contains the following five function subsystems.

Oscillator — For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The IM4702/12 can be driven from two alternate clock sources: (1) When the \bar{E}_{CP} (External Clock Enable) input is LOW, the CP input is the clock source. (2) When the \bar{E}_{CP} input is HIGH, a crystal connected between I_x and O_x , or a signal applied to the I_x input, is the clock source.

Prescaler (Scan Counter) — The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered outputs Q_0 , Q_1 , and Q_2 .

Table 1: Clock Modes and Initialization

I_x	\bar{E}_{CP}	CP	Operation
	H	L	Clocked from I_x
X	L		Clocked from CP
X	H	H	Continuous Reset
X	L		Reset During First CP = HIGH Time

- H = HIGH Level
- L = LOW Level
- X = Don't Care
- = 1st HIGH Level Clock Pulse After \bar{E}_{CP} Goes LOW
- = Clock Pulses

0373-8

Counter Network — The prescaler output Q_2 is a square wave of $1/8$ the input frequency, and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is $16 \times 9.6\text{kHz} = 153.6\text{kHz}$. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

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NOTE: All typical values have been characterized but are not tested.

The other five bit rates are generated by individual counters:

- bit rate 1200 is divided by 6 to generate bit rate 200,
- bit rate 200 is divided by 4 to generate bit rate 50,
- bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of -0.87% ,
- bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of -0.83% , and
- bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the $\div 16$ feature of the UART, the resulting distortion is less than 0.78% regardless of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer — The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs (Q_0-Q_2). Table 2 lists the correspondence between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, non-standardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

Initialization (Reset) — The initialization circuit generates a common master reset signal for all flip-flops in the IM4702/12. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the \bar{E}_{CP} input goes LOW. Upon initialization, all counters are reset and all outputs will be in the LOW state. When \bar{E}_{CP} is HIGH, selecting the Crystal input, CP must be LOW; a HIGH level on CP would apply a continuous reset.

All inputs to the 4702/12 except I_x have on-chip pull-up circuits; the I_x input of the 4712 has a high value resistor tied to O_x .

Table 2: Truth Table for Rate Select Inputs

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

L = LOW Level
H = HIGH Level

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576MHz.

Table 3: Crystal Specifications

Parameters	Typical Crystal Spec
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250 Ω
Unwanted Modes	-6dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF \pm 0.5pF

APPLICATIONS

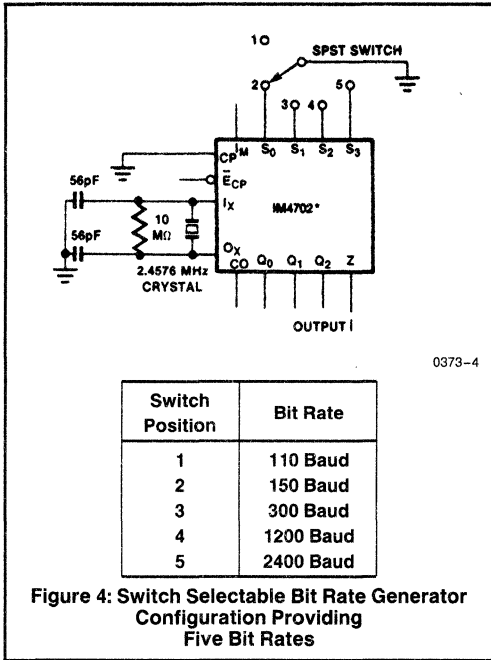
Single Channel Bit Rate Generator

Figure 4 shows the simplest application of the IM4702/12. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 100, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

This mode of operation is commonly chosen for applications using industry standard 1402/6402 UARTs.

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NOTE: All typical values have been characterized but are not tested.



0373-4

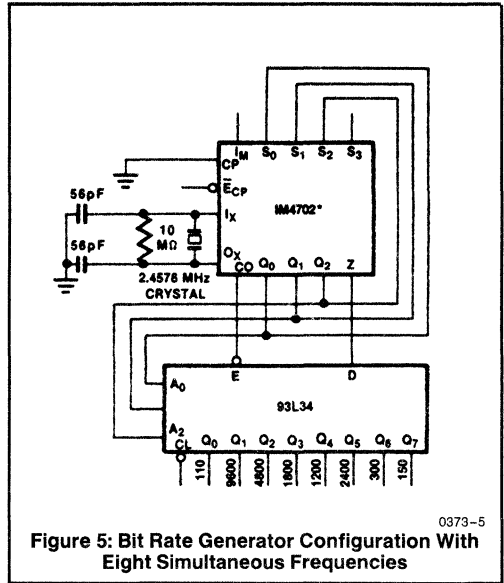
Figure 4: Switch Selectable Bit Rate Generator Configuration Providing Five Bit Rates

Simultaneous Generation of Several Bit Rates

Figure 5 shows a simple scheme that generates eight bit rates on eight output lines, using one IM4702/12 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q₀ to Q₂) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select inputs of the multiplexer causes the IM4702/12 to sequentially interrogate the state of eight different frequency signals. The 93L34 Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) into eight parallel output frequency signals. In the simple scheme of Figure 5, input S₃ is left open (HIGH) and the following bit rates are generated:

- Q₀: 110 Baud Q₃: 1800 Baud Q₆: 300 Baud
- Q₁: 9600 Baud Q₄: 1200 Baud Q₇: 150 Baud
- Q₂: 4800 Baud Q₅: 2400 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

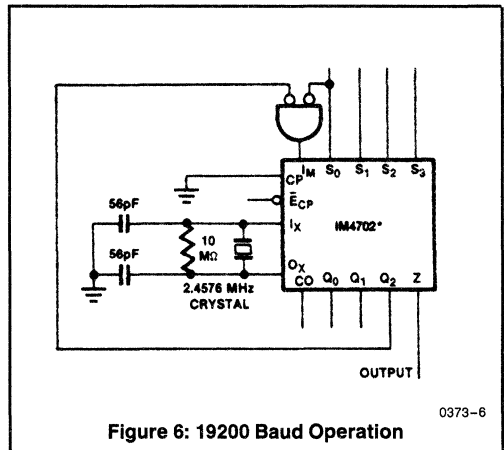


0373-5

Figure 5: Bit Rate Generator Configuration With Eight Simultaneous Frequencies

19200 Baud Operation

A 19200 baud signal is available on the Q₂ output, but is not internally connected to the multiplexer. This signal can be generated on the Z output by connecting the Q₂ output to the I_m input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the IM4702/12. (See Figure 6).



0373-6

Figure 6: 19200 Baud Operation

* The 4712 may replace the 4702 in the above applications with the standard 2.4576MHz crystal. The two external capacitors and one resistor are not required when using the 4712.

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NOTE: All typical values have been characterized but are not tested.

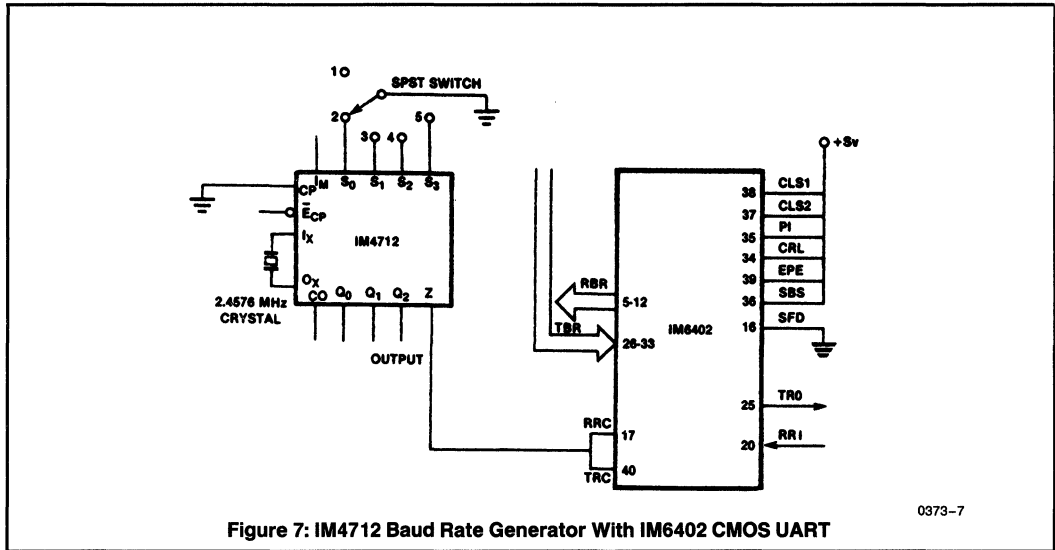


Figure 7: IM4712 Baud Rate Generator With IM6402 CMOS UART

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NOTE: All typical values have been characterized but are not tested.

IM6402/IM6403

Universal Asynchronous Receiver Transmitter (UART)



GENERAL DESCRIPTION

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 8.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

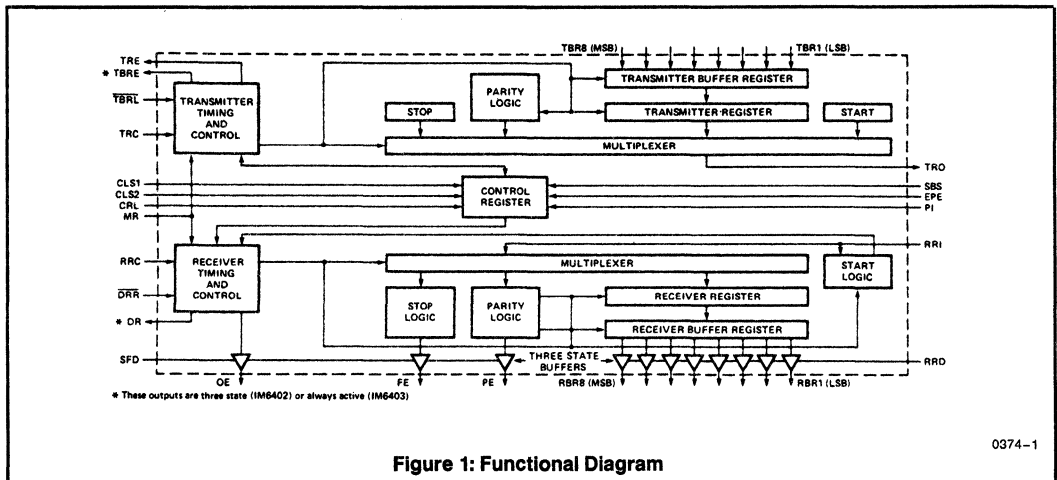
The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 4.

FEATURES

- Low Power — Less Than 10mW Typ. at 2MHz
- Operation Up to 4MHz Clock (IM6402A)
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible With Industry Standard UART's (IM6402)
- On-Chip Oscillator With External Crystal (IM6403)
- Operating Voltage —
 - IM6402-1/03-1: 5V
 - IM6402A/03A: 4-11V
 - IM6402/03: 5V

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-IPL	IM6402/03AIPL	IM6402/03IPL
CERAMIC PKG	IM6402-1/03-11JL	IM6402/03AIJL	IM6402/03IJL
MILITARY TEMP.	IM6402-1/03-1MJL	IM6402/03AMJL	—
MILITARY TEMP. WITH /Hi-Rel processing	IM6402-1/03-1MJL/HR	IM6402/03AMJL/HR	—



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (IM6402/03)

Operating Temperature	-40°C to +85°C
IM6402/03 (I)	-40°C to +85°C
Storage Temperature Range	-65°C to 150°C
Supply Voltage (V _{DD} -V _{SS})	+8.0V
Voltage On Any Input or Output Pin (V _{SS} - 0.3V)	to (V _{DD} + 0.3V)
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

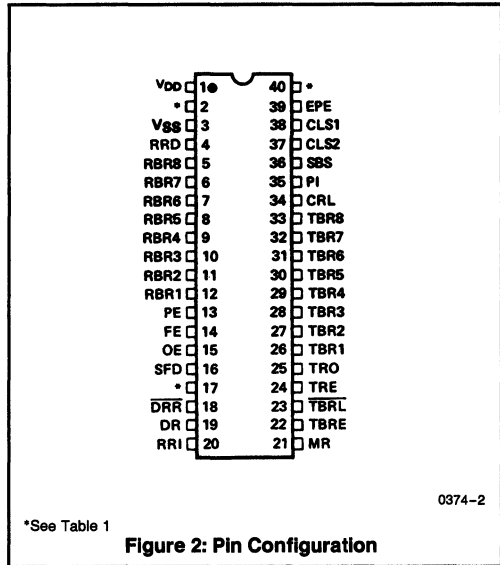


TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT TTL CLOCK	IM6402 w/EXT CMOS CLOCK
2	N/C	Divide Control	Divide Control	Divide Control
17	RRC	XTAL	External Clock Input	No Connection
19	Tri-State	Always Active	Always Active	Always Active
22	Tri-State	Always Active	Always Active	Always Active
40	TRC	XTAL	V _{SS}	External Clock Input

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10% V_{SS} = 0V, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ²	MAX	UNIT
V _{IH}	Input Voltage High		V _{DD} - 2.0			V
V _{IL}	Input Voltage Low				0.8	V
I _{IL}	Input Leakage [1]	V _{SS} ≤ V _{IN} ≤ V _{DD}	-5.0		5.0	μA
V _{OH}	Output Voltage High	I _{OH} = -0.2mA	2.4			V
V _{OL}	Output Voltage Low	I _{OL} = 1.6mA			0.45	V
I _{OLK}	Output Leakage	V _{SS} ≤ V _{OUT} ≤ V _{DD}	-5.0		5.0	μA
I _{STBY}	Power Supply Current Standby	V _{IN} = V _{SS} or V _{DD}		1.0	800	μA
I _{DD}	Power Supply Current IM6402	f _c = 500kHz			1.2	mA
I _{DD}	Power Supply Current IM6403	f _{crystal} = 2.46MHz			3.7	mA
C _{IN}	Input Capacitance [1] [3]	T _A = 25°C		7.0	8.0	pF
C _O	Output Capacitance [1] [3]	T _A = 25°C		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
 2. V_{DD} = 5V, T_A = 25°C.
 3. These parameters are guaranteed but not 100% tested.

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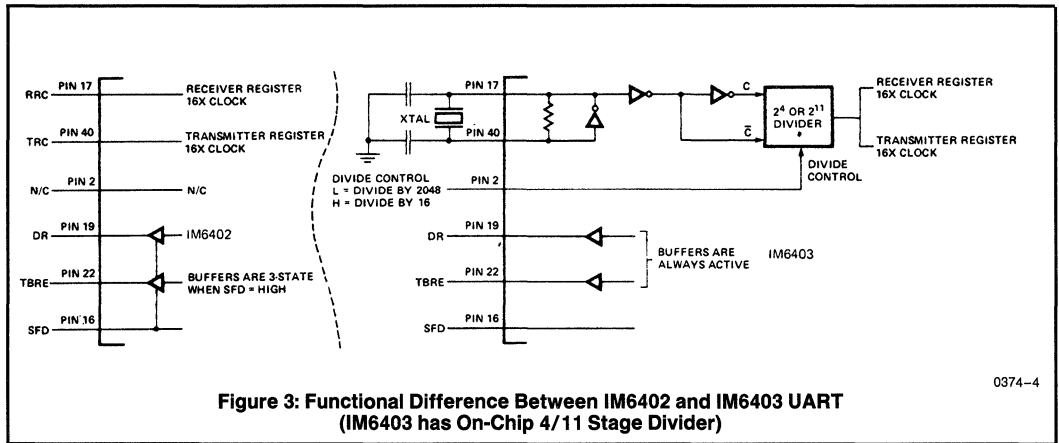
NOTE: All typical values have been characterized but are not tested.

IM6402/IM6403



AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ± 10% V_{SS} = 0V, C_L = 50pF, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ²	MAX	UNIT
f _c	Clock Frequency IM6402	See Timing Diagrams (Figures 4,5,6)	D.C.		1.0	MHz
f _{crystal}	Crystal Frequency IM6403				2.46	MHz
t _{pw}	Pulse Widths CRL, DR _R , TBRL		225	50		ns
t _{mr}	Pulse Width MR		600	200		ns
t _{ds}	Input Data Setup Time		75	20		ns
t _{dh}	Input Data Hold Time		90	40		ns
t _{en}	Output Enable Time			80	190	ns



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The IM6403 differs from the IM6402 on three inputs (RRC, TRC, pin 2) as shown in Figure 3. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 12). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

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NOTE: All typical values have been characterized but are not tested.

IM6402/IM6403



IM6402/IM6403

(IM6402AI/AM, IM6403AI/AM) ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) +12.0V
 Voltage On Any Input or Output Pin ($V_{SS}-0.3V$)
 to ($V_{DD}+0.3V$)

Operating Temperature Range
 IM6402AI/03AI -40°C to +85°C
 IM6402AM/03AM -55°C to +125°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=4.0V$ to $11.0V$, $V_{SS}=0V$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ²	MAX	UNIT
V_{IH}	Input Voltage High		70% V_{DD}			V
V_{IL}	Input Voltage Low				10% V_{DD}	V
I_{IL}	Input Leakage [1] [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1.0		1.0	μA
V_{OH}	Output Voltage High	$I_{OH} = 0mA$		$V_{DD}-0.01$		V
V_{OL}	Output Voltage Low	$I_{OL} = 0mA$		$V_{SS}+0.01$		V
I_{OLK}	Output Leakage	$V_{SS} \leq V_{OUT} \leq V_{DD}$	-1.0		1.0	μA
I_{CC}	Power Supply Current Standby	$V_{IN} = V_{SS}$ or V_{DD}		5.0	500	μA
I_{CC}	Power Supply Current IM6402A	$f_{crystal} = 4MHz$			9.0	mA
I_{CC}	Power Supply Current IM6403A	$f_{crystal} = 3.58MHz$			13.0	mA
C_{IN}	Input Capacitance [1] [3]	$T_A = 25^\circ C$		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	$T_A = 25^\circ C$		8.0	10.0	pF

NOTE: 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
 2. $V_{DD} = 5V$, $T_A = 25^\circ C$.
 3. These parameters are guaranteed but not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{DD} = 10.0V \pm 5\%$, $V_{SS} = 0V$, $C_L = 50pF$, T_A = Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ²	MAX	UNIT
f_c	Clock Frequency IM6402A	See Timing Diagrams (Figures 4,5,6)	D.C.		4.0	MHz
$f_{crystal}$	Crystal Frequency IM6403A				6.0	MHz
t_{pw}	Pulse Widths CRL, DRR, TBRL		100	40		ns
t_{mr}	Pulse Width MR		400	200		ns
t_{ds}	Input Data Setup Time		40	0		ns
t_{dh}	Input Data Hold Time		30	30		ns
t_{en}	Output Enable Time			40	70	ns

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NOTE: All typical values have been characterized but are not tested.

IM6402/IM6403



(IM6402-1I/1M, IM6403-1I/1M)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) +8.0V
 Voltage On Any Input or Output Pin ($V_{SS}-0.3V$)
 to ($V_{DD}+0.3V$)

Operating Temperature Range

IM6402-1I/03-1I -40°C to +85°C
 IM6402-1M/03-1M -55°C to +125°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0 \pm 10\% V_{SS}=0V, T_A=$ Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ²	MAX	UNIT
V_{IH}	Input Voltage High		$V_{DD}-2.0$			V
V_{IL}	Input Voltage Low				0.8	V
I_{IL}	Input Leakage [1] [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1.0		1.0	μA
V_{OH}	Output Voltage High	$I_{OH} = -0.2mA$	2.4			V
V_{OL}	Output Voltage Low	$I_{OL} = 2.0mA$			0.45	V
I_{OLK}	Output Leakage	$V_{SS} \leq V_{OUT} \leq V_{DD}$	-1.0		1.0	μA
I_{CC}	Power Supply Current Standby	$V_{IN} = V_{SS}$ or V_{DD}		1.0	100	μA
I_{CC}	Power Supply Current IM6402 Dynamic	$f_c = 2MHz$			1.9	mA
I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal} = 3.58MHz$			5.5	mA
C_{IN}	Input Capacitance [1] [3]	$T_A = 25^\circ C$		7.0	8.0	pF
C_O	Output Capacitance [1] [3]	$T_A = 25^\circ C$		8.0	10.0	pF

- NOTE:** 1. Except IM6403 XTAL input pins (i.e. pins 17 and 40).
 2. $V_{DD}=5V, T_A=25^\circ C$.
 3. These parameters are guaranteed but not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0V \pm 10\% V_{SS}=0V, C_L=50pF, T_A=$ Operating Temperature Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ²	MAX	UNIT
f_c	Clock Frequency IM6402-1	See Timing Diagrams (Figures 4,5,6)	D.C.		2.0	MHz
$f_{crystal}$	Crystal Frequency IM6403-1				3.58	MHz
t_{pw}	Pulse Widths CRL, DRR, TBRL		150	50		ns
t_{mr}	Pulse Width MR		400	200		ns
t_{ds}	Input Data Setup Time		50	20		ns
t_{dh}	Input Data Hold Time		60	40		ns
t_{en}	Output Enable Time			80	160	ns

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NOTE: All typical values have been characterized but are not tested.

TIMING DIAGRAMS

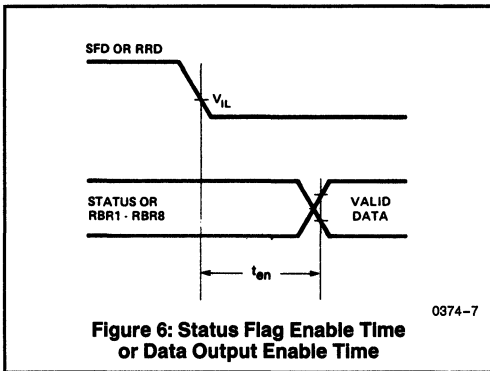
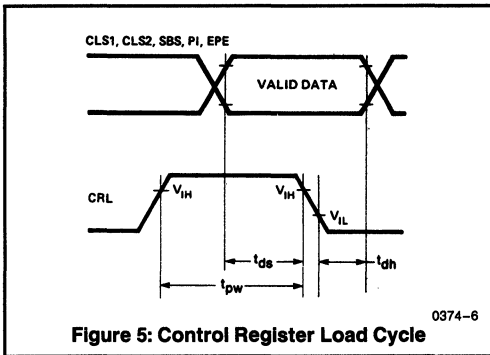
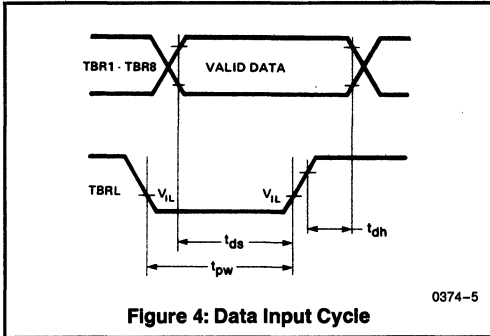


Table 1: IM6402/3 Pin Description

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	V_{SS}	Negative Supply
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e., DRR; active low).

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NOTE: All typical values have been characterized but are not tested.

Table 1: IM6402/3 Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR*, TBRE* to a high impedance state. See Block Diagram and Figure 6. * IM6402 only.
17	IM6402-RRC IM6403-XTAL	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 4.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

Table 1: IM6402/3 Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 5.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits)(CLS1 high CLS2 low 6-bits)(CLS1 low CLS2 high 7-bits)(CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

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NOTE: All typical values have been characterized but are not tested.

Table 2: Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

x= Don't Care

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal.

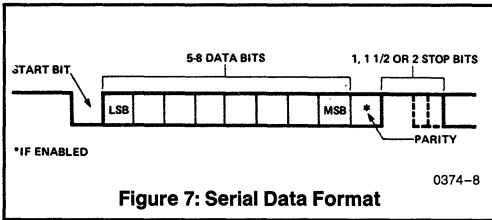


Figure 7: Serial Data Format

Transmitter timing is shown in Figure 8. Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high.

Output data is clocked by TRClock, which is 16 times the data rate. A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Data is automatically transferred to the transmitter register and transmission of that character begins.

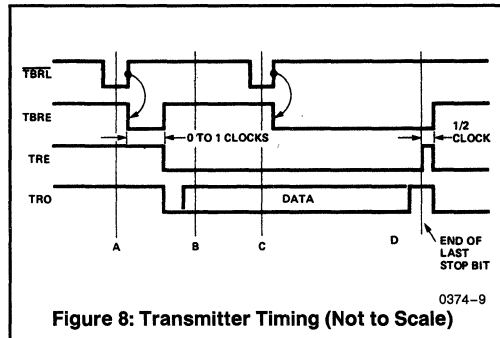
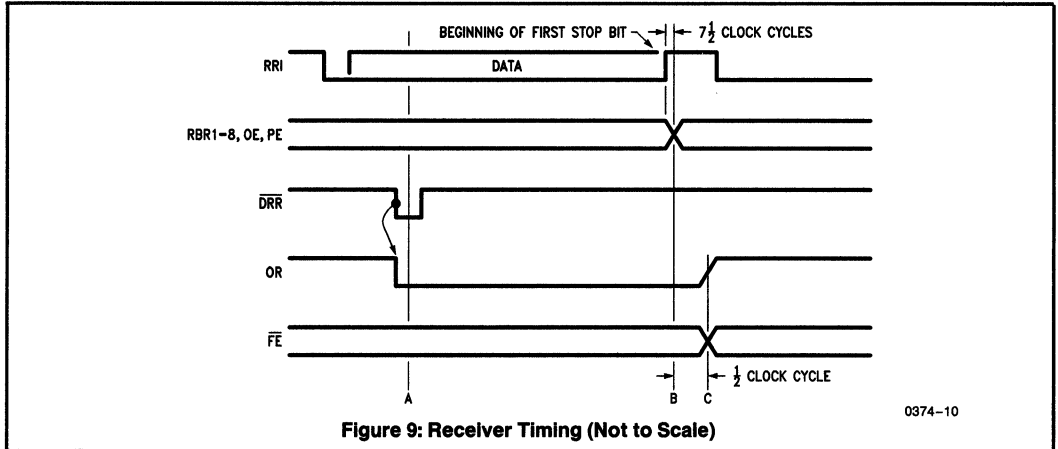


Figure 8: Transmitter Timing (Not to Scale)

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NOTE: All typical values have been characterized but are not tested.



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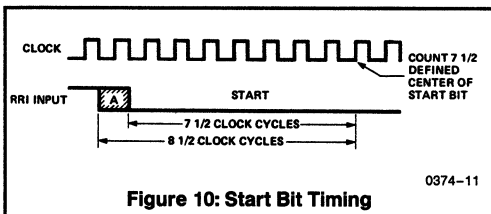
RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 9.

A low level on \overline{DRR} Reset clears the DReady line. During the first stop bit, data is transferred from the receiver register to the RRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RRegister. A logic high on PError indicates a parity error. $\frac{1}{2}$ clock cycle later, DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

START BIT DETECTION

The receiver uses a 16X clock for timing. (See Figure 10.) The start bit (A) could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count $7\frac{1}{2}$. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within $\pm\frac{1}{2}$ clock cycle, $\pm\frac{1}{32}$ bit or $\pm 3.125\%$. The receiver begins searching for the next start bit at the center of the first stop bit.



0374-11

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 11 shows how the IM6402 can be interfaced to an IM80C48 microcomputer system.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs *should be tied to either V_{DD} or V_{SS}* .

The baud rate at which the transmitter and receiver will operate is determined by the IM4702 Baud Rate Generator.

To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM80C48 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not re-trigger RESET. A long reset pulse after power-up ($\sim 20\text{ms}$) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a \overline{DRR} is performed.

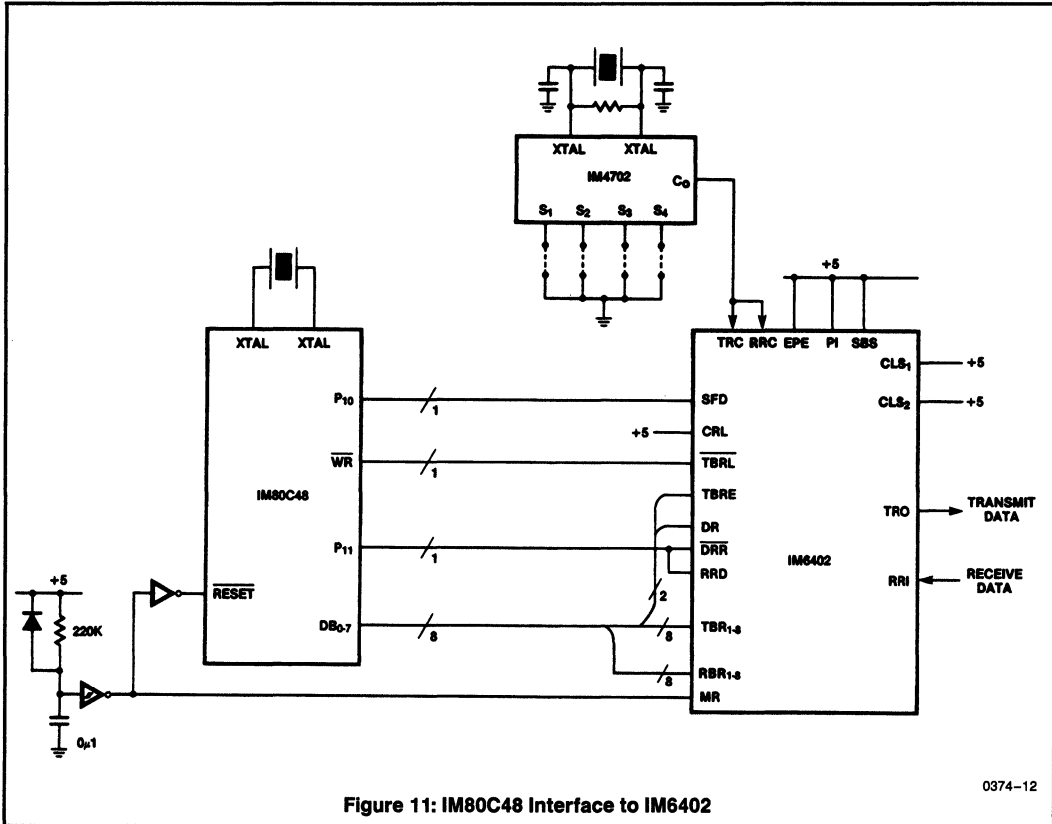


Figure 11: IM80C48 Interface to IM6402

0374-12

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NOTE: All typical values have been characterized but are not tested.

ICL232

+ 5 Volt Powered Dual RS-232 Transmitter/Receiver



PRELIMINARY
Subject To Change Without Notice

GENERAL DESCRIPTION

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C specifications. It requires a single +5V power supply, and features two on-board charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300 ohms power-off source impedance. The receivers can handle up to ± 30 volts, and have a 3 to 7 kilohms input impedance. The receivers also have hysteresis to improve noise rejection.

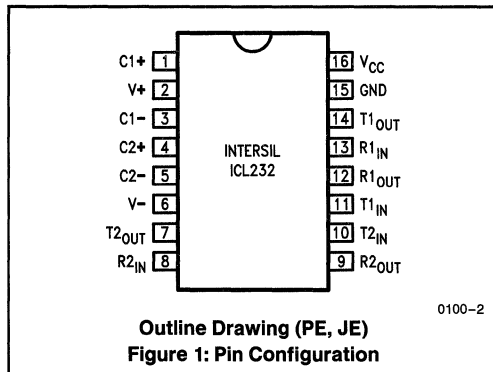
Typical Applications

Any System Requiring RS-232 Communications Port:

- Computers—Portable and Mainframe
- Peripherals—Printers and Terminals
- Portable Instrumentation
- Modems
- Dataloggers

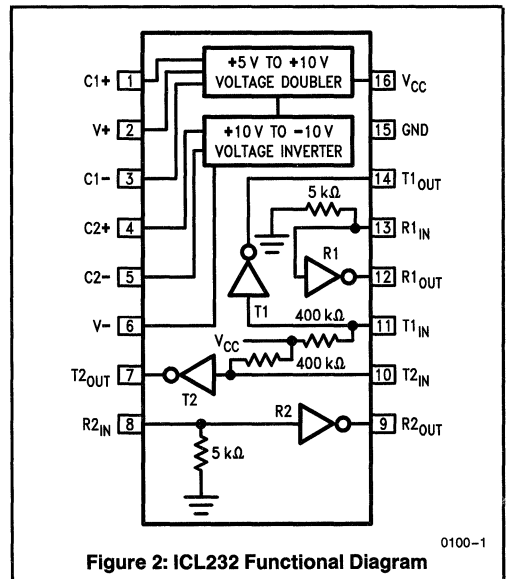
ORDERING INFORMATION

Part	Temperature Range	Package
ICL232CPE	0°C to +70°C	16 Pin Plastic DIP
ICL232CJE		16 Pin CERDIP
ICL232IPE	-25°C to +85°C	16 Pin Plastic DIP
ICL232IJE		16 Pin CERDIP
ICL232MJE	-55°C to +125°C	16 Pin CERDIP



FEATURES

- Meets All RS-232C Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Quadrupler
- Low Power Consumption
- ESD Protection > 2000V
- 2 Drivers
 - $\pm 9V$ Output Swing for +5V Input
 - 300 Ohms Power-off Source Impedance
 - Output Current Limiting
 - TTL/CMOS Compatible
 - 30 V/us Maximum Slew Rate
- 2 Receivers
 - $\pm 30V$ Input Voltage Range
 - 3 to 7 kohms Input Impedance
 - 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges



ABSOLUTE MAXIMUM RATINGS

V _{CC} to ground	+ 6 Volts
V ⁺ to ground	+ 12 Volts
V ⁻ to ground	- 12 Volts
Input Voltages	
T _{1in} , T _{2in}	-0.3 to (V _{CC} + 0.3V)
R _{1in} , R _{2in}	± 30V
Output Voltages	
T _{1out} , T _{2out}	(V ⁺ + 0.3) to (V ⁻ - 0.3V)
R _{1out} , R _{2out}	-0.3 to (V _{CC} + 0.3V)
Short Circuit Duration	
T _{1out} , T _{2out}	Continuous
Continuous Total Power Dissipation (T _a = 25°C)	
CERDIP Package	500mW derate 9.5 mW/°C above 70°C
Plastic Package	375mW derate 7.0 mW/°C above 70°C

Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Operating Temperature Range	
ICL232C	0°C to +70°C
ICL232I	-25°C to +85°C
ICL232M	-55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, T_a = operating temperature range,

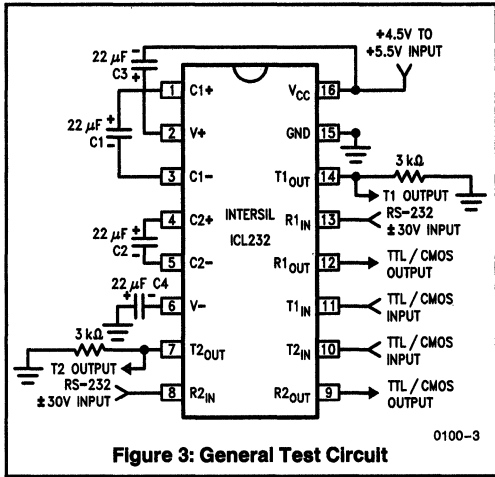
Test Circuit as in Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
T _{OUT}	Transmitter Output Voltage Swing	T _{1OUT} , T _{2OUT} loaded with 3 kΩ to ground	±5	±9	±10	V
I _{CC}	Power Supply Current	Outputs Unloaded, T _a = 25°C		5	10	mA
V _{IL}	T _{in} , Input Logic Low				0.8	V
V _{IH}	T _{in} , Input Logic High		2.0			V
I _p	Logic Pullup Current	T _{1in} , T _{2in} = 0V		15	200	μA
V _{in}	RS-232 Input Voltage Range		-30		+30	V
R _{in}	Receiver Input Impedance	V _{in} = ±3V, ±25V	3.0	5.0	7.0	kΩ
V _{IHL}	Receiver Input Low Threshold	V _{CC} = 5.0V, T _a = 25°C	0.8	1.2		V
V _{IHLH}	Receiver Input High Threshold	V _{CC} = 5.0V, T _a = 25°C		1.7	2.4	V
V _{hyst}	Receiver Input Hysteresis		0.2	0.5	1.0	V
V _{OL}	TTL/CMOS Receiver Output Voltage Low	I _{out} = 3.2mA		0.1	0.4	V
V _{OH}	TTL/CMOS Receiver Output Voltage High	I _{out} = -1.0mA	3.5	4.6		V
t _{pd}	Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5		μs
SR	Instantaneous Slew Rate	C _L = 10 pF, R _L = 3 kΩ, T _a = 25°C (Note 1, 2)			30	V/μs
SR _t	Transition Region Slew Rate	R _L = 3 kΩ, C _L = 2500 pF Measured from +3V to -3V or -3V to +3V		3		V/μs
R _{out}	Output Resistance	V _{CC} = V ⁺ = V ⁻ = 0V, V _{out} = +2V	300			Ω
I _{SC}	RS-232 Output Short Circuit Current	T _{1out} , T _{2out} shorted to GND		±10		mA

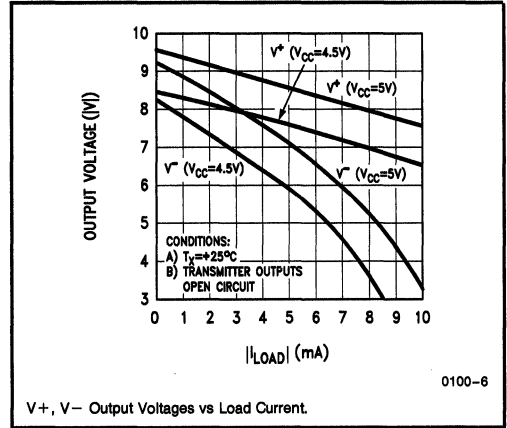
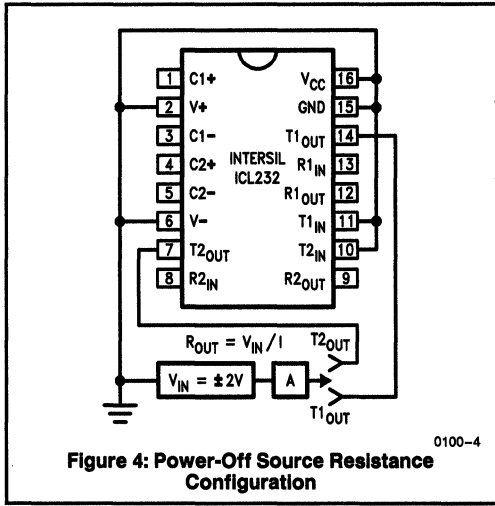
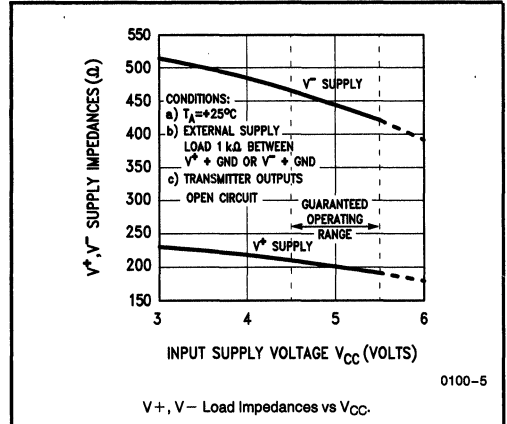
NOTE 1: Guaranteed by design.
NOTE 2: See Figure 5 for definition.

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NOTE: All typical values have been characterized but are not tested.



TYPICAL PERFORMANCE CHARACTERISTICS



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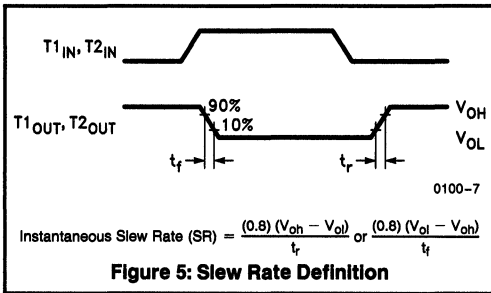
NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS-232C specifications and features low power consumption. The functional diagram (Figure 2) illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage quadrupler, dual transmitters, and dual receivers.

Voltage Converter

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C2 equal to twice V_{CC}. At the same time, C3 is also charged to 2V_{CC}, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to -2V_{CC}. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V⁺) is approximately 200 ohms, and the output impedance of the inverter (V⁻) is approximately 450 ohms. The test circuit (Figure 3) uses 22 uF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V⁺ and V⁻ supplies.

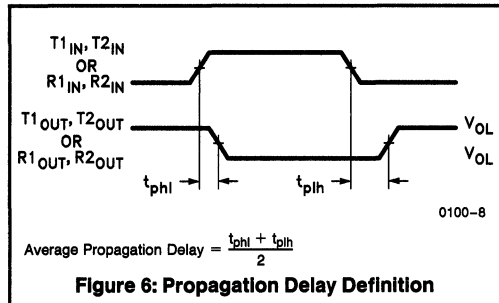


Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V⁻ at the output, and a logic 0 results in a voltage between +5V and (V⁺ - 0.6V). Each transmitter input has an internal 400 kilohm pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of ±5V minimum with the worst case conditions of: both transmitters driving 3kohm minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/us. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300 ohms with ±2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to ±30V while presenting the required 3 to 7 kilohms input impedance even if the power is off (V_{CC}=0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.



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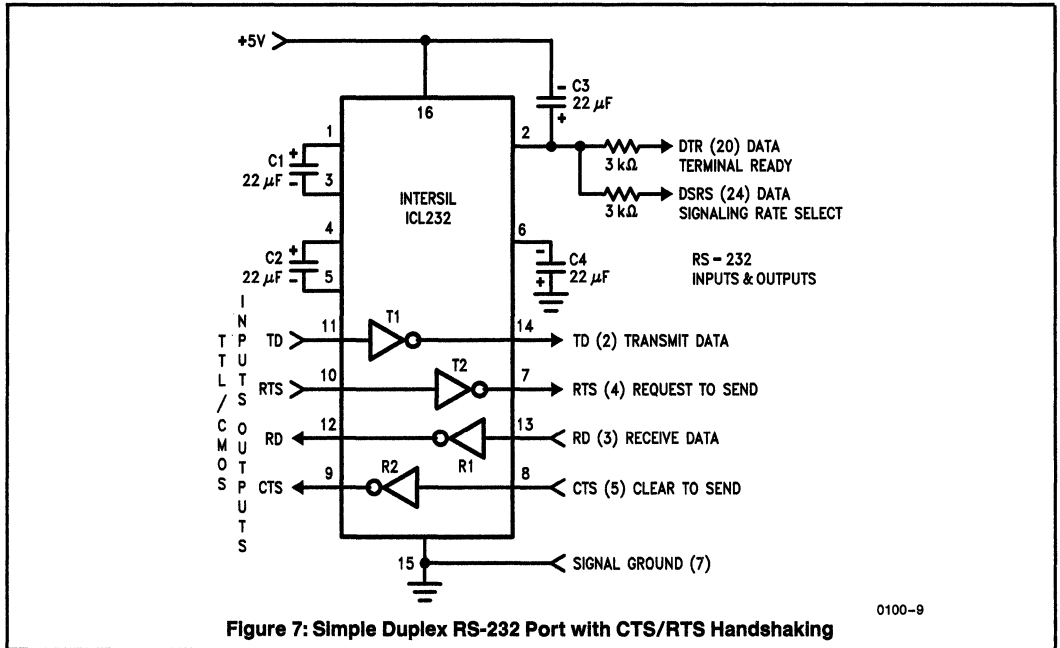
NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where $\pm 12V$ power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 7. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a $3\text{ k}\Omega$ resistor connected to V^+ .

In applications requiring four RS-232 inputs and outputs (Figure 8), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.



0100-9

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NOTE: All typical values have been characterized but are not tested.

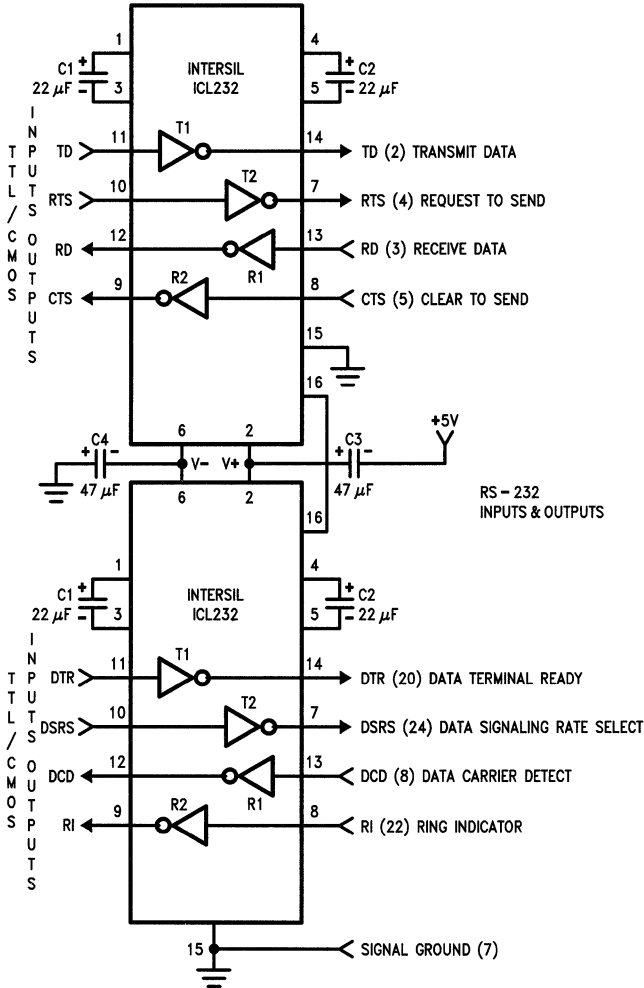


Figure 8: Combining 2 ICL232 for 4 Pairs of RS-232 Inputs and Outputs

0100-10

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NOTE: All typical values have been characterized but are not tested.

Section 12 — Digital Signal Processing

IM29C128	12-1
IM29C510	12-7
EVK-128	12-19

IM29C128

Finite Impulse Response Filter Controller



IM29C128

GENERAL DESCRIPTION

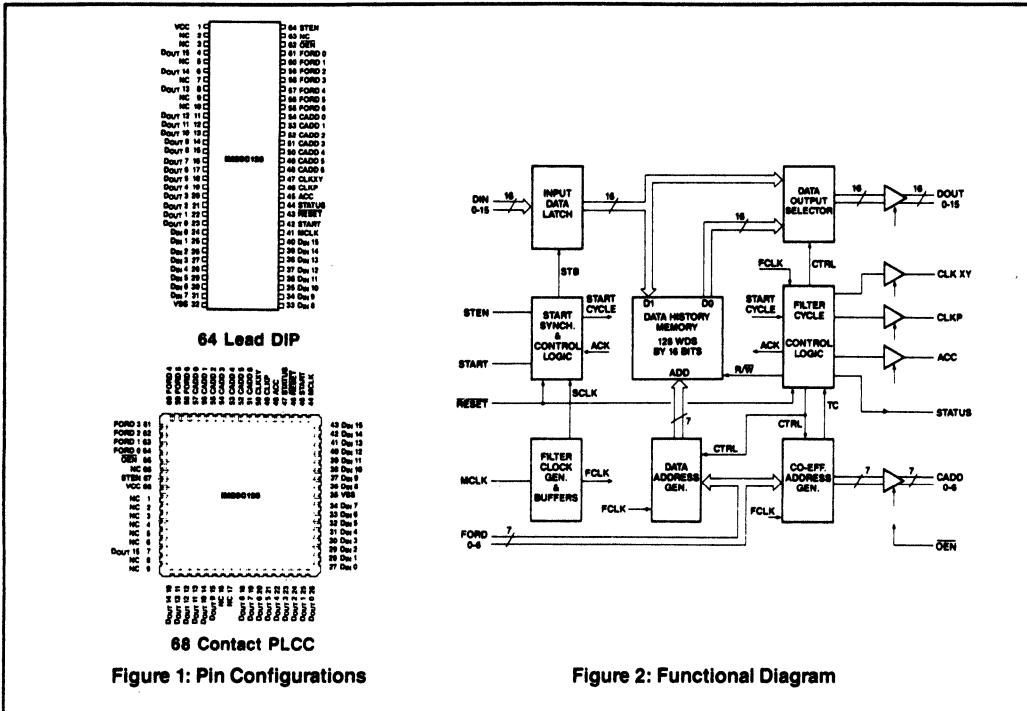
The 16 bit FIR Filter Controller (FFC) provides all the data history, storage and programmable filter cycle control logic required to implement FIR filters of up to 128 filter points. When used in conjunction with an external filter coefficient memory, of up to 128 words by 16 bits, and an industry standard 16 bit Multiplier-Accumulator (MAC), the FFC provides the system designer with the ability to implement a powerful FIR filter with only three ICs. The FFC provides all the control signals required to operate the MAC and the coefficient memory as tri-stateable devices, allowing multiplexed usage of these resources. The FFC's asynchronous interface enables easy integration of the FIR filter in any system environment. It incorporates a 16 bit data I/O path, a 128 word by 16 bit RAM memory, and programmable filter control logic capable of handling filter order lengths of up to 128 points.

FEATURES

- FIR Filter Building Block
- Filter Orders from 1 to 128 Points
- 128 Words by 16 Bit Data Memory
- Works with IM29C510 Multiplier-Accumulator (MAC) or Equivalent
- 80ns Minimum Filter Cycle Period with 25 MHz Master Clock Input
- Low Power CMOS Technology
- Full TTL Compatibility
- 68 Pin PLCC and 64 Pin DIP

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IM29C128CD64	0°C to +70°C	DIP
IM29C128MD64	-55°C to +125°C	DIP
IM29C128CN68	0°C to +70°C	PLCC



0106-1

12

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601100-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD}) -0.5 to +7 Volts
 Input/Output Voltage (V_{IN}/V_{OUT}) -0.3 to V_{DD} +0.3 Volts
 Storage Temperature (T_{STG}) -65 to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ MIL, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ IND, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ IND

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V_{IL}	Low Level Input Voltage			0.8	V	$V_{OUT} = 4.5$ $I_{OH} = 0$
V_{IH}	High Level Input Voltage MCLK Only	2 3				$V_{OUT} = 0.5$ $I_{OH} = 0$
V_{OL}	Low Level Output Voltage		0.15	0.4		$V_{IN} = V_{DD}$ $I_{OL} = 3.2\text{mA}$ $I_{OL} = 4.0\text{mA}$
V_{OH}	High Level Output Voltage	3.0	4.7			
I_{IL}, I_{IH}	Input Leakage Current	-1		+1	μA	$V_{IN} = 0$ or V_{DD}
I_{OZ}	3 State Output Leakage Current	-1		+1	μA	$V_{OUT} = 0$ or V_{DD}
I_{DD}	Operating Current		40	50	mA	$M_{CLK} = 25\text{MHz}$

See "Note", Paragraph 5.8.1 Timing Reference Inputs when they switch, either V_{IL} or V_{IH} Outputs 1.5V.

AC CHARACTERISTICS (See Figure 4)

Note: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ Mil., $V_{IH\text{MIN}} = 2.4\text{V}$, $V_{IH\text{MIN}}\text{CLK} = 3.5\text{V}$, $T_A = +40^\circ\text{C}$ to $+85^\circ\text{C}$ Ind., $V_{IL\text{MAX}} = 0.4\text{V}$, $V_{IL\text{MAX}}\text{CLK} = 0.4\text{V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ Com., $V_{CC} = 5.0\text{V} \pm 10\%$, Output Load Cap = 50 pF Max.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
T_{CLK}	Master Clock (MCLK) Cycle Period	40			ns
T_{CH}	MCLK High Period	20	15		$T_{CLK} - 20$ ns
T_{CL}	MCLK Low Period	20	15		$T_{CLK} - 20$ ns
T_{FLH}	FCLK High from MCLK		9		ns
T_{FHL}	FCLK Low from MCLK		9		ns
T_{ENS}	STEN Set-Up Time Before Start	10	2.5 - 5.0		ns
T_{ENH}	STEN Hold Time After Start	100%			T_{CLK}
T_{STH}	Start Hold Time	100%			T_{CLK}
T_{DIS}	Data Input (DIN) Set-Up Time Before Start	-5	-10		ns
T_{DIH}	Data Input Hold Time After Start	100%			T_{CLK}
T_{SSH}	Status High from Start (MCLK High)		27	40	ns
T_{SMH}	Status High from MCLK (Start High)		32	50	ns
T_{SHL}	Status Low from MCLK (End of Cycle)		32	50	ns
T_{ON}	$\overline{\text{OEN}}$ Low to DOUT and CADD Outputs Active (On)		15	30	ns
T_{OFF}	$\overline{\text{OEN}}$ High to DOUT and CADD Outputs Off (Hi-Z)		25	35	ns
T_{CON}	$\overline{\text{OEN}}$ Low to CLKXY, CLKP and ACC Outputs Active		15	25	ns
T_{COFF}	$\overline{\text{OEN}}$ High to CLKXY, CLKP and ACC Outputs Off (Hi-Z)		25	35	ns
T_{LDA}	MCLK to Data Out (DOUT) Valid: Latched Data In Selected (Cycle 1 Only)		60	80	ns
T_{RDA}	MCLK to DOUT Valid: RAM Data Selected		60	80	ns
T_{CAD}	MCLK to CADD 0-6 Address Valid		35	50	ns
T_{XHL}, T_{PHL}	MCLK to Clock-XY or CLKP Low		28	40	ns
T_{XHL}, T_{PLH}	MCLK to Clock-XY or CLKP High		28	40	ns
T_{AHL}	MCLK to Acc High		38	50	ns
T_{ALH}	MCLK to Acc Low		38	50	ns
T_{RST}	RESET Active Low Time		200%		T_{CLK}
T_{LD}	MCLK to CADD or DADD Loaded to FORD Value During Reset		35	50	ns

0106-2

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Data samples are input to the FFC via a 16 bit data port (DIN0-15), and are internally latched following the rising edge of a valid START command signal. The occurrence of a valid START command also causes the control logic to execute a computational cycle for the selected filter order length (1 to 128) determined by the Filter Order control inputs (FORD 0-6). The timing for each of the filter point sub-cycles, is controlled by the master clock input (MCLK), which operates at twice the desired Filter clock (FCLK) frequency.

Each computational cycle begins at the first rising edge of FCLK following a valid START command. During the first filter point cycle, the new input data is stored in the FFC data RAM at the address corresponding to the current sample time period (Dn). The data value is also output to the Multiplier-Accumulator (MAC) via a 16 bit Tri-state output port (DOUT 0-15). The 7 bit address corresponding to the first filter coefficient value (C0) is simultaneously output to the coefficient memory via a tri-state output port (CADD 0-6). During the second half of this FCLK period (i.e., LOW), the FFC outputs a control signal to the MAC (CLKXY), which is used to latch both the sample data from the FFC and the coefficient data from the coefficient memory.

At the next rising edge of FCLK, both of the address counters within the FFC are incremented. The RAM data value corresponding to the previous sample time period (Dn-1) is then fetched and output to the MAC via the data output port. The address for the sec-

ond coefficient value (C1) is output to the coefficient memory via the coefficient address output port. During this entire FCLK period, the FFC outputs a LOW value on the ACC control signal to the MAC which shall prepare it to store the product of the previous data and coefficient values. During the LOW period of FCLK, the FFC outputs both the CLKXY signal and a second signal, CLKP, which is used by the MAC to store the results of the previous multiplication. At the end of this FCLK period, ACC returns HIGH until the next computational cycle.

For each of the subsequent filter point sub-cycles, the FFC outputs the appropriate sample data and coefficient address following the rising edge of FCLK, and outputs both CLKXY and CLKP during the LOW period of the FCLK. This shall continue until the programmed number of filter point subcycles (filter order) has been executed.

During the FCLK period following the last filter point sub-cycle, a final CLKP signal is output to the MAC to cause it to store the results of the last filter point subcycle. The coefficient address counter is then reset to its initial value in preparation for the next computational cycle, at the next data sample input time. The RAM address counter however remains at its last value, which corresponds to the most ancient data sample in memory. At the next computational cycle, the new sample data shall replace the old data at this location and become the "current" data value (Dn). The sample data value input during this last cycle shall then be regarded as the "previous data sample" (i.e. Dn-1).

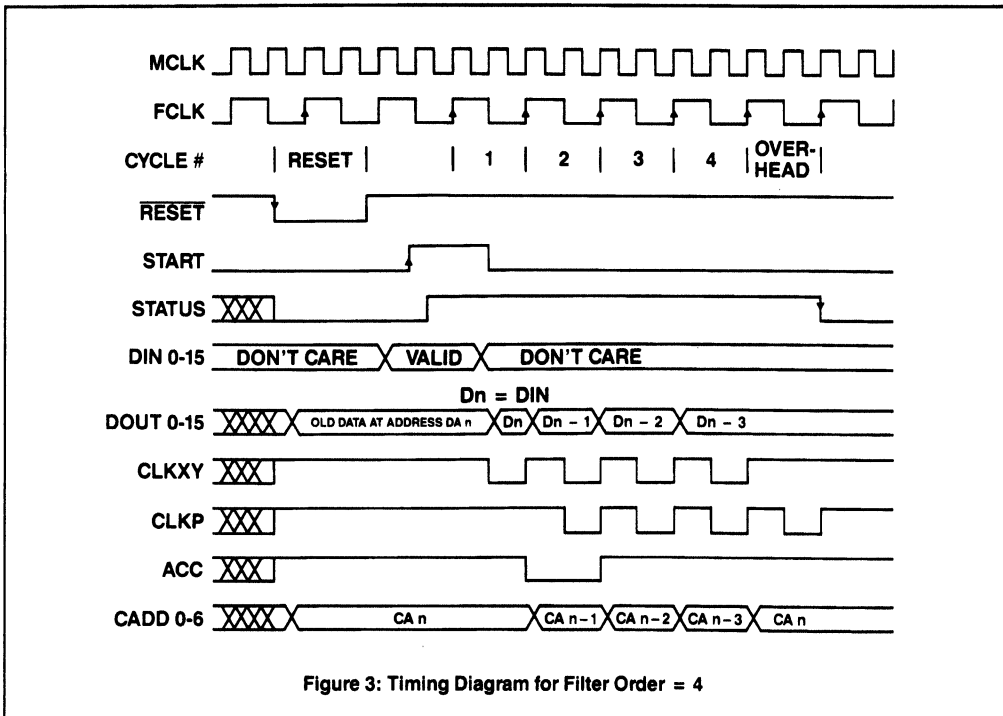


Figure 3: Timing Diagram for Filter Order = 4

0106-3

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NOTE: All typical values have been characterized but are not tested.

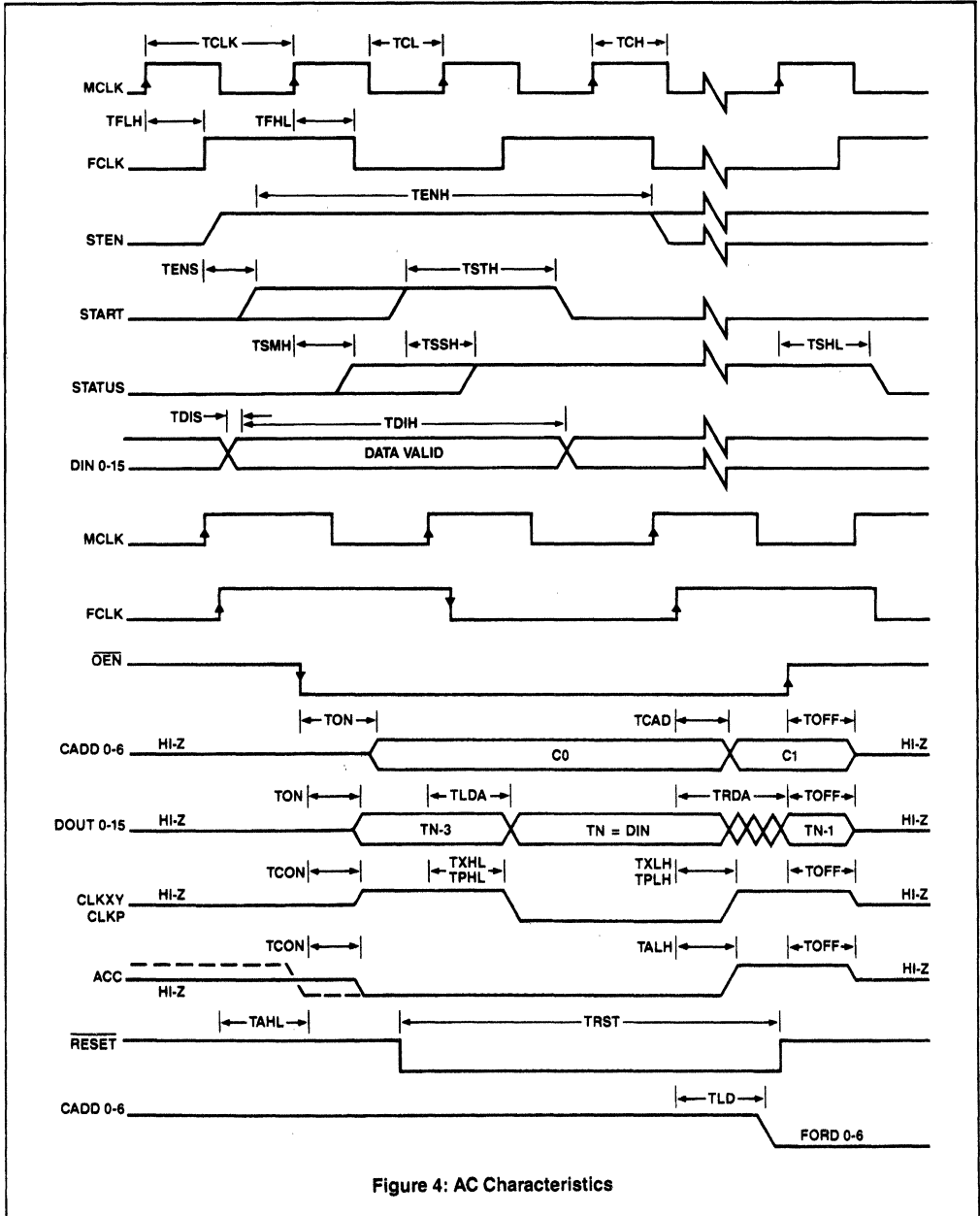
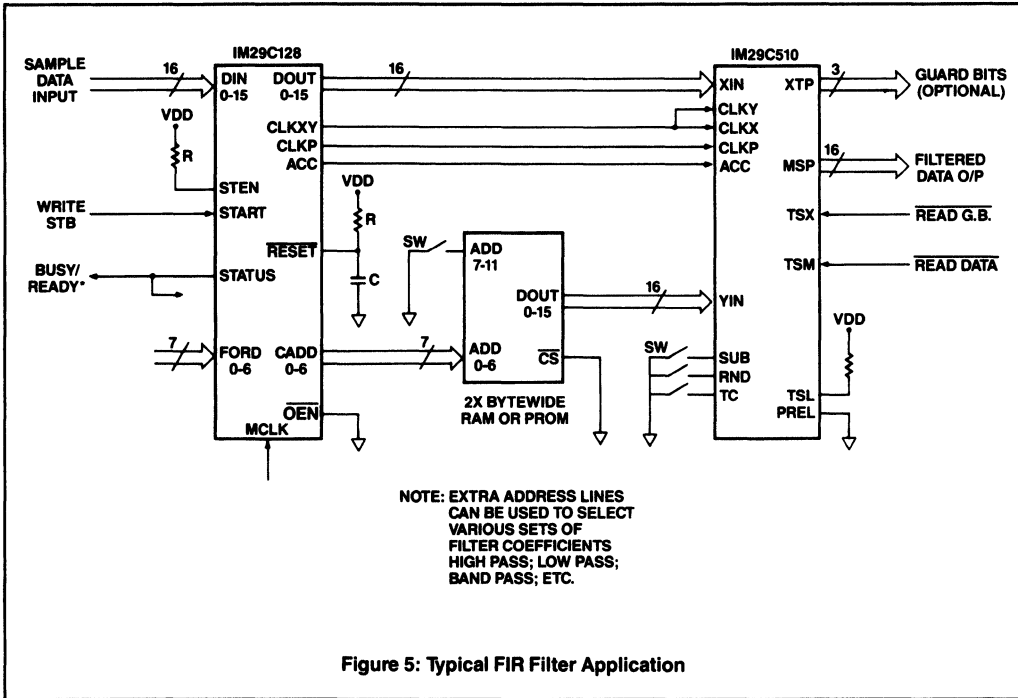


Figure 4: AC Characteristics

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NOTE: All typical values have been characterized but are not tested.



PIN DESCRIPTIONS

PIN #		NAME	DESCRIPTION
68 PLCC	64 DIP		
1	—	NC	
2	—	NC	
3	—	NC	
4	—	NC	
5	—	NC	
6	—	NC	
7	4	DOUT 15	16 bit non-inverting tri-state Data output. During the first period of the Filter control cycle, the data output value shall be the same as the input data value present at the rising edge of the START command. During subsequent periods of the control cycle, the data output values shall be those fetched from the data history RAM, beginning with the most recent "previous" sample. The Data output port shall be enabled whenever \overline{OEN} is LOW. DOUT 15 is the MSB.
8	—	NC	
9	—	NC	
10	6	DOUT 14	See DOUT 15.
11	8	DOUT 13	See DOUT 15.
12	11	DOUT 12	See DOUT 15.
13	12	DOUT 11	See DOUT 15.
14	13	DOUT 10	See DOUT 15.
15	14	DOUT 9	See DOUT 15.
16	—	NC	
17	—	NC	
18	15	DOUT 8	See DOUT 15.
19	16	DOUT 7	See DOUT 15.
20	17	DOUT 6	See DOUT 15.

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NOTE: All typical values have been characterized but are not tested.

PIN #		NAME	DESCRIPTION
68 PLCC	64 DIP		
21	18	DOUT 5	See DOUT 15.
22	19	DOUT 4	See DOUT 15.
23	20	DOUT 3	See DOUT 15.
24	21	DOUT 2	See DOUT 15.
25	22	DOUT 1	See DOUT 15.
26	23	DOUT 0	See DOUT 15. LSB
27	24	DIN 0	16 bit data input. Internally latched upon valid START command.
28	25	DIN 1	See DIN 0.
29	26	DIN 2	See DIN 0.
30	27	DIN 3	See DIN 0.
31	28	DIN 4	See DIN 0.
32	29	DIN 5	See DIN 0.
33	30	DIN 6	See DIN 0.
34	31	DIN 7	See DIN 0.
35	32	VSS	Ground
36	33	DIN 8	See DIN 0.
37	34	DIN 9	See DIN 0.
38	35	DIN 10	See DIN 0.
39	36	DIN 11	See DIN 0.
40	37	DIN 12	See DIN 0.
41	38	DIN 13	See DIN 0.
42	39	DIN 14	See DIN 0.
43	40	DIN 15	See DIN 0.
44	41	MCLK	Master Clock
45	42	START	Asynchronous Start control input. Initiates filter control cycle upon rising edge. Valid only if STEN is HIGH, and STATUS is LOW. Start is internally synchronized to the Filter Clock (FCLK), allowing for full asynchronous operation of the FFC with respect to the external Host or controller.
46	43	RESET	Active LOW Reset control input. Forces cycle control logic to standby mode, ready for valid START command. Forces both memory address counters to load the selected Filter Order value. Must be held LOW for at least two full periods of MCLK.
47	44	STATUS	Active HIGH FFC Status output. Output set to HIGH upon reception of valid START command and reset to LOW at end of Filter control cycle. Falling edge of STATUS may be used by HOST TO latch valid result from MAC, and to initiate subsequent cycle.
48	45	ACC	Tri-state control output to Product register of MAC. LOW value forces MAC to load the multiplier product into the Product register. HIGH value forces MAC to load output of the accumulator into the Product register. ACC shall be enabled whenever OEN is LOW.
49	46	CLKP	Tri-state control clock to Product register of MAC. Rising edge of CLKP used to latch product of multiplier or accumulator (as determined by ACC) into Product register. CLKP shall be enabled when OEN is LOW.
50	47	CLKXY	Tri-state control clock output to X and Y registers of MAC. Rising edge of CLKXY used by MAC to latch data from FFC into X register and data from Coefficient memory into Y register. CLKXY output shall be enabled whenever OEN is LOW.
51	48	CADD 6	7 bit tri-state Coefficient Address output. During the Filter control cycle, the Coefficient Address begins at the selected Filter Order value and then counts down to zero. The Coefficient memory must therefore be organized such that the coefficient values C0, C1, C2, etc. shall be located at memory address N, N-1, N-2, etc. respectively. The Address output port shall be enabled whenever OEN is LOW.
52	49	CADD 5	See CADD 6.
53	50	CADD 4	See CADD 6.
54	51	CADD 3	See CADD 6.
55	52	CADD 2	See CADD 6.
56	53	CADD 1	See CADD 6.
57	54	CADD 0	See CADD 6.
58	55	FORD 6	7 Bit active HIGH Filter Order control inputs. Input value of magnitude N will result in execution of Filter Length of N + 1. Allows programmable selection of Filter lengths of 1 to 128 points. MSB
59	56	FORD 5	See FORD 6.
60	57	FORD 4	See FORD 6.
61	58	FORD 3	See FORD 6.
62	59	FORD 2	See FORD 6.
63	60	FORD 1	See FORD 6.
64	61	FORD 0	See FORD 6. LSB
65	62	OEN	Active LOW Output Enable control signal. Disables all outputs except STATUS when HIGH.
66	—	NC	
67	64	STEN	Active HIGH Start Enable control. Enables START command input when HIGH.
68	1	VCC	+5 Volts.

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NOTE: All typical values have been characterized but are not tested.

IM29C510

CMOS 16 x 16 Bit, 65 ns (Commercial) 75 ns (Military) Multiplier/Accumulator



IM29C510

GENERAL DESCRIPTION

The IM29C510 is a high-speed 16 x 16 Bit Parallel Multiplier/Accumulator which operates at a 65 ns clock rate (more than 15 MHz Multiply/Accumulate rate). The 2 input registers, x and y, accept 16 bit twos complement or unsigned magnitude operands and produce a 32 bit product, with accumulation up to 35 bits.

To simplify bus interfacing and maximize system throughput, product outputs, x-inputs and y-inputs are individually and independently clocked. The Least Significant Product (the LSP) is multiplexed with the y-inputs, Most Significant Product (MSP), and Extended Product (XTP) are independently tri-stateable. These registers are positive edge-triggered D-type flip-flops.

Individual three-state output ports for the XTP and the MSP are provided. Preloading during tri-state is accomplished through the tri-stated output pins for the MSP and EXP, and through the y-input pins for the LSP. Operation of the Accumulator is controlled by the signals ACC (Accumulate), SUB (Subtract), and PREL (Preload).

The IM29C510 16 x 16 Bit Multiplier/Accumulator is pin and function compatible with the industry standard TDC1010. Depending on the multiply-accumulate rate, the device operates with the same speed at one-sixth or less power dissipation than the bipolar versions. (Worst Case CMOS power consumption decreases with decreasing clock rate).

The IM29C510 can operate as a 16 x 16 Bit Multiplier only as well as a 16 x 16 Bit Multiplier/Accumulator.

APPLICATIONS

- Radar/Sonar Signal Processors
- Array Processors
- Video Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Image Processors
- FIR Filters

FEATURES

- Low Power CMOS
- 65 ns Multiply/Accumulate Time
- 16 x 16 Bit Parallel Multiplication with Accumulation to 35 Bits
- Selectable Accumulate, Subtract, Round, and Preload of Accumulator
- Fully TTL Compatible I/O
- Three-State Outputs
- Two's Complement or Unsigned Magnitude Arithmetic
- 64 Lead DIP, 68 Pin PLCC
- Pin Compatible with Industry Standard MACs
- Full Mil Screening Available

ORDERING INFORMATION

Part Number	Clock Speed	Temperature Range	Package
Commercial: IM29C510CP68-65 IM29C510CP64-65	65 ns	0° to +70°C 0° to +70°C	68 Lead PLCC 64 Pin DIP
Industrial: IM29C510ID64-70	70 ns	-40° to +85°C	64 Pin DIP, Ceramic
Military: IM29C510MD64-75	75 ns	-55°C to +125°C	64 Pin DIP, Ceramic

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NOTE: All typical values have been characterized but are not tested.

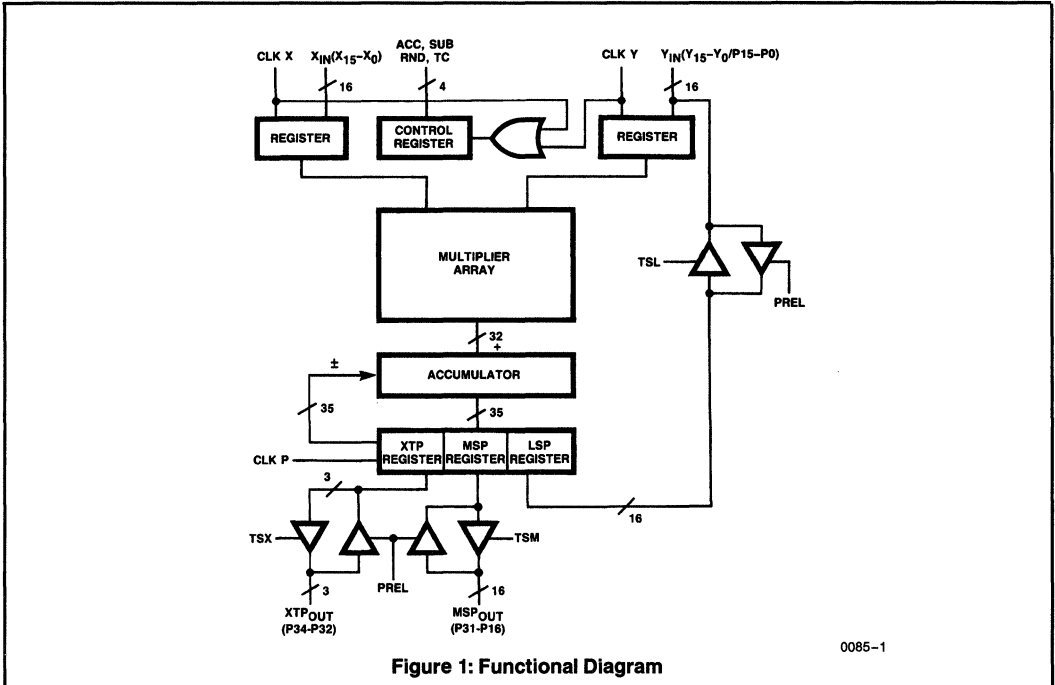
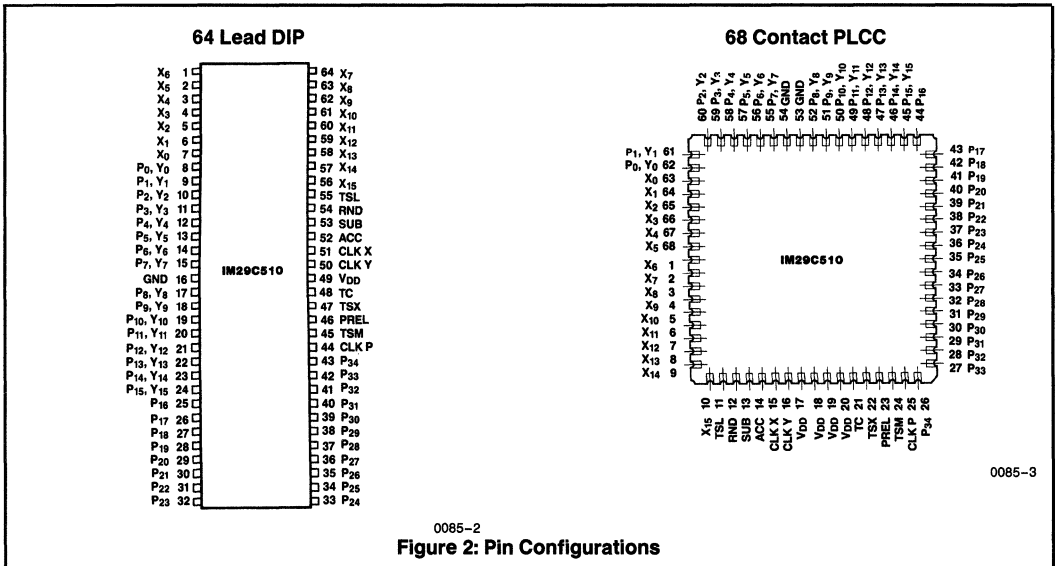


Figure 1: Functional Diagram



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

beyond which the device will be damaged

Supply Voltage	0V to + 7.0V
Input Voltage	-0.3V to (V _{DD} + 0.3V)
Output	
Applied Voltage	-0.3V to (V _{DD} + 0.3V)
Short-circuit duration	
(single output in high state to ground)	1 sec
Temperature	
Operating, Case	-60°C to + 130°C
Junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	-65°C to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS within specified operating conditions

Symbol	Parameter	Test Conditions	Temperature Range						Units
			Commercial		Industrial		Military		
			Min	Max	Min	Max	Min	Max	
I _{DDQ}	Supply Current, Quiescent	V _{DD} = Max, V _{IN} = 0V TSL, TSM, TSX = 5.0V		5		10		10	mA
I _{DDU}	Supply Current Unloaded (Note 1)	V _{DD} = Max, F = Clock Cycle Time TSL, TSM, TSX = 5.0V		120		130		130	mA
I _{IL}	Input Current, Logic LOW	V _{DD} = Max, V _I = 0.4V X _{IN} Controls, Clocks Y _{IN}	-75 -75	+75 +75	-75 -75	+75 +75	-75 -75	+75 +75	μA μA
I _{IH}	Input Current, Logic HIGH	V _{DD} = Max, V _I = 2.4V X _{IN} Controls, Clocks Y _{IN}	-75 -75	+75 +75	-75 -75	+75 +75	-75 -75	+75 +75	μA μA
I _I	Input Current, Max Input Voltage	V _{DD} = Max, V _I = V _{DD}		+75		+75		+75	μA
V _{OL}	Output Voltage, Logic LOW	V _{DD} = Min, I _{OL} = Max		0.4		0.4		0.4	V
V _{OH}	Output Voltage, Logic HIGH	V _{DD} = Min, I _{OH} = Max	2.4		2.4		2.4		V
I _{OZL}	Hi-Z Output Leakage Current Output LOW	V _{DD} = Max, V _I = 0.4V	-75	+75	-75	+75	-75	+75	μA
I _{OZH}	Hi-Z Output Leakage Current Output HIGH	V _{DD} = Max, V _I = 2.4V	-75	+75	-75	+75	-75	+75	μA
I _{OS}	Short-Circuit Output Current	V _{DD} = Max, Output HIGH, One Pin to Ground One Second Duration Max		-100		-100		-100	mA
C _I	Input Capacitance (Note 3)	T _A = 25°C, F = 1 MHz		15		15		15	pF
C _O	Output Capacitance (Note 3)	T _A = 25°C, F = 1 MHz		15		15		15	pF

NOTE 1: Guaranteed to maximum clock rate.

2: Worst case, all inputs and outputs toggling at maximum rate.

3: Sampled and not 100% tested.

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NOTE: All typical values have been characterized but are not tested.

SWITCHING CHARACTERISTICS within specified operating conditions (Note 1)

Symbol	Parameter	Test Conditions	Temperature Range						Units
			Commercial		Industrial		Military		
			Min	Max	Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	$V_{DD} = \text{Min}$		65		70		75	ns
t_D	Output Delay	$V_{DD} = \text{Min}$, Test Load: $V_{LOAD} = 2.2V$		35		35		40	ns
t_{ENA}	Three-State Output Enable Delay	$V_{DD} = \text{Min}$, Test Load: $V_{LOAD} = 1.5V$		35		35		40	ns
t_{DIS}	Three-State Output Disable Delay	$V_{DD} = \text{Min}$, Test Load: $V_{LOAD} = 2.6V$ for $T_{DIS0} 0.0V$ for t_{DIS1} (Note 2)		35		35		40	ns

NOTE 1: All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA} which are shown in Figure 5.

- 2: t_{DIS1} denotes the transition from logical 1 to three-state
 t_{DIS0} denotes the transition from logical 0 to three-state
 Transition is measured ± 500 mV from steady state voltage.

DC CHARACTERISTICS over operating range unless otherwise specified

Symbol	Description	Conditions	Min	Max	Units
V_{IH}	Input High Level		2.0		V
V_{IL}	Input Low Level			0.8	V
V_{OH}	Output High Level	$V_{CC} = \text{Min}$, $I_{OH} = -0.4$ mA	2.4		V
V_{OL}	Output Low Level	$V_{CC} = \text{Max}$, $I_{OL} = 4.0$ mA		0.4	V
I_{IH}	Input High Current	$V_{CC} = \text{Max}$		75	μA
I_{IL}	Input Low Current	$V_{CC} = \text{Max}$		75	μA

AC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4)

Symbol	Description	Commercial		Industrial		Military		Units
		Min	Max	Min	Max	Min	Max	
t_{MA}	Multiply/Accumulate Time		65		70		75	ns
t_D	Output Delay		35		40		40	ns
t_{ENA}	Three-State Output Enable Delay	35		35		40		ns
t_{DIS}	Three-State Output Disable Delay	35		35		40		ns
t_{PWL}	Clock Pulse Width (LOW)	25		25		30		ns
t_{PWH}	Clock Pulse Width (HIGH)	25		25		30		ns
t_S	Input Setup Time (Data, ACC, SUB, RND, TC)	25		25		30		ns
t_H	Input Hold Time (Data, SUB, RND, TC)	3		3		3		ns
t_S	Input Setup Time (PREL, TSX, TSM, TSL)	25		25		30		ns
t_H	Input Hold Time (PREL, TSX, TSM, TSL)	3		3		3		ns

NOTE 3: All transitions are measured at 1.5V.

4: $V_{IH} = 2.4V$ and $V_{IL} = 0.4V$.

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NOTE: All typical values have been characterized but are not tested.

OPERATION

A set of control words supplied by the CPU programs the functional operation of the IM29C510 16 x 16 Bit Multiplier/Accumulator. These control words include the signals ACC (Accumulate), PREL (Preload), and SUB (Subtract).

OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Temperature Range									Units
			Commercial			Industrial		Military				
			Min	Nom	Max	Min	Max	Min	Nom	Max		
V _{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.5	4.5	5.0	5.5	V	
t _{PWL}	Clock Pulse Width, LOW		25			25		30			ns	
t _{PWH}	Clock Pulse Width, HIGH		25			25		30			ns	
t _S	Input Setup Time		25			25		30			ns	
t _H	Input Hold Time		3			3		3			ns	
V _{IL}	Input Voltage Logic LOW				0.8		0.8			0.8	V	
V _{IH}	Input Voltage, Logic HIGH		2.0			2.0		2.0			V	
I _{OL}	Output Current, Logic LOW				4.0		4.0			4.0	mA	
I _{OH}	Output Current, Logic HIGH				-0.4	-0.4				-0.4	mA	
T _A	Ambient Temperature, Still Air		0		70	-40	+85	-55		+125	°C	

OPERATING RANGES

Commercial Devices

Temperature T_A = 0°C to +70°C

Supply Voltage V_{CC} = +4.75V to 5.25V

Industrial Devices

Temperature T_A = -40°C to +85°C

Supply Voltage V_{CC} = +4.5V to 5.5V

Military Devices

Temperature T_C = -55°C to +125°C

Supply Voltage V_{CC} = +4.5V to 5.5V

POWER

The IM29C510 16 x 16 Bit Multiplier/Accumulator operates from a single +5V supply. All ground and power lines must be connected.

Name	Function	Value	DIP Package	PLCC Package
V _{DD}	Positive Supply Voltage	+5.0V	Pin 49	Pins 17, 18, 19, 20
GND	Ground	0.0V	Pin 16	Pins 53, 54

DATA INPUTS

The IM29C510 16 x 16 Bit Multiplier/Accumulator has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The sign information for the two's complement notation is carried by the Most Significant Bits (MSBs), X_{15} and Y_{15} . Bits remaining are designated X_{14} through X_0 and Y_{14} through Y_0 . The Least Significant Bits are X_0 and Y_0 .

When data are present at the X and Y inputs, they are clocked into the input registers at the rising edge of the appropriate clock. Table 3 shows the input and output formats for fractional two's complement notation, integer two's complement notation, fractional unsigned magnitude notation, and integer unsigned magnitude notation.

Table 1

Name	Function	DIP Package	PLCC Package
X_{15}	X Data MSB	Pin 56	Pin 10
X_{14}		Pin 57	Pin 9
X_{13}		Pin 58	Pin 8
X_{12}		Pin 59	Pin 7
X_{11}		Pin 60	Pin 6
X_{10}		Pin 61	Pin 5
X_9		Pin 62	Pin 4
X_8		Pin 63	Pin 3
X_7		Pin 64	Pin 2
X_6		Pin 1	Pin 1
X_5		Pin 2	Pin 68
X_4		Pin 3	Pin 67
X_3		Pin 4	Pin 66
X_2		Pin 5	Pin 65
X_1		Pin 6	Pin 64
X_0	X Data LSB	Pin 7	Pin 63
Y_{15}	Y Data MSB	Pin 24	Pin 45
Y_{14}		Pin 23	Pin 46
Y_{13}		Pin 22	Pin 47
Y_{12}		Pin 21	Pin 48
Y_{11}		Pin 20	Pin 49
Y_{10}		Pin 19	Pin 50
Y_9		Pin 18	Pin 51
Y_8		Pin 17	Pin 52
Y_7		Pin 15	Pin 55
Y_6		Pin 14	Pin 56
Y_5		Pin 13	Pin 57
Y_4		Pin 12	Pin 58
Y_3		Pin 11	Pin 59
Y_2		Pin 10	Pin 60
Y_1		Pin 9	Pin 61
Y_0	Y Data LSB	Pin 8	Pin 62

DATA OUTPUTS

The IM29C510 16 x 16 Bit Multiplier/Accumulator has a 35-bit two's complement or unsigned magnitude results that yields the sum of the products of the previous products which have been accumulated plus the two input data values. This output is expressed as two 16-bit output words: the Most Significant Product (MSP) and the Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). If two's complement notation is used, the Most Significant Bit (MSB) of the XTP is the sign bit.

Table 2

Name	Function	DIP Package	PLCC Package
P34	Product MSB	Pin 43	Pin 26
P33		Pin 42	Pin 27
P32		Pin 41	Pin 28
P31		Pin 40	Pin 29
P30		Pin 39	Pin 30
P29		Pin 38	Pin 31
P28		Pin 37	Pin 32
P27		Pin 36	Pin 33
P26		Pin 35	Pin 34
P25		Pin 34	Pin 35
P24		Pin 33	Pin 36
P23		Pin 32	Pin 37
P22		Pin 31	Pin 38
P21		Pin 30	Pin 39
P20		Pin 29	Pin 40
P19		Pin 28	Pin 41
P18		Pin 27	Pin 42
P17		Pin 26	Pin 43
P16		Pin 25	Pin 44
P15		Pin 24	Pin 45
P14		Pin 23	Pin 46
P13		Pin 22	Pin 47
P12		Pin 21	Pin 48
P11		Pin 20	Pin 49
P10		Pin 19	Pin 50
P9		Pin 18	Pin 51
P8		Pin 17	Pin 52
P7		Pin 15	Pin 55
P6		Pin 14	Pin 56
P5		Pin 13	Pin 57
P4		Pin 12	Pin 58
P3		Pin 11	Pin 59
P2		Pin 10	Pin 60
P1	Pin 9	Pin 61	
P0	Product LSB	Pin 8	Pin 62

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CLOCKS

The IM29C510 16 x 16 Bit Multiplier/Accumulator has an individual clock line for each of the input registers plus one for the product register, for a total of three clock lines. Data present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC) and SUBtract (SUB) inputs are registered with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. If normally HIGH clock signals are used, special attention to the clock signals is required. Loading problems with these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	DIP Package	PLCC Package
CLK X	Clock Input Data X	Pin 51	Pin 15
CLK Y	Clock Input Data Y	Pin 50	Pin 16
CLK P	Clock Product Register	Pin 44	Pin 25

CONTROLS

THE IM29C510 16 x 16 Bit Multiplier/Accumulator has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, and MSP, and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Preload Truth Table (Table 6)). First, all output buffers are forced into the high-impedance state. Second, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P when any or all of TSX, TSM, and TSL are also HIGH. Normal data setup and hold times apply to the logical AND of PREL as well as to the data being preloaded, and to the relevant three-state control (TSX, TSM, TSL). These setup and hold times are with respect to the rising edge of CLK P.

Addition of a "1" to the MSB of the LSP for rounding is controlled by the RouND (RND) controls. A "1" is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it, when RND is HIGH.

How the device interprets data on the X and Y inputs is controlled by the Two's Complement (TC) controls. TC HIGH make both inputs two's complement inputs. TC LOW makes both inputs magnitude only inputs.

The content of the output register is added to or subtracted from the next product generated when ACCumulate (ACC) is HIGH. Their sum is returned to the output registers at the next rising edge of clock P. Multiplication without accumulation is performed and the next product generated is stored into the output registers directly when ACC is LOW. To eliminate the need for a separate "clear" operation, this operation is used for the first term in a summation.

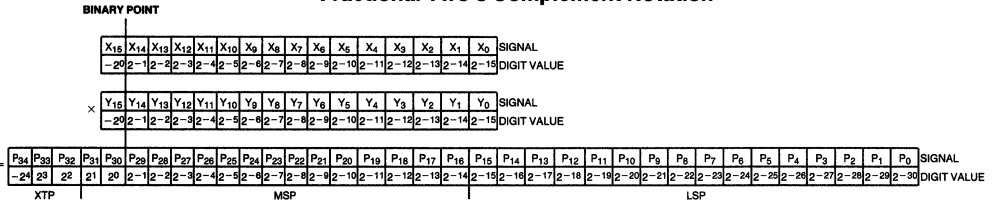
The SUBtract (SUB) control is used in conjunction with the ACC control. The content of the output register is subtracted from the next product generated and the difference is returned to the output register, when both the ACC and SUB controls are HIGH.

NOTE: The previous output is subtracted from the product, NOT the product from the previous output.

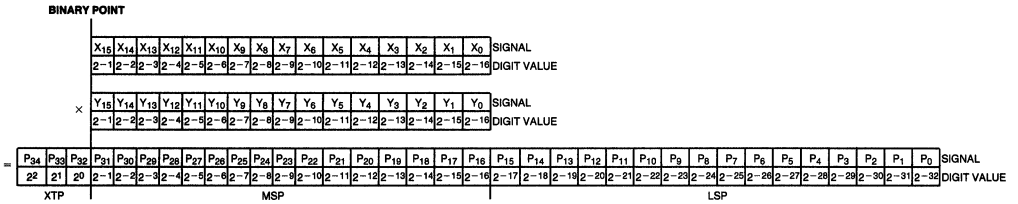
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NOTE: All typical values have been characterized but are not tested.

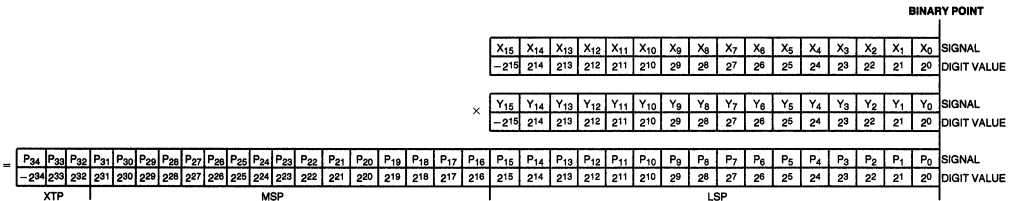
Table 3: Data Formats
Fractional Two's Complement Notation



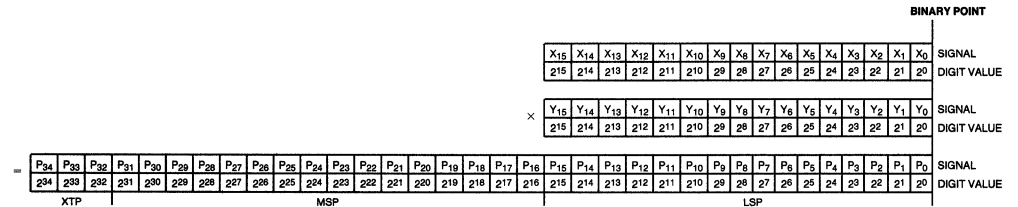
Fractional Unsigned Magnitude Notation



Integer Two's Complement Notation



Integer Unsigned Magnitude Notation



The RND, TC, ACC, and SUB inputs are registered with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. If normally HIGH clock signals are

used, special attention to the clock signal is required. Loading problems of these four control signals can be avoided by the use of normally LOW clocks.

Table 4

Name	Function	DIP Package	PLCC Package
TSX	XTP Three-State Control	Pin 47	Pin 22
TSM	MSP Three-State Control	Pin 45	Pin 24
TSL	LSP Three-State Control	Pin 55	Pin 11
PREL	Preload Control	Pin 46	Pin 23
RND	Round Control Bit	Pin 54	Pin 12
TC	Two's Complement Control	Pin 48	Pin 21
ACC	Accumulate Control	Pin 52	Pin 14
SUB	Subtract Control	Pin 53	Pin 13

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NOTE: All typical values have been characterized but are not tested.

Table 5: Pin Assignments

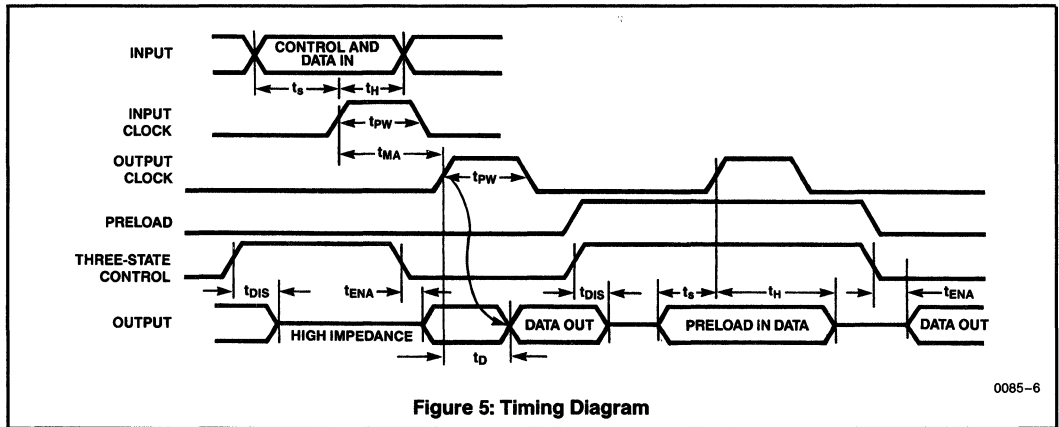
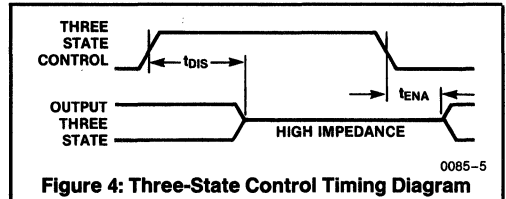
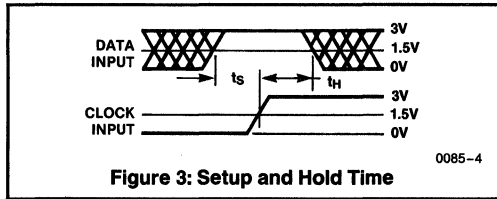
Pin Name	Function	Input/Output	DIP Package	PLCC Package
X ₆		I	Pin 1	Pin 1
X ₅		I	Pin 2	Pin 68
X ₄		I	Pin 3	Pin 67
X ₃		I	Pin 4	Pin 66
X ₂		I	Pin 5	Pin 65
X ₁		I	Pin 6	Pin 64
X ₀	X Input LSB	I	Pin 7	Pin 63
P ₀ -Y ₀	Product/Y Input LSB	I/O	Pin 8	Pin 62
P ₁ -Y ₁		I/O	Pin 9	Pin 61
P ₂ -Y ₂		I/O	Pin 10	Pin 60
P ₃ -Y ₃		I/O	Pin 11	Pin 59
P ₄ -Y ₄		I/O	Pin 12	Pin 58
P ₅ -Y ₅		I/O	Pin 13	Pin 57
P ₆ -Y ₆		I/O	Pin 14	Pin 56
P ₇ -Y ₇		I/O	Pin 15	Pin 55
GND		Ground	Pin 16	Pin 53, 54
P ₈ -Y ₈		I/O	Pin 17	Pin 52
P ₉ -Y ₉		I/O	Pin 18	Pin 51
P ₁₀ -Y ₁₀		I/O	Pin 19	Pin 50
P ₁₁ -Y ₁₁		I/O	Pin 20	Pin 49
P ₁₂ -Y ₁₂		I/O	Pin 21	Pin 48
P ₁₃ -Y ₁₃		I/O	Pin 22	Pin 47
P ₁₄ -Y ₁₄		I/O	Pin 23	Pin 46
P ₁₅ -Y ₁₅	Product/Y Input MSB	I/O	Pin 24	Pin 45
P ₁₆		O	Pin 25	Pin 44
P ₁₇		O	Pin 26	Pin 43
P ₁₈		O	Pin 27	Pin 42
P ₁₉		O	Pin 28	Pin 41
P ₂₀		O	Pin 29	Pin 40
P ₂₁		O	Pin 30	Pin 39
P ₂₂		O	Pin 31	Pin 38
P ₂₃		O	Pin 32	Pin 37
P ₂₄		O	Pin 33	Pin 36
P ₂₅		O	Pin 34	Pin 35
P ₂₆		O	Pin 35	Pin 34
P ₂₇		O	Pin 36	Pin 33
P ₂₈		O	Pin 37	Pin 32
P ₂₉		O	Pin 38	Pin 31
P ₃₀		O	Pin 39	Pin 30
P ₃₁		O	Pin 40	Pin 29
P ₃₂		O	Pin 41	Pin 28
P ₃₃		O	Pin 42	Pin 27
P ₃₄	Product MSB	O	Pin 43	Pin 26
CLKP	Clock Product Register	I	Pin 44	Pin 25
TSM	MSP Three-State Control	I	Pin 45	Pin 24
PREL	Preload Control	I	Pin 46	Pin 23
TSX	XTP Three-State Control	I	Pin 47	Pin 22
TC	Two's Complement Control	I	Pin 48	Pin 21
V _{DD}	Positive Supply Voltage	V _{DD}	Pin 49	Pin 17, 18, 19, 20

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NOTE: All typical values have been characterized but are not tested.

Table 5: Pin Assignments (Continued)

Pin Name	Function	Input/Output	DIP Package	PLCC Package
CLKY	Clock Input Data Y	I	Pin 50	Pin 16
CLKX	Clock Input Data X	I	Pin 51	Pin 15
ACC	Accumulate Control	I	Pin 52	Pin 14
SUB	Subtract Control	I	Pin 53	Pin 13
RND	Round Control Bit	I	Pin 54	Pin 12
TSL	LSP Three-State Control	I	Pin 55	Pin 11
X ₁₅	X Input MSB	I	Pin 56	Pin 10
X ₁₄		I	Pin 57	Pin 9
X ₁₃		I	Pin 58	Pin 8
X ₁₂		I	Pin 59	Pin 7
X ₁₁		I	Pin 60	Pin 6
X ₁₀		I	Pin 61	Pin 5
X ₉		I	Pin 62	Pin 4
X ₈		I	Pin 63	Pin 3
X ₇		I	Pin 64	Pin 2



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NOTE: All typical values have been characterized but are not tested.

Table 6: Preload Truth Table

PREL (Note 1)	TSX (Note 1)	TSM (Note 1)	TSL (Note 1)	XTP	MSP	LSP
L	L	L	L	Register → Output Pin	Register → Output Pin	Register → Output Pin
L	L	L	H	Register → Output Pin	Register → Output Pin	Hi Z
L	L	H	L	Register → Output Pin	Hi Z	Register → Output Pin
L	L	H	H	Register → Output Pin	Hi Z	Hi Z
L	H	L	L	Hi Z	Register → Output Pin	Register → Output Pin
L	H	L	H	Hi Z	Register → Output Pin	Hi Z
L	H	H	L	Hi Z	Hi Z	Register → Output Pin
L	H	H	H	Hi Z	Hi Z	Hi Z
H ²	L	L	L	Hi Z	Hi Z	Hi Z
H ²	L	L	H	Hi Z	Hi Z	Hi Z Preload
H ²	L	H	L	Hi Z	Hi Z Preload	Hi Z
H ²	L	H	H	Hi Z	Hi Z Preload	Hi Z Preload
H ²	H	L	L	Hi Z Preload	Hi Z	Hi Z
H ²	H	L	H	Hi Z Preload	Hi Z	Hi Z Preload
H ²	H	H	L	Hi Z Preload	Hi Z Preload	Hi Z
H ²	H	H	H	Hi Z Preload	Hi Z Preload	Hi Z Preload

NOTE 1: PREL, TSX, TSM, and TSL are not registered.

2: PREL HIGH inhibits any change of output register for those outputs in which the three-state control is LOW.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 6 and 7

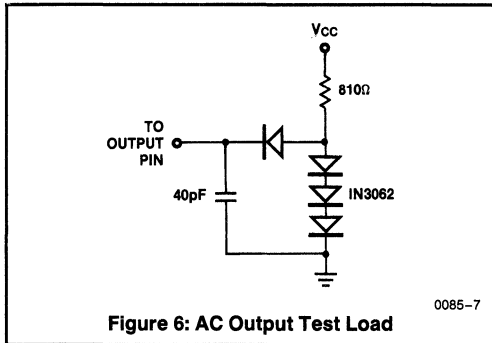


Figure 6: AC Output Test Load

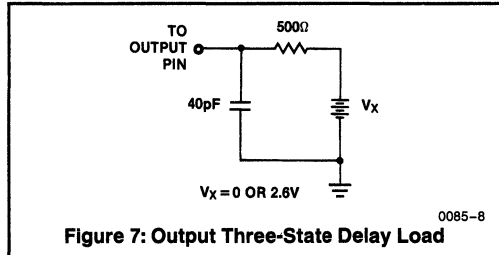
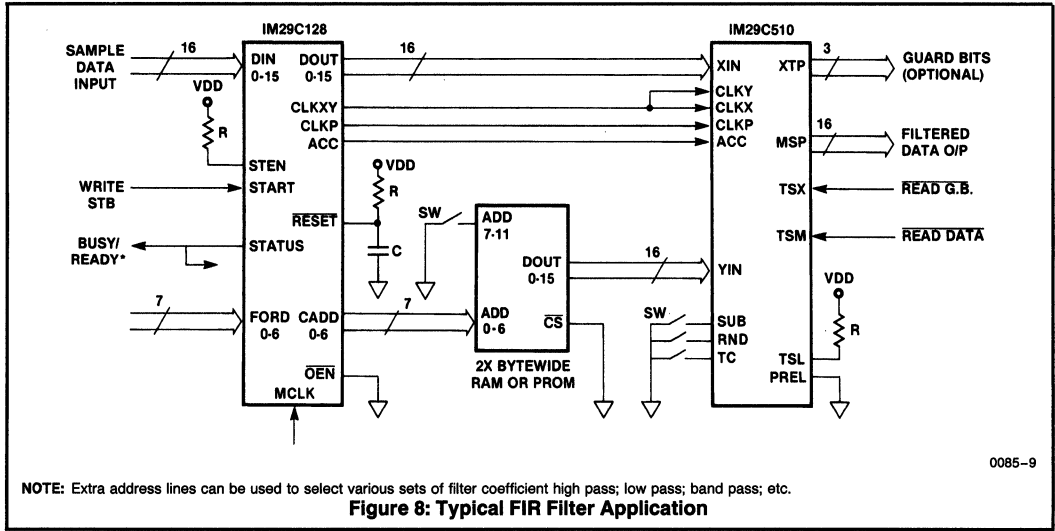


Figure 7: Output Three-State Delay Load

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

EVK-128

Data Conversion and FIR Filtering System



EVK-128

GENERAL DESCRIPTION

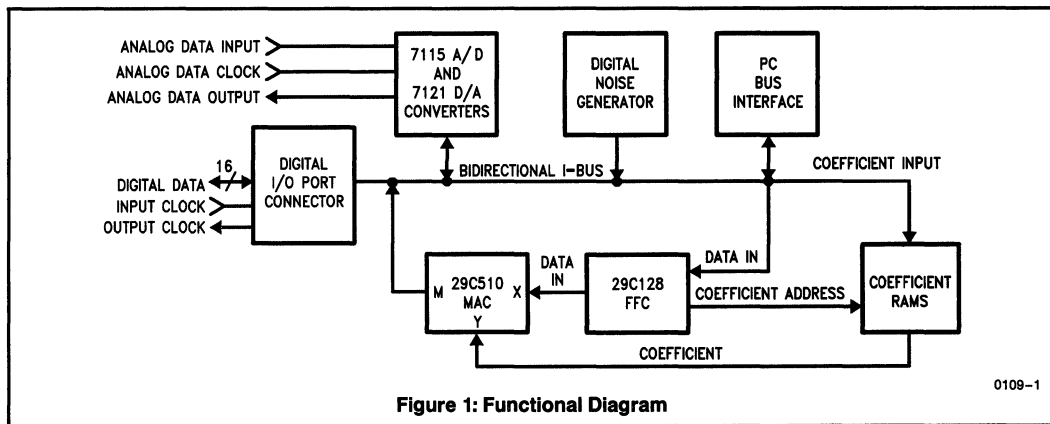
The Intersil EVK-128 provides a moderate speed data acquisition, conversion, and digital filtering system for the IBM PC and most compatibles. Consisting of a board which plugs into and occupies a single slot on the PC, the card digitally filters data with a filter length of 0 (unfiltered) to 128 taps, utilizing the Intersil IM29C128 Finite Impulse Response Filter Controller (FFC) and 29C510 16 bit Multiplier-Accumulator (MAC). Throughput is a function of required filter length, with an 80 nS per tap processing rate.

The ICL7115 converts analog signals to 14 bit words at up to 32.727 KHz rate, while the ICL7121 converts a 16 bit digital data stream to analog. Edge mounted connectors allow simple analog I/O. The A/D and/or D/A converters may be bypassed for processing of digital data, input or output via externally accessible edge mounted connectors or the PC bus. This also allows nonreal time processing or storage of data to or from a disk, for example.

Also included is a floppy disk with an easy-to-use menu driven FIR filter design program for the PC, including coefficient calculations, time and frequency calculations and plotting capabilities, and prompts for controlling the different modes of operation of the board. The package contains complete documentation, including detailed schematics, printed circuit layout, parts list, timing diagrams, and applications literature. The user may copy any of this for his own system design, if desired.

FEATURES

- Occupies Single IBM PC Slot
- On Board 14 Bit ICL7115 A/D Converter
- On Board 16 Bit ICL7121 D/A Converter
- All Necessary Software Provided
- Digital Filters of 1 to 128 Taps
- Versatile I/O Options
- On Board Digital Noise Generator
- Complete Documentation Package
- Fully Tested, Ready to Plug In and Use
- S/N > 84 dB



0109-1

12

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601120-002

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The EVK-128 is designed to be mapped into a 16-byte block of addresses in the I/O space of the PC. The base address is set by means of a DIP switch so as not to conflict with other boards. An expansion decoding scheme is used to map these 16 addresses into a 1K block. The first 512 locations are used to address the coefficient RAM, and the rest are available for control, test, and data transfer functions. The address translation from 16 to 1K is handled by the provided software.

There are two registers which determine the configuration of the board: the Filter Order Register (FOR), and the Mode Register (MR). Bits 0 to 6 of the FOR hold the filter order (number of taps). Bit 7 is used to give a software reset to the board. Bits 1 to 3 of the MR are used to select between the A/D, digital noise generator, or external digital inputs. This scheme gives the flexibility to mix analog and digital I/O. Bit 0 is used to enable the external digital output, and bit 4 is used to select between 1 of 2 possible banks of coefficient RAM memory. Table 1 shows the addresses for the various control functions.

The analog sample rate is set internally at 32.727 kHz. An external clock may be provided through the back connectors in lieu of the internal one, as long as the logic swing is between 0 to 5 volts. The external digital connection is via a

20-pin header and uses 16 bits of parallel data and a non-overlapping clock scheme to manage data over the bidirectional bus.

The control pattern for the sample/hold, A/D, and D/A is downloaded under software control from the PC, as is the seed value for the Digital Noise Generator (DNG). Since the DNG shift register is 20 bits long, the resulting sequence will exhibit a high degree of randomness.

Table 1: PC Address Map

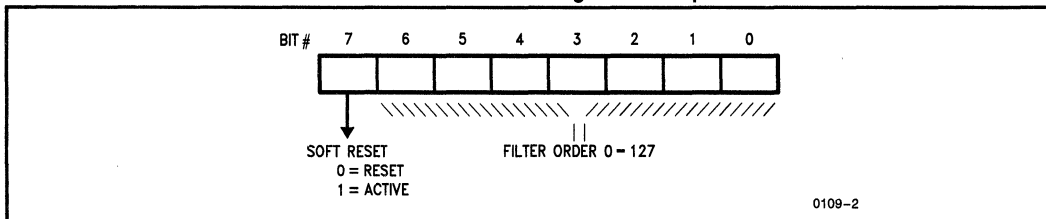
Relative Address	Description
000-1FE	Load Coefficient RAM
200, 201	Write Data Word to FFC
202, 203	Write Filter Order Register
204, 205	Read Data Word from MAC
206, 207	Read A/D into PC
206, 207	Write PC into D/A
208, 209	Write Mode Register
20A, 20B	Load Digital Noise Seed
20C, 20D	Read/Write A/D Control Pattern
20E	Start all Operations Except FFC
20F	Start all Operations Including FFC

Table 2: Mode Register Bit Map

Bit #	4	3	2	1	0
	FN	ADM	DNGM	DIM	DOM
	Filter Number A = 0, B = 1	A/D Output Enable Mask	Digital Noise Enable Mask	Digital Input Enable Mask	Digital Output Enable Mask

0 = Disable 1 = Enable

Table 3: Filter Order Register Bit Map



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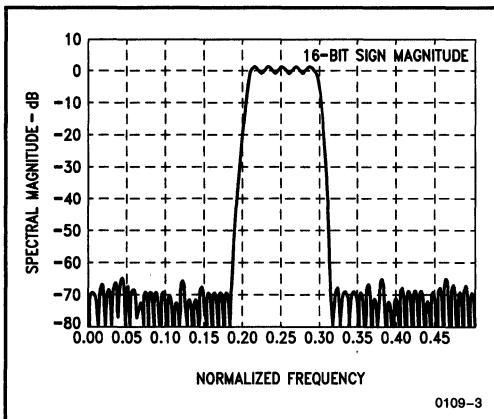
NOTE: All typical values have been characterized but are not tested.

Sample plot from filter design software. The plot itself is from the program run on a COMPAQ II and plotted on an OKIDATA 193, but most common dot matrix printers, like the EPSON, are supported.

**SPECIFICATIONS FOR A BANDPASS
EQUI RIPPLE
FIR FILTER OF LENGTH 125**

End of Lower Stopband (Hz)	19
Beginning of Passband (Hz)	21
End of Passband (Hz)	29
Beginning of Upper Stopband (Hz)	31
Maximum Passband Attenuation (dB)	0.6
Minimum Stopband Attenuation (dB)	72

Although the above plot shows the kind of response possible with less than 128 taps, longer filters can be implemented if non-realtime processing is allowed. Data could be stored on the computer (e.g., floppy or Winchester) and cycled through the filter board, processing up to 128 taps with each pass. Furthermore, data recorded offline somewhere else could be loaded and processed easily via the backplane. The board could also function as a powerful development tool, a pedagogical tool, or, more obviously, as a system for actual data conversion and filtering.



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NOTE: All typical values have been characterized but are not tested.

Section 13 — Display Drivers

ICM7211	13-1
ICM7212	13-1
ICM7218	13-12
ICM7228	13-23
ICM7231	13-36
ICM7232	13-36
ICM7233	13-36
ICM7243	13-55



ICM7211/12

4-Digit LCD/LED Display Driver



ICM7211/12

GENERAL DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled, low leakage, open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package and all inputs are fully protected against static discharge.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7211AMIJL	-40°C to +85°C	40 Pin Cerdip
ICM7211IPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AMIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211MIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7211AEV/KIT	—	EVALUATION KIT

ICM7211 (LCD) FEATURES

- Four Digit Non-Multiplexed 7 Segment LCD Display Outputs With Backplane Driver
- Complete Onboard RC Oscillator to Generate Backplane Frequency
- Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master
- ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible With Siliconix DF411)
- ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface
- ICM7211 Decodes Binary Hexadecimal; ICM7211A Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)

ICM7212 (LED) FEATURES

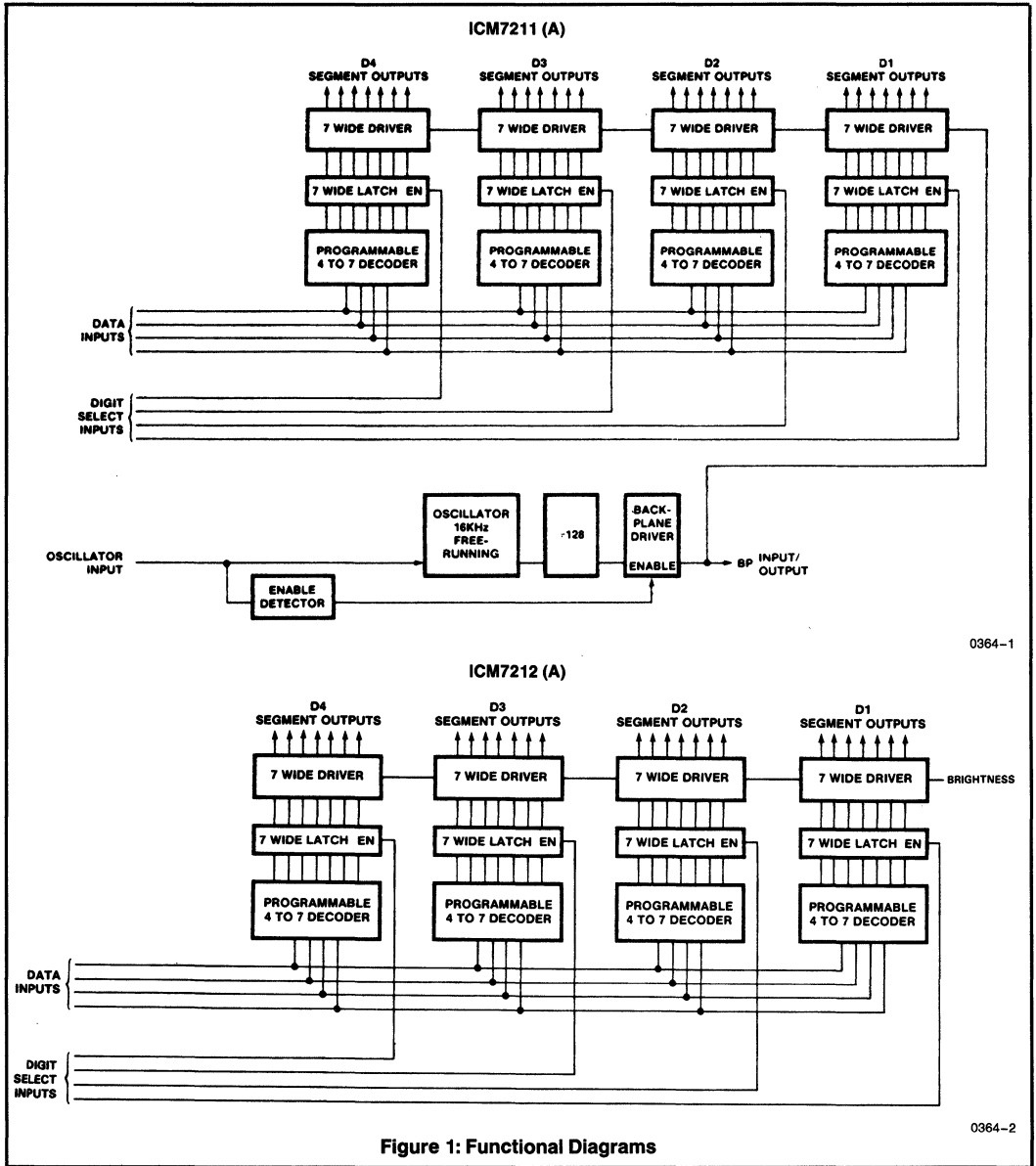
- 28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at > 5mA Per Segment
- Brightness Input Allows Direct Control of LED Segment Current With a Single Potentiometer or Digitally as a Display Enable
- ICM7212M and ICM7212A Devices Provide Same Input Configuration and Output Decoding Options as the ICM7211

Part Number	Temperature Range	Package
ICM7212AIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212IPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212MIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212AMIPL	-40°C to +85°C	40 Pin PLASTIC
ICM7212AEV/KIT	—	EVALUATION KIT

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NOTE: All typical values have been characterized but are not tested.



0364-1

0364-2

Figure 1: Functional Diagrams

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NOTE: All typical values have been characterized but are not tested.

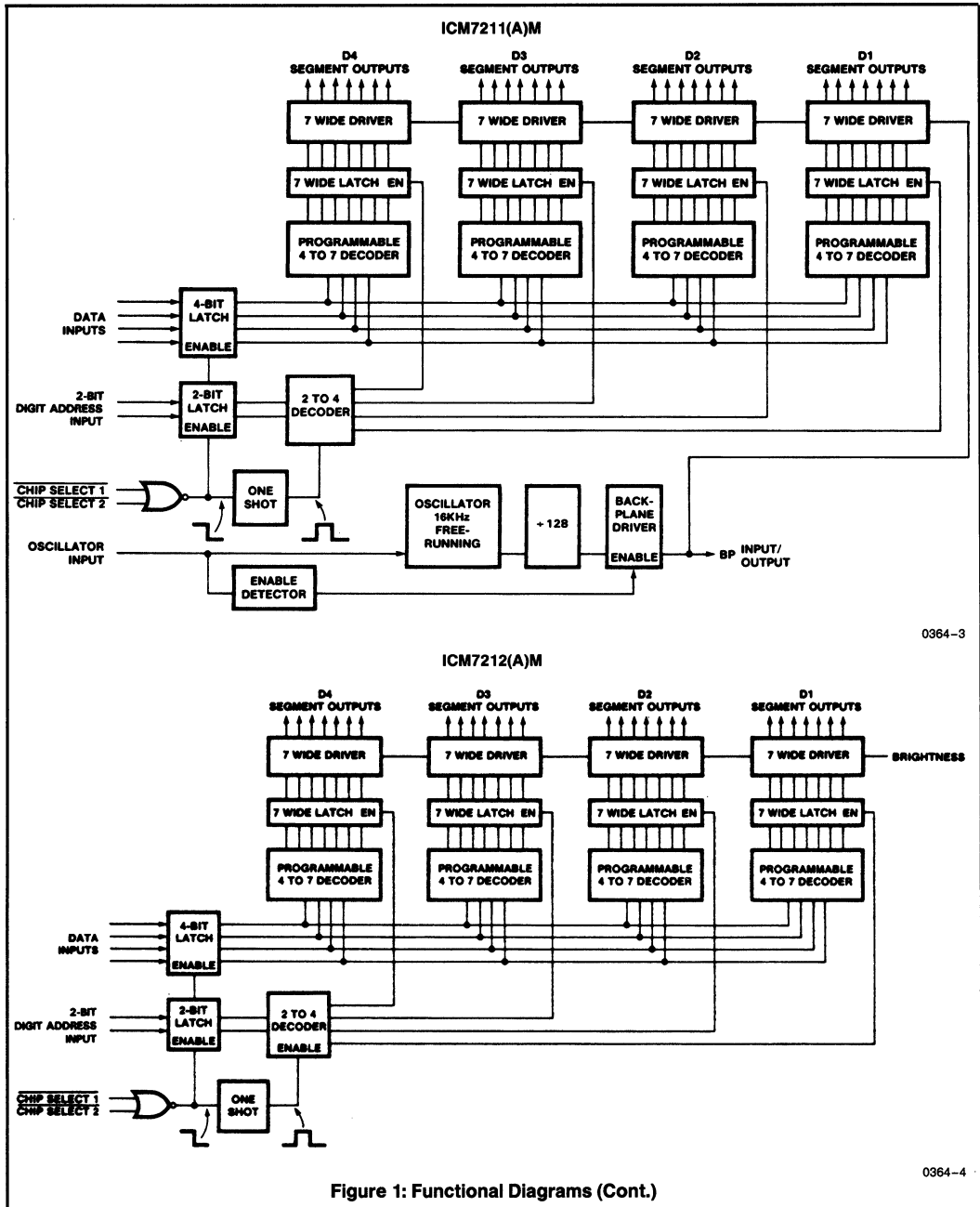


Figure 1: Functional Diagrams (Cont.)

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) 0.5W@70°C
 Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
 Input Voltage (Any Terminal) (Note 2)
 $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$

Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -55°C to +125°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

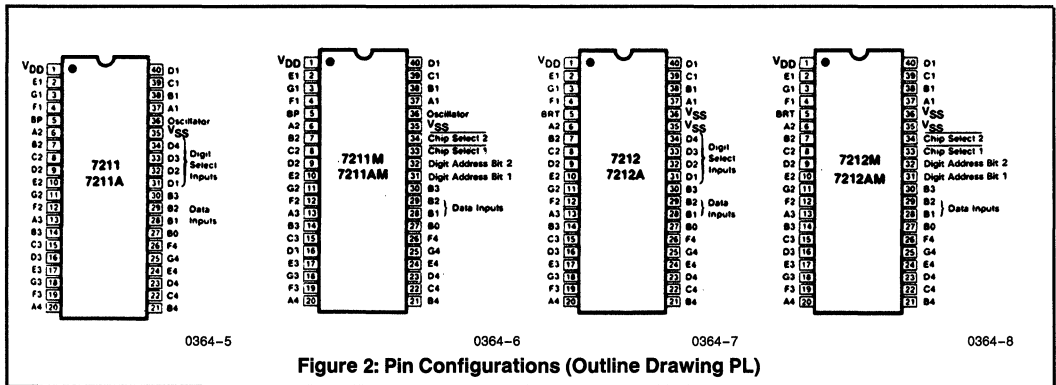


Figure 2: Pin Configurations (Outline Drawing PL)

ELECTRICAL CHARACTERISTICS

ICM7211 CHARACTERISTICS (LCD) $V_{DD} = 5V \pm 10\%$, $T_A = 25^\circ C$, $V_{SS} = 0V$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD} - V_{SS}$)		3	5	6	V
I_{DD}	Operating Current	Test circuit, Display blank		10	50	μA
I_{OSCI}	Oscillator Input Current	Pin 36		± 2	± 10	
t_R, t_F	Segment Rise/Fall Time	$C_L = 200pF$		0.5		μs
t_R, t_F	Backplane Rise/Fall Time	$C_L = 5000pF$		1.5		
f_{OSC}	Oscillator Frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane Frequency	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD} - V_{SS}$)		4	5	6	V
I_{STBY}	Operating Current Display Off	Pin 5 (Brightness), Pins 27-34 - V_{SS}		10	50	μA
I_{DD}	Operating Current	Pin 5 at V_{DD} , Display all 8's		200		mA
I_{SLK}	Segment Leakage Current	Segment Off		± 0.01	± 1	μA
I_{SEG}	Segment On Current	Segment On, $V_O = +3V$	5	8		mA

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NOTE: All typical values have been characterized but are not tested.

INPUT CHARACTERISTICS (ICM7211 AND ICM7212)

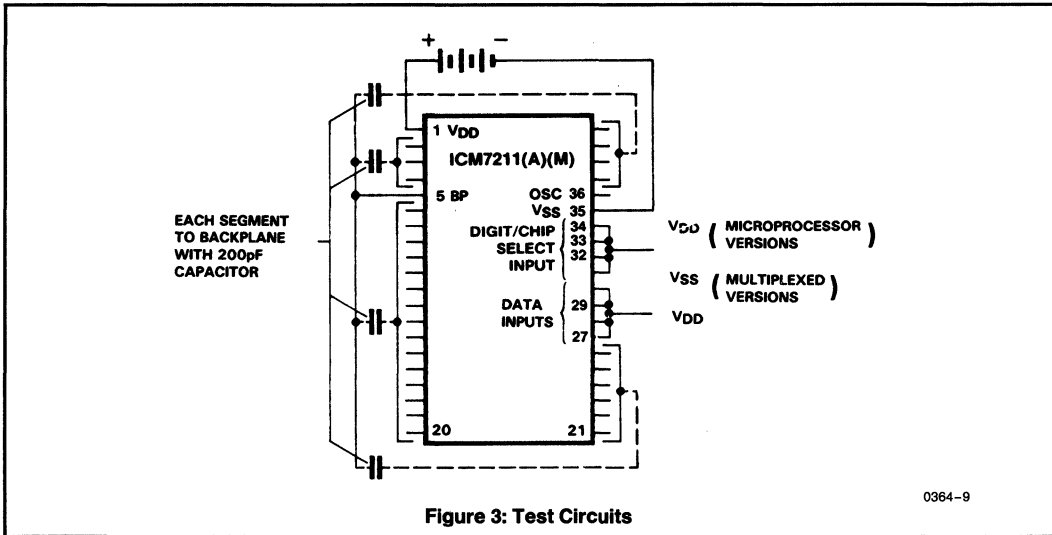
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" input voltage		4			V
V_{IL}	Logical "0" input voltage				1	V
I_{ILK}	Input leakage current	Pins 27-34		$\pm .01$	± 1	μA
C_{IN}	Input capacitance	Pins 27-34		5		pF
I_{BPLK}	BP/Brightness input leakage	Measured at Pin 5 with Pin 36 at V_{SS}		$\pm .01$	± 1	μA
C_{BPI}	BP/Brightness input capacitance	All Devices		200		pF

AC CHARACTERISTICS — MULTIPLEXED INPUT CONFIGURATION

t_{WH}	Digit Select Active Pulse Width	Refer to Timing Diagrams	1			μs
t_{DS}	Data Setup Time		500			ns
t_{DH}	Data Hold Time		200			ns
t_{IDS}	Inter-Digit Select Time		2			μs

AC CHARACTERISTICS — MICROPROCESSOR INTERFACE

t_{WL}	Chip Select Active Pulse Width	other Chip Select either held active, or both driven together	200			ns
t_{DS}	Data Setup Time		100			ns
t_{DH}	Data Hold Time		10	0		ns
t_{CS}	Inter-Chip Select Time		2			μs

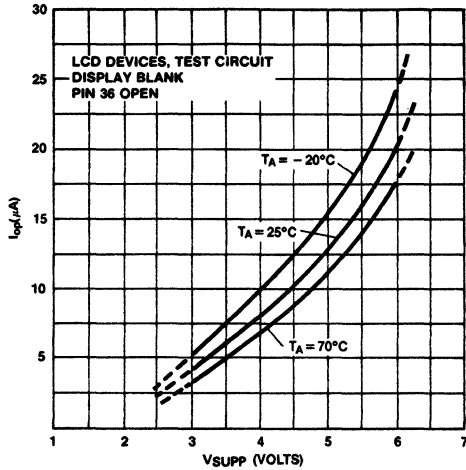


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NOTE: All typical values have been characterized but are not tested.

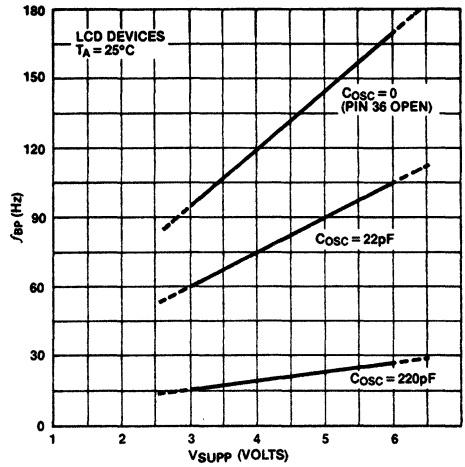
TYPICAL PERFORMANCE CHARACTERISTICS

ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



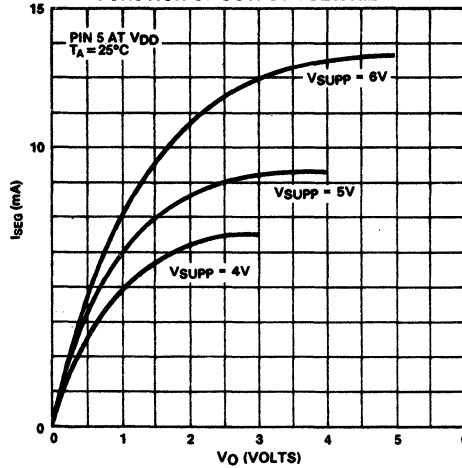
0364-10

ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



0364-11

ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

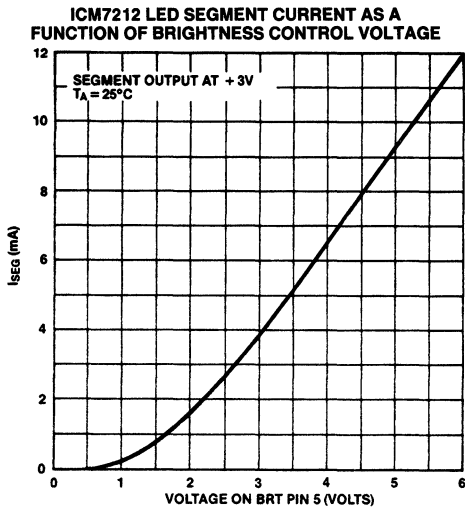


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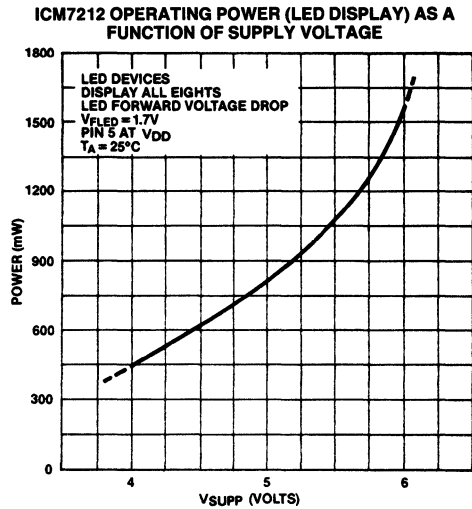
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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



0364-13



0364-14

INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

Input	Terminal	Test Conditions	Function	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V_{DD} V_{SS}	Oscillator input	Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)

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NOTE: All typical values have been characterized but are not tested.

ICM7211/ICM7212 MULTIPLEXED-BINARY INPUT CONFIGURATION

Input	Terminal	Test Conditions	Function
D1	31	V _{DD} = Active V _{SS} = Inactive	D1 Digit Select (Least significant)
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 Digit Select (Most significant)

ICM7211M/ICM7212M MICROPROCESSOR INTERFACE INPUT CONFIGURATION

Input	Description	Terminal	Test Conditions	Function
DA1	Digit Address Bit 1 (LSB)	31	V _{DD} = Logical One V _{SS} = Logical Zero	DA1 & DA2 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V _{DD} = Inactive V _{SS} = Active	When both $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

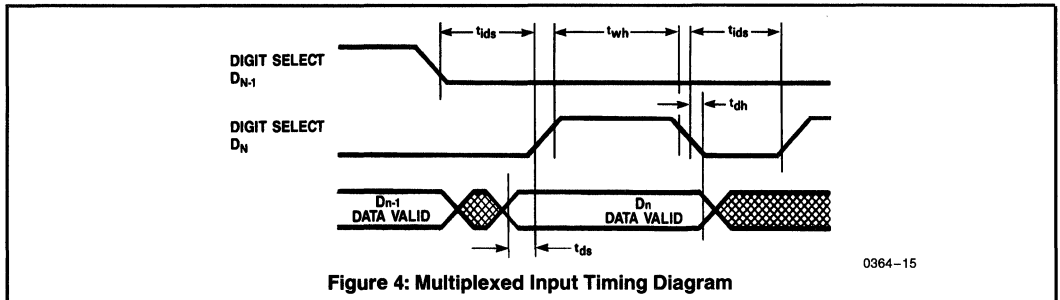


Figure 4: Multiplexed Input Timing Diagram

0364-15

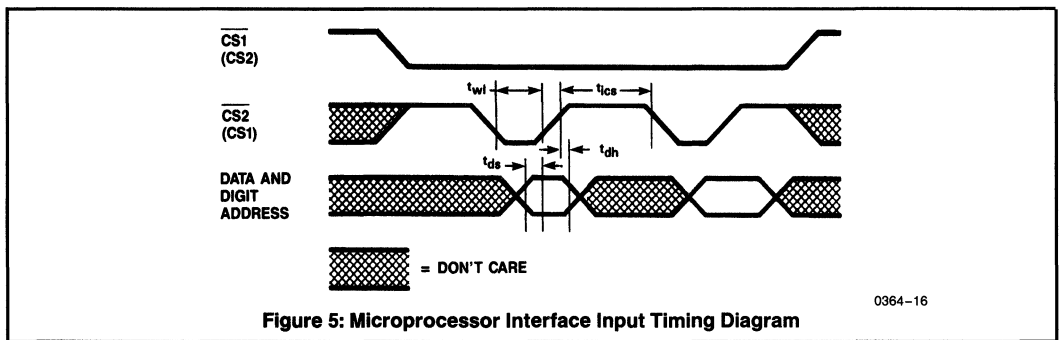


Figure 5: Microprocessor Interface Input Timing Diagram

0364-16

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NOTE: All typical values have been characterized but are not tested.

DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to V_{SS}. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters. It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V_{DD}.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above V_{SS}). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED DEVICES

The LED devices in the family (ICM7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four-digit, seven-segment common-anode LED displays. These devices include 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain, n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 7. The potentiometer should be a high value (100KΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED devices have two connections for V_{SS}; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (-15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V_{SUPP} - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

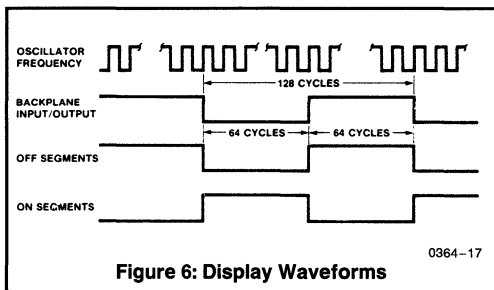


Figure 6: Display Waveforms

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NOTE: All typical values have been characterized but are not tested.

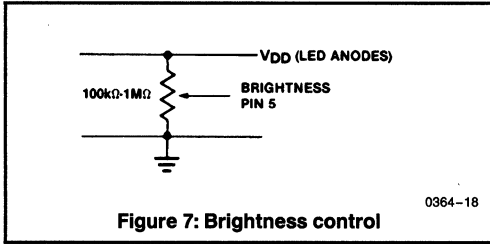


Figure 7: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level=logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211, ICM7211M, ICM7212, and ICM7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, ICM7212A, and ICM7212AM decode the binary input into the same seven-segment output as in the ICM7218 "Code B", ie 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

TABLE 1: Output Codes

BINARY				HEXADECIMAL ICM7211 ICM7211M	CODE B ICM7211A ICM7212AM
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	A
1	0	1	1	b	E
1	1	0	0	c	H
1	1	0	1	d	L
1	1	1	0	e	P
1	1	1	1	f	(BLANK)

0364-19

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For large quantity orders custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least

significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30.

The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

An address of 00 writes into D4, DA2=0, DA1=1 writes into D3, DA2=1, DA1=0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 5, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

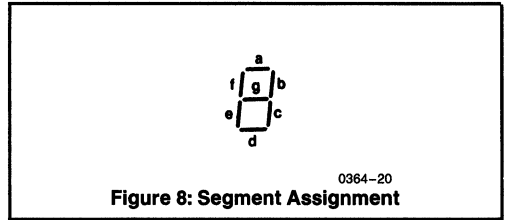


Figure 8: Segment Assignment

APPLICATIONS

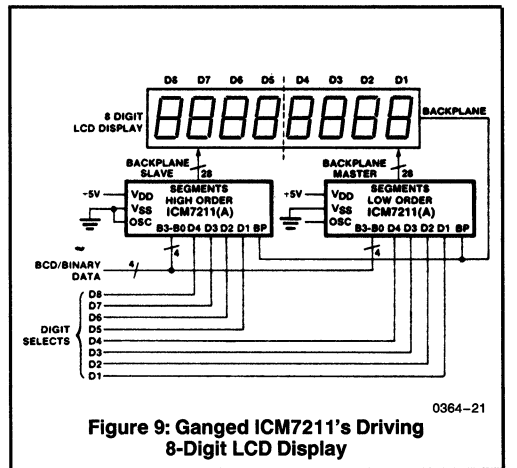


Figure 9: Ganged ICM7211's Driving 8-Digit LCD Display

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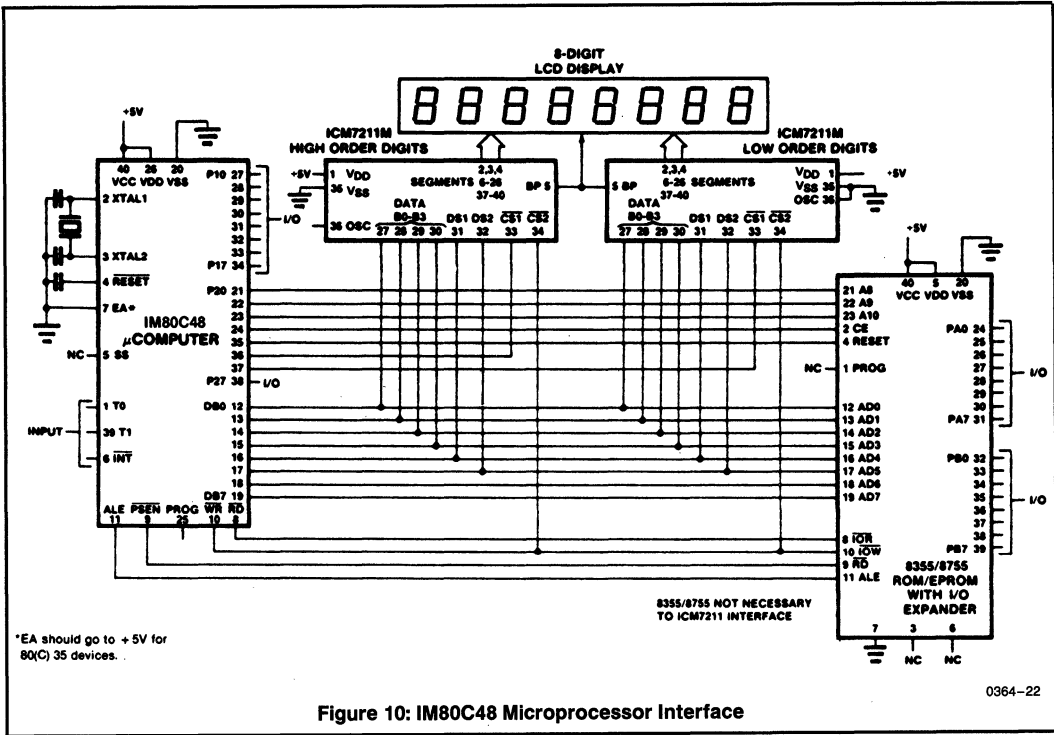


Figure 10: IM80C48 Microprocessor Interface

ICM7218
ICM7218 **ICM7218**
8-Digit LED
Multiplexed Display Driver



GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, 2 types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7218A and ICM7218B feature 2 control lines (WRITE and MODE) which write either 4 bits of control information (DATA COMING, SHUTDOWN, DECODE, and HEXA/CODE B) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going WRITE pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7218C and ICM7218D feature 2 control lines (WRITE and HEXA/CODE B/SHUTDOWN), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the WRITE line low. Only Hexadecimal and Code B formats are available for display outputs.

The ICM7218E provides 4 input lines for control information (WRITE, HEXA/CODE B, DECODE and SHUTDOWN), 8 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the WRITE line. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

FEATURES

- Microprocessor Compatible — C, D, E Versions
- Total Circuit Integration On Chip Includes:
 - a) Digit and Segment Drivers
 - b) All Multiplex Scan Circuitry
 - c) 8 Byte Static Display Memory
 - d) 7 Segment Hexadecimal and Code B Decoders (Pin Selectable)
- Output Drive Suitable for Large LED Displays
- Common Anode and Common Cathode Versions
- Single 5 Volt Supply Required
- Data Retention to 2 Volts Supply
- Shutdown Feature — Turns Off Display and Puts Chip Into Low Power Dissipation Mode
- Sequential and Random Access Versions
- Decimal Point Drive On Each Digit

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7218AIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218BIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218CIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218DIJI	-40°C to +85°C	28-PIN CERDIP
ICM7218EIJL	-40°C to +85°C	40-PIN CERDIP

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
 Digit Output Current 300mA
 Segment Output Current 50mA
 Input Voltage
 (any terminal) $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
 (Note 1)

Power Dissipation (28 Pin CERDIP) 1 W (Note 2)
 Power Dissipation (40 Pin CERDIP) 1 W (Note 2)
 Operating Temperature Range $-40^{\circ}C$ to $+85^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10sec) $300^{\circ}C$

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.
2: These limits refer to the package and will not be obtained during normal operation. Derate above $50^{\circ}C$ by $25mW$ per $^{\circ}C$.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

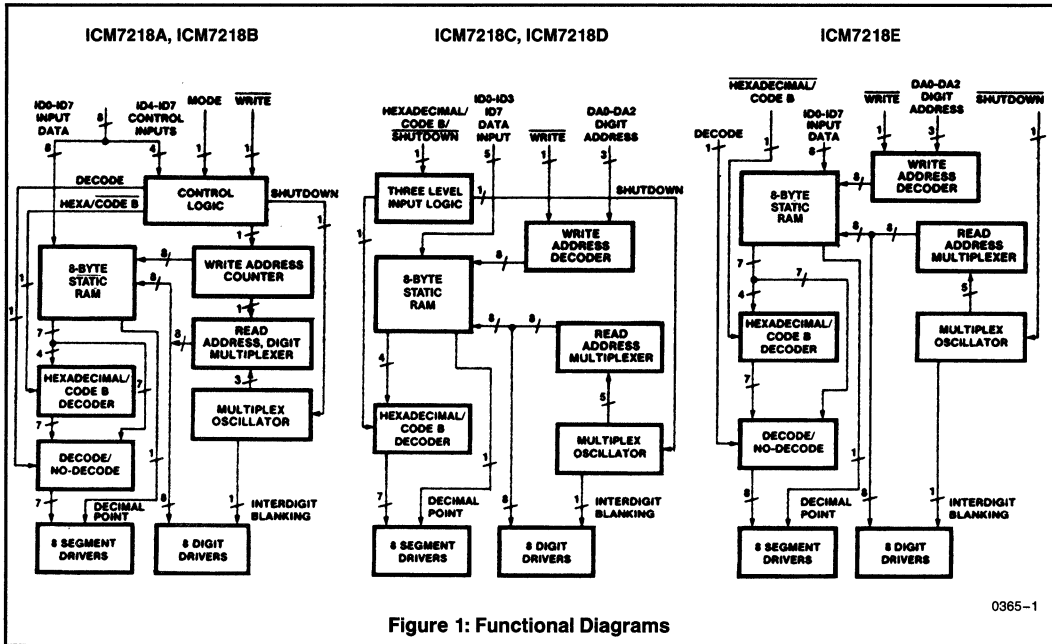
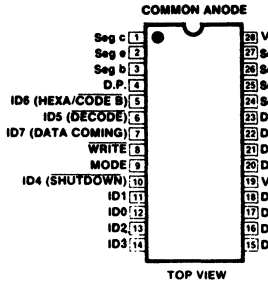


Figure 1: Functional Diagrams

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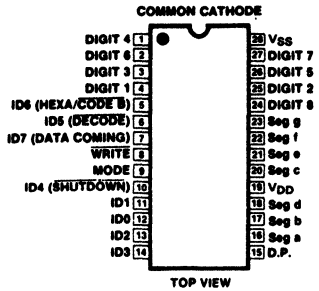
NOTE: All typical values have been characterized but are not tested.

ICM7218A*
(OUTLINE DWG JI)



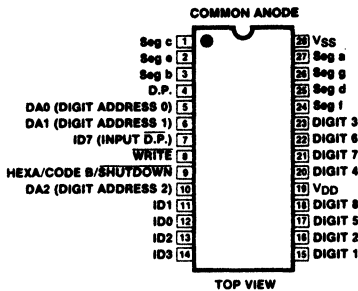
0365-2

ICM7218B*
(OUTLINE DRAWING JI)



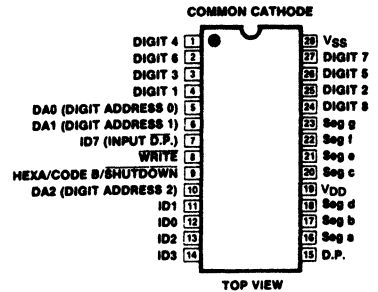
0365-3

ICM7218C
(OUTLINE DRAWING JI)



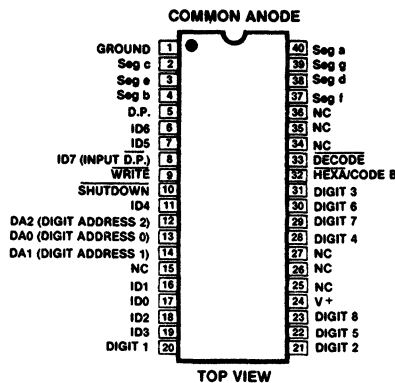
0365-4

ICM7218D
(OUTLINE DRAWING JI)



0365-5

ICM7218E*
(OUTLINE DRAWING DL)



0365-6

* Note: Pins 5,6,7,10 are under control of Mode pin 9.

Figure 2: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

 $V_{DD}=5V, V_{SS}=0V, T_A=25^{\circ}C, \text{Display Diode drop}=1.7V$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Supply Voltage Range	Operating	4		6	V
		Power Down Mode	2		6	V
I_Q	Quiescent Supply Current	Shutdown (Note 3)	6	10	300	μA
I_{DD}	Operating Supply Current	Common Anode SEGS On SEGS Off			2.5	mA
		Common Cathode SEGS On SEGS Off			500	μA
Note 4		700			μA	
		500			μA	
I_{DIG}	Digit Drive Current	Common Anode $V_{out}=V_{DD}-2.0V$	140	200		mA
		Common Cathode $V_{out}=V_{SS}+1.0V$	50	100		mA
I_{DLK}	Digit Leakage Current	Shutdown Mode				
		Common Anode $V_{out}=2V$ Common Cathode $V_{out}=5V$			100 100	μA μA
I_{SEG}	Peak Segment Drive Current	Common Anode $V_{out}=V_{SS}+1.0V$	20	40		mA
		Common Cathode $V_{out}=V_{DD}-2.0V$	-10	-20		mA
I_{SLK}	Segment Leakage Current	Shutdown Mode				
		Common Anode $V_{out}=V_{DD}$ Common Cathode $V_{out}=V_{SS}$			100 100	μA μA
f_{MUX}	Display Scan Rate	Per Digit		250		Hz
V_{IH} V_{IF} V_{IL} Z_{IN}	Three Level Input: Pin 9 ICM7218C/D Logical "1" Input Voltage Floating Input Logical "0" Input Voltage Three Level Input Impedance	Hexadecimal	4.5			V
		Code B	2.0		3.0	V
		Shutdown			0.4	V
		Note 3		100		k Ω
V_{IH} V_{IL}	Logical "1" Input Voltage Logical "0" Input Voltage		3.5			V
					0.8	V
t_{WL}	Write Pulse Width (Low)	7218A, B	550	400		ns
t_{WL}	Write Pulse Width (Low)	7218C, D, E	400	250		ns
t_{MH}	Mode Hold Time	7218A, B	150			ns
t_{MS}	Mode Set Up Time	7218A, B	500			ns
t_{DS}	Data Set Up Time		500			ns
t_{DH}	Data Hold Time	7218 A,B	50			ns
		7218 C,D,E	125			ns
t_{AS}	Digit Address Set Up Time	ICM7218C, D, E	500			ns
t_{AH}	Digital Address Hold Time	ICM7218C, D, E	0			ns
Z_{IN}	Data Input Impedance	5-10 pF Gate Capacitance		10 ¹⁰		Ohms

TABLE 1: INPUT DEFINITIONS ICM7218A and B

Input	Terminal	Logic Level	Function	
$\overline{\text{WRITE}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory	
MODE	9	High Low	Load Control bits on Write Pulse Load Input Data on Write Pulse	
ID4 SHUTDOWN	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Display Disabled)
ID5 ($\overline{\text{DECODE}}$)		6	High Low	No Decode Decode
ID6 (HEXA/CODE B)		5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING)		7	High Low	Data Coming No Data Coming } Control Word
ID0-ID7	MODE Low	11,12,13,14, 5,6,10,7		Display Data Inputs (Notes 4, 5)

TABLE 2: INPUT DEFINITIONS ICM7218C and D

Input	Terminal	Logic Level	Function
$\overline{\text{WRITE}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
HEXA/CODE B/ $\overline{\text{SHUTDOWN}}$	9 (Note 3)	High Floating Low	Hexadecimal Decoding Code B Decoding Shutdown (Oscillator, Decoder and Display Disabled)
DA0 – DA2	10,6,5		Digit Address Inputs
ID0 – ID3 ID (INPUT D.P.)	14,13,11,12 7		Display Data Inputs Decimal Point Input

NOTE 3: In the ICM7218C and D (random access versions) the HEXA/CODE B/ $\overline{\text{SHUTDOWN}}$ Input (Pin 9) has internal biasing resistors to hold it at $V_{DD}/2$ when Pin 9 is open circuited. These resistors consume power and result in a quiescent supply current (I_Q) of typically $50\mu\text{A}$. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

- 4: ID0-ID3 = Don't care when writing control data
ID4-ID6 = Don't care when writing Hex/Code B data
ID7 = Decimal Point data
(The display blanks on ICM7218A/B versions when writing in data)
- 5: In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents an "on" segment, (i.e. segments are positive true, decimal point is negative true).
- 6: Common Anode segment drivers and Common Cathode Digit Drivers have $20\text{k}\Omega$ pullup resistors.

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NOTE: All typical values have been characterized but are not tested.

TABLE 3: INPUT DEFINITIONS ICM7218E

Input	Terminal	Logic Level	Function
WRITE	9	High Low	Input Latches Not Updated Input Latches Updated
SHUTDOWN	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
DECODE	33	High Low	No Decode Decode
HEXA/CODE B	32	High Low	Code B Decoding Hexadecimal Decoding
DA0 – DA2 Digit Address (0,1,2)	13,14,12		Digit Address Inputs
ID0 – ID6 ID7 (INPUT D.P.)	17,16,18,19,11,7,6 8		Display Data Inputs (Note 5) Display Data/Decimal Point Input

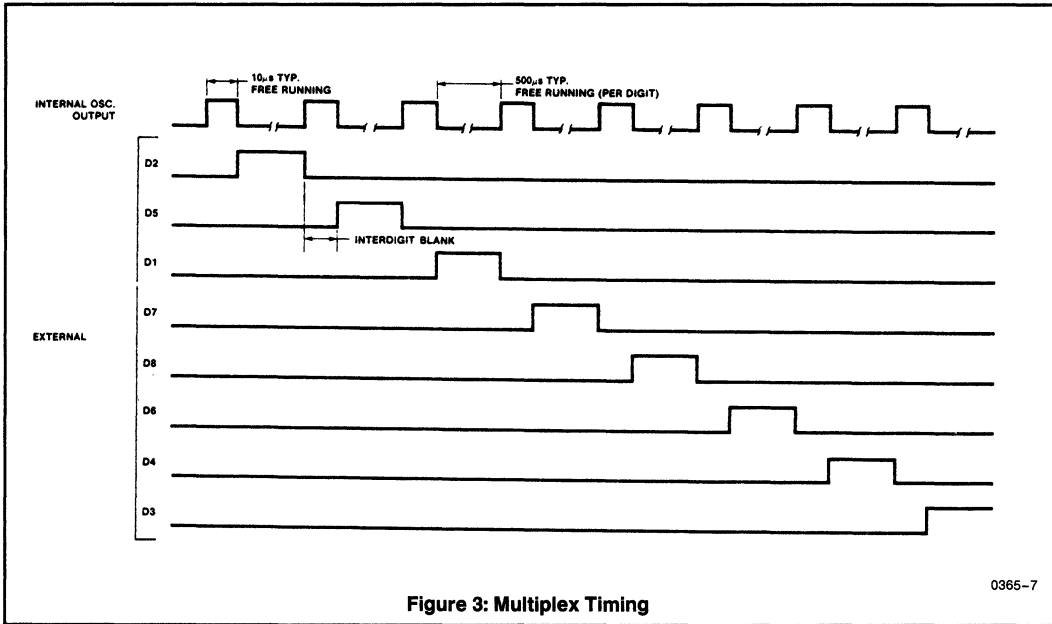


Figure 3: Multiplex Timing

0365-7

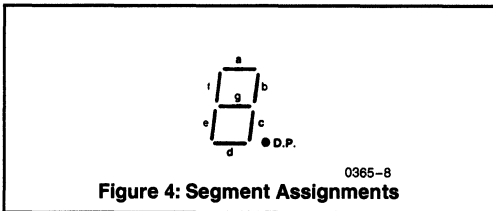


Figure 4: Segment Assignments

0365-8

DETAILED DESCRIPTION

DECODE Operation

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary code plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

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NOTE: All typical values have been characterized but are not tested.

The 7 segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: $\overline{D.P.}$ a b c e g f d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "zero" represents an "on" segment.

HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (-), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0, and decimal point data is set up on ID7.

Decimal	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HEXA CODE	0 1 2 3 4 5 6 7 8 9 A b C d E F
CODE B	0 1 2 3 4 5 6 7 8 9 - E H L P (BLANK)

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically $10\mu\text{A}$ at $V_{DD} = 5\text{V}$), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown — only the display output sections of the device are disabled in this mode.

Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2 volts without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With segment peak drive current of 40mA typically, this results in 5mA average drive. The common cathode drive capability is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately $10\mu\text{s}$ occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drives together to drive a 4 digit display, 5mA average segment drive current can be obtained.

Power Dissipation Considerations

Assuming common anode drive at $V_{DD} = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will therefore be 640mW, rising to about 900mW, for all '8' 's displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Sequential Addressing Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and WRITE low. The instructions occur on 4 lines and are — $\overline{\text{DECODE}}$ /no Decode, type of Decode (if desired), $\overline{\text{SHUTDOWN}}$ /no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going WRITE pulse. After all 8 digit memory locations have been written to, additional transitions of the WRITE input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

Random Access Input Drive Considerations (ICM7218C/D/E)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the WRITE pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

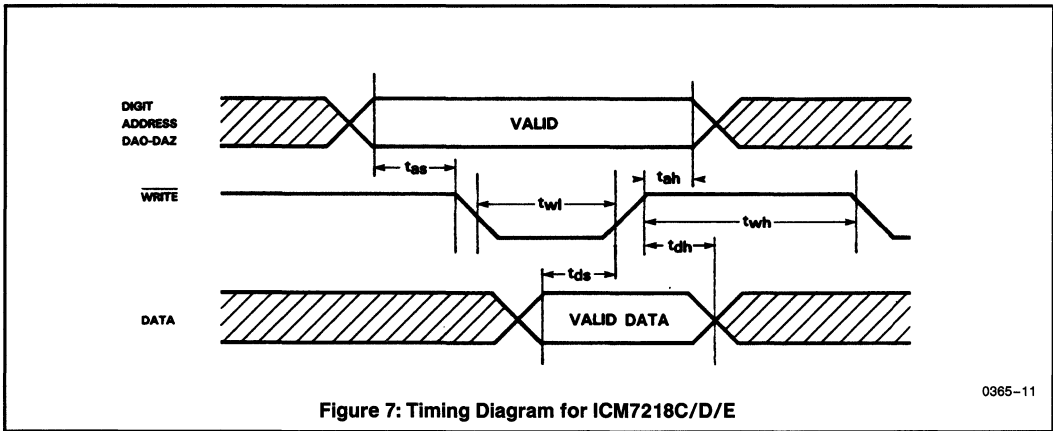
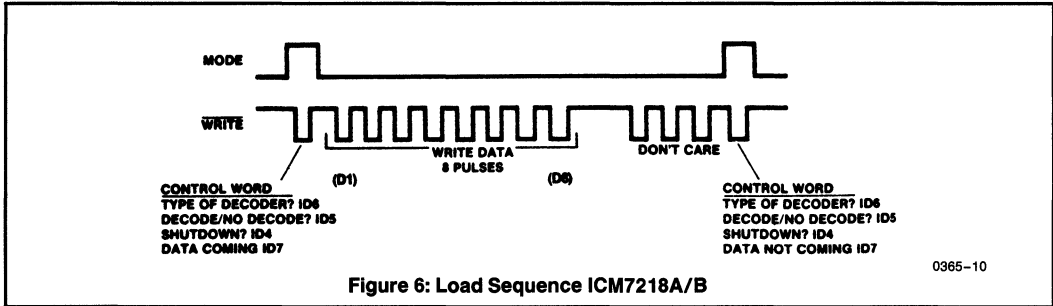
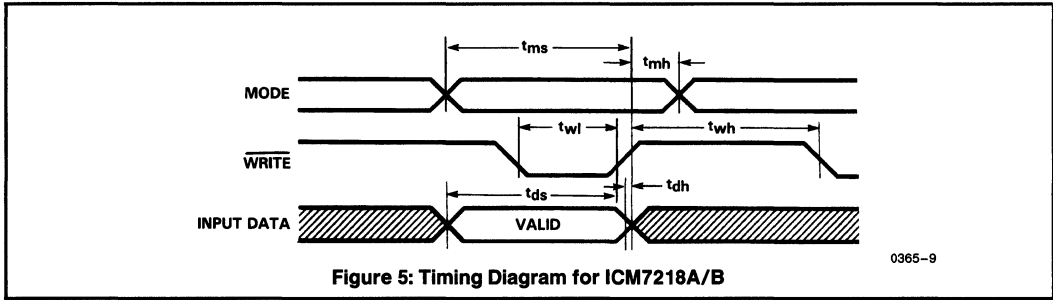
Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the WRITE pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 7).

Supply Capacitor

A $0.1\mu\text{F}$ capacitor is recommended between V_{DD} and V_{SS} to bypass multiplex noise.

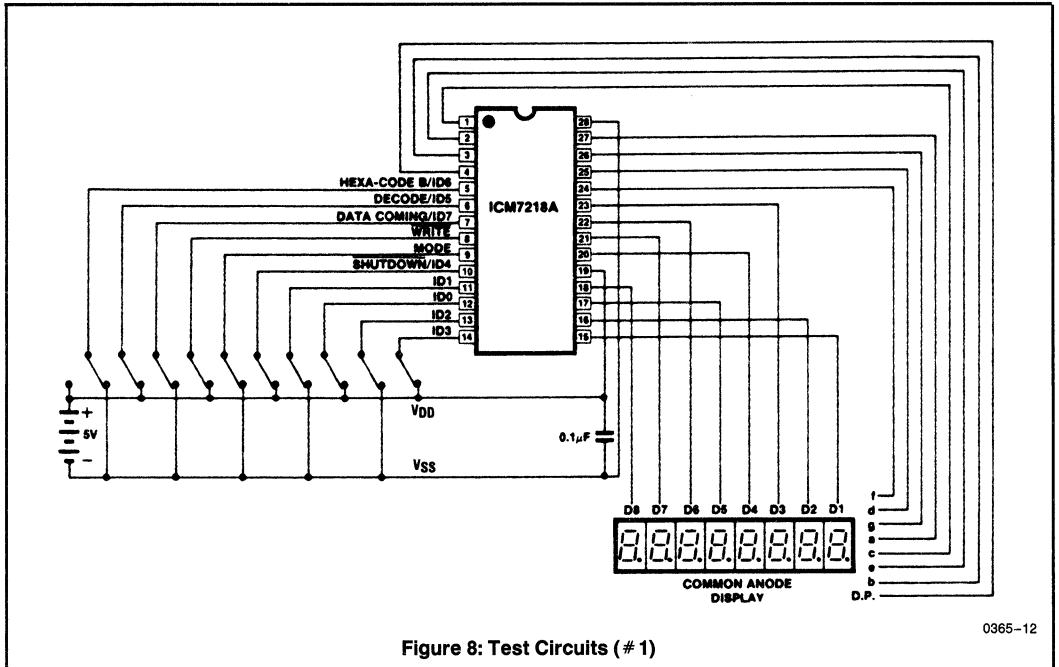
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NOTE: All typical values have been characterized but are not tested.

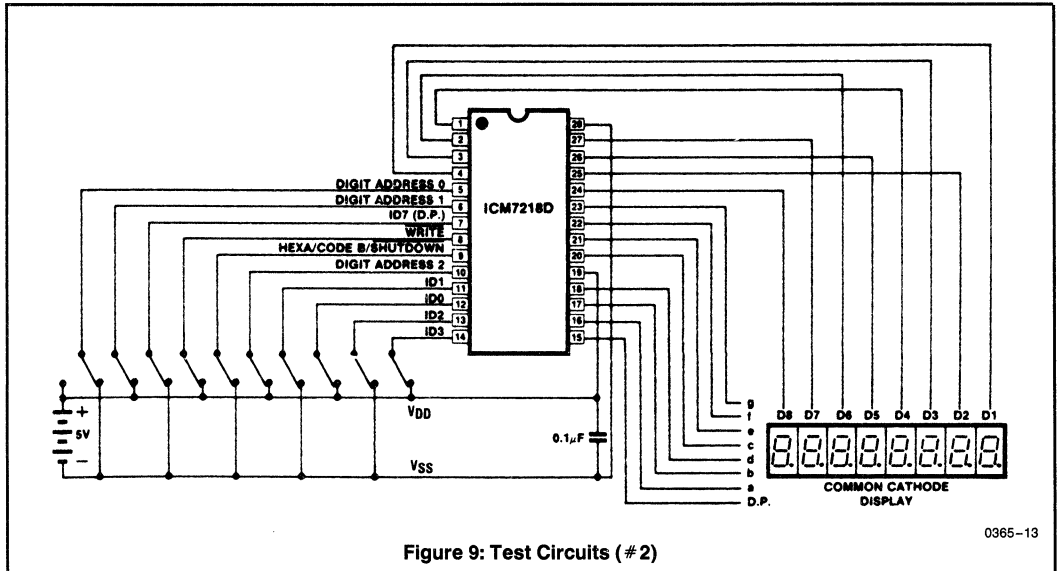


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NOTE: All typical values have been characterized but are not tested.



0365-12



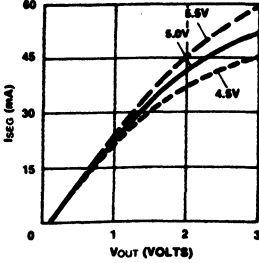
0365-13

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NOTE: All typical values have been characterized but are not tested.

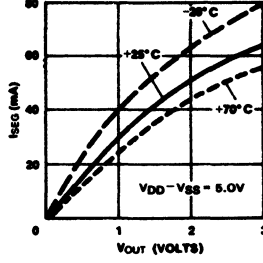
TYPICAL PERFORMANCE CHARACTERISTICS

COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT} AT 25°C



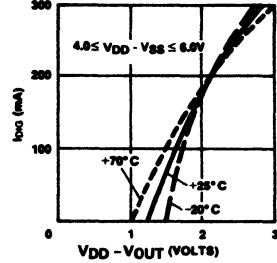
0365-14

COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT}



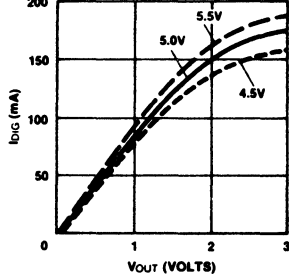
0365-15

COMMON ANODE DIGIT DRIVER
I_{DIG} vs. (V_{DD} - V_{OUT})



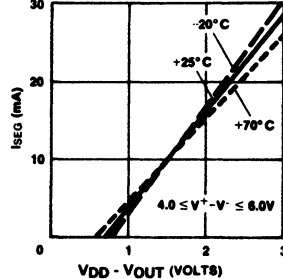
0365-16

COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT} AT 25°C



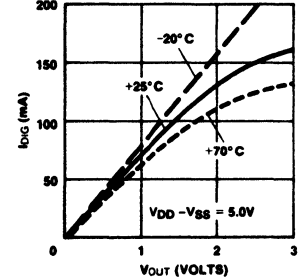
0365-17

COMMON CATHODE SEG. DRIVER
I_{SEG} vs. (V_{DD} - V_{OUT})



0365-18

COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}



0365-19

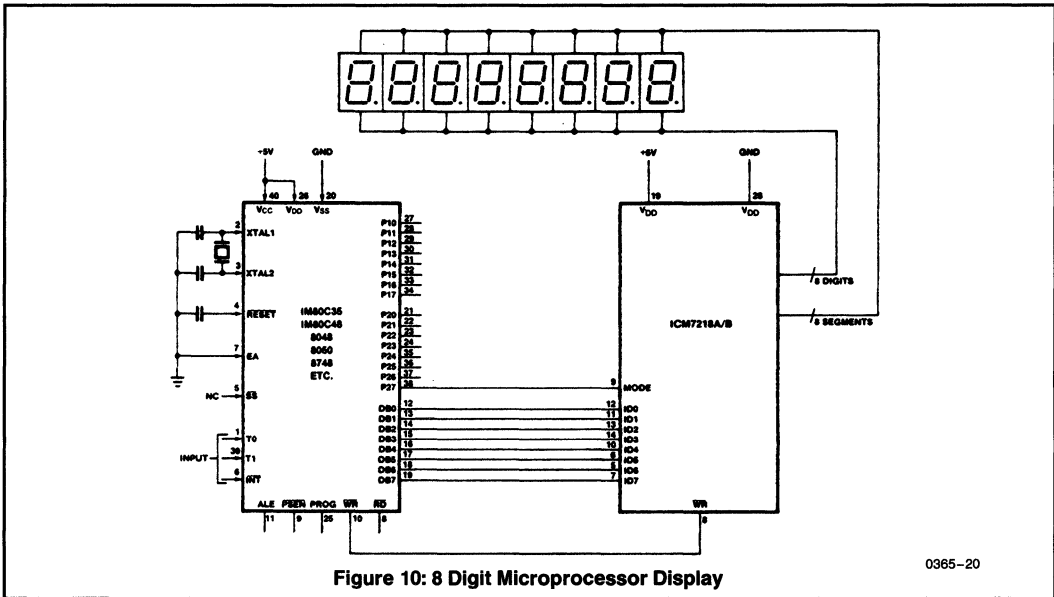


Figure 10: 8 Digit Microprocessor Display

0365-20

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NOTE: All typical values have been characterized but are not tested.

APPLICATION EXAMPLES
8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Figure 10 shows a display interface using the ICM7218A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7218 display interface on successive WRITE pulses. The MODE input to the 7218 is connected to one of the I/O port pins on the microcontroller. When MODE is high a control word is transferred; when MODE is low data is transferred. Sequential locations in the 8-byte static memory are automatically loaded on each successive WRITE pulse. After eight WRITE pulses have occurred, further pulses are ignored until a new control word is transferred. (See Figure 6). This also allows writing to other peripheral devices without disturbing the ICM7218A/B.

16 DIGIT MICROPROCESSOR DISPLAY

In this application (see Figure 11), both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0. Dis-

play data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218's simultaneously.

The display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7218's from the processor on port lines P26 and P27.

NO DECODE APPLICATION

The ICM7218 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments \times 8 digits = 64 dots \div 2 per red or green = 32 channels).

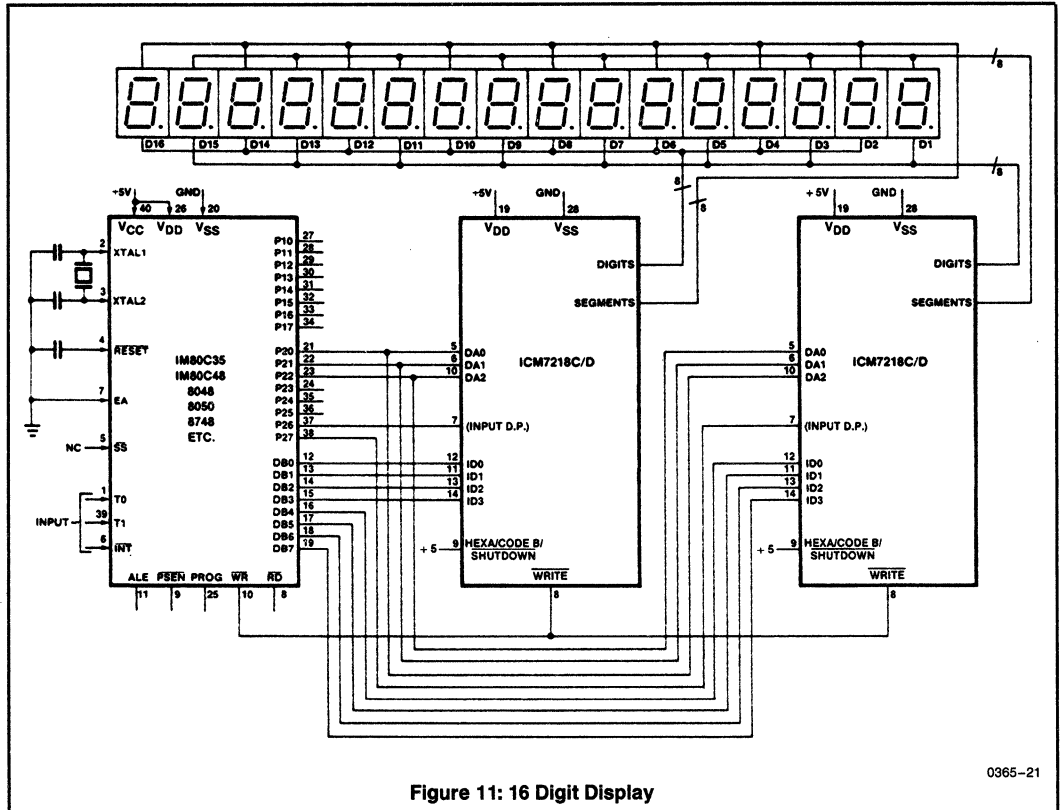


Figure 11: 16 Digit Display

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NOTE: All typical values have been characterized but are not tested.

ICM7228

8-Digit LED Multiplexed Display Driver



ICM7228

GENERAL DESCRIPTION

The ICM7228 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, 2 types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7228A and ICM7228B feature 2 control lines (WRITE and MODE) which write either 4 bits of control information (DATA COMING, SHUTDOWN, DECODE, and HEXA/CODE B) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going WRITE pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7228C and ICM7228D feature 2 control lines (WRITE and HEXA/CODE B/SHUTDOWN), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the WRITE line low. Only Hexadecimal and Code B formats are available for display outputs.

FEATURES

- **Microprocessor Compatible**
- **Total Circuit Integration On Chip Includes:**
 - (a) Digit and Segment Drivers
 - (b) All Multiplex Scan Circuitry
 - (c) 8 Byte Static Display Memory
 - (d) 7 Segment Hexadecimal and Code B Decoders (Pin Selectable)
- **Output Drive Suitable for Large LED Displays**
- **Common Anode and Common Cathode Versions**
- **Single 5V Supply Required**
- **Data Retention to 2V Supply**
- **Shutdown Feature—Turns Off Display and Puts Chip into Low Power Dissipation Mode**
- **Sequential and Random Access Versions**
- **Decimal Point Drive On Each Digit**
- **Non-Overlapping Digit Strobe**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7228AIJI	-40°C to +85°C	28-Pin CERDIP
ICM7228BIJI	-40°C to +85°C	28-Pin CERDIP
ICM7228CIJI	-40°C to +85°C	28-Pin CERDIP
ICM7228DIJI	-40°C to +85°C	28-Pin CERDIP
ICM7228AIPi	-40°C to +85°C	28-Pin Plastic DIP
ICM7228BIPi	-40°C to +85°C	28-Pin Plastic DIP
ICM7228CIPi	-40°C to +85°C	28-Pin Plastic DIP
ICM7228DIPi	-40°C to +85°C	28-Pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$)6V
Digit Output Current500 mA
Segment Output Current100 mA
Input Voltage (any terminal)	... ($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$) (Note 1)
Power Dissipation1.5W (Note 2)
Operating Temperature Range $-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM728 should be turned on first.

2: These limits refer to the package and will not be obtained during normal operation. Derate above $50^{\circ}C$ by 25 mW per $^{\circ}C$.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

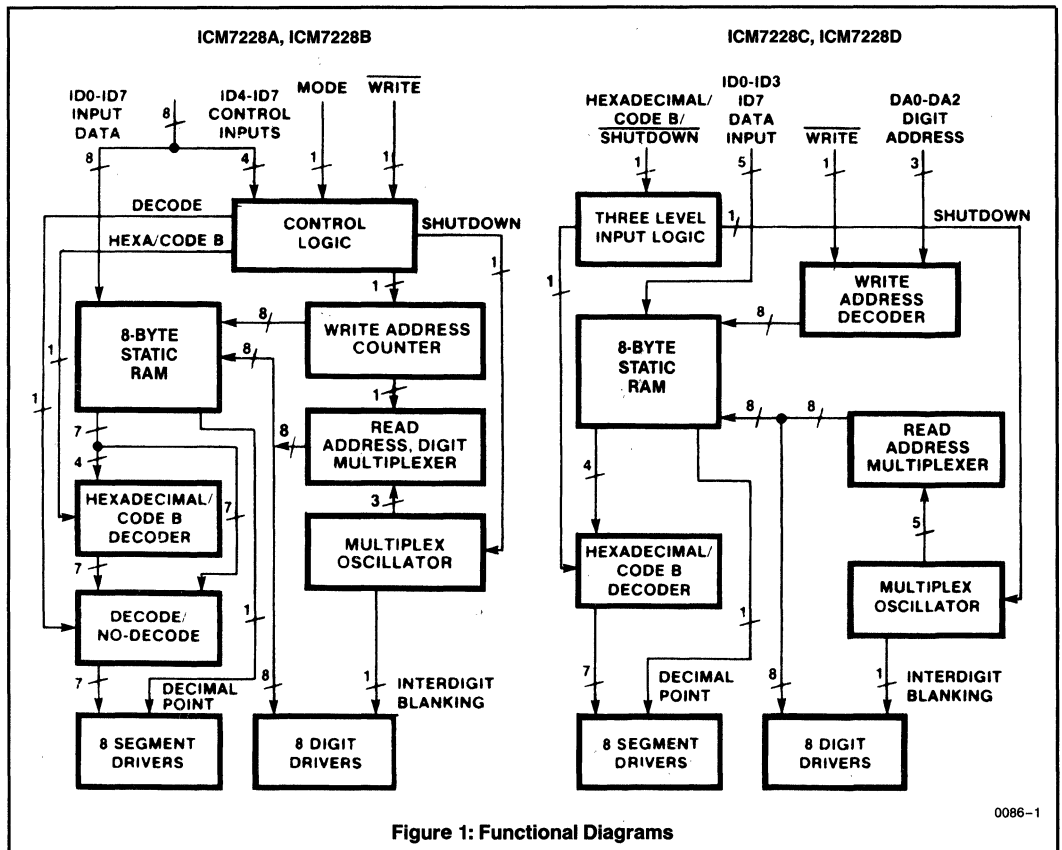
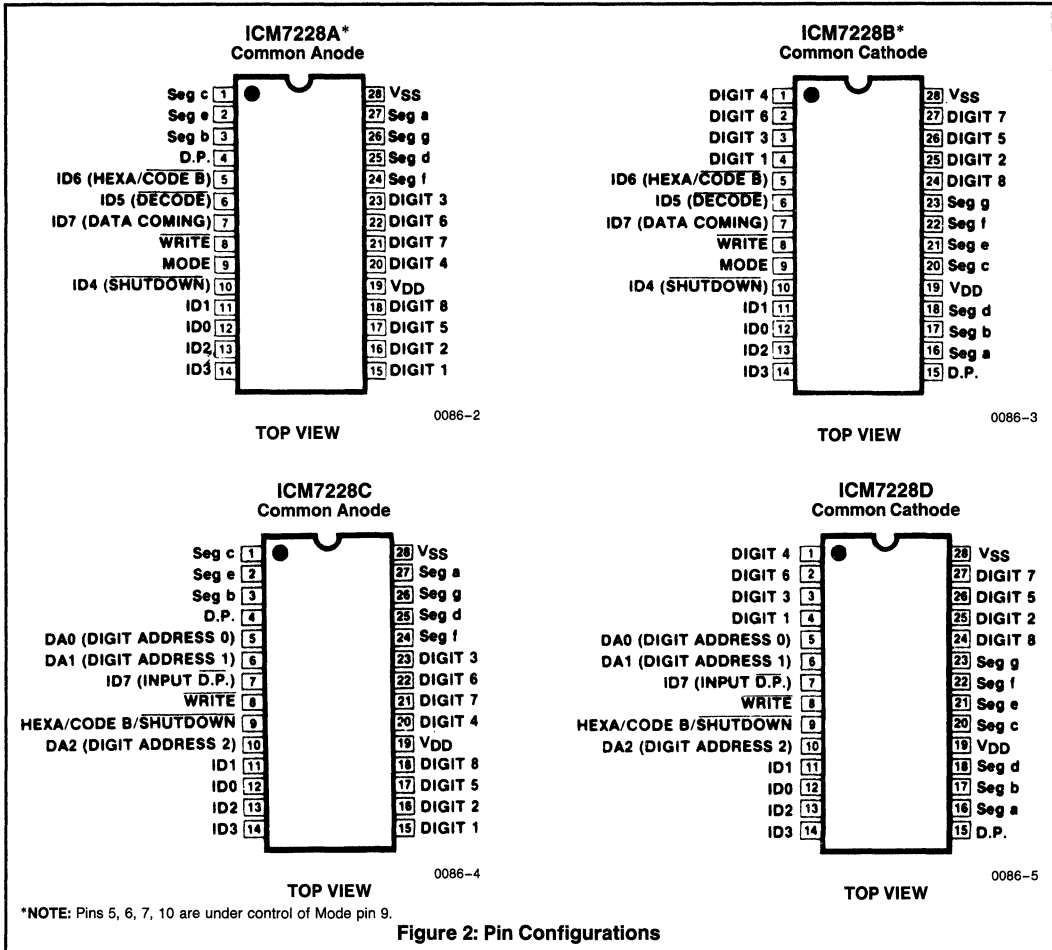


Figure 1: Functional Diagrams

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NOTE: All typical values have been characterized but are not tested.



ELECTRICAL CHARACTERISTICS $V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Test Conditions	$T_A = 25^\circ C$			$-40^\circ C \leq T_A \leq +85^\circ C$			Units
			Min	Typ	Max	Min	Typ	Max	
V_{SUPPLY}	Supply Voltage Range	Operating	4		6	4		6	V
		Power Down Mode	2			2			
I_Q	Quiescent Supply Current	Shutdown, 7228A, 7228B		1	100		1	100	μA
		Shutdown, 7228C, 7228D		2.5	100		2.5	100	
I_{DD}	Operating Supply Current	Common Anode Segments = ON Outputs = OPEN		200	450		200	450	μA
		Common Anode Segments = OFF Outputs = OPEN		100	450		100	450	
		Common Cathode Segments = ON Outputs = OPEN		250	450		250	450	
		Common Cathode Segments = OFF Outputs = OPEN		175	450		175	450	
I_{DIG}	Digit Drive Current	Common Anode $V_{OUT} = V_{DD} - 2.0V$	200			175			mA
		Common Cathode $V_{OUT} = V_{SS} + 1.0V$	50			40			
I_{DLK}	Digit Leakage Current	Shutdown Mode Common Anode $V_{OUT} = 2.0V$		1	100		1	100	μA
		Shutdown Mode Common Cathode $V_{OUT} = 5.0V$		1	100		1	100	
I_{SEG}	Peak Segment Drive Current	Common Anode $V_{OUT} = V_{SS} + 1.0V$	20	25		20			mA
		Common Cathode $V_{OUT} = V_{DD} - 2.0V$	10	12		10			
I_{SLK}	Segment Leakage Current	Shutdown Mode Common Anode $V_{OUT} = V_{DD}$		1	50		1	50	μA
		Shutdown Mode Common Cathode $V_{OUT} = V_{SS}$		1	50		1	50	
I_{IL}	Input Leakage Current	All Inputs Except Pin 9 7228C, 7228D $V_{IN} = V_{SS}$			1			1	μA
		All Inputs Except Pin 9 7228C, 7228D $V_{IN} = 5.0V$			-1			-1	
f_{MUX}	Display Scan Rate	Per Digit	125	150		80		Hz	
t_{IDB}	Inter-Digit Blanking Time		2	10		2		μs	
V_{INH}	Logical "1" Input Voltage	Three Level Input: Pin 9 7228C, 7228D Hexadecimal $V_{DD} = 5V$	4.2			4.2		V	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$ (Continued)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			Units
			Min	Typ	Max	Min	Typ	Max	
V_{INF}	Floating Input	Three Level Input: Pin 9 7228C, 7228D Code B $V_{DD} = 5V$	2.0		3.0	2.0		3.0	V
V_{INL}	Logical "0" Input Voltage	Three Level Input: Pin 9 7228C, 7228D Shutdown $V_{DD} = 5V$			0.8			0.8	V
Z_{IN}	Three Level Input Impedance	$V_{CC} = 5V$ Pin 9 of 7228C & 7228D	50			50			k Ω
V_{IH}	Logical "1" Input Voltage	All Inputs Except Pin 9 of 7228C, 7228D $V_{DD} = 5V$	2.0			2.0			V
V_{IL}	Logical "0" Input Voltage				0.8			0.8	

AC ELECTRICAL CHARACTERISTICS $V_{DD} = 5V \pm 10\%$, $V_{IL} = 0.4V$, $V_{IH} = 2.4V$

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			Units
			Min	Typ	Max	Min	Typ	Max	
t_{WL}	Write Pulsewidth (Low)		200	100		250			ns
t_{WH}	Write Pulsewidth (High)		850	540		1200			ns
t_{MH}	Mode Hold Time	7228A, 7228B	0	-65		0			ns
t_{MS}	Mode Setup Time	7228A, 7228B	250	150		250			ns
t_{DS}	Data Setup Time		250	160		250			ns
t_{DH}	Data Hold Time	7228A, 7228B	0	-60		0			ns
		7228C, 7228D	0	-60		0			ns
t_{AS}	Digit Address Setup Time	7228C, 7228D	250	110		250			ns
t_{AH}	Digit Address Hold Time	7228C, 7228D	0	-60		0			ns

TABLE 1: INPUT DEFINITIONS ICM7228A AND B

Input	Terminal	Logic Level	Function	
WRITE	8	High Low	Input Not Loaded into Memory Input Loaded into Memory	
MODE	9	High Low	Load Control Bits on Write Pulse Load Input Data on Write Pulse	
ID4 SHUTDOWN	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Display Disabled)
ID5 (DECODE)		6	High Low	No Decode Decode
ID6 (HEXA/CODE B)		5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING)		7	High Low	Data Coming No Data Coming } Control Word
ID0-ID7	MODE Low	11, 12, 13, 14, 5, 6, 10, 7	Display Data Inputs (Notes 4, 5)	

TABLE 2: INPUT DEFINITIONS ICM7228C AND D

Input	Terminal	Logic Level	Function
WRITE	8	High Low	Input Not Loaded into Memory Input Loaded into Memory
HEXA/CODE B/SHUTDOWN	9 (Note 3)	High Floating Low	Hexadecimal Decoding Code B Decoding Shutdown (Oscillator, Decoder and Display Disabled)
DA0-DA2	10, 6, 5		Digit Address Inputs
ID0-ID3 ID7 (Input D.P.)	14, 13, 11, 12 7		Display Data Inputs Decimal Point Input

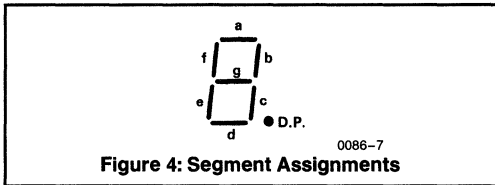
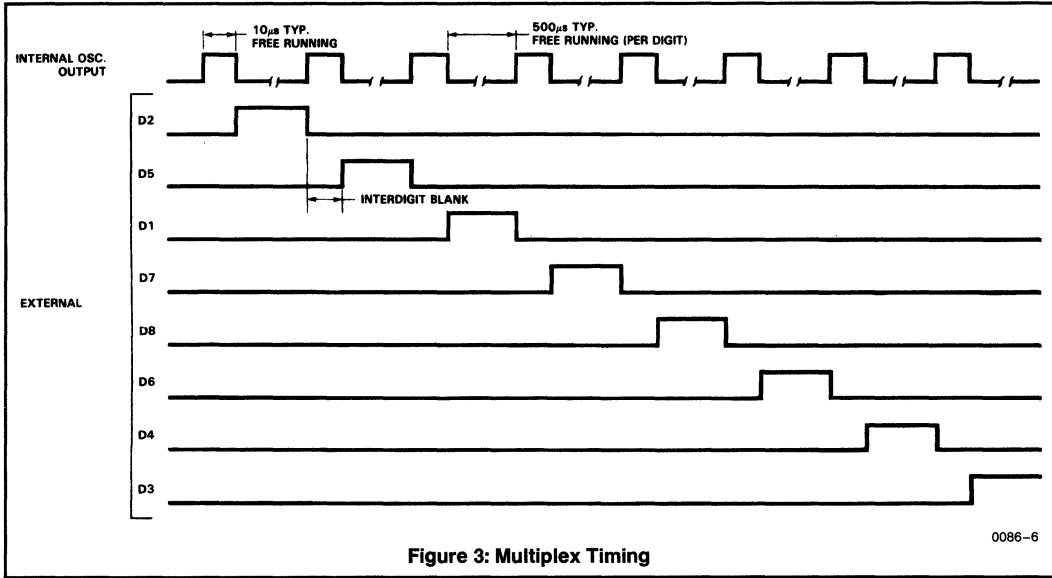
NOTE 3: In the ICM7228C and D (random access versions) the HEXA/CODE B/SHUTDOWN Input (Pin 9) has internal biasing resistors to hold it at $V_{DD}/2$ when Pin 9 is open circuited. These resistors consume power and result in a quiescent supply current (I_Q) of typically 50 μ A. The ICM7228A, B devices do not have these biasing resistors and thus are not subject to this condition.

- 4: ID0-ID3 = Don't care when writing control data
 ID4-ID6 = Don't care when writing Hex/Code B data
 ID7 = Decimal point data
 (The display blanks on ICM7228A/B versions when writing in data)

- 5: In the No Decode format, "Ones" represent "on" segments for all inputs except for the Decimal Point where "Zero" represents an "on" segment (i.e., segments are positive true, decimal point is negative true).

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NOTE: All typical values have been characterized but are not tested.



Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HEXA CODE	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
CODE B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(Blank)

DETAILED DESCRIPTION

DECODER Operation

For the ICM7228A/B products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary code plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

The 7 segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0
 Output Segments: D.P. a b c e g f d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "Zero" represents an "on" segment.

HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (-), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0, and decimal point data is set up on ID7.

SHUTDOWN

SHUTDOWN performs several functions: it puts the device into a very low dissipation mode (typically 1 µA at VDD = 5V), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown — only the display output sections of the device are disabled in this mode.

Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2 volts without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With segment peak drive current of 40 mA typically, this results in 5 mA average drive. The common cathode drive capability is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

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NOTE: All typical values have been characterized but are not tested.

Inter Digit Blanking

A blanking time of 2 μ s minimum, 10 μ s typical occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drives together to drive a 4 digit display.

Power Dissipation Considerations

Assuming common anode drive at $V_{DD} = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200 mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7228. The device power dissipation will therefore be 640 mW, rising to about 900 mW, for all "8"s displayed. Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.

Sequential Addressing Considerations (ICM7228A/B)

The control instructions are read from the input bus lines if MODE is high and WRITE low. The instructions occur on 4 lines and are — DECODE/no Decode, type of Decode (if desired), SHUTDOWN/no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going WRITE pulse. After all 8 digit memory locations have been written to, additional transitions of the WRITE input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

Random Access Input Drive Considerations (ICM7228C/D)

Control instructions are provided to the ICM7228C/D by a single three level input terminal (Pin 9), which operates independently of the WRITE pulse.

Data can be written into memory on the ICM7228C/D by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the WRITE pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 7.)

Supply Capacitor

A 0.1 μ F capacitor is recommended between V_{DD} and V_{SS} to bypass multiplex noise.

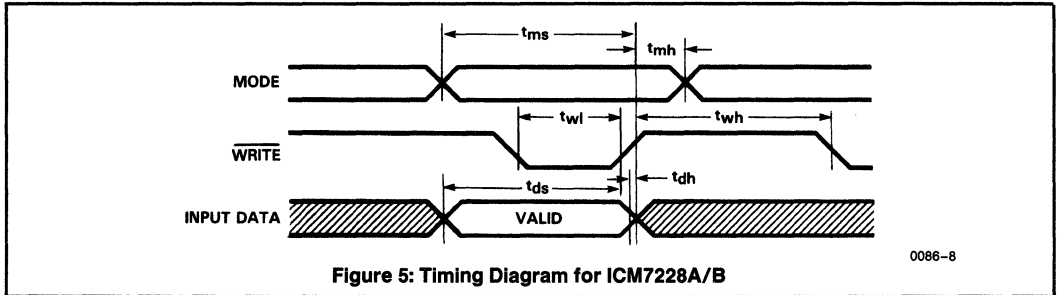
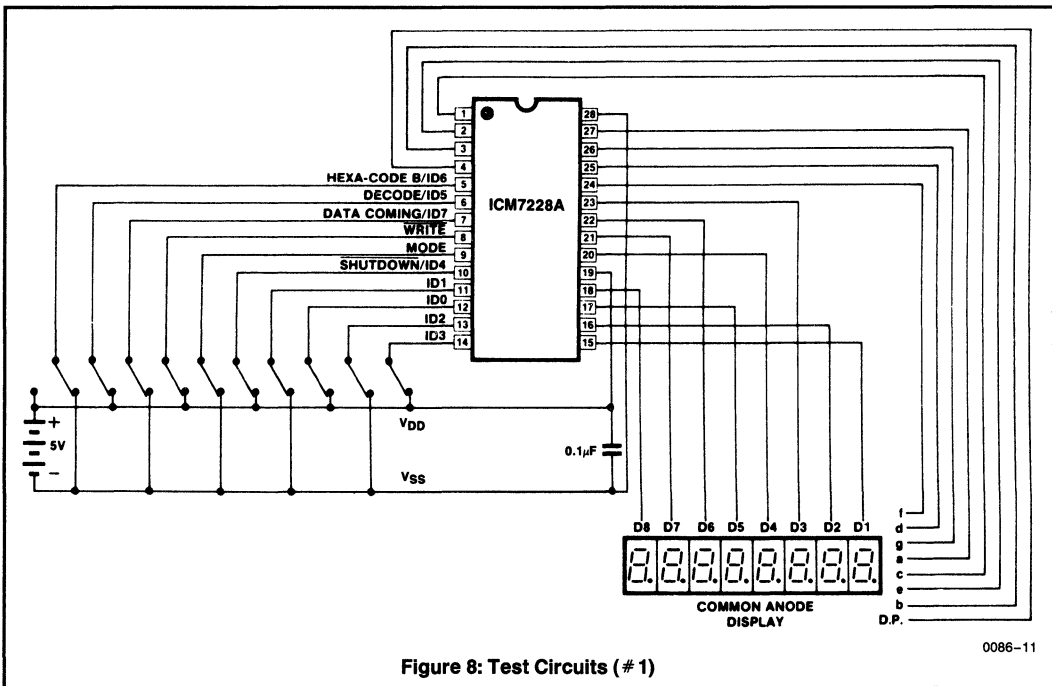
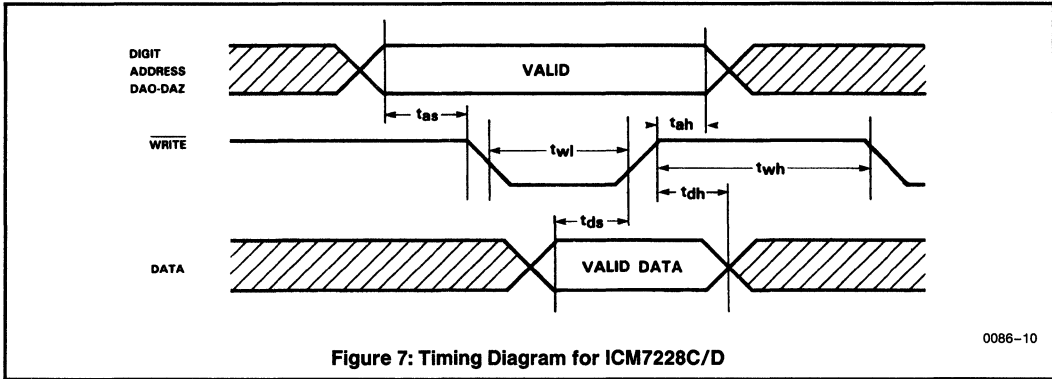
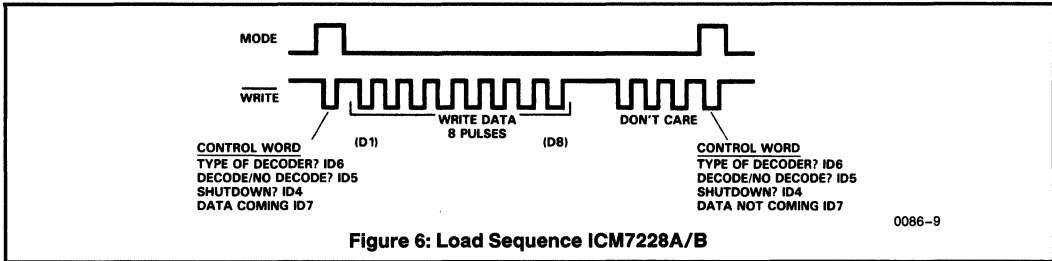


Figure 5: Timing Diagram for ICM7228A/B

0086-8

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NOTE: All typical values have been characterized but are not tested.



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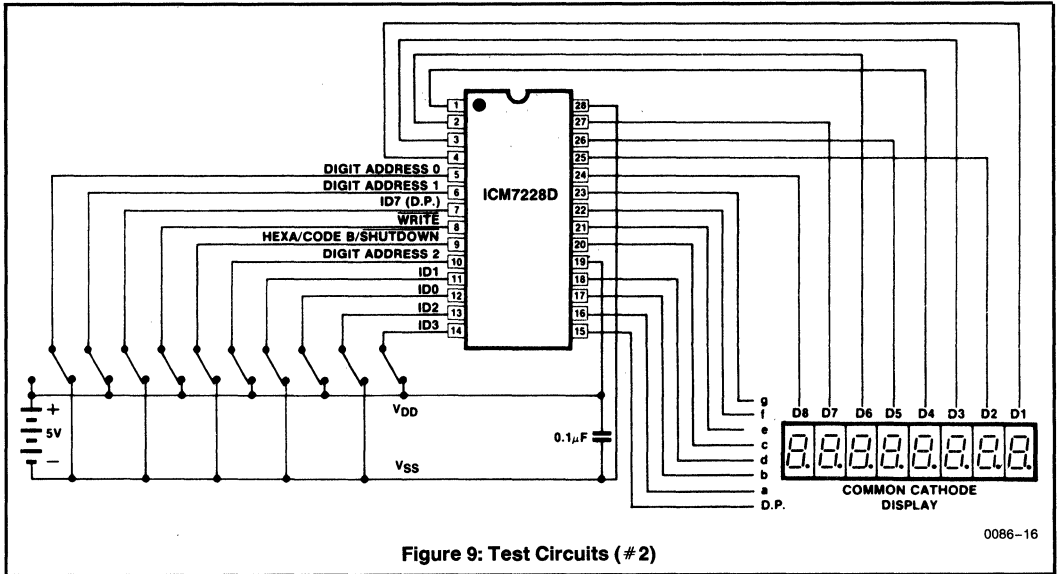


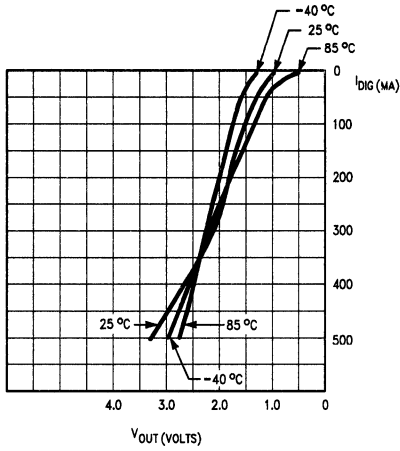
Figure 9: Test Circuits (# 2)

0086-16

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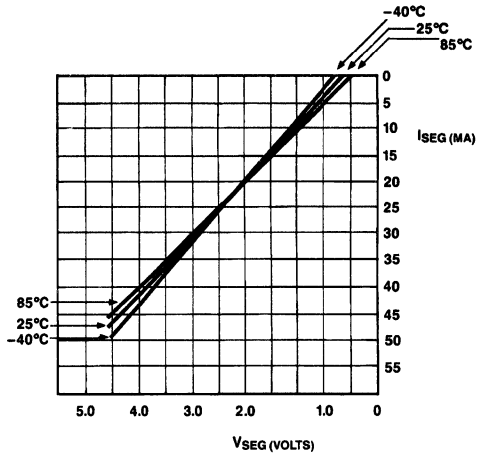
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



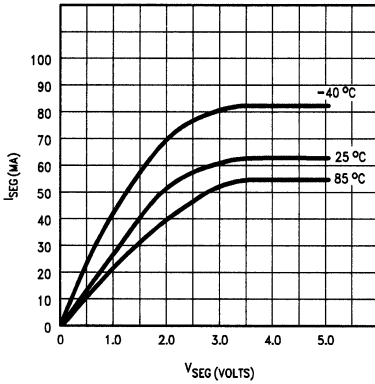
0086-12

Common Anode Digit Driver
 I_{DIG} vs $(V_{DD}-V_{OUT})$ @ T_A °C



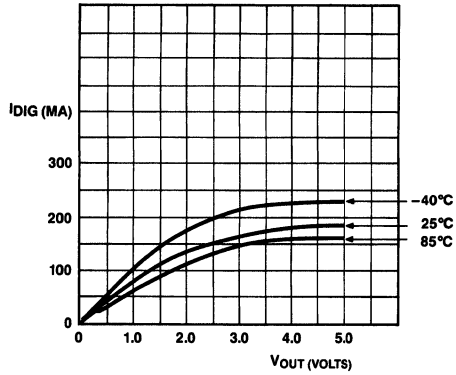
0086-13

Common Cathode Segment Driver
 I_{SEG} vs $(V_{DD}-V_{OUT})$ @ T_A °C



0086-14

Common Anode Segment Driver
 I_{SEG} vs V_{OUT} @ T_A °C



0086-15

Common Cathode Digit Driver
 I_{DIG} vs V_{OUT} @ T_A °C

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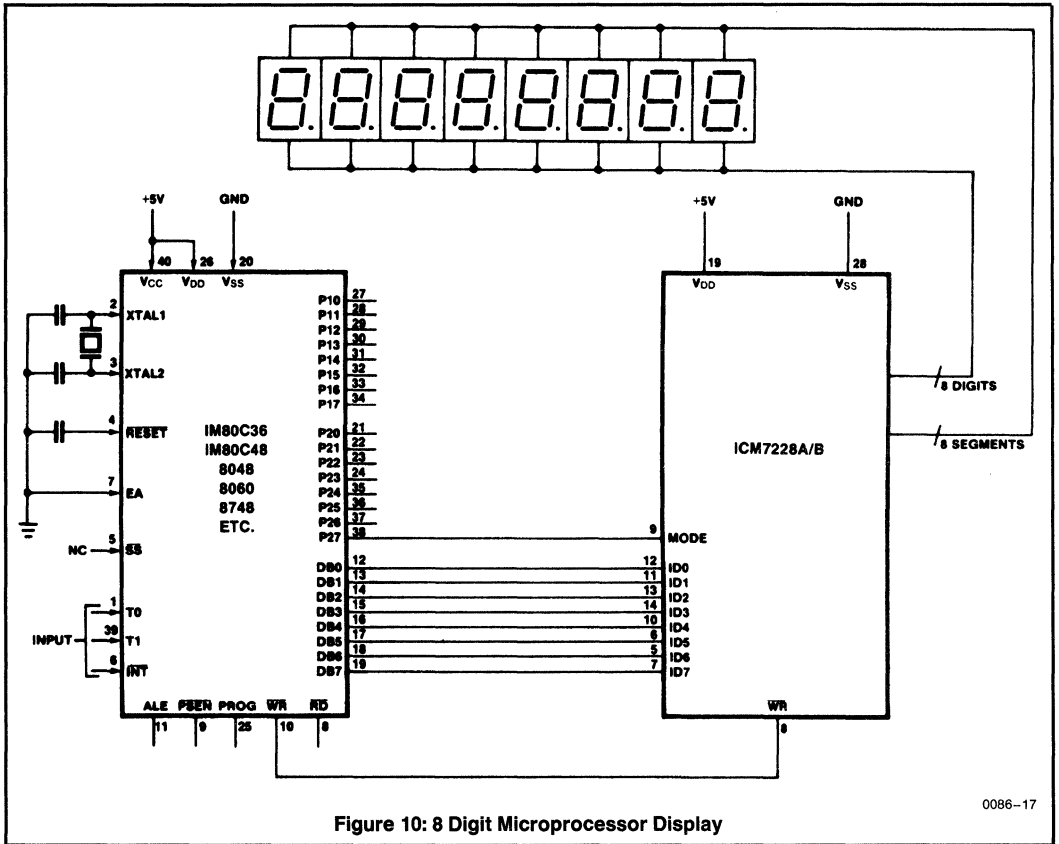


Figure 10: 8 Digit Microprocessor Display

0086-17

APPLICATION EXAMPLES

8 Digit Microprocessor Display Application

Figure 10 shows a display interface using the ICM7228A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7228 display interface on successive WRITE pulses. The MODE input to the 7228 is connected to one of the I/O port pins on the microcontroller. When MODE is high a control word is transferred; when MODE is low data is transferred. Sequential locations in the 8-byte static memory are automatically loaded on each successive WRITE pulse. After eight WRITE pulses have occurred, further pulses are ignored until a new control word is transferred (see Figure 6). This also allows writing to other peripheral devices without disturbing the ICM7228A/B.

16 Digit Microprocessor Display

In this application (see Figure 11), both ICM7228's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7228's simultaneously.

The display digits from both ICM7228's are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7228's from the processor on port lines P26 and P27.

No Decode Application

The ICM7228 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7228 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments x 8 digits = 64 dots ÷ 2 per red or green = 32 channels).

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NOTE: All typical values have been characterized but are not tested.

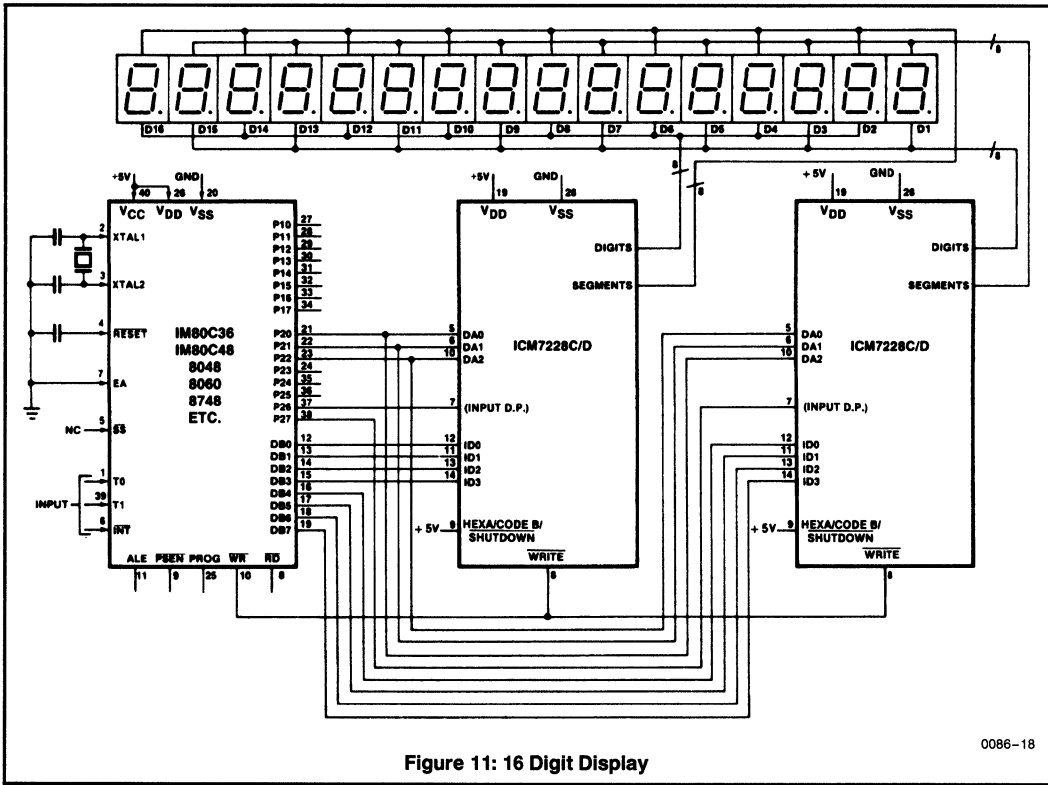


Figure 11: 16 Digit Display

0086-18

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NOTE: All typical values have been characterized but are not tested.

ICM7231-ICM7233

Numeric/Alphanumeric Triplexed LCD Display Driver



GENERAL DESCRIPTION

The ICM7231-7233 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

FEATURES

- **ICM7231: Drives 8 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**
- **ICM7232: Drives 10 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Serial Format**
- **ICM7233: Drives 4 Characters of 18 Segments Address and Data Input in Parallel Format**
- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display Are Provided**
- **Display Voltage Independent of Power Supply**
- **On-Chip Oscillator Provides All Display Timing**
- **Total Power Consumption Typically 200 μ W, Maximum 500 μ W at 5V**
- **Low-Power Shutdown Mode Retains Data With 5 μ W Typical Power Consumption at 5V, 1 μ W at 2V**
- **Direct Interface to High-Speed Microprocessors**

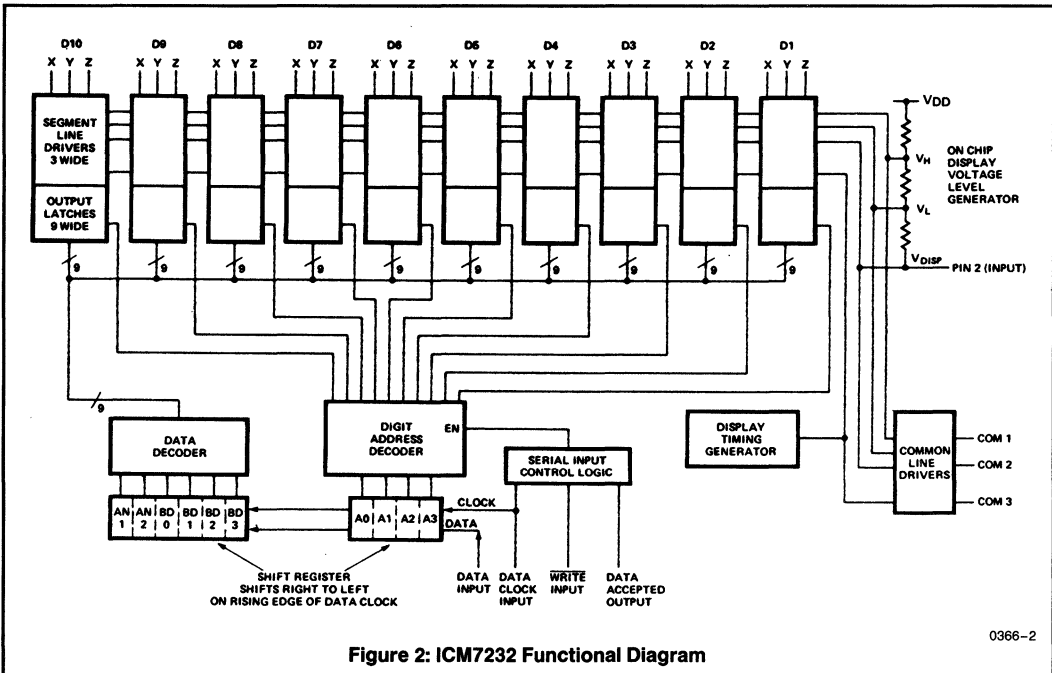
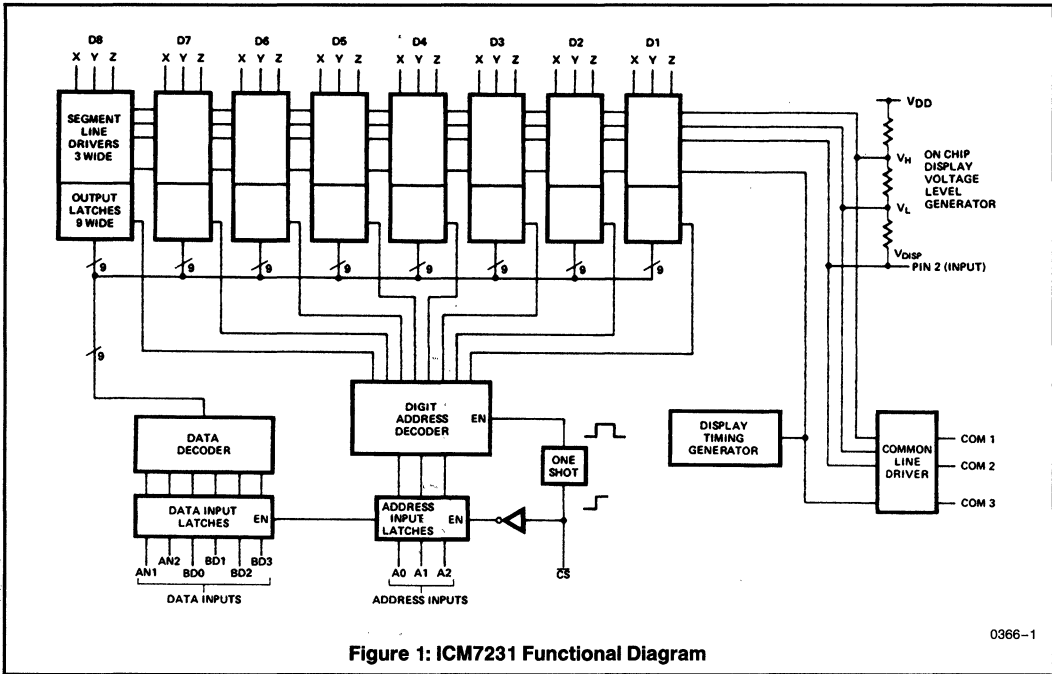
ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7231AFIJL	-25°C to +85°C	40 pin Cerdip
ICM7231AFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7231BFIJL	-25°C to +85°C	40 pin Cerdip
ICM7231BFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7231CFIJL	-25°C to +85°C	40 pin Cerdip
ICM7231CFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7232AFIJL	-25°C to +85°C	40 pin Cerdip
ICM7232AFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7232BFIJL	-25°C to +85°C	40 pin Cerdip
ICM7232BFIPL	-25°C to +85°C	40 pin PLASTIC Dip

Part Number	Temperature Range	Package
ICM7232CRIJL	-25°C to +85°C	40 pin Cerdip
ICM7232CRIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7233AEV/KIT		Evaluation Kit.
ICM7233AFIJL	-25°C to +85°C	40 pin Cerdip
ICM7233AFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7233BFIPL	-25°C to +85°C	40 pin PLASTIC Dip
ICM7233BFIJL	-25°C to +85°C	40 pin Cerdip

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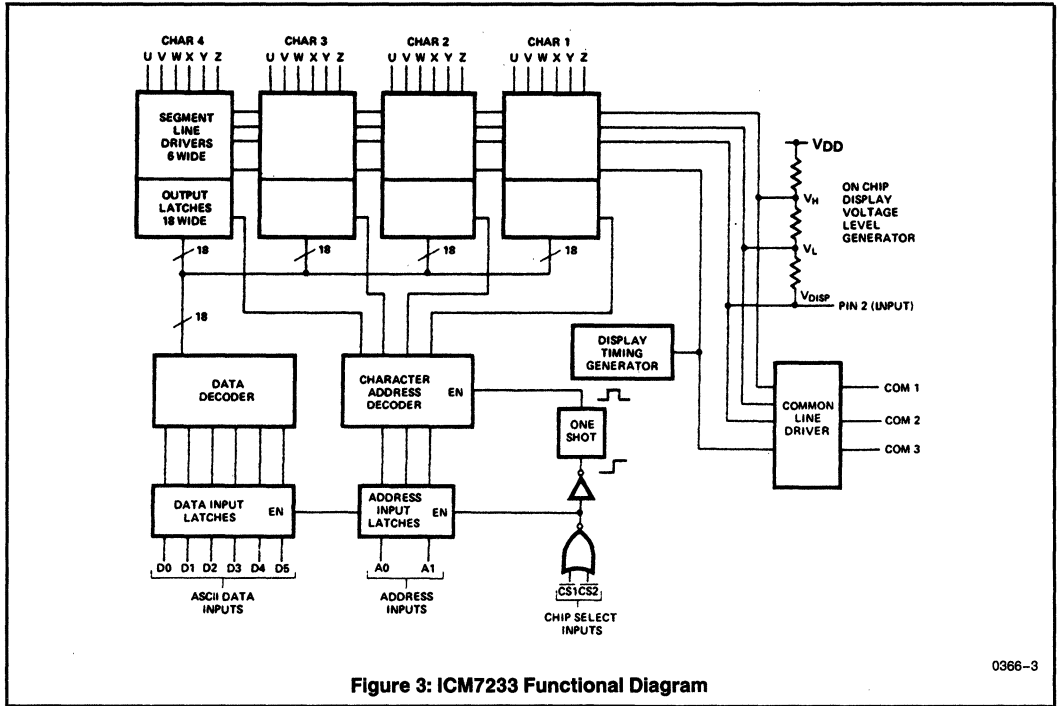


Figure 3: ICM7233 Functional Diagram

0366-3

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NOTE: All typical values have been characterized but are not tested.

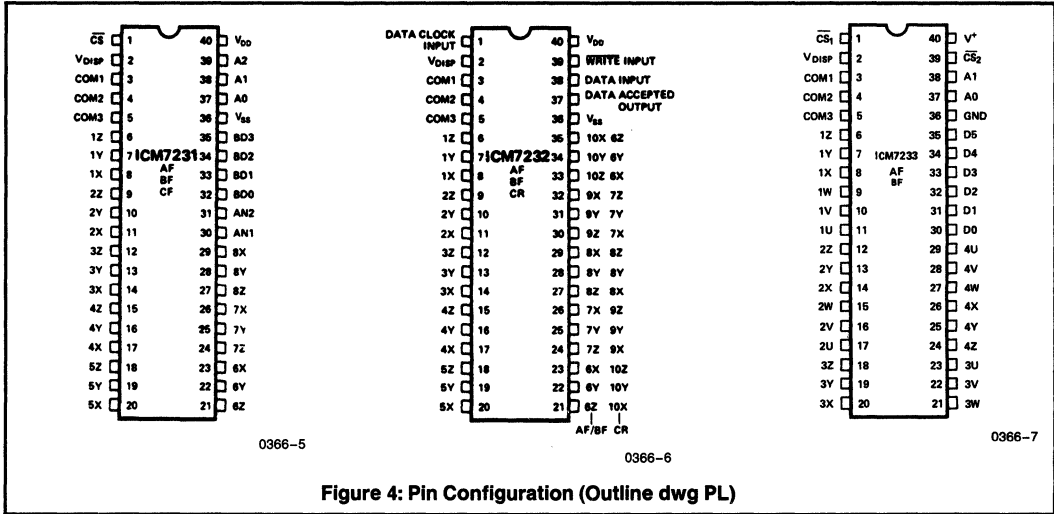
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
 Input Voltage^[2] $V_{SS} - 0.3 \leq V_{IN} \leq 6.5$
 Display Voltage^[2] $-0.3 \leq V_{DISP} \leq +0.3$

Power Dissipation^[1] 0.5W @ 70°C
 Operating Temperature Range -25°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10sec) 300°C

- Notes:** 1. This limit refers to that of the package and will not be obtained during normal operation.
 2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V_{DD} but not more than 6.5 volts above V_{SS} .

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS ($V^+ = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -25^\circ C$ to $+85^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions/Description	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		4.5	>4	5.5	V
V_{DD}	Data Retention Supply Voltage	Guaranteed Retention at 2V	2	1.6		V
I_{DD}	Logic Supply Current	Current from V_{DD} to Ground excluding Display. $V_{DISP} = 2V$		30	100	μA
I_S	Shutdown Total Current	V_{DISP} Pin 2 Open		1	10	μA
V_{DISP}	Display Voltage Range	$V_{SS} \leq V_{DISP} \leq V_{DD}$	0		V_{DD}	V
I_{DISP}	Display Voltage Setup Current	$V_{DISP} = 2V$ Current from V_{DD} to V_{DISP} On-Chip		15	30	μA
R_{DISP}	Display Voltage Setup Resistor Value	One of Three Identical Resistors in String	40	75		k Ω
	DC Component of Display Signals	(Sample Test only)		1/4	1	% ($V_{DD} - V_{DISP}$)
f_{DISP}	Display Frame Rate	See Figure 6	60	90	120	Hz
V_{IL}	Input Low Level	ICM7231, ICM7233 Pins 30-35, 37-39, 1			0.8	V
V_{IH}	Input High Level		2.0			V
I_{ILK}	Input Leakage	ICM7232, Pins 1, 38, 39 (Note 1)		0.1	1	μA
C_{IN}	Input Capacitance			5		pF
V_{OL}	Output Low Level	Pin 37, ICM7232, $I_{OL} = 1mA$,			0.4	V
V_{OH}	Output High Level	$V_{DD} = 4.5V$, $I_{OH} = -500\mu A$	4.1			V
T_{OP}	Operating Temperature Range	Industrial Range	-25		+85	$^\circ C$

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NOTE: All typical values have been characterized but are not tested.

ICM7231-ICM7233



AC CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $-20^{\circ}C \leq T_A \leq +85^{\circ}C$)

PARALLEL INPUT (ICM7231, ICM7233) See Figure 14

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{cs}	Chip Select Pulse Width	(Note 1)	500	350		ns
t_{ds}	Address/Data Setup Time	(Note 1)	200			ns
t_{dh}	Address/Data Hold Time	(Note 1)	0	-20		ns
t_{ics}	Inter-Chip Select Time	(Note 1)	3			μs

SERIAL INPUT (ICM7232) See Figures 15, 16

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{cl}	Data Clock Low Time	(Note 1)	350			ns
t_{ch}	Data Clock High Time	(Note 1)	350			ns
t_{ds}	Data Setup Time	(Note 1)	200			ns
t_{dh}	Data Hold Time	(Note 1)	0	-20		ns
t_{wp}	Write Pulse Width	(Note 1)	500	350		ns
t_{wll}	Write Pulse to Clock at Initialization	(Note 1)	1.5			μs
t_{odl}	Data Accepted Low Output Delay	(Note 1)		200	400	ns
t_{odh}	Data Accepted High Output Delay	(Note 1)		1.5	3	μs
t_{cws}	Write Delay After Last Clock	(Note 1)	350			ns

NOTE 1: For design reference only, not 100% tested.

TABLE OF FEATURES

Type Number	Output Code	Annunciator Locations	Input	Output
ICM7231AF	Hexadecimal	Both Annunciators on COM3	Parallel Entry 4 bit Data	8 Digits plus 16 Annunciators
ICM7231BF	Code B		2 bit Annunciators	
ICM7231CF	Code B	1 Annunciator COM1 1 Annunciator COM3	3 bit Address	
ICM7232AF	Hexadecimal	Both Annunciators on COM3	Serial Entry 4 bit Data	10 Digits plus 20 Annunciators
ICM7232B	Code B		2 bit Annunciators	
ICM7232CR	Code B	1 Annunciator COM1 1 Annunciator COM3	4 bit Address	
ICM7233AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7233BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters

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NOTE: All typical values have been characterized but are not tested.

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

Terminal	Pin No.	Description	Function
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant } 4 Bit Binary Data Inputs Most Significant }	Input Data (See Table 1) HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant } 3 Bit Digit Address Inputs Most Significant }	
\overline{CS}	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit

NOTE: 3. \overline{CS} has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

ICM7233 PARALLEL INPUT ALPHA DISPLAY

Terminal	Pin No.	Description	Function
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant } 6 Bit (ASCII) Data Inputs Most Significant }	Input Data See Table 4 HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1	37 38	Least Significant } Address Inputs Most Significant }	
$\overline{CS1}$ $\overline{CS2}$	39 1	Chip Select Inputs (Note 4)	Both inputs LOW load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.

NOTE 4: $\overline{CS1}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided either by pulling it high when inactive, or ensuring frequent activity.

ICM7232 SERIAL DATA AND ADDRESS INPUT

Terminal	Pin No.	Description	Function
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
WRITE Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of WRITE triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits

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NOTE: All typical values have been characterized but are not tested.

ALL DEVICES

Terminal	Pin No.	Description	Function
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V_{DD} chip is shutdown; oscillator stops, all display pins to V_{DD}).
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On ICM7231/33) (On ICM7232)	Drive display segments, or columns.
V_{DD}	40	Chip Positive Supply	
V_{SS}	36	Chip Negative Supply	

ICM7231 FAMILY DESCRIPTION

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits.

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

The ICM7233 has a parallel input structure similar to the ICM7231, but the decoding and the outputs are organized to drive four 18-segment alphanumeric characters. The six data bits represent a 6-bit ASCII code.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Intersil's MAXCMOS® process and all inputs are protected against static discharge.

TRIPLEXED (1/3 MULTIPLEXED) LIQUID CRYSTAL DISPLAYS

Figure 5 shows the connection diagram for a typical 7-segment display font with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 6 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "Y" segment line. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Figure 6 also shows the waveform of the "Y" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 7. Figure 8 shows the voltage across the "g" seg-

ment for the same four combinations of ON/OFF segments in Figure 6.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 8 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always $1.92 V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 9 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7233 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V_{DD} and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V_{DD} - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below V_{SS} . This can cause device latch up and destruction of the chip.

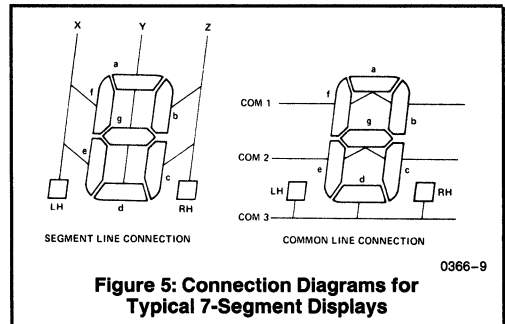
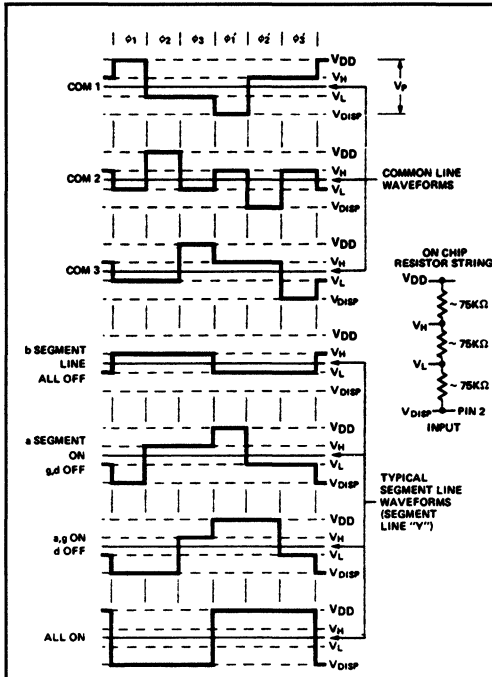


Figure 5: Connection Diagrams for Typical 7-Segment Displays

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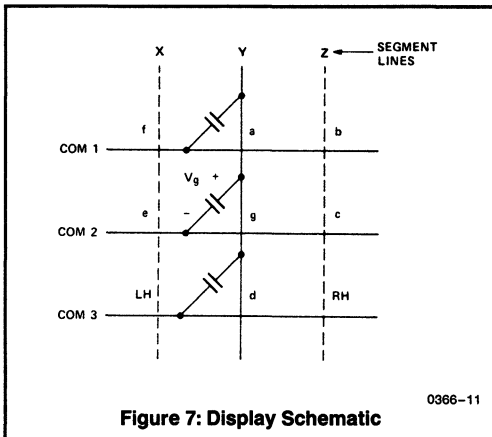
NOTE: All typical values have been characterized but are not tested.



0366-10

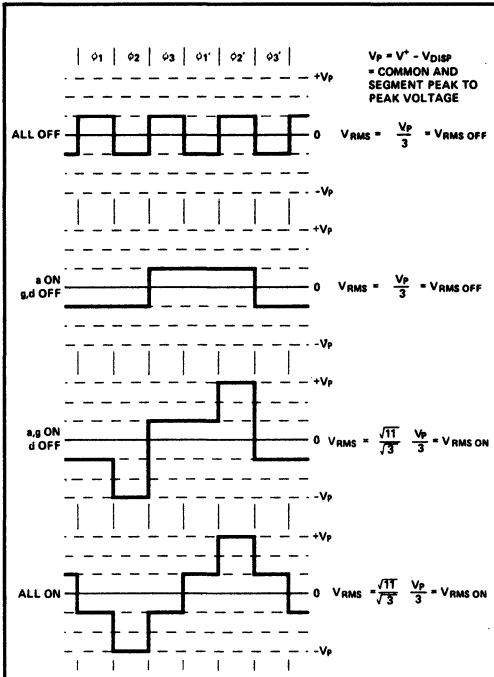
Figure 6: Display Voltage Waveforms

NOTE: ϕ_1, ϕ_2, ϕ_3 - COMMON HIGH WITH RESPECT TO SEGMENT.
 $\phi_1', \phi_2', \phi_3'$ - COMMON LOW WITH RESPECT TO SEGMENT.
 COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'
 COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'
 COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'



0366-11

Figure 7: Display Schematic



0366-12

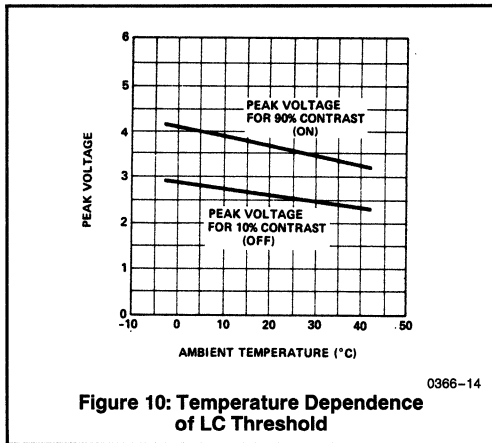
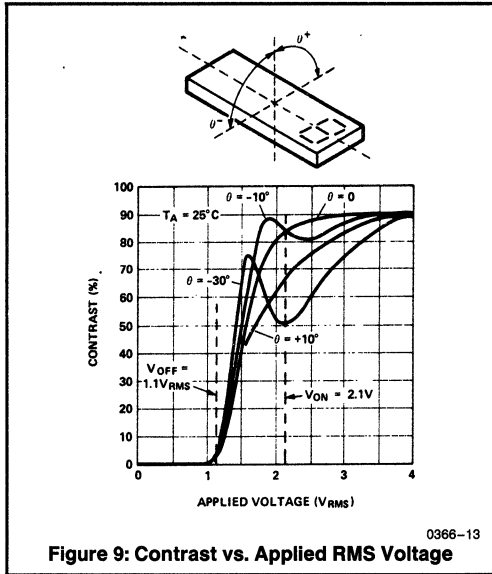
Figure 8: Voltage Waveforms on Segment g(Vg)

$$\text{VOLTAGE CONTRAST RATIO} = \frac{V_{RMS\ ON}}{V_{RMS\ OFF}} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$$

NOTE: ϕ_1, ϕ_2, ϕ_3 - COMMON HIGH WITH RESPECT TO SEGMENT.
 $\phi_1', \phi_2', \phi_3'$ - COMMON LOW WITH RESPECT TO SEGMENT.
 COM 1 ACTIVE DURING ϕ_1 AND ϕ_1'
 COM 2 ACTIVE DURING ϕ_2 AND ϕ_2'
 COM 3 ACTIVE DURING ϕ_3 AND ϕ_3'

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NOTE: All typical values have been characterized but are not tested.



TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer.

Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

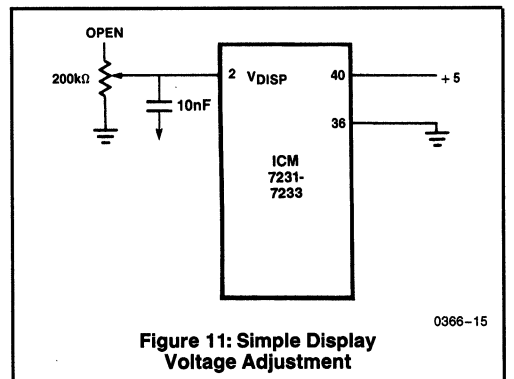
A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_p , when the threshold voltage drops below $V_p/3$ OFF segments begin to be visible. Figure 10 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 9.

For applications where the display temperature does not vary widely, V_p may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_p/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_p) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to V_{SS} as shown in Figure 11. A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.



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NOTE: All typical values have been characterized but are not tested.

Figure 12(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20 μ A flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 9 and 10. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of -2 mV/ $^{\circ}$ C; five in series gives -10 mV/ $^{\circ}$ C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 12(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about -2 mV/ $^{\circ}$ C) is also multiplied. The transistor should have a beta of at least 100 with a collector current of 10 μ A. The inexpensive 2N2222 shown in the figure is a suitable device.

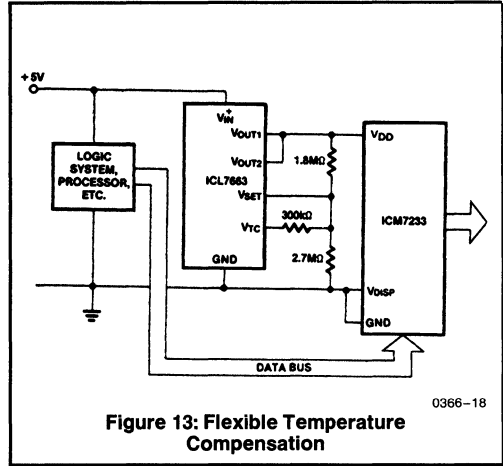


Figure 13: Flexible Temperature Compensation

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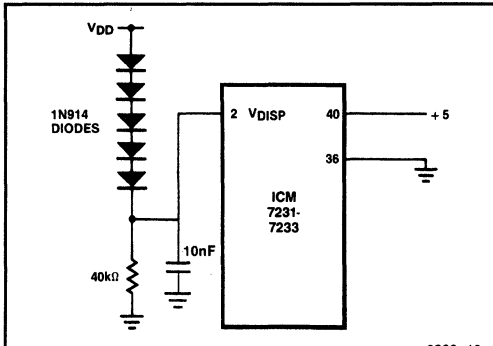


Figure 12(a): String of Diodes

0366-16

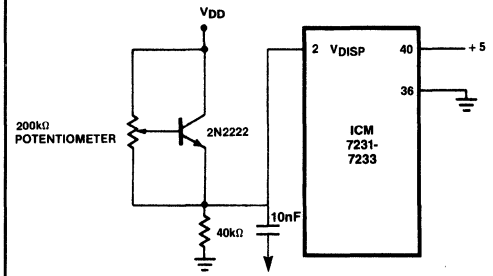


Figure 12(b): Transistor-Multiplier

0366-17

Figure 12: Diode-based Temperature Compensation

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NOTE: All typical values have been characterized but are not tested.

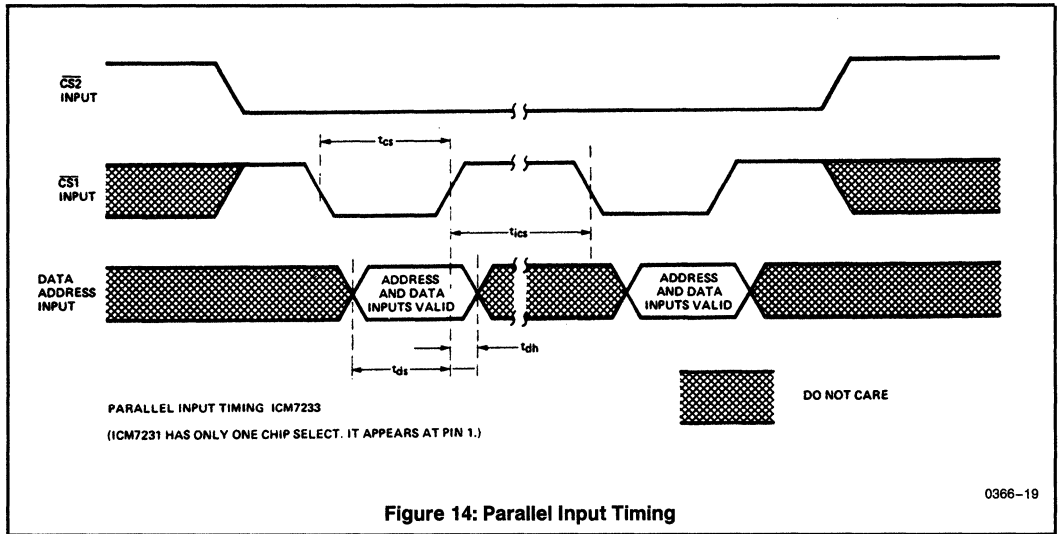


Figure 14: Parallel Input Timing

0366-19

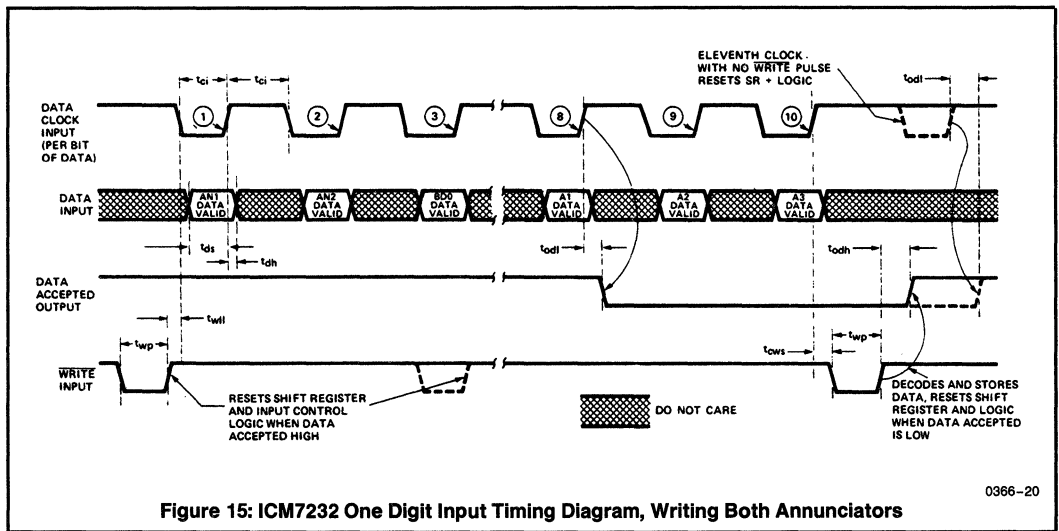


Figure 15: ICM7232 One Digit Input Timing Diagram, Writing Both Annunciators

0366-20

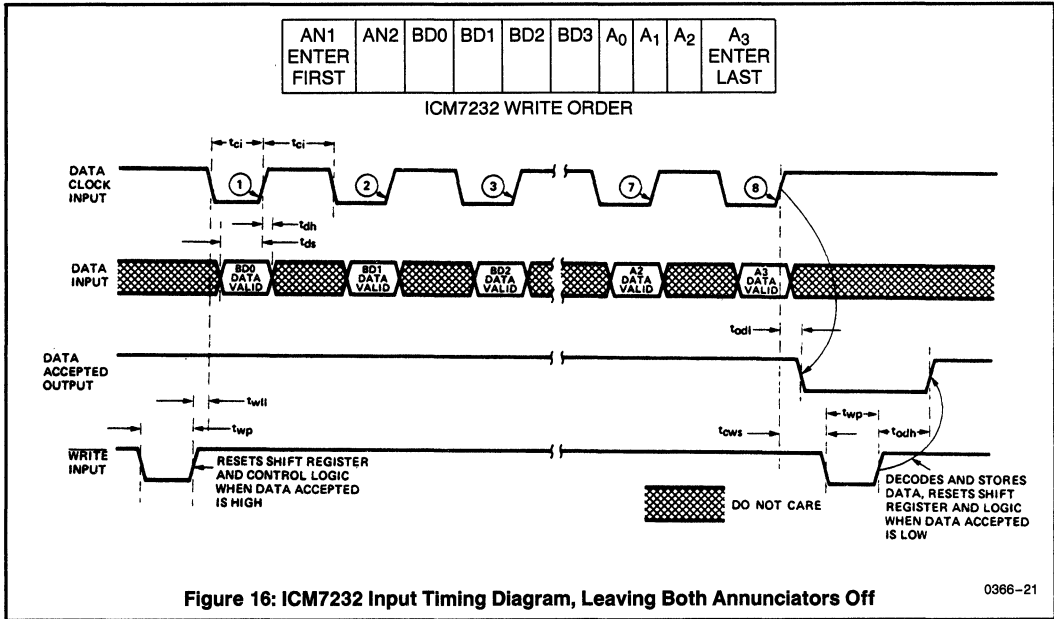
For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to V_{SS} . The inputs of the chip are designed such that they may be driven above V_{DD} without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663, as shown in Figure 13. This circuit allows independent adjustment of both voltage and temperature compensation.

DESCRIPTION OF OPERATION PARALLEL INPUT OF DATA AND ADDRESS (ICM7231, ICM7233)

The parallel input structure of the ICM7231 and ICM7233 devices is organized to allow simple, direct interfacing to all microprocessors, (see functional diagrams Figures 1 and 3). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input. In the ICM7233, the two Chip Selects are equivalent; when both are low, the latches are transparent and the data is latched on the rising edge of either Chip Select.

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NOTE: All typical values have been characterized but are not tested.



The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input devices are shown in Figure 14, with the values for setup, hold, and pulse width times shown in the AC Characteristics section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

SERIAL INPUT OF DATA AND ADDRESS (ICM7232)

The ICM7232 trades six pins used as data inputs on the ICM7231 and ICM7233 for six more segment lines, allowing two more 9-segment digits. This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to functional diagram, Figure 2 and timing diagrams, Figures 15 and 16. The interface consists of four pins: DATA Input, DATA CLOCK Input, WRITE Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the WRITE input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the WRITE input will not

change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 15. First, when DATA ACCEPTED is high, send a WRITE pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at WRITE will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 16.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

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NOTE: All typical values have been characterized but are not tested.

ICM7231-ICM7233



The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a WRITE pulse, none of the outputs will be changed.

DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on COM3. The display connections for one digit of this display are shown in Figure 17. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on COM1 (AN2) and the right hand annunciator (usually a decimal point) on COM3 (AN1). (See Figure 18). The "C" devices provide only a "Code B" output for the 7-segments.

The ICM7233 is supplied in "A" and "B" versions. Both versions decode an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and two "dots". The "A" devices have numbers which are half width and the "B" devices have full width numbers. The layout for a single character is shown in Figure 19 with output decoding shown in Table 4.

TABLE 1. BINARY DATA DECODING (ICM7231/32)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	c	H
1	1	0	1	d	L
1	1	1	0	e	P
1	1	1	1	F	BLANK

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TABLE 2. ADDRESS DECODING (ICM7231/32)

Code Input				Display Output
ICM7232 Only A3	A2	A1	A0	Digit Selected
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON COM 3	ICM7231C ICM7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0	8	8
0	1	8	8
1	0	8	8
1	1	8	8

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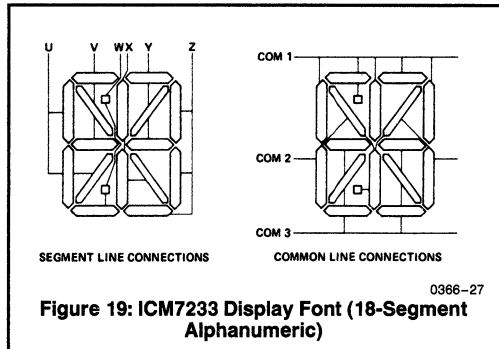
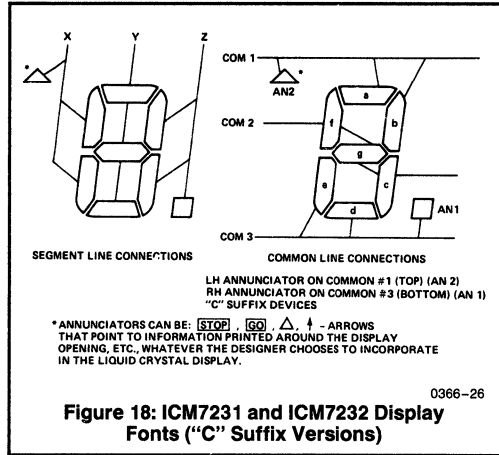
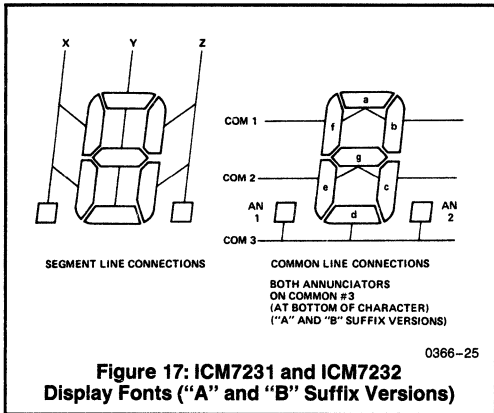
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NOTE: All typical values have been characterized but are not tested.

EVALUATION KITS

After purchasing a sample of the ICM7231/32/33, the majority of users will want to build a sample display. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering kits which contain all the necessary components to build 8 character displays. With the help of such a kit, an engineer or technician can have the system "up and running" in about half an hour.

The ICM7233EV/KIT contains the appropriate ICs, a circuit board, a Multiplexed LCD display 16/18 segment, passive components, and miscellaneous hardware.



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ICM7231-ICM7233



COMPATIBLE DISPLAYS

Compatible displays are manufactured by:
 G.E. Displays Inc., Beechwood, Ohio
 (216)831-8100 (#356E3R99HJ)
 Epson America Inc., Torrance CA
 (Model Numbers LDB726/7/8).
 Seiko Instruments USA Inc., Torrance CA
 (Custom Displays)
 Crystaloid, Hudson, OH

TABLE 4. DATA DECODING 6-BIT ASCII → 18 SEGMENT (ICM7233)

CODE INPUT				DISPLAY OUTPUT			
D3	D2	D1	D0	0,0	0,1	1,0	1,1
0	0	0	0	P	P		00
0	0	0	1	A	Q	!	11
0	0	1	0	B	R	"	22
0	0	1	1	C	S	£	33
0	1	0	0	J	T	\$	44
0	1	0	1	E	U	%	55
0	1	1	0	F	V	¢	66
0	1	1	1	G	W	'	77
1	0	0	0	H	X	<	88
1	0	0	1	I	Y	>	99
1	0	1	0	J	Z	*	:
1	0	1	1	K	[+	;
1	1	0	0	L	\	,	ˆ
1	1	0	1	M]	-	=
1	1	1	0	N	^	.	˜
1	1	1	1	O	ˆ	/	ˇ

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TABLE 5. ADDRESS DECODING (ICM7233)

Code Input		Digit Selected
A1	A0	
0	0	D1
0	1	D2
1	0	D3
1	1	D4
0	0	D5
0	1	NONE
1	0	NONE
1	1	NONE

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TYPICAL APPLICATIONS

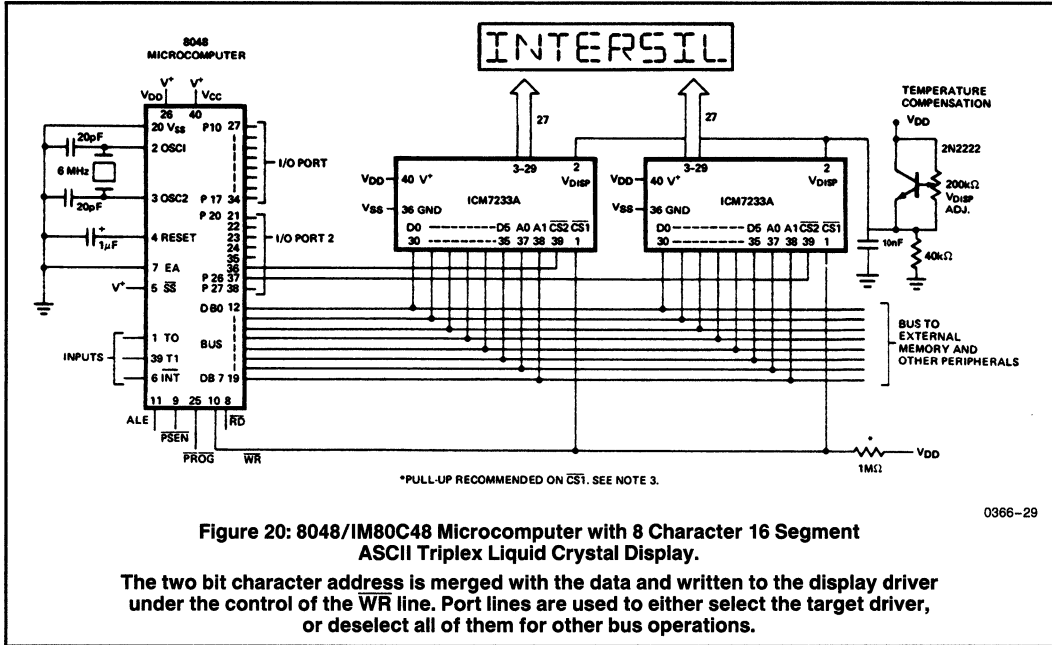


Figure 20: 8048/IM80C48 Microcomputer with 8 Character 16 Segment ASCII Triplex Liquid Crystal Display.

The two bit character address is merged with the data and written to the display driver under the control of the WR line. Port lines are used to either select the target driver, or deselect all of them for other bus operations.

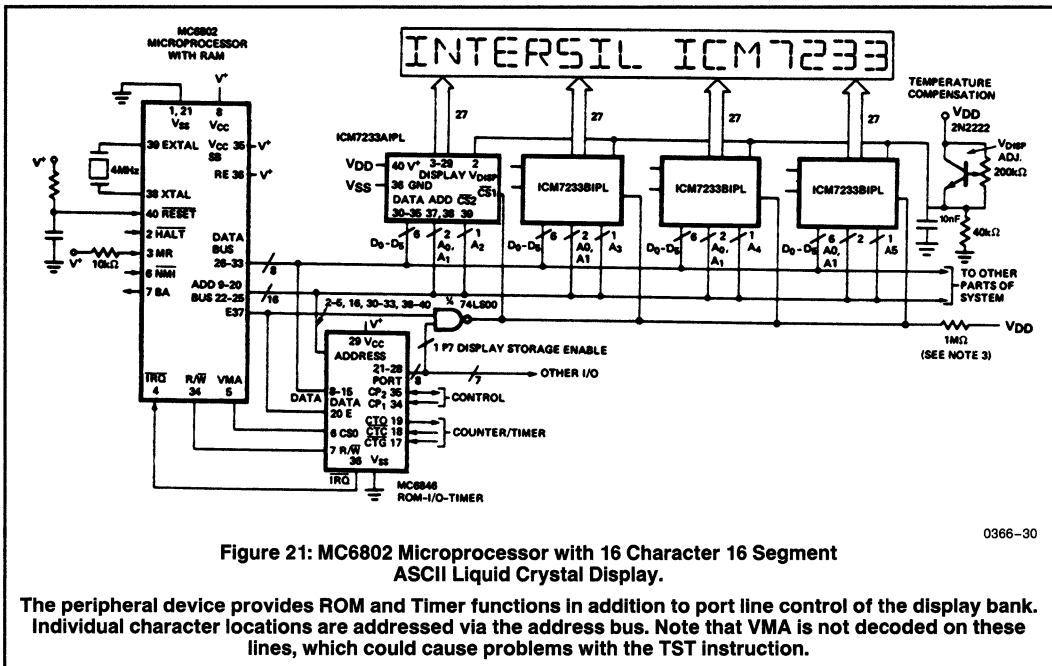
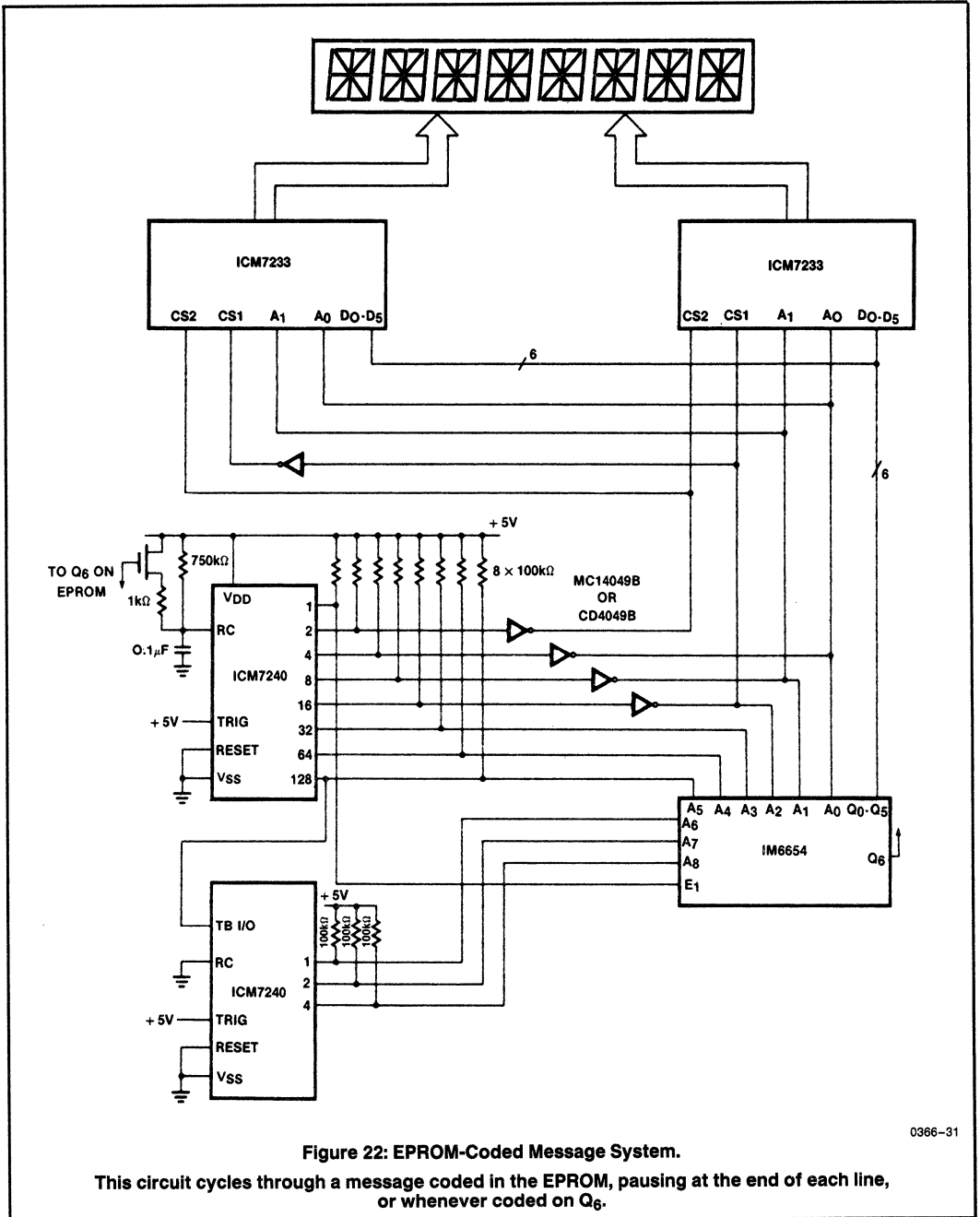


Figure 21: MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

The peripheral device provides ROM and Timer functions in addition to port line control of the display bank. Individual character locations are addressed by the address bus. Note that VMA is not decoded on these lines, which could cause problems with the TST instruction.

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NOTE: All typical values have been characterized but are not tested.

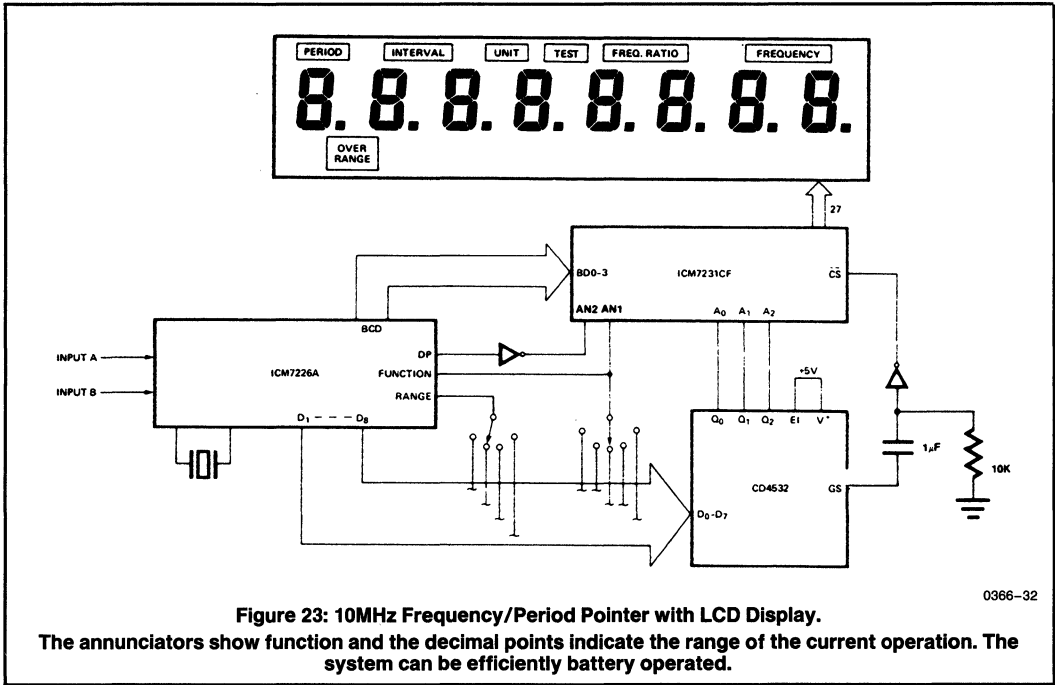


Figure 23: 10MHz Frequency/Period Pointer with LCD Display.

The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.

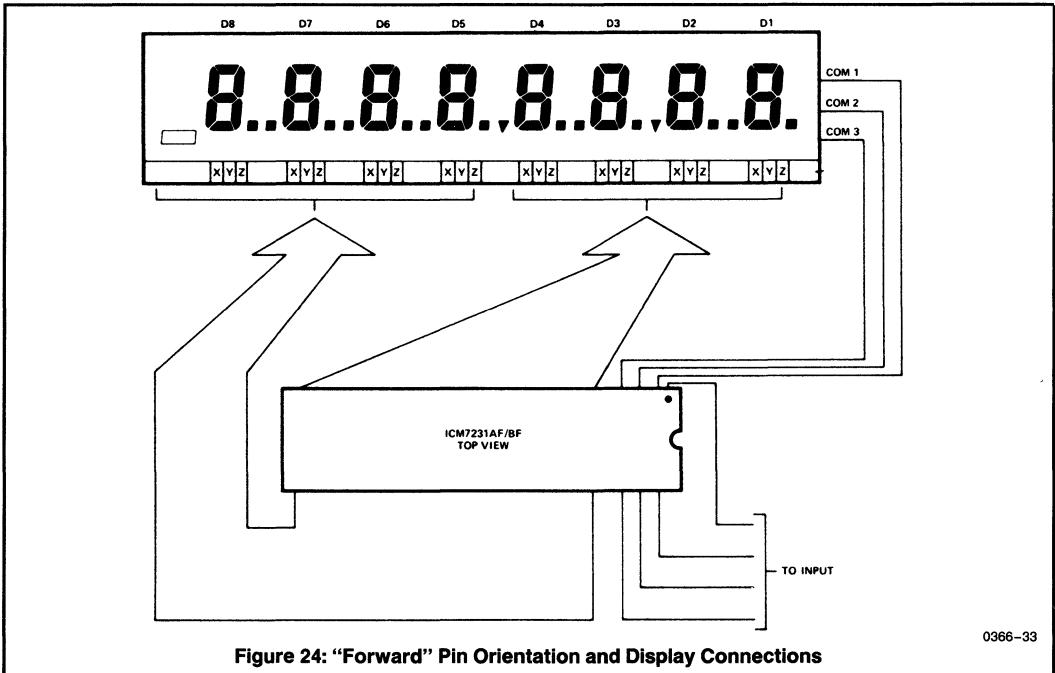
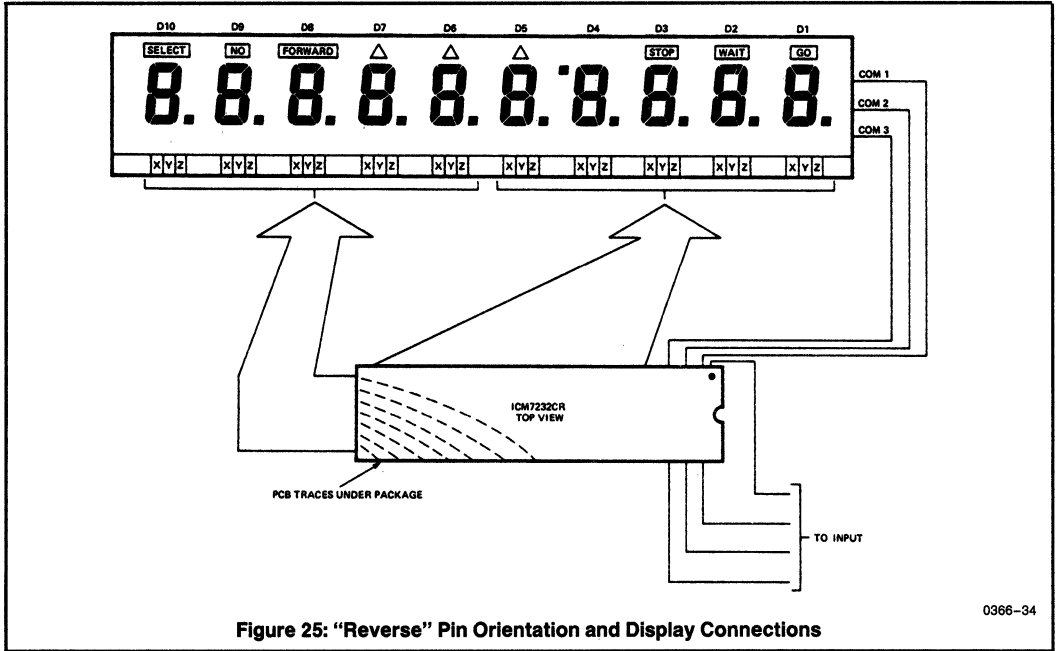


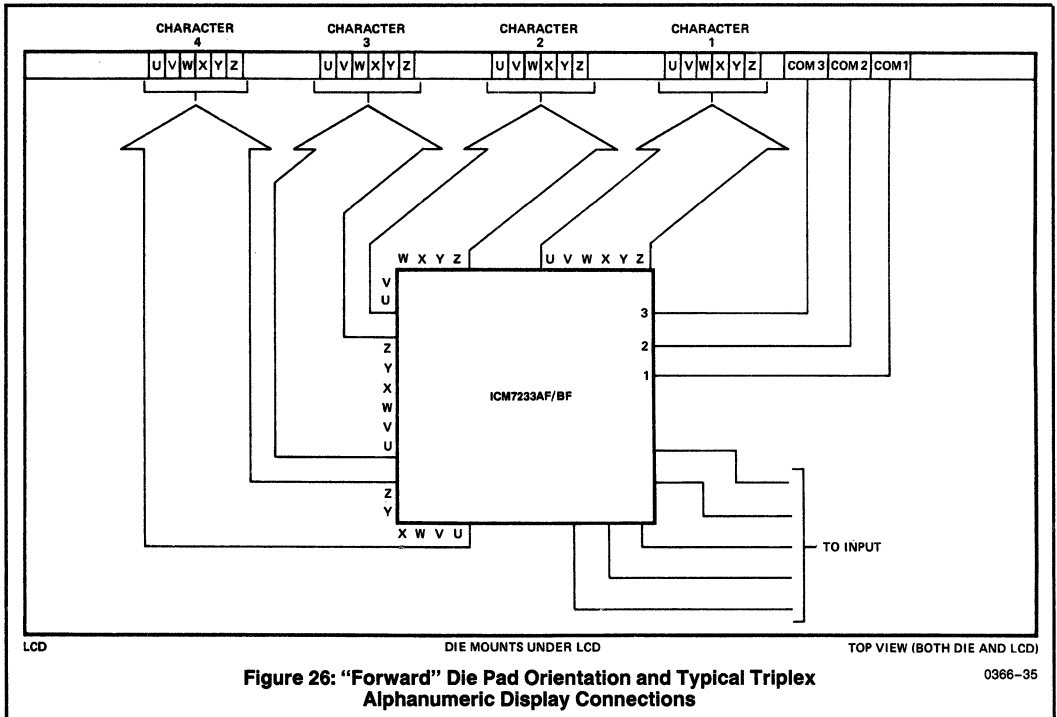
Figure 24: "Forward" Pin Orientation and Display Connections

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

ICM7243

8-Character LED

μ P-Compatible Display Driver



ICM7243

GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8x6 memory, high power character and segment drivers, and the multiplex scan circuitry.

Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Serial** (MODE=1) or **Random** (MODE=0). In the **Serial Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPLAY FULL signal is provided after 8 entries; this signal can be used for cascading. A CLEAR pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

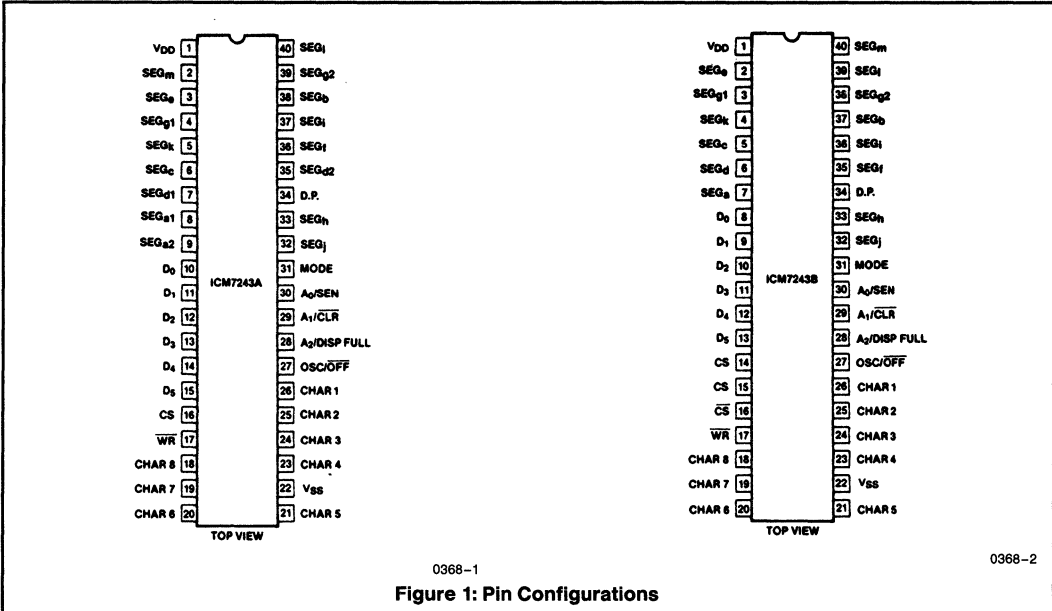
The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARACTER drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

FEATURES

- 14- and 16-Segment Fonts With Decimal Point
- Mask Programmable For Other Font-Sets Up to 64 Characters
- Microprocessor Compatible
- Directly Drives Small Common Cathode Displays
- Cascadable Without Additional Hardware
- Standby Feature Turns Display Off; Puts Chip in Low Power Mode
- Serial Entry or Random Entry of Data Into Display
- Single +5V Operation
- Character and Segment Drivers, All MUX Scan Circuitry, 8x6 Static Memory and 64-Character ASCII Font Generator Included On-Chip

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7243AIJL	-20°C to +85°C	CERDIP
ICM7243BIJL	-20°C to +85°C	CERDIP
ICM7243B EV/KIT		
ICM7243AIPL	-20°C to +85°C	PLASTIC
ICM7243BIPL	-20°C to +85°C	PLASTIC



0368-1
Figure 1: Pin Configurations

0368-2

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
 CHARACTER Output Current 300mA
 SEGMENT Output Current 30mA
 Input Voltage (Any Terminal) .. ($V_{DD} + 0.3V$) to ($V_{SS} - 0.3V$)
 Power Dissipation 1W

Operating Temperature Range (I) -25°C to +85°C
 Storage Temperature Range -55°C to +125°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

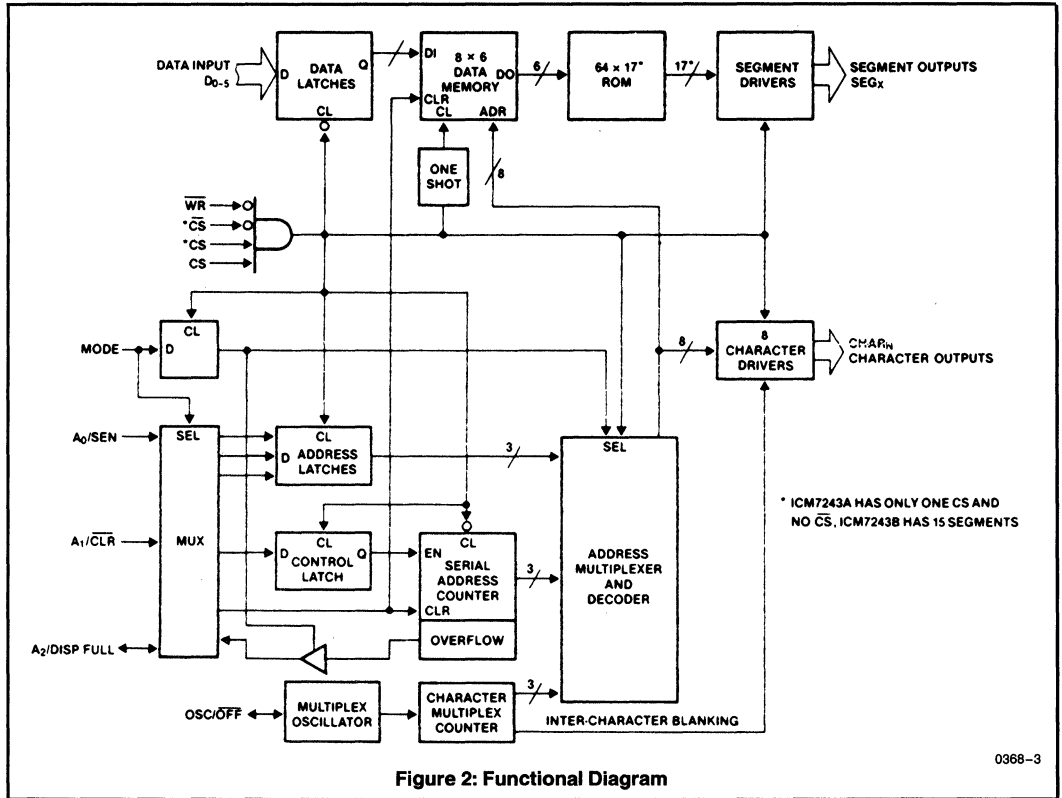


Figure 2: Functional Diagram

DC ELECTRICAL CHARACTERISTICS ($V_{DD} = 5V, V_{SS} = 0V, T_A = 25^\circ C$ unless otherwise stated)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{SUPP}	Supply Voltage ($V_{DD} - V_{SS}$)		4.75	5.0	5.25	V
I_{DD}	Operating Supply Current	$V_{SUPP} = 5.25V, 10$ Segments ON, All 8 Characters		180		mA
I_{STBY}	Quiescent Supply Current	$V_{SUPP} = 5.25V, OSC/OFF$ Pin < 0.5V, $CS = V_{SS}$		30	250	μA
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current		-10		+10	μA

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NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C unless otherwise stated)

(Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I _{CHAR}	CHARacter Drive Current	V _{SUPP} = 5V, V _{OUT} = 1V	140	190		mA
I _{CHLK}	CHARacter Leakage Current				100	μA
I _{SEG}	SEGment Drive Current	V _{SUPP} = 5V, V _{OUT} = 2.5V	14	19		mA
I _{SLK}	SEGment Leakage Current			0.01	10	μA
V _{OL}	DISPlay FULL Output Low	I _{OL} = 1.6mA			0.4	V
V _{OH}	DISPlay FULL Output High	I _{IH} = 100μA	2.4			V
f _{ds}	Display Scan Rate			400		Hz

AC ELECTRICAL CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V.

V_{DD} = 5V, T_A = 25°C unless otherwise stated).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t _{WPI}	WR, CLeaR Pulse Width Low		300	250		ns
t _{WPH}	WR, CLeaR Pulse Width High (Note 1)			250		
t _{DH}	Data Hold Time		0	-100		
t _{DS}	Data Setup Time		250	150		
t _{AH}	Address Hold Time		125			
t _{AS}	Address Setup Time		40	15		
t _{CS}	CS, CS Setup Time		0			
t _T	Pulse Transition Time				100	
t _{SEN}	SEN Setup Time		0	-25		
t _{WDF}	Display Full Delay		700	480		

CAPACITANCE

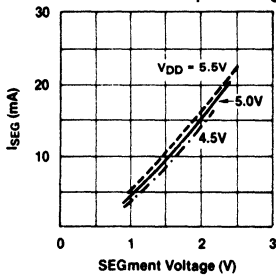
Symbol	Test	Min	Typ	Max	Units
C _{IN}	Input Capacitance (Note 2)		5		pF
C _O	Output Capacitance (Note 2)		5		pF

NOTES: 1. In Serial mode WR high must be ≥ T_{SEN} + T_{WDF}.
 2. For design reference only, not 100% tested.

*Not tested. (Guaranteed)

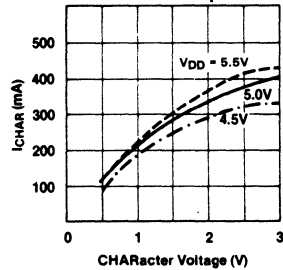
TYPICAL PERFORMANCE CHARACTERISTICS

SEGment Current vs Output Voltage



0368-4

CHARacter Current vs Output Voltage



0368-5

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NOTE: All typical values have been characterized but are not tested.

ICM7243A/B DISPLAY FONT AND SEGMENT ASSIGNMENTS

Note: Some display manufacturers use different designations for some of the segments. Check data sheets carefully.

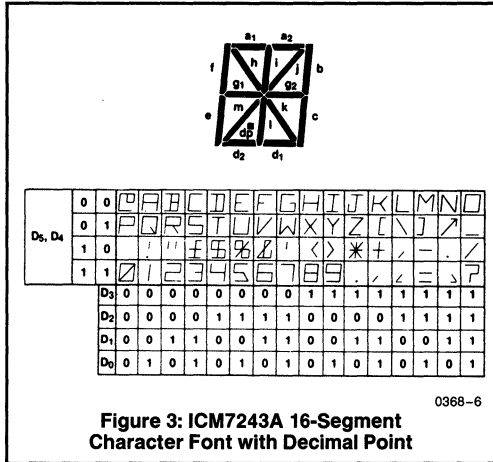


Figure 3: ICM7243A 16-Segment Character Font with Decimal Point

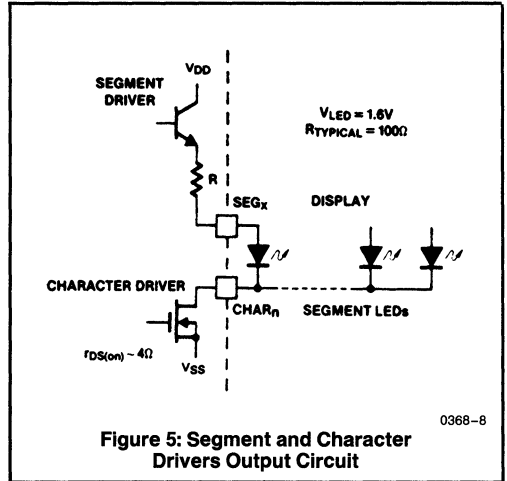
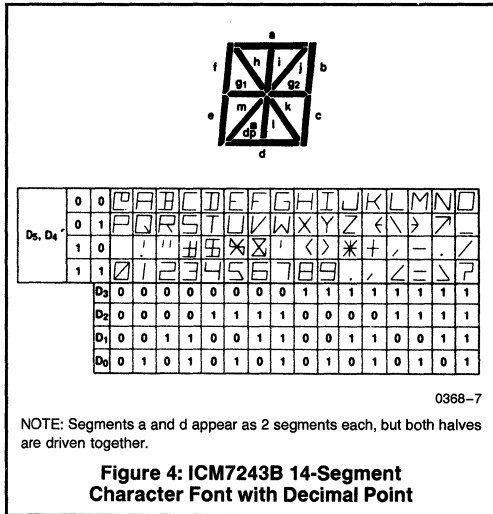


Figure 5: Segment and Character Drivers Output Circuit



NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

Figure 4: ICM7243B 14-Segment Character Font with Decimal Point

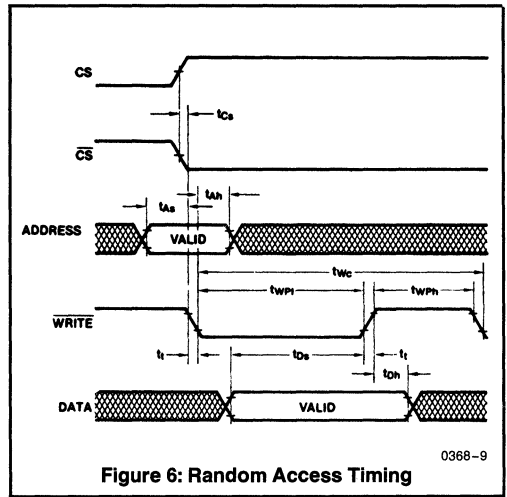


Figure 6: Random Access Timing

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NOTE: All typical values have been characterized but are not tested.

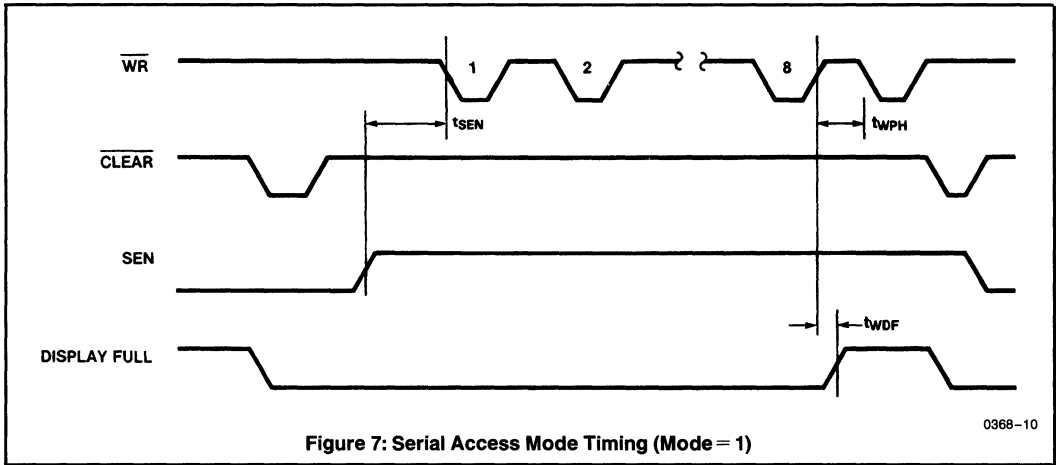


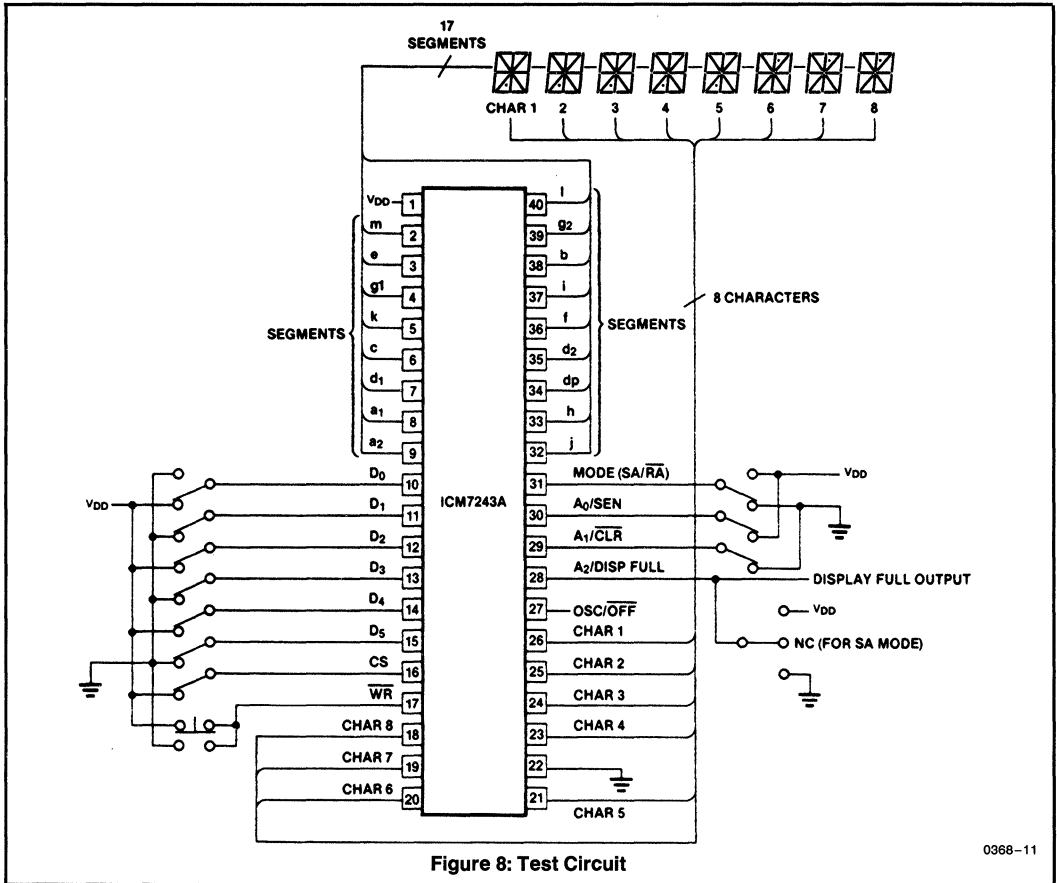
Figure 7: Serial Access Mode Timing (Mode = 1)

TABLE 1: PIN DESCRIPTIONS, ICM7243A(B)

Signal	Pin	Function
D ₀ - D ₅	10 - 15 (8 - 13)	Six-Bit ASCII Data input pins (active high).
CS, \overline{CS}	16 (14 - 16)	Chip Select for decoding from μ P address bus, etc.
\overline{WR}	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and \overline{WR} can be used as \overline{CS} .
MODE	31	Selects data entry MODE. High selects Serial Access (SA) mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the Random Access (RA) mode where data is displayed on the character addressed via A ₀ -A ₂ Address pins.
A ₀ /SEN	30	In RA mode it is the LSB of the character Address. In SA mode it is used for cascading display driver/controllers for displays of more than 8 characters (active high enables driver controller).
A ₁ / \overline{CLEAR}	29	In RA mode this is the second bit of the address. In SA mode, a low input will CLEAR the Serial Address Counter, the Data Memory and the display.
A ₂ /DISPlay FULL	28	In RA mode this is the MSB of the Address. In SA mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/ \overline{OFF}	27	OSCillator input pin. Adding capacitance to V _{DD} will lower the internal oscillator frequency. An external oscillator is also applied to this pin. A low puts the display controller/driver into a quiescent mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG _a - SEG _m , D.P.	2 - 9 (7), 32 - 40	SEGment driver outputs.
CHARacter 1 - 8	18 - 21, 23 - 26	CHARacter driver outputs.

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NOTE: All typical values have been characterized but are not tested.



0368-11

DETAILED DESCRIPTION

WR, CS, CS. These pins are immediately functionally ANDed, so all actions described as occurring on an edge of WR, with CS and CS enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5ns) greater than from WR or CS due to the additional inverter required on the former.

MODE. The MODE pin input is latched on the falling edge of WR (or its equivalent, see above). The location in Data Memory where incoming data will be placed is determined either from the Address pins or the Serial Address Counter, under control of this latch, which also controls the function of A0/SEN, A1/CLR, and A2/DISPLAY FULL.

Random Access Mode. When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A0, A1 and A2 will be latched by the falling

edge of WR (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by WR.

Serial Access Mode. If the internal latch is set for **Serial Access (SA)**, (MODE latched high), the Serial ENable input on SEN will be latched on the falling edge of WR (or its equivalent). The CLR input is asynchronous, and will force-clear the Serial Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPLAY FULL output is always active in SA mode also, and indicates the overflow status of the Serial Address Counter. If this output is low, and SEN is (latched as) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of WR. If SEN is low, or DISPLAY FULL is high, no action will occur. This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Serial Access** mode.

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NOTE: All typical values have been characterized but are not tested.

Changing Modes. Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of \overline{WR} (or its equivalent). When changing mode from **Serial Access** to **Random Access**, note that $A_2/\text{DISP FULL}$ will be an output until \overline{WR} has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Serial Access**, $A_1/\overline{\text{CLR}}$ should be high to avoid inadvertent clearing of the Data Memory and Serial Address Counter. DISP FULL will become active immediately after the falling edge of \overline{WR} .

Data Entry. The input Data is latched on the rising edge of \overline{WR} (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the \overline{WR} input.

OSC/OFF. The device includes a one-pin relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V_{DD} at the OSC/OFF pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARACTER strobe lines (see **Display Output**). An intercharacter blanking signal is derived from the pre-divider. An additional comparator on the OSC/OFF input detects a level lower than the relaxation oscillator's range, and

blanks the display, disables the DISP FULL output (if active), and clears the pre-divider and Multiplex Counter. This puts the circuit in a low-power-dissipation mode in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output. The address output of the Multiplex Counter is multiplexed into the address input of the Data Memory, except during \overline{WR} operations (in **Serial Access** mode, with SEN high and DISP FULL low), to control display operations. The address decoder also drives the CHARACTER outputs, except during the inter-character blanking interval (nominally about $5\mu\text{s}$). Each CHARACTER output lasts nominally about $300\mu\text{s}$, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARACTER and SEGment outputs are disabled during \overline{WR} operations (with SEN high and DISP FULL Low for **Serial Access** mode). The outputs may also be disabled by pulling OSC/OFF low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

APPLICATIONS

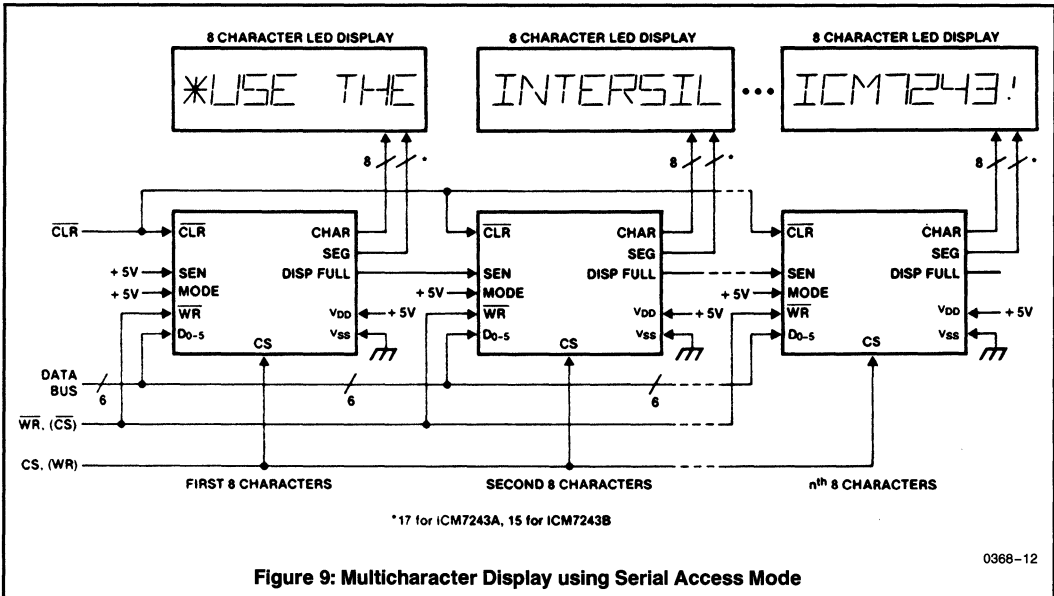


Figure 9: Multicharacter Display using Serial Access Mode

0368-12

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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

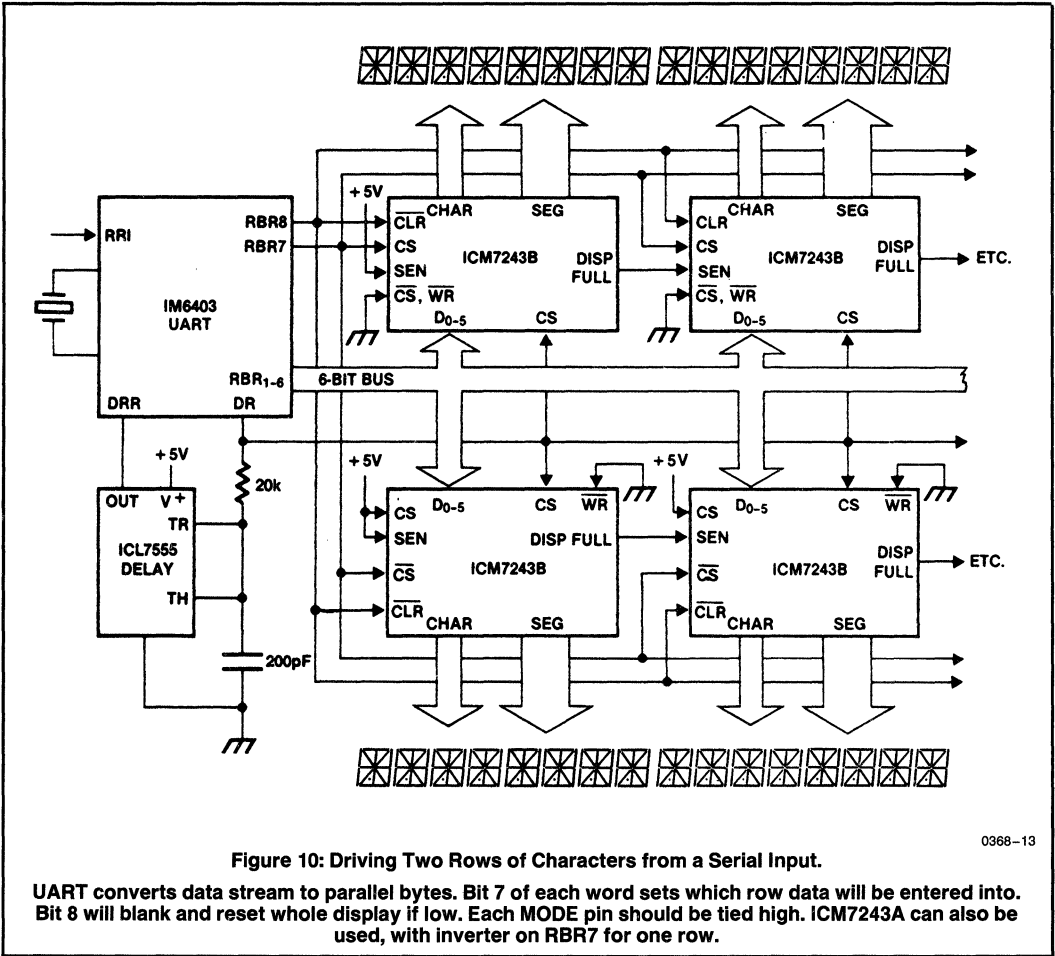


Figure 10: Driving Two Rows of Characters from a Serial Input.

0368-13

UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

COMPONENT SELECTION

Displays suitable for use with the ICM7243 may be obtained from the following manufacturers; among others:

Hewlett Packard Components, Palo Alto, California (415) 857-6620 (part #HDSP6508, HDSP6300)

General Instruments Inc., Palo Alto, California (415) 493-0400 (part #MAN2815)

Texas Instruments Inc., Dallas, Texas (214) 995-6611 (part #HDSP6508)

A.N.D., Burlingame, California (415) 347-9916 (part #AND370R)

IEE Inc., Van Nuys, California (213) 787-0311 (part #LR3784R)

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NOTE: All typical values have been characterized but are not tested.

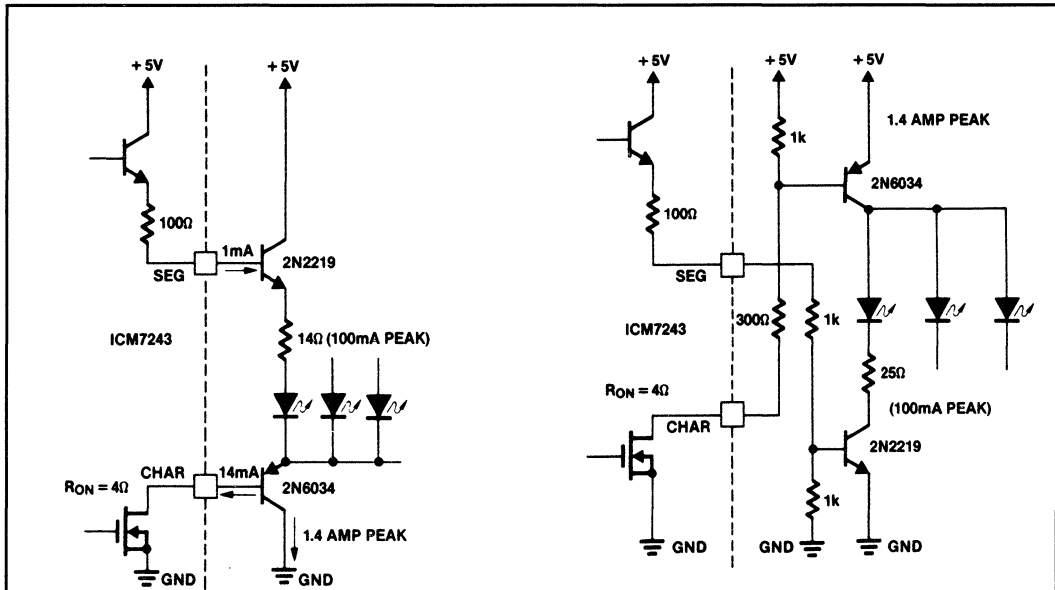
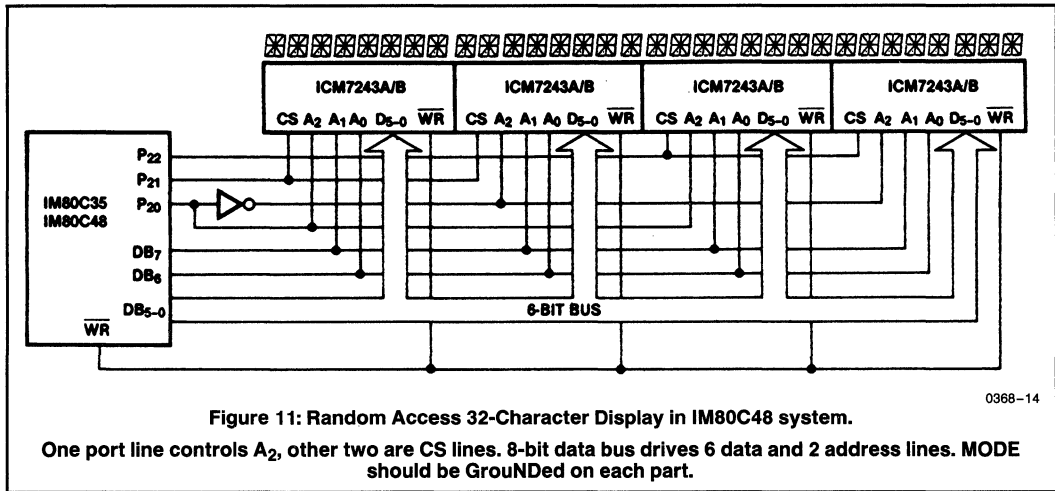


Figure 12: Driving Large Displays.

The circuits of Figures 12a and 12b can be used to drive 0.5" or larger alphanumeric displays, either common cathode (12a) or common anode (12b).

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NOTE: All typical values have been characterized but are not tested.

Section 14 — Timers/Clocks/ Counters with Display Drivers

ICM7170	14-1
ICM7207/A	14-14
ICM7208	14-19
ICM7209	14-26
ICM7215	14-29
ICM7216A	14-36
ICM7216B	14-36
ICM7216C	14-36
ICM7216D	14-36
ICM7217	14-54
ICM7227	14-54
ICM7224	14-72
ICM7225	14-72
ICM7226A/B	14-80
ICM7236	14-93
ICM7240	14-98
ICM7250	14-98
ICM7242	14-108
ICM7249	14-114
ICM7555	14-123
ICM7556	14-123

ICM7170

μ P-Compatible Real-Time Clock



ICM7170

GENERAL DESCRIPTION

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Intersil's silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from 1/100 seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{acc}) of 300ns eliminates the need for any microprocessor wait states or software overhead. Furthermore, the ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts. The first type is the periodic interrupt (i.e., 100Hz, 10Hz, etc.) which can be programmed by the internal interrupt control register to provide 7 different output signals. The second type is the alarm interrupt. The alarm time is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power-Down Detector eliminates the need for external components to support the battery back-up function. When a power-down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7170IPG	-40°C to +85°C	24-Pin Plastic Dip
ICM7170IDG	-40°C to +85°C	24-Pin Ceramic
ICM7170IBG	-40°C to +85°C	24-Pin S.O.I.C. (Surface Mount)
ICM7170MDG	-55°C to +125°C	24-Pin Ceramic
ICM7170MDG/883C	-55°C to +125°C	24-Pin Ceramic
ICM7170AIPG	-40°C to +85°C	24-Pin Plastic Dip
ICM7170AIBG	-40°C to +85°C	24-Pin S.O.I.C.

"A" Parts Screened to $< 4 \mu A I_{STBY}$ @ 32 KHz

FEATURES

- 883B-Rev C Compliant
- 8-Bit μ P Bus Compatible
—Multiplexed or Direct Addressing
- Regulated Oscillator Supply Ensures Frequency Stability and Low Power
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll-Over During Read
- Full Calendar With Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less Than 300ns
- 4 Programmable Crystal Oscillator Frequencies over Industrial Temp Range
- 3 Programmable Crystal Oscillator Frequencies over Military Temp Range
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: $2 \mu A$ Typ. at 3.0V and 32kHz Crystal

APPLICATIONS

- Portable and Personal Computers • Data Logging
- Industrial Control Systems • Point Of Sale

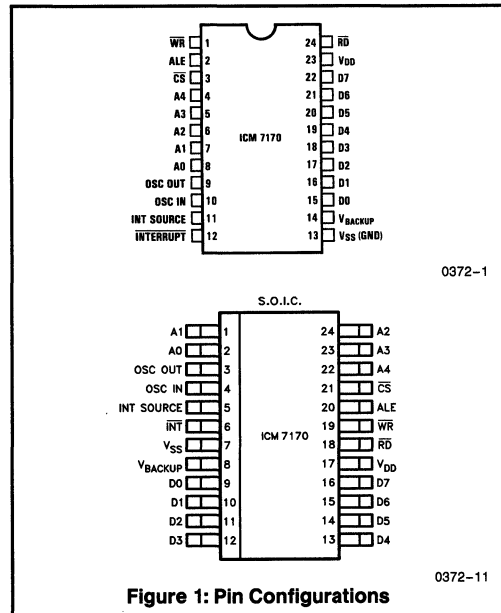


Figure 1: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 8V
 Power Dissipation (Note 1) 500mW
 Input Voltage (Any Terminal)
 (Note 2) $V_{DD} + 0.3V$ to $V_{SS} - 0.3V$

Operating Temperature $-40^{\circ}C$ to $+85^{\circ}C$
 Storage Temperature $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10sec) $300^{\circ}C$

NOTE 1: $T_A = 25^{\circ}C$.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

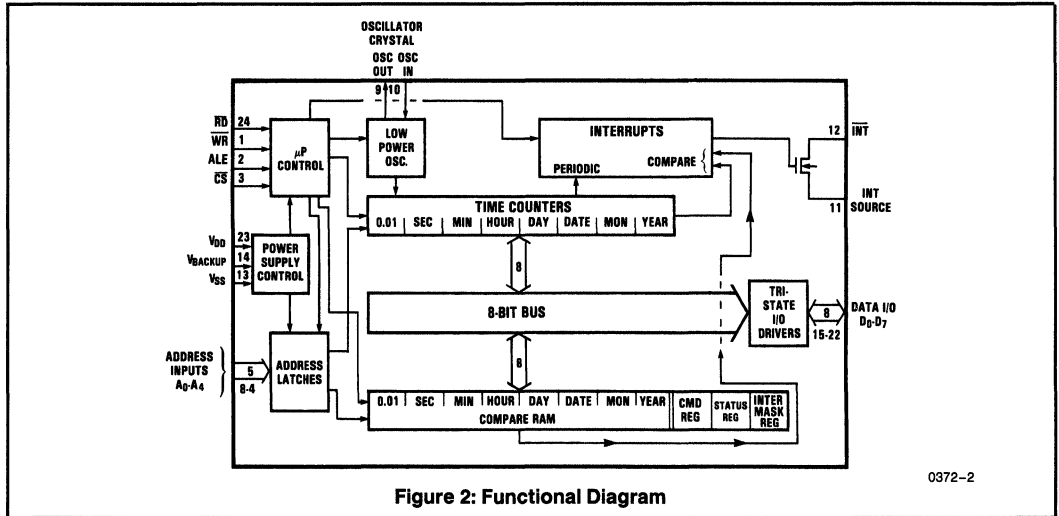


Figure 2: Functional Diagram

0372-2

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

($T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{DD} = +5V \pm 10\%$, $V_{BACKUP} = V_{DD}$, $V_{SS} = 0V$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Specification			Units
			Min	Typ	Max	
V_{DD}	V_{DD} Supply Range	$F_{OSC} = 32kHz$	1.9		5.5	V
		$F_{OSC} = 1, 2, 4MHz$	2.6		5.5	
$I_{STBY(1)}$	Standby Current	$F_{OSC} = 32kHz$ Pins 1-8, 15-22 & 24 = V_{DD} $V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD} - 3.0V$	7170	2.0	20.0	μA
			7170A	2.0	5.0	
$I_{STBY(2)}$	Standby Current	$F_{OSC} = 4MHz$ Pins 1-8, 15-22 & 24 = V_{DD} $V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD} - 3.0V$		20	150	μA
$I_{DD(1)}$	Operating Supply Current	$F_{OSC} = 32kHz$ Read/Write Operation at 100Hz		0.3	1.2	mA
$I_{DD(2)}$	Operating Supply Current	$F_{OSC} = 32kHz$ Read/Write Operation at 1MHz		1.0	2.0	mA
V_{IL}	Input low voltage (Except Osc.)	$V_{DD} = 5.0V$			0.8	V

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS

($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 10\%$, $V_{\text{BACKUP}} = V_{DD}$, $V_{SS} = 0\text{V}$ unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Specification			Units
			Min	Typ	Max	
V_{IH}	Input high voltage (Except Osc.)	$V_{DD} = 5.0\text{V}$	2.4			V
V_{OL}	Output low voltage (Except Osc.)	$I_{OL} = 1.6\text{mA}$			0.4	V
V_{OH}	Output high voltage except INTERRUPT (Except Osc.)	$I_{OH} = -400\mu\text{A}$	2.4			V
I_{IL}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS}	-10	0.5	+10	μA
I_{OL}	Tristate leakage current (D ₀ -D ₇)	$V_0 = V_{DD}$ or V_{SS}	-10	0.5	+10	μA
V_{BATTERY}	Backup Battery Voltage	$F_{\text{OSC}} = 1, 2, 4\text{MHz}$	2.6		$V_{DD} - 1.3$	V
V_{BATTERY}	Backup Battery Voltage	$F_{\text{OSC}} = 32\text{kHz}$	1.9		$V_{DD} - 1.3$	V
I_{OL}	Leakage current INTERRUPT	$V_0 = V_{DD}$ INT SOURCE connected to V_{SS}		0.5	10	μA
$C_{I/O}$	CAPACITANCE D ₀ -D ₇				8	pF
C_{ADDRESS}	CAPACITANCE A ₀ -A ₄				6	pF
C_{CONTROL}	CAP. RD, WR, CS ALE				6	pF
C_{IN} Osc.	Total Osc. Input Cap.				3	pF

AC CHARACTERISTICS ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 10\%$, $V_{\text{BACKUP}} = V_{DD}$, D₀-D₇ Load
Capacitance = 150pF, $V_{IL} = 0.4\text{V}$, $V_{IH} = 2.8\text{V}$ unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ CYCLE TIMING				
t_{rd}	READ to DATA valid		250	ns
t_{acc}	ADDRESS valid to DATA valid		300	ns
t_{cyc}	READ cycle time	400		ns
t_{rx}	$\overline{\text{RD}}$ high to bus tristate*		25*	ns
t_{as}	ADDRESS to READ set up time*	50		ns
t_{ar}	ADDRESS HOLD time after READ*	0		ns
*Guaranteed Parameter by Design				
WRITE CYCLE TIMING				
t_{ad}	ADDRESS valid to WRITE strobe	50		ns
t_{wa}	ADDRESS hold time for WRITE	0		ns
t_{wl}	WRITE pulse width, low	100		ns
t_{wh}	WRITE high time	300		ns
t_{rh}	Read high time	150		ns
t_{dw}	DATA IN to WRITE set up time	100		ns
t_{wd}	DATA IN hold time after WRITE	30		ns
t_{cyc}	WRITE cycle time	400		ns
MULTIPLEXED MODE TIMING				
t_{ij}	ALE Pulse Width, High	50		ns
t_{al}	ADDRESS to ALE set up time	30		ns
t_{ia}	ADDRESS hold time after ALE	30		ns

Capacitance values are maximum values and are sample tested only.

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**ICM 7170 ELECTRICAL CHARACTERISTICS (TEST SPECIFICATION)
FOR MIL-STD-883 COMPLIANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8V
Power Dissipation (Note 1)	500mW
Input Voltage (Any Terminal)	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE 1: $T_A = 25^\circ C$.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $V_{BACKUP} = V_{DD}$, $T_A = -55^\circ C$ to $+125^\circ C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Specification			Units
			Min	Typ	Max	
V_{DD}	V_{DD} Supply Range	$F_{OSC} = 32kHz$	1.9		5.5	V
		$F_{OSC} = 1, 2MHz$	2.6		5.5	
$I_{STBY(1)}$	Standby Current	$F_{OSC} = 32 kHz$ All chip I/O to V_{DD} $V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} - 3.0V$		2.0	40	μA
$I_{STBY(2)}$	Standby Current	$F_{OSC} = 1, 2MHz$ All chip I/O to V_{DD} 7170A $V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} - 3.0V$		30	200 5.0	μA
$I_{DD(1)}$	Operating Supply Current	$F_{OSC} = 32 kHz$ Read/Write Operation at 100 Hz		0.3	1.2	mA
$I_{DD(2)}$	Operating Supply Current	$F_{OSC} = 32 kHz$ Read/Write Operation at 1 MHz		1.0	2.0	mA
V_{IL}	Input Low Voltage (Except Osc.)	$V_{DD} = 5.0V$			0.8	V
V_{IH}	Input High Voltage (Except Osc.)	$V_{DD} = 5.0V$	2.8			
V_{OL}	Output Low Voltage (Except Osc.)	$I_{OL} = 1.6 mA$			0.5	V
V_{OH}	Output High Voltage Except INTERRUPT (Except Osc.)	$I_{OH} = 400\mu A$	2.5			V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS}	-10	0.5	+10	μA
I_{OL}	Tristate Leakage Current (D ₀ -D ₇)	$V_{IN} = V_{DD}$ or V_{SS}	-10	0.5	+10	μA
$V_{BATTERY}$	Backup Battery Voltage	OSG = 32 kHz	1.9		$V_{DD} - 1.5$	V
I_{OL}	Leakage Current INTERRUPT	$V_0 = V_{DD}$ or V_{SS}		0.5	10	μA
		INT SOURCE connected to V_{SS}				

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NOTE: All typical values have been characterized but are not tested.

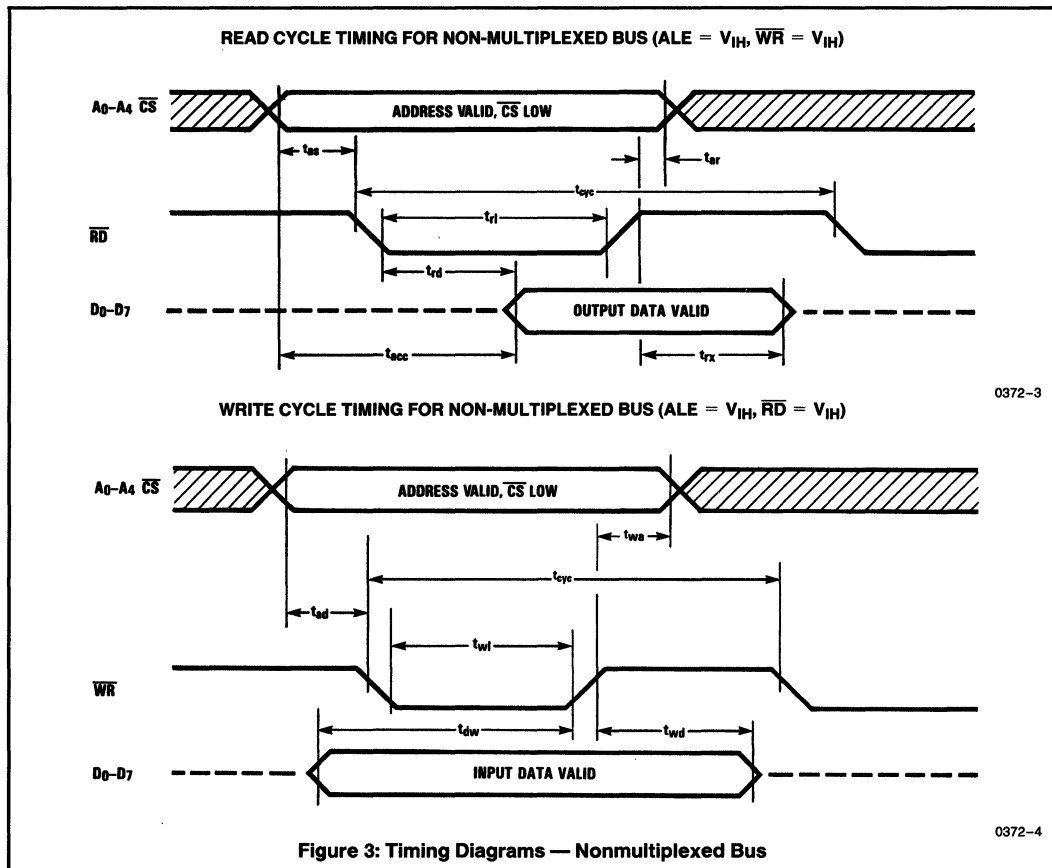
AC CHARACTERISTICS ($T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$, $V_{\text{BACKUP}} = V_{DD}$, $D_0\text{--}D_7$ Load
 Capacitance = 150 pF, $V_{IL} = 0.4\text{V}$, $V_{IH} = 3.20\text{V}$ unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ CYCLE TIMING				
t_{rd}	READ to DATA Valid		250	ns
t_{ACC}	ADDRESS Valid to DATA Valid		350	ns
t_{cyc}	READ Cycle Time	450		ns
t_{rx}	\overline{RD} High to Bus Tristate		100	ns
t_{as}	ADDRESS to READ Set Up Time	100		ns
t_{ar}	ADDRESS HOLD Time after READ	50		ns
t_{rh}	READ High Time	200		ns
WRITE CYCLE TIMING				
t_{ad}	ADDRESS Valid to WRITE Strobe	100		ns
t_{wa}	ADDRESS Hold Time after WRITE	50		ns
t_{wl}	WRITE Pulse Low Width	125		ns
t_{wh}	WRITE Pulse Width High	325		ns
t_{dw}	DATA IN to WRITE Set Up Time	125		ns
t_{wd}	DATA IN Hold Time after WRITE	50		ns
t_{cyc}	WRITE Cycle Time	450		ns
MULTIPLEXED MODE TIMING				
t_{ll}	ALE Width	50		ns
t_{al}	ADDRESS to ALE Set Up Time	30		ns
t_{la}	ADDRESS Hold Time after ALE	40		ns

PRELIMINARY
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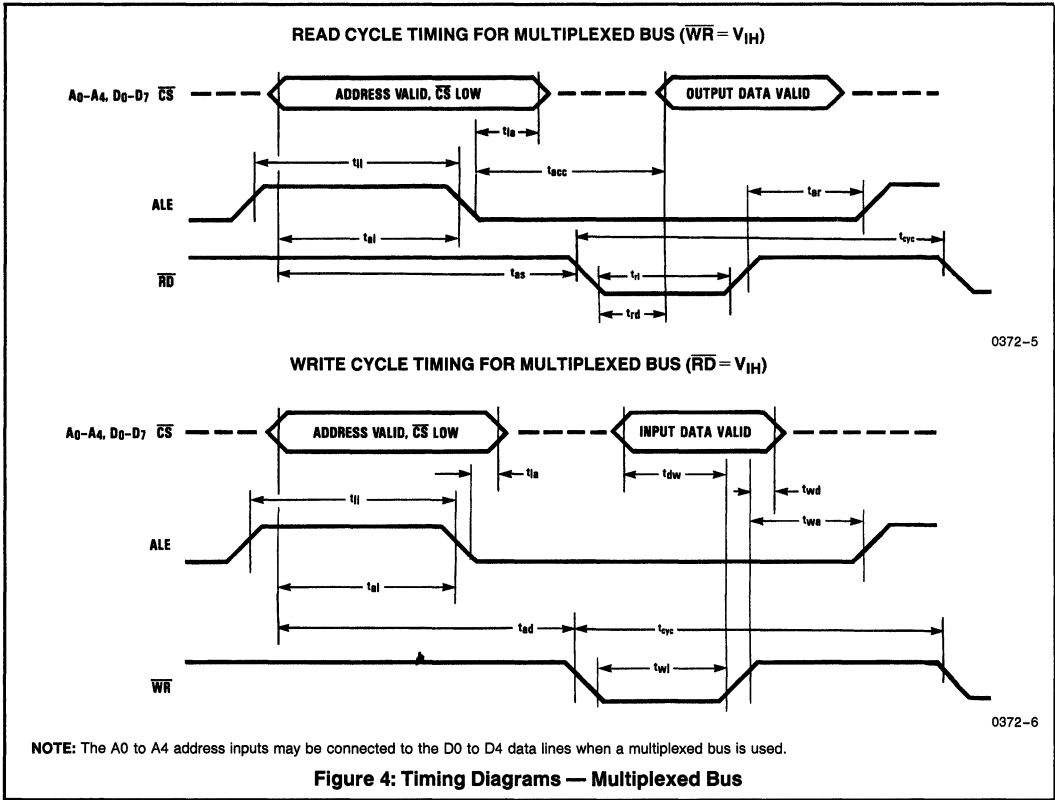


Table 1

Signal	Pin	Description
\overline{WR}	1	Write input
ALE	2	Address latch enable input
\overline{CS}	3	Chip select input
A4-A0	4-8	Address inputs
OSC OUT	9	Oscillator output
OSC IN	10	Oscillator input
INT SOURCE	11	Interrupt source
$\overline{INTERRUPT}$	12	Interrupt output
$V_{SS}(GND)$	13	Digital common
V_{BACKUP}	14	Battery negative side
D0-D7	15-22	Data I/O
V_{DD}	23	Positive digital supply
\overline{RD}	24	Read input

DETAILED DESCRIPTION

Oscillator

This circuit uses a regulated CMOS Pierce oscillator, for maximum accuracy, stability, and low-power consumption. Externally, one crystal and two capacitors are required. One of the capacitors is variable and is used to trim or tune the oscillator output. Typical values for these capacitors are $C_{IN} = 15pF$ and $C_{OUT} = 10 - 35pF$, or approximately double the recommended C_{LOAD} for the crystal being used. Both capacitors must be connected from the respective oscillator pins to V_{DD} for maximum stability.

The oscillator output is divided down to 4000Hz by one of four selected ratios, via a variable prescaler. The ICM7170 can use any one of four different low-cost crystals: 4.194304MHz, 2.097152MHz, 1.048576MHz, or 32.768kHz. The ICM7170MDG is available with 3 crystal frequency options only. (4.194304 MHz is not avail. with military version.) The command register must be programmed for the frequency of the crystal chosen, and this in turn will determine the prescaler's divide ratio.

Command Register frequency selection is written to the D0 and D1 bits at address 11H and the 12 or 24 hour format is determined by bit D2, as shown in Table 4.

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The 4000Hz signal is divided down further to 100Hz, which is used as the clock for the counters. Time and calendar information is provided by 8 consecutive addressable, programmable counters: 100ths of seconds, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format and is configured into 8 bits per digit. See Table 4 for address information. Any unused bits are held at logic "0" during a read and ignored during a write operation.

Alarm Compare RAM

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 100ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate 'M' bit in Compare RAM should be set to logic "1".

The 'M' bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 4 shows addresses and Mask bit information.

Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100 Hz, 10 Hz, once per second, once per minute, once per hour, or once per day. The 100 Hz and 10 Hz interrupts have instantaneous errors of $\pm 2.5\%$ and $\pm 0.15\%$ respectively. This is because non-integer divider circuitry is used to generate these signals from the crystal frequency, which is a power of 2. The time average of these errors over a 1 second period, however, is zero. Consequently, the 100 Hz or 10 Hz interrupts are not suitable as an aid in tuning the oscillator; the 1 second interrupt must be used instead.

The periodic interrupts can occur concurrently and in addition to alarm interrupts. They are controlled by bits in the interrupt mask register, and are enabled by setting the appropriate bit to a "1" as shown in Table 5. Bits D0 through D6 in the mask register, in conjunction with bits D0 through D6 of the status register, control the generation of interrupts according to Figure 5.

The interrupt status register, when read, indicates the cause of the interrupt and resets itself on the rising edge of the RD signal. When any of the counters having a corresponding bit in the status register roll over to zero, that bit is set to a "1" regardless of whether the corresponding bit in the interrupt mask register is set or not. This also applies to the alarm compare bit.

Consequently, when the status register is read it will always indicate which counters have rolled over to zero and if an alarm compare occurred, since the last time it was read. This requires some special software considerations. If a slow interrupt is enabled (i.e. hourly or daily), the program must always check the slowest interrupt that has been enabled first, because all the other lower order bits in the status register will be set to "1" as well. Bit D7 is the global interrupt bit, and when set to a "1", indicates that the 7170 did indeed generate a hardware interrupt. This is useful when other interrupting devices in addition to the 7170 are attached to the system microprocessor, and all devices must be polled to determine which one generated the interrupt.

Table 2: Command Register Format

COMMAND REGISTER ADDRESS (10001b, 11h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	n/a	Test	Int.	Run	12/24	Freq	Freq

Table 3: Command Register Bit Assignments

D1	D0	Crystal Frequency	D2	24/12 Hour Format	D3	Run/Stop	D4	Interrupt Enable	D5	Test Bit
0	0	32.768kHz	0	12 hour mode	0	Stop	0	Interrupt disabled	0	Normal Mode
0	1	1.048576MHz	1	24 hour mode	1	Run	1	Interrupt enable	1	Test Mode
1	0	2.097152MHz								
1	1	4.194304MHz								

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NOTE: All typical values have been characterized but are not tested.

Table 4: Address Codes and Functions

Address						Function	DATA								Value
A4	A3	A2	A1	A0	HEX		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	00	Counter-1/100 seconds	-	0-99
0	0	0	0	1	01	Counter-hours	-	-	-	0-23
						12 Hour Mode	*	.	.	-	1-12
0	0	0	1	0	02	Counter-minutes	-	-	0-59
0	0	0	1	1	03	Counter-seconds	-	-	0-59
0	0	1	0	0	04	Counter-month	-	-	-	-	1-12
0	0	1	0	1	05	Counter-date	-	-	-	1-31
0	0	1	1	0	06	Counter-year	-	0-99
0	0	1	1	1	07	Counter-day of week	-	-	-	-	-	.	.	.	0-6
0	1	0	0	0	08	RAM-1/100 seconds	M	0-99
0	1	0	0	1	09	RAM-hours	-	M	-	0-23
						12 hour Mode	*	M	-	-	1-12
0	1	0	1	0	0A	RAM-minutes	M	-	0-59
0	1	0	1	1	0B	RAM-seconds	M	-	0-59
0	1	1	0	0	0C	RAM-month	M	-	-	-	1-12
0	1	1	0	1	0D	RAM-date	M	-	-	1-31
0	1	1	1	0	0E	RAM-year	M	0-99
0	1	1	1	1	0F	RAM-day of week	M	-	-	-	-	.	.	.	0-6
1	0	0	0	0	10	Interrupt Status and Mask Register	+	
1	0	0	0	1	11	Command register	-	-	

NOTES: Address 10010 to 11111 (12h to 1Fh) are unused.
 '+' Unused bit for Interrupt Mask Register, MSB bit for Interrupt Status Register.
 '-' Indicates unused bits.
 '**' AM/PM indicator bit in 12 hour format. Logic "0" indicates AM, logic "1" indicates PM.
 'M' Alarm compare for particular counter will be enabled if bit is set to logic "0".

Table 5: Interrupt and Status Registers Format

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
Not Used	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm

INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
Global Interrupt	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm

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NOTE: All typical values have been characterized but are not tested.

Interrupt Operation

The interrupt output N-channel MOSFET is active at all times when the Interrupt Enable bit is set (bit 4 of the Command Register), and operates in both the standby and battery backup modes.

Since system power is usually applied between V_{DD} and V_{SS} , the user can connect the Interrupt Source (pin #11) to V_{SS} . This allows the Interrupt Output to turn on only while system power is applied and will not be pulled to V_{SS} during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (V_{BACKUP}). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

Power-Down Detector

The ICM7170 contains an on-chip power-down detector that eliminates the need for external components to support

the battery-backup switchover function, as shown in Figure 6. Whenever the voltage from the V_{SS} pin to the V_{BACKUP} pin is less than approximately 1.0V (the V_{th} of the N-channel MOSFET), the data bus I/O buffers in the 7170 are automatically disabled and the chip cannot be read or written to. This prevents random data from the microprocessor being written to the clock registers as the power supply is going down.

Actual switchover to battery operation occurs when the voltage on the V_{BACKUP} pin is within ± 50 mV of V_{SS} . This switchover uncertainty is due to the offset voltage of the CMOS comparator that is used to sense the battery voltage. During battery backup, device operation is limited to time-keeping and interrupt generation only, thus achieving micro-power current drain. If an external battery-backup switchover circuit is being used with the 7170, the V_{BACKUP} pin should be tied to the V_{DD} pin. The same also applies if standby battery operation is not required.

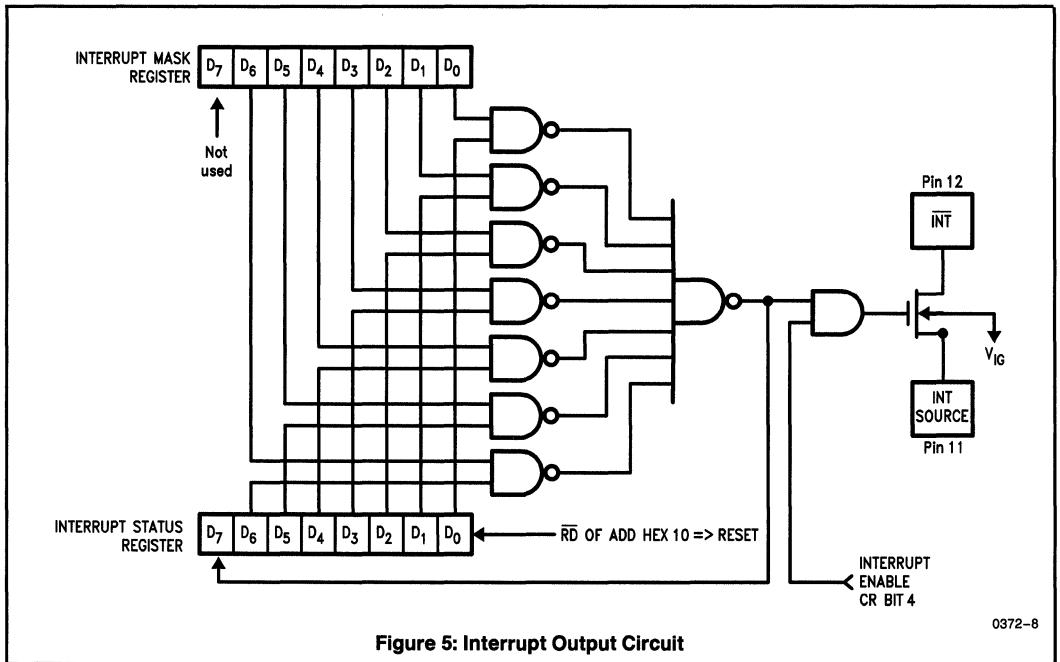


Figure 5: Interrupt Output Circuit

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NOTE: All typical values have been characterized but are not tested.

Time Synchronization

Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

Latched Data

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is stored into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again.

Control Lines

The \overline{RD} , \overline{WR} , and \overline{CS} signals are active low inputs. Data is placed on the bus from counters or registers when \overline{RD} is a logic "0". Data is transferred to counters or registers when \overline{WR} is a logic "0". \overline{RD} and \overline{WR} must be accompanied

by a logical "0" \overline{CS} as shown in Figures 3 and 4. The 7170 will also work satisfactorily with \overline{CS} grounded. This access also to be controlled by \overline{RD} and \overline{WR} only.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0-A4 to the data lines D0-D4. To address the chip, the address is placed on the bus and ALE is strobed. On the falling edge, the address and \overline{CS} information is read into the address latch and buffer. \overline{RD} and \overline{WR} are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to V_{DD} .

Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz counter to the oscillator's output. The peak-to-peak voltage used to drive osc. out should not be greater than the oscillator's regulated voltage. The signal must be referenced to V_{DD} .

Oscillator Tuning

Oscillator tuning should not be attempted by direct monitoring of the oscillator pins, unless very specialized equipment is used. External connections to the oscillator pins cause capacitive loading of the crystal, and shift the oscillator frequency. As a result, the precision setting being at-

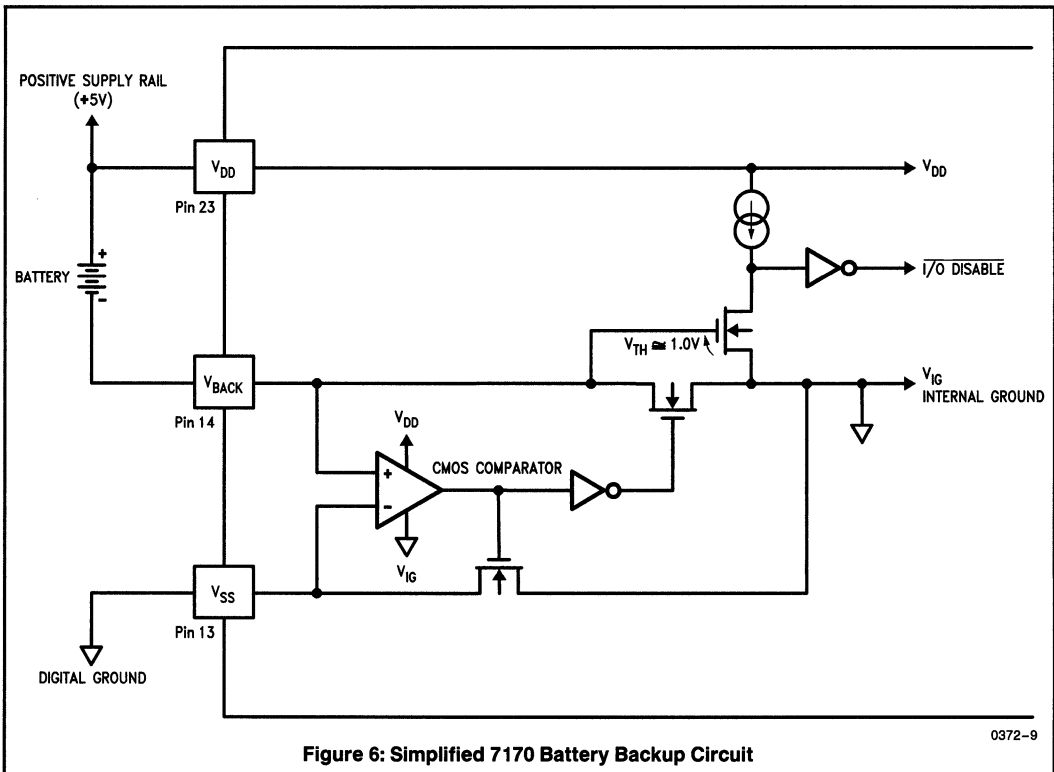


Figure 6: Simplified 7170 Battery Backup Circuit

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NOTE: All typical values have been characterized but are not tested.

tempted is corrupted. One indirect method of determining the oscillator frequency is to measure the period between interrupts on the Interrupt Output pin (#12). This measurement must be relative to the falling edges of the $\overline{\text{INTERRUPT}}$ pin. The oscillator set-up and tuning can be performed as follows:

- 1) Select one of 4, readily-available oscillator frequencies and place the crystal between OSC IN (pin #10) and OSC OUT (pin #9).
- 2) Connect a fixed capacitor from OSC IN to V_{DD} .
- 3) Connect a variable capacitor from OSC OUT to V_{DD} . In cases where the crystal selected is a 32kHz Statek type ($C_L = 9\text{pF}$), the typical value of $C_{IN} = 15\text{pF}$ and $C_{OUT} = 5\text{pf} - 35\text{pF}$.
- 4) Place a $4.7\text{K}\Omega$ resistor from the $\overline{\text{INTERRUPT}}$ pin to V_{DD} , and connect the INT SOURCE pin to V_{SS} .
- 5) Apply 5V power and insure the clock is not in stand-by mode.
- 6) Write all 0's to the Interrupt Mask Register, disabling all interrupts.
- 7) Write to the Command Register with the desired oscillator frequency, Hours mode (12 hour or 24 hour), Run = "1", Interrupt Enable = "1", and Test = "0".
- 8) Write to the Interrupt Mask Register, enabling one-second interrupts only.
- 9) Monitor the $\overline{\text{INTERRUPT}}$ output pin with a precision period counter and trim the OSC OUT capacitor for a reading of 1.000000 seconds. The period counter must be triggered on the falling edge of the interrupt output for this measurement to be accurate.
- 10) Read the Interrupt Status Register. This action resets the interrupt output back to a logic "1" level.
- 11) Repeat steps 9 and 10 with a software loop. A suitable computer should be used.

PCB DESIGN CONSIDERATION

- 1) Layout Quartz Crystal traces as short as possible.
- 2) Keep Crystal traces as far as possible from other traces.
- 3) PCB must accept both Saronix and Statek 32.768kHz Crystals.
- 4) Completely surround crystal traces with V_{DD} trace.
- 5) Try to keep oscillator traces on one side of the PCB.
- 6) Trimmer capacitor must be accessible from the top of the PCB after it is inserted into the appropriate connector.
- 7) The fixed and variable oscillator capacitors must be referenced to V_{DD} . V_{SS} is not an AC ground for the oscillator.

APPLICATION NOTES

Digital Input Termination During Backup

To ensure low current drain during battery backup operation, none of the digital inputs to the 7170 should be allowed to float. This keeps the input logic gates out of their transition region, and prevents crossover current from flowing which will shorten battery life. The address, data, $\overline{\text{CS}}$, and ALE pins should be pulled to either V_{DD} or V_{SS} , and the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs should be pulled to V_{DD} . This is necessary whether the internal battery switchover circuit is used or not.

IBM/PC Evaluation Circuit

Figure 7 shows the schematic of a board that has been designed to plug into an IBM PC or compatible computer. It features full buffering of all 7170 address and data lines, and switch selectable I/O block select. A provision for setting the priority level of the 7170 periodic interrupt has also been added.

Batteries	Crystals
Panasonic Rayovac	Statek 32kHz CX-IV SARONIX 32kHz NTF3238

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NOTE: All typical values have been characterized but are not tested.

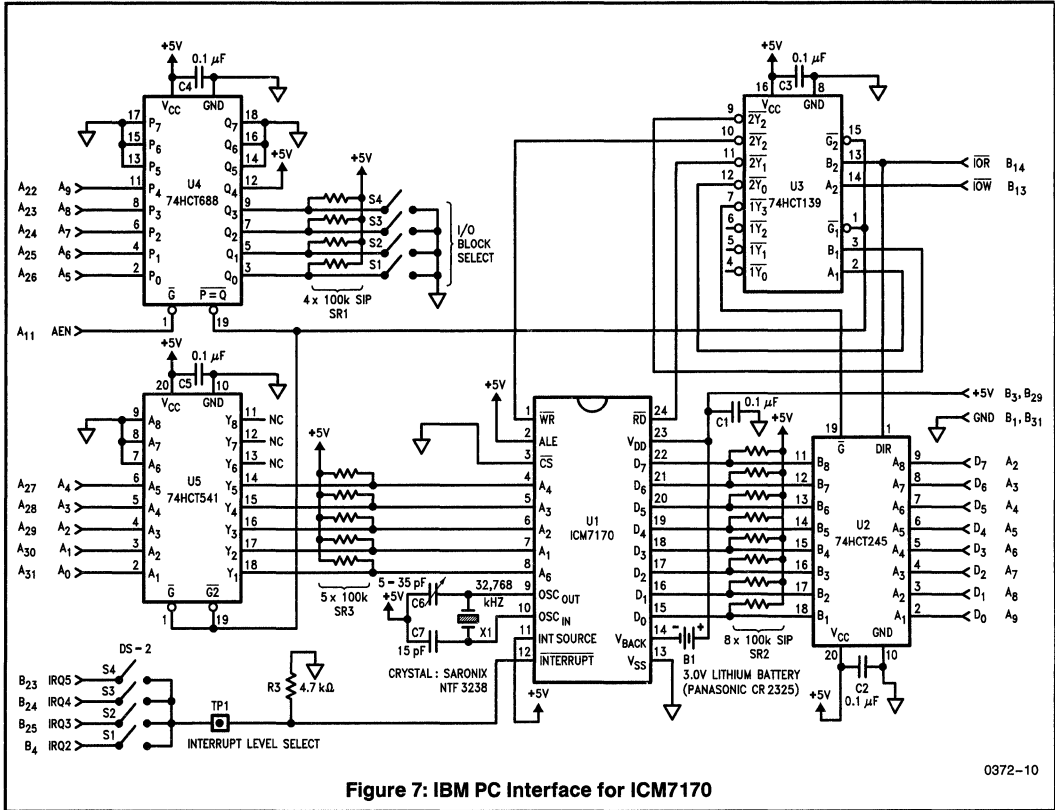


Figure 7: IBM PC interface for ICM7170

0372-10

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NOTE: All typical values have been characterized but are not tested.

ICM7207/A CMOS Timebase Generator



GENERAL DESCRIPTION

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts. The typical power dissipation is less than 2mW when using an oscillator frequency of 6.5536MHz with the 7207 and 5.24288MHz with the 7207A.

In the 7207/A the GATING OUTPUT, $\overline{\text{ReSeT}}$, and the MULTIPLEX output provide both pull up and pull down, eliminating the need for 3 external resistors; although, buffering must be provided if interfacing with TTL is required.

ORDERING INFORMATION

Order Number	Temperature Range	Package
ICM7207JD	-25°C to +85°C	14-Pin CERDIP
ICM7207IPD	-25°C to +85°C	14-Pin PLASTIC DIP
ICM7207EV/Kit	—	EV/Kit*
ICM7207AJD	-25°C to +85°C	14-Pin CERDIP
ICM7207AIPD	-25°C to +85°C	14-Pin PLASTIC DIP
ICM7207AEV/Kit	—	EV/Kit*

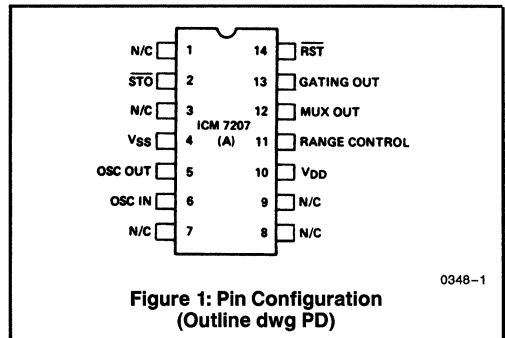
*These EV/Kits contain just the IC and the corresponding crystal. The ICM7207A is also used in the 4½-Digit Counter/Driver kits, the ICM7224 EV/Kit, ICM7225 EV/Kit, and ICM7236 EV/Kit, which include several ICs, a crystal, PC board, and some passive components.

FEATURES

- Stable HF Oscillator
- Low Power Dissipation $\leq 2\text{mW}$ With 5 Volt Supply
- Counter Chain Has Outputs at $\div 2^{12}$ and $\div 2^n$ or $\div (2^n \times 10)$; $n = 17$ for 7207, and 20 for 7207A
- Low Impedance Output Drivers ≤ 100 Ohms
- Count Windows of 10/100ms (7207 With 6.5536MHz Crystal) or 0.1/1 Sec. (7207A With 5.24288MHz Crystal)

APPLICATIONS

- System Timebases
- Oscilloscope Calibration Generators
- Marker Generator Strokes
- Frequency Counter Controllers



0348-1

Figure 1: Pin Configuration (Outline dwg PD)

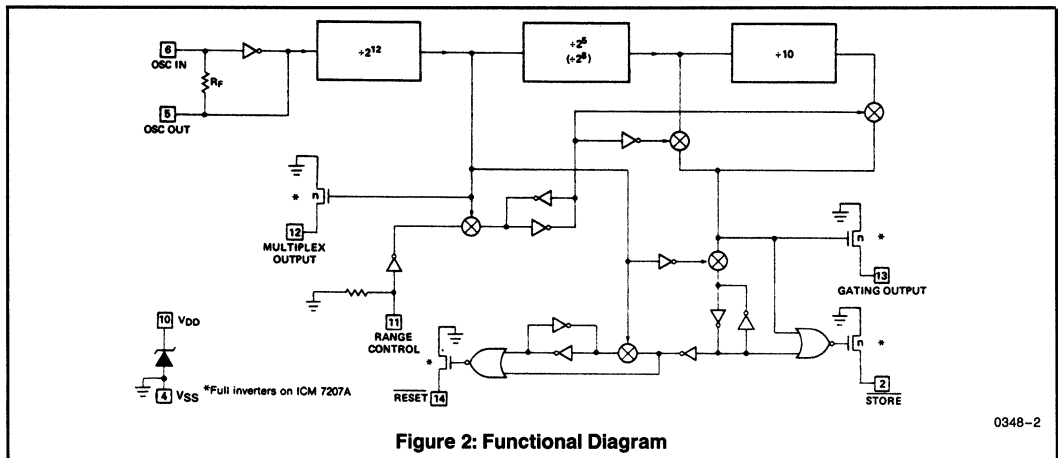


Figure 2: Functional Diagram

0348-2

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$)	6.0V
Input Voltages	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Output Voltages:	
7207	V_{SS} to $+6V$
7207A	V_{DD} to V_{SS}

Output Currents	25mA
Power Dissipation @ 25°C Note 1	200mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature Range	-65°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$f_{osc} = 6.5536\text{MHz}(7207), 5.24288\text{MHz}(7207A), V_{DD} = 5V, T_A = 25^\circ\text{C}, V_{SS} = 0V$, test circuit unless otherwise specified.

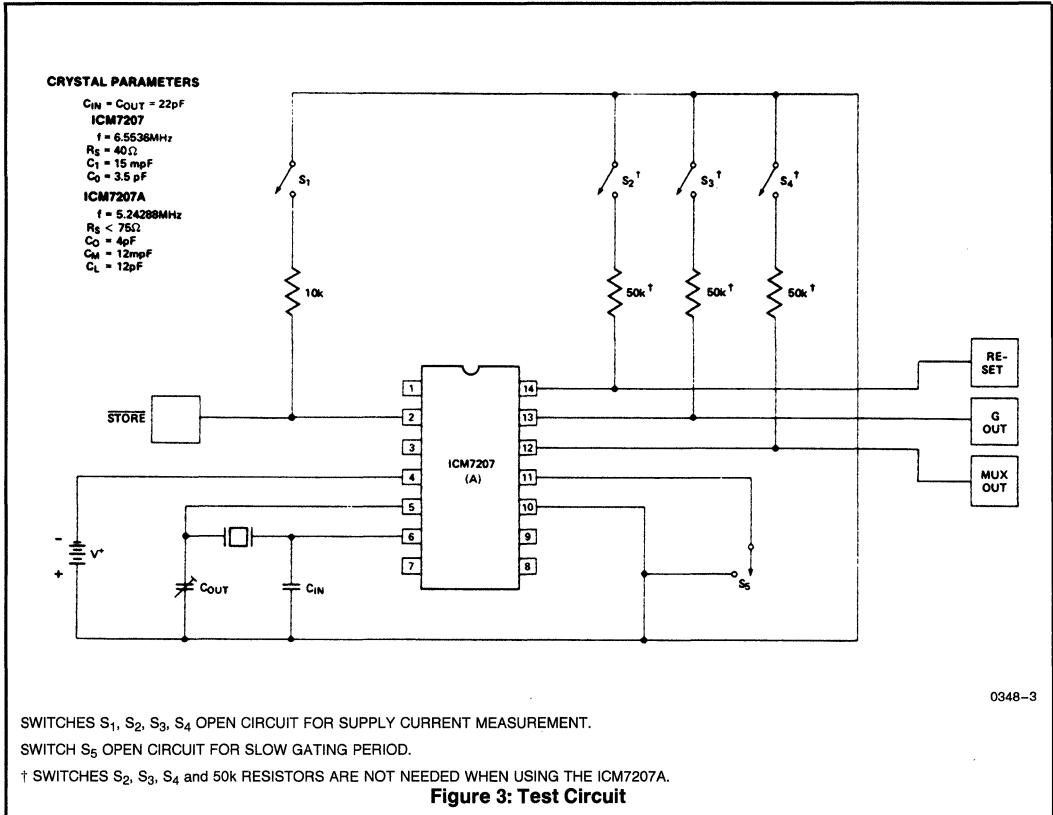
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage Range	-20°C to +85°C	4		5.5	V
I_{DD}	Supply Current	All outputs open circuit		260	1000	μA
$R_{ds(on)}$	Output on Resistances	Output current = 5mA All outputs		50	120	Ω
I_{OLK}	Output Leakage Currents	All outputs (STORE only)			50	μA
(R_{OUT})	(Output Resistance Terminals 12,13,14)	Output current = 50 μA , 7207A only			33K	Ω
I_{pd}	Input Pulldown Current	Terminal 11 connected to V_{DD}		50	200	μA
	Input Noise Immunity		25			% supply voltage
f_{osc}	Oscillator Frequency Range	Note 2	2		10	MHz
f_{STAB}	Oscillator Stability	$C_{IN} = C_{OUT} = 22\text{pF}$		0.2	1.0	ppm/V
r_{OSC}	Oscillator Feedback Resistance	Quartz crystal open circuit Note 3	3			M Ω

NOTES: 2. Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.

3. The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

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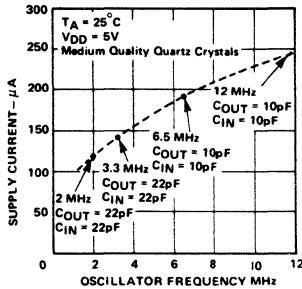
NOTE: All typical values have been characterized but are not tested.



0348-3

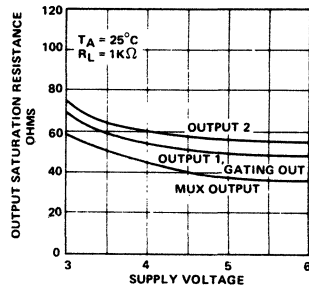
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



0348-4

OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE

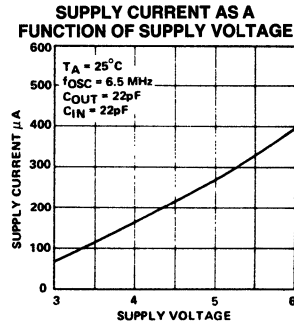
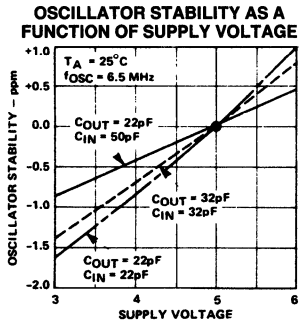


0348-5

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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



0348-6

0348-7

OUTPUT TIMING WAVEFORMS 7207 (7207A)

Crystal Frequency = 6.5536(5.24288)MHz

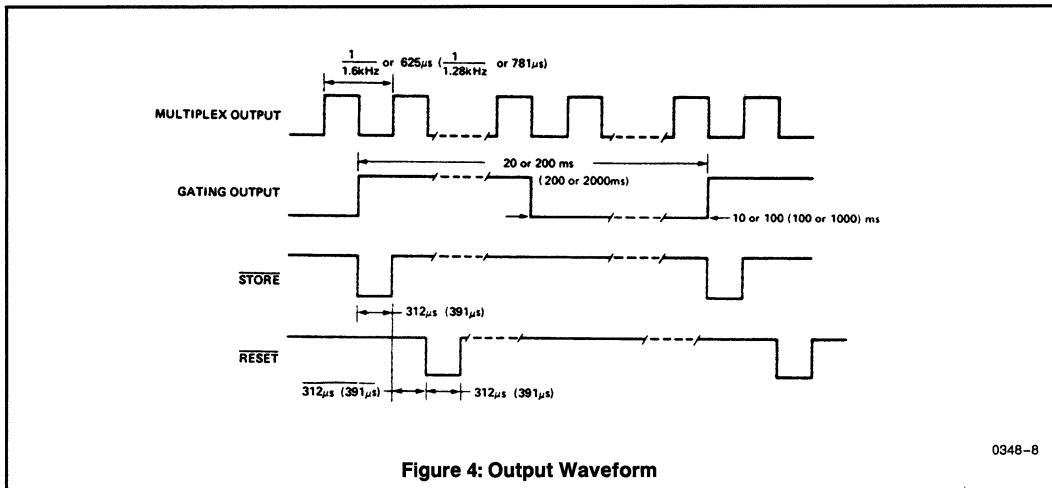


Figure 4: Output Waveform

0348-8

DETAILED DESCRIPTION

Referring to the Test Circuit, Figure 3, the crystal oscillator frequency is divided by 2¹² to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to V_{DD} or V_{SS} (open circuit).

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (C_L) be no greater than 15pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5mpF and a load capacitance of 15pF. The fixed capacitor C_{IN} should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05ppm per 0.1 volt change of supply voltage.

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NOTE: All typical values have been characterized but are not tested.

FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

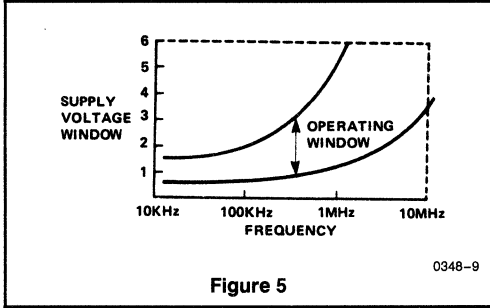


Figure 5

For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

APPLICATION

A PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet. Other frequency counters using the ICM7207/A can be constructed using the ICM7224, ICM7225, and ICM7236, for LCD, LED and VF displays. The latter are available as EV/Kits also.

QUARTZ CRYSTAL MANUFACTURERS

The following list of possible suppliers is intended to be of assistance in putting a design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Intersil.

- a) CTS Knights, Sandwich, Illinois, (815) 786-8411
- b) Motorola Inc., Franklin Park, Illinois (312) 451-1000
- c) Sentry Manufacturing Co., Chickasaw, Oklahoma (405) 224-6780
- d) Tyco Filters Division, Phoenix, Arizona (602) 272-7945
- e) M-Tron Inds., Yankton, South Dakota (605) 665-9321
- f) Saronix, Palo Alto, California (415) 856-6900

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NOTE: All typical values have been characterized but are not tested.

ICM7208

7-Digit LED Display Counter



ICM7208

GENERAL DESCRIPTION

The ICM7208 is a fully integrated seven decade counter-decoder-driver and is manufactured using Intersil's low voltage metal gate CMOS process.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signal gating.

FEATURES

- Low Operating Power Dissipation < 10mW
- Low Quiescent Power Dissipation < 5mW
- Counts and Displays 7 Decades
- Wide Operating Supply Voltage Range $2V \leq V_{DD} \leq 6V$
- Drives Directly 7 Decade Multiplexed Common Cathode LED Display
- Internal Store Capability
- Internal Inhibit to Counter Input
- Test Speedup Point

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7208IPI	-25°C to +85°C	28 Lead Plastic DIP

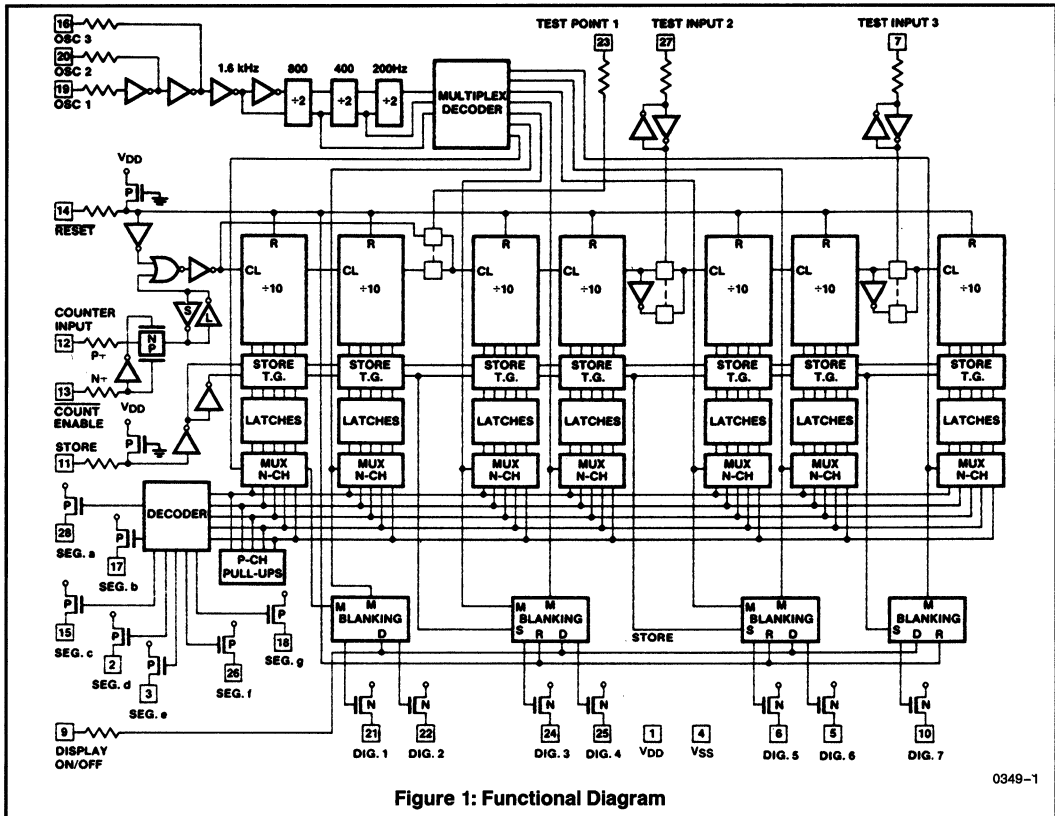


Figure 1: Functional Diagram

0349-1

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ($V_{DD} - V_{SS}$) 6V
 Input Voltage Range (any input terminal)
 (Note 2) $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
 Output Digit Drive Current (Note 3) 150mA
 Output Segment Drive Current 30mA
 Power Dissipation (Note 1) 1W
 Operating Temperature Range $-25^{\circ}C$ to $+85^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10sec) $300^{\circ}C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

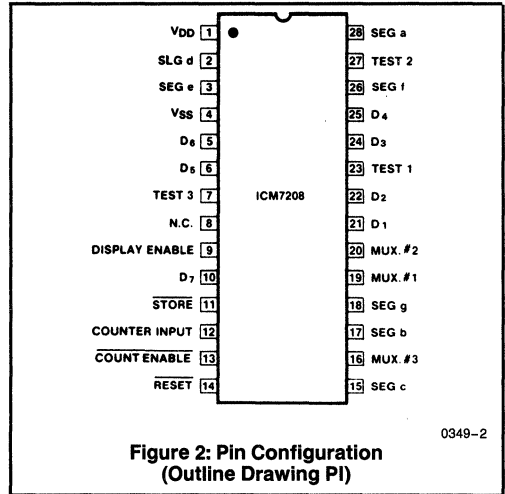


Figure 2: Pin Configuration (Outline Drawing PI)

0349-2

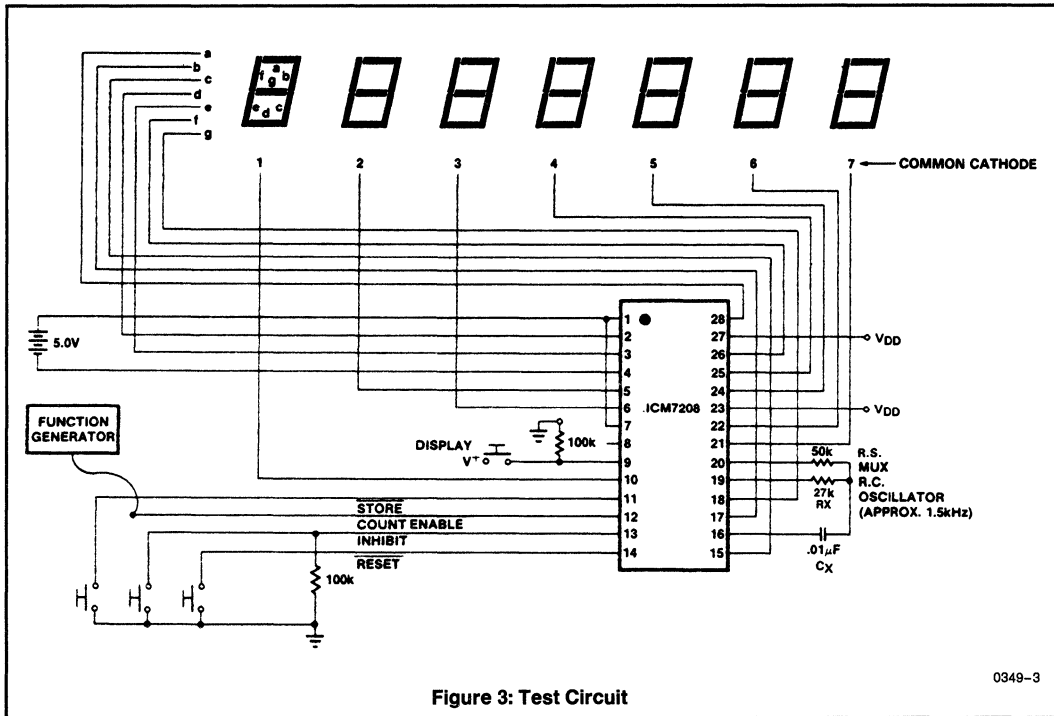
ELECTRICAL CHARACTERISTICS ($V_{DD}=5V, V_{SS}=0V, T_A=25^{\circ}C$, display off, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{Q1}	Quiescent Current	All controls plus terminal 19 connected to V_{DD} No multiplex oscillator		30	300	μA
I_{Q2}	Quiescent Current	All control inputs plus terminal 19 connected to V_{DD} except STORE which is connected to V_{SS}		70	350	
I_{DD1}	Operating Supply Current	All inputs connected to V_{DD} , RC multiplexer osc operating $f_{in} < 25kHz$		210	500	
I_{DD2}	Operating Supply Current	$f_{in} = 2MHz$			700	
V_{SUPPLY}	Supply Voltage Range	$f_{in} \leq 2MHz$	3.5		5.5	
R_{DIG}	Digit Driver On Resistance			4	12	Ω
I_{DIG}	Digit Driver Leakage Current				500	μA
r_{SEG}	Segment Driver On Resistance			40		Ω
I_{SLK}	Segment Driver Leakage Current				500	μA
R_p	Pullup Resistance of RESET or STORE Inputs		100	400		k Ω
R_{IN}	COUNTER INPUT Resistance	Terminal 12 either at V_{DD} or V_{SS}			100	
V_{HIN}	COUNTER INPUT Hysteresis Voltage			25	50	mV

- NOTES:**
- This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
 - The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.
 - The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

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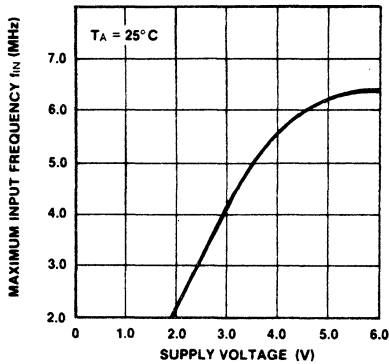
NOTE: All typical values have been characterized but are not tested.



0349-3

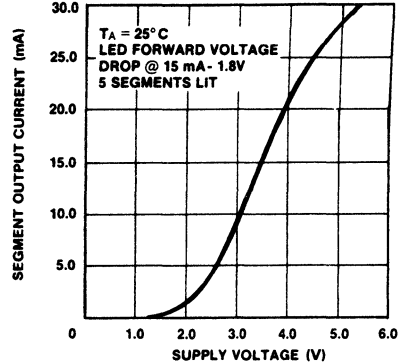
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



0349-4

SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

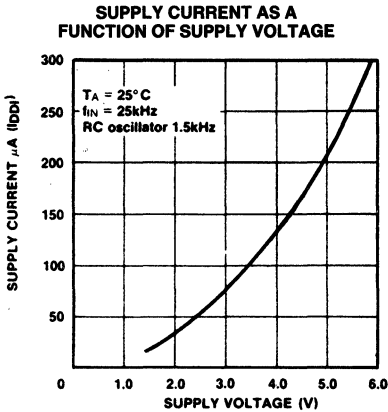


0349-5

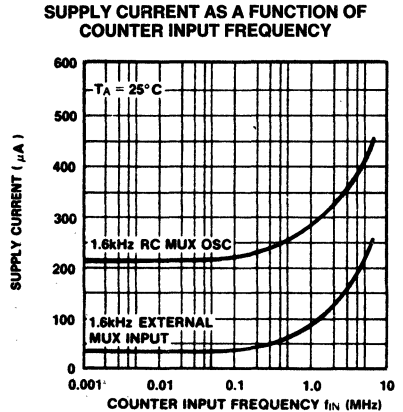
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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



0349-6



0349-7

TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

CONTROL INPUT DEFINITIONS

Input	Terminal	Voltage	Function
1. DISPLAY	9	V _{DD} V _{SS}	Display On Display Off
2. STORE	11	V _{DD} V _{SS}	Counter Information Latched Counter Information Transferring
3. ENABLE	13	V _{DD} V _{SS}	Input to Counter Blocked Normal Operation
4. RESET	14	V _{DD} V _{SS}	Normal Operation Counters Reset

COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

DETAILED DESCRIPTION

Format of Signal to be Counted

The noise immunity of the COUNTER INPUT Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply.

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately 10⁻⁴ V/μs, at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

When driving the input of the ICM7208 from TTL, a 1k-5kΩ pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit current could exceed 150mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with 500μA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

Display Multiplex Rate

The ICM7208 has approximately 0.5μs overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

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NOTE: All typical values have been characterized but are not tested.

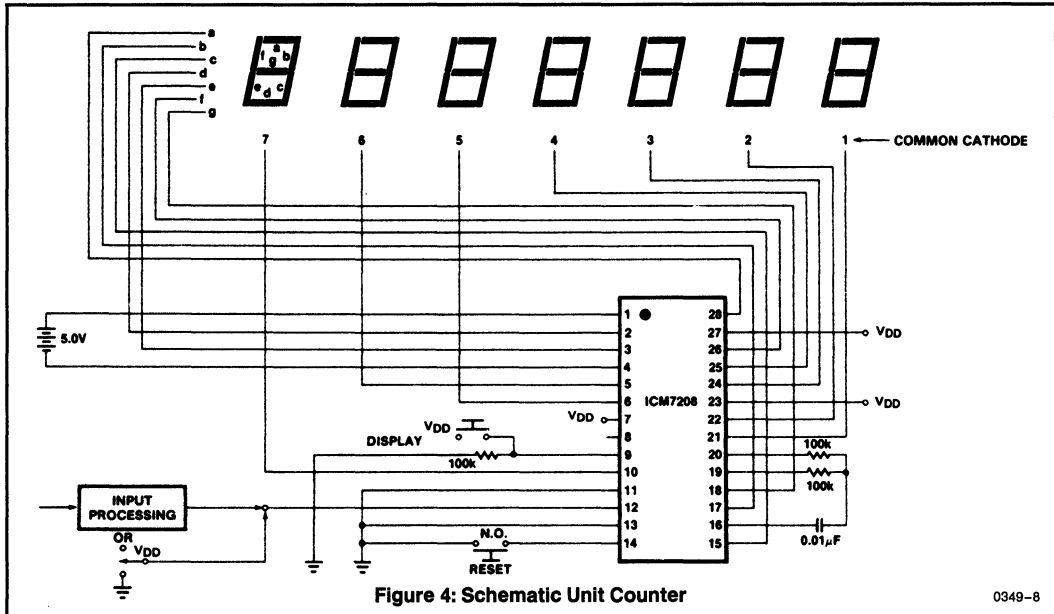


Figure 4: Schematic Unit Counter

0349-8

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input. For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

The multiplex oscillator is eight times the multiplex rate. The frequency is given using the following formula:

$$f = \frac{1}{2.2R_x C_x}$$

R_s should always be $\leq 1M\Omega$ and $R_s = kR_x$ where k is in the range 2-10.

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.

Unit Counter

Figure 4 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4×1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems

due to the SPDT switch the ICM7208 contains an input latch on chip.

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 5). The ICM7207 uses a crystal controlled oscillator to provide the store and reset pulses together with the counting window. Figure 6 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches, and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

Using a 6.5536MHz quartz crystal and the ICM7207 driving the ICM7208, two ranges of counting may be obtained, using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

The ICM7207 provides the multiplex frequency reference of 1.6kHz.

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NOTE: All typical values have been characterized but are not tested.

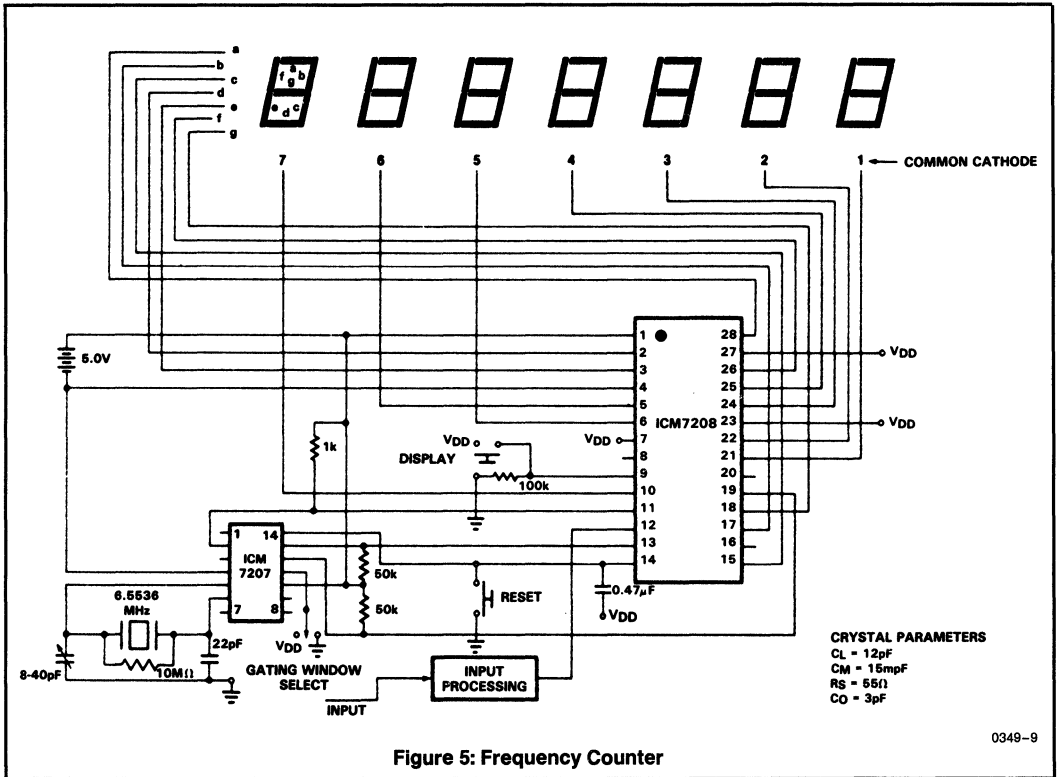


Figure 5: Frequency Counter

Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.

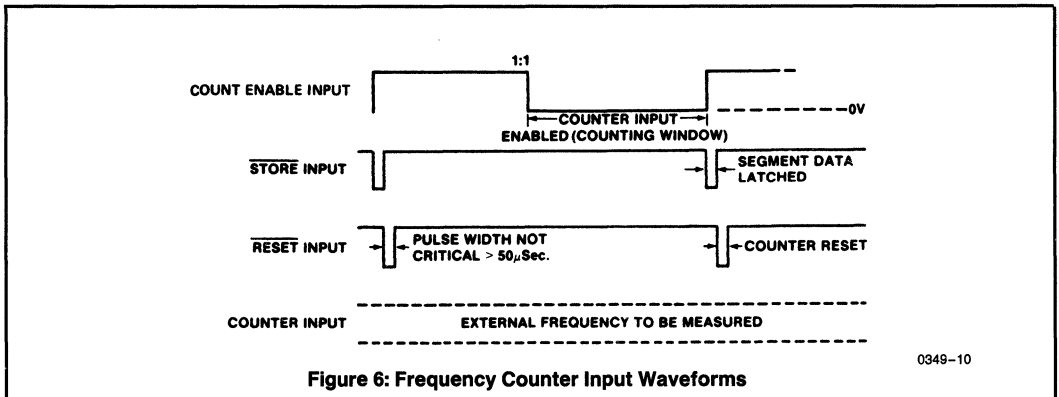


Figure 6: Frequency Counter Input Waveforms

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NOTE: All typical values have been characterized but are not tested.

Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure

8 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 7.

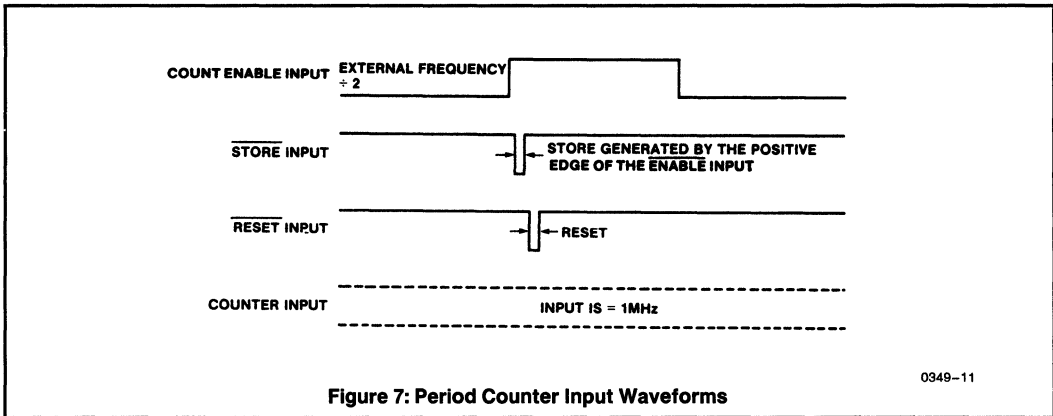


Figure 7: Period Counter Input Waveforms

0349-11

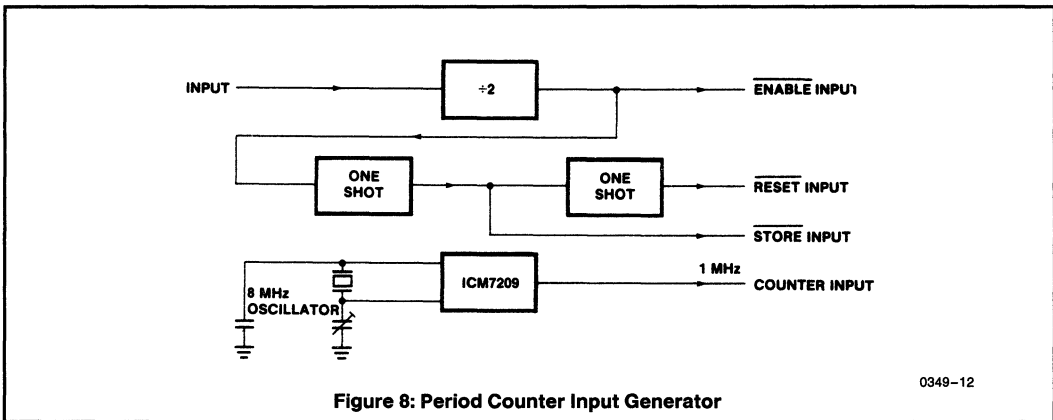


Figure 8: Period Counter Input Generator

0349-12

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NOTE: All typical values have been characterized but are not tested.

ICM7209 Timebase Generator



GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

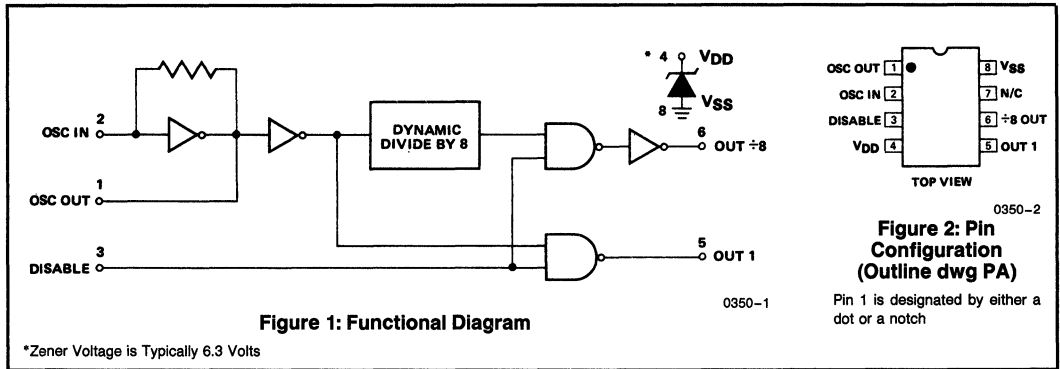
The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7209IJA	-20°C to +85°C	8 pin Cerdip
ICM7209IPA	-20°C to +85°C	8 pin PLASTIC

FEATURES

- High Frequency Operation — 10MHz Guaranteed
- Requires Only A Quartz Crystal and Two Capacitors
- Bipolar, CMOS Compatibility
- High Output Drive Capability — 5×TTL Fanout With 10ns Rise and Fall Times
- Low Power — 50mW at 10MHz
- Choice of Two Output Frequencies — Osc., and Osc. ÷ 8 Frequencies
- Disable Control for Both Outputs
- Wide Industrial Temperature Range — -20°C to +85°C



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V	Power Dissipation (25°C)	300mW
Output Voltages	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	Storage Temperature	-55°C to +125°C
Input Voltages	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	Operating Temperature Range	-20°C to +85°C
		Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD}-V_{SS}=5V$, test circuit, $f_{osc}=10MHz$, $T_A=25^\circ C$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current	Note 1 No Load		11	20	mA
C_D	Disable Input Capacitance			5		pF
I_{ILK}	Disable Input Leakage	Either '1' or '0' state			± 10	μA
V_{OL}	Output Low State	Either OUT 1 or OUT $\div 8$ simulated 5xTTL loads			0.4	V
V_{OH}	Output High State	Either OUT 1 or OUT $\div 8$ simulated 5xTTL loads	4.0	4.9		
t_R	Output Rise Time (Note 3)	Either OUT 1 or OUT $\div 8$ simulated 5xTTL loads		10		ns
t_F	Output Fall Time (Note 3)	Either OUT 1 or OUT $\div 8$ simulated 5xTTL loads		10		
f_{OSC}	Minimum OSC Frequency for $\div 8$ Output	Note 2	2			MHz
	Output $\div 8$ duty cycle	Any operating frequency Low state : High state		7:9		
GM	Oscillator Transconductance		80	200		μS

- NOTES:**
- The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.
 - The $\div 8$ circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.
 - Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

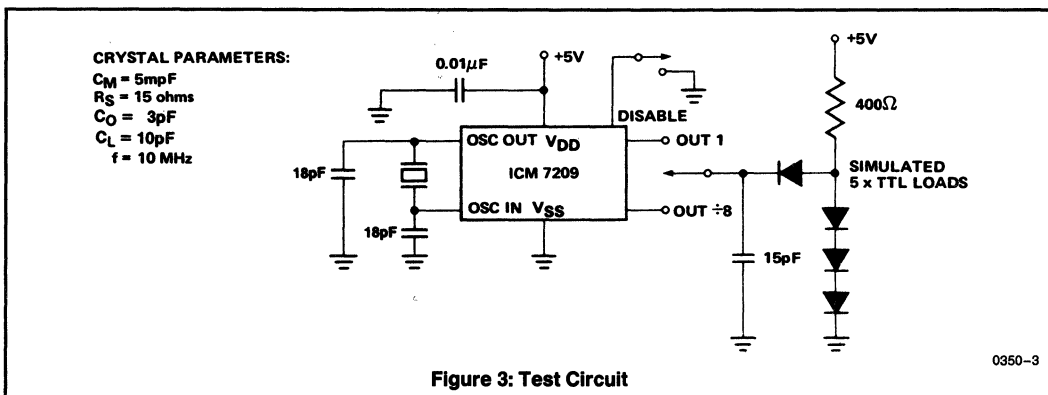
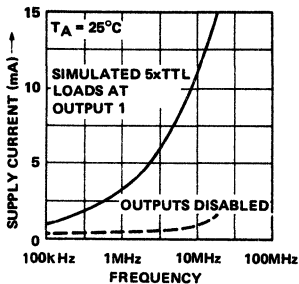
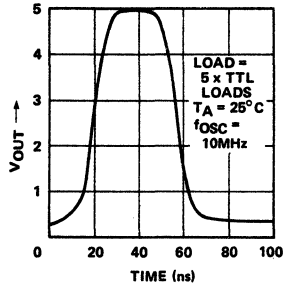


Figure 3: Test Circuit

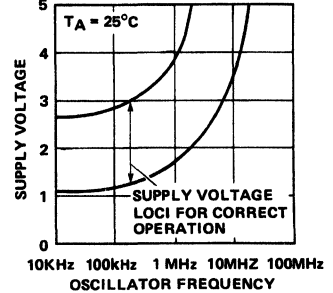
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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS ($V_{DD}-V_{SS}=5V$)

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY

TYPICAL OUT 1 RISE AND FALL TIMES


Rise and fall times of OUT $\div 8$ are similar to those of OUT 1.

SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF $\div 8$ COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY.

DETAILED DESCRIPTION
OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10kHz) to 10MHz.

The oscillator circuit consumes about $500\mu A$ of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

THE $\div 8$ OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to

store voltage levels instead of latches (which are used in static dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see TYPICAL PERFORMANCE CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consist of CMOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other CMOS gates operating with a 5 volt supply, or TTL compatible MOS gates. The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be dramatically reduced.

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NOTE: All typical values have been characterized but are not tested.

ICM7215

6-Digit LED Display

4-Function Stopwatch



ICM7215

GENERAL DESCRIPTION

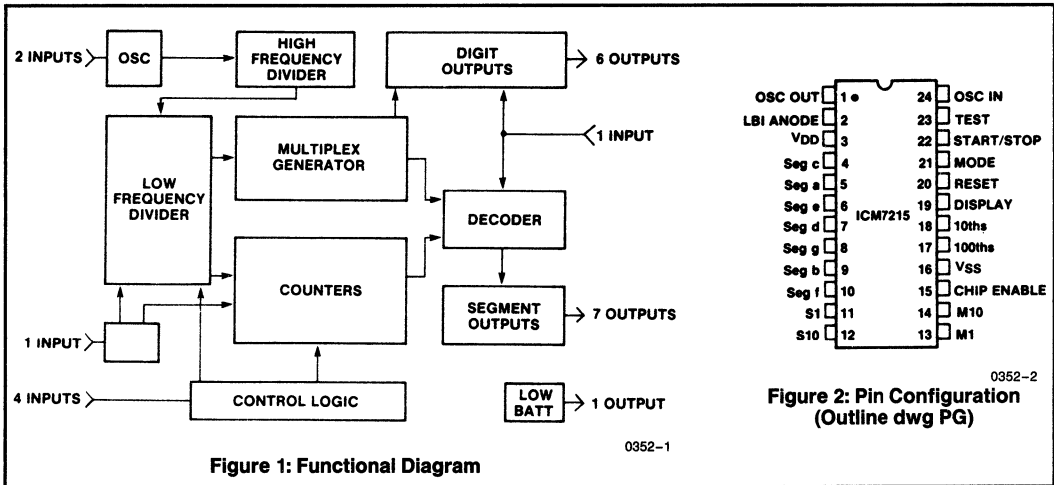
The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED. The only components required for a complete stopwatch are the display, three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an ON-OFF switch. For a two function stopwatch, or to add a display off feature, one additional slide switch is required. The circuit divides the oscillator frequency by 2^{15} to obtain 100Hz, which is fed to the fractional seconds, seconds and minutes counters, while an intermediate frequency is used to obtain the 1/6 duty cycle 1.07kHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP.

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICM7215IPG	0°C to +70°C	24-Pin PLASTIC DIP
ICM7215/D	—	DICE

FEATURES

- **Four Functions:** Start/Stop/Reset, Split, Taylor, Time Out
- **Six Digit Display:** Ranges Up to 59 Minutes 59.99 Seconds
- **High LED Drive Current:** 13mA Peak Per Segment at 16.7% Duty Cycle With 4.0 Volt Supply
- **Requires Only Three Low Cost SPST Switches Without Loss of Accuracy:** Start/Stop, Reset, Display Unlock
- **Chip Enable Pin Turns Off Both Segment and Digit Outputs; Can Be Used for Multiple Circuits Driving One Display**
- **Low Battery Indicator**
- **Digit Blanking On Seconds and Minutes**
- **Wide Operating Range:** 2.0 to 5.0 Volts
- **1kHz Multiplex Rate Prevents Flickering Display**
- **Can Be Used Easily In Four Different Single Function Stopwatches or Two Two-Function Stopwatches:** Start/Stop/Reset With Time-out, Split With Taylor. The Component Count for A Three- or Four-Function Stopwatch Will Be Slightly Greater
- **Retrofit to ICM7205 for Split and/or Taylor Applications**



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS})	5.5V	Storage Temperature	-65°C to +150°C
Power Dissipation (Note 1)	0.75W	Input Voltage	($V_{SS}-0.3V$) to ($V_{DD}+0.3V$)
Operating Temperature	0°C to +70°C	Output Voltage	V_{SS} to V_{DD}

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: ($T_A = +25^\circ\text{C}$, stopwatch circuit, $V_{DD} = 4.0V$, $V_{SS} = 0V$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SUPPLY}	Supply Voltage ($V_{DD} - V_{SS}$)	$-20^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	2.0		5.0	V
I_{DD}	Supply Current	Display off		0.6	1.5	mA
I_{SEG}	Segment Current Peak Average	5 segments lit 1.8 Volts across display	9.0	13.2 2.2		
I_{SW}	Switch Actuation Current	All inputs except CHIP ENABLE		20	50	μA
	Switch Actuation Current	Chip enable		50	200	
I_{DLK}	Digit Leakage Current	$V_{DIG} = 2.0V$			50	
I_{SLK}	Segment Leakage Current	$V_{SEG} = 2.0V$			100	
V_{LBI}	Low Battery Indicator Trigger Voltage		2.2		2.8	V
I_{LBI}	LBI Output Current	$V_{DD} = 2.0V$, $V_{LBI} = 1.6V$		2.0		mA
f_{STAB}	Oscillator Stability	$V_{DD} = 2.0V$ to $V_{DD} = 5.0V$		6		ppm
g_m	Oscillator Transconductance	$V_{DD} = 2.0V$	120			μS
C_{OSCI}	Oscillator Input Capacitance			30		pF

NOTE: 1. The output devices on the ICM7215 have very low impedance characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA.

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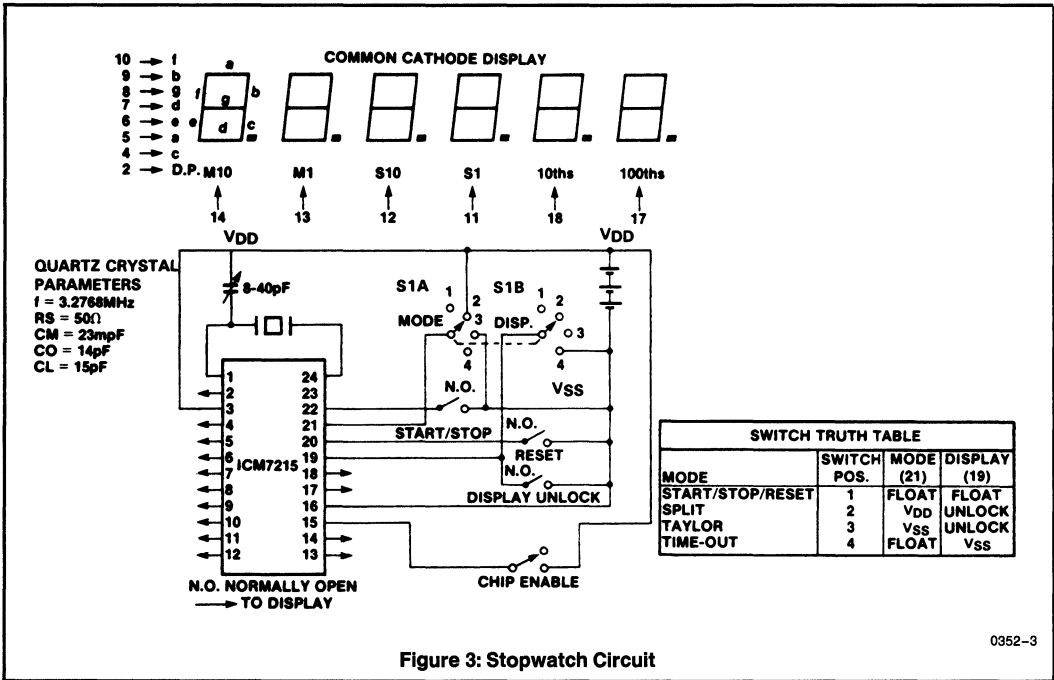
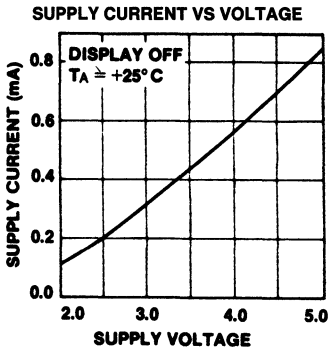


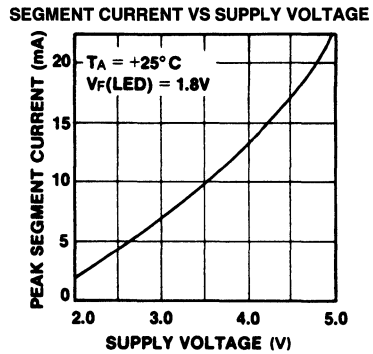
Figure 3: Stopwatch Circuit

0352-3

TYPICAL PERFORMANCE CHARACTERISTICS



0352-4

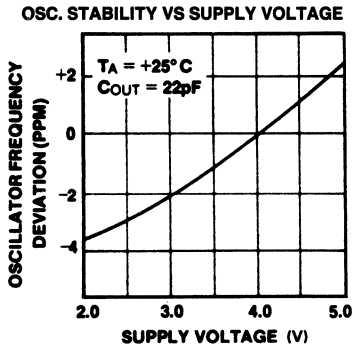


0352-5

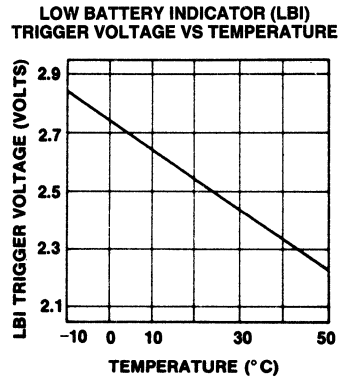
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NOTE: All typical values have been characterized but are not tested.

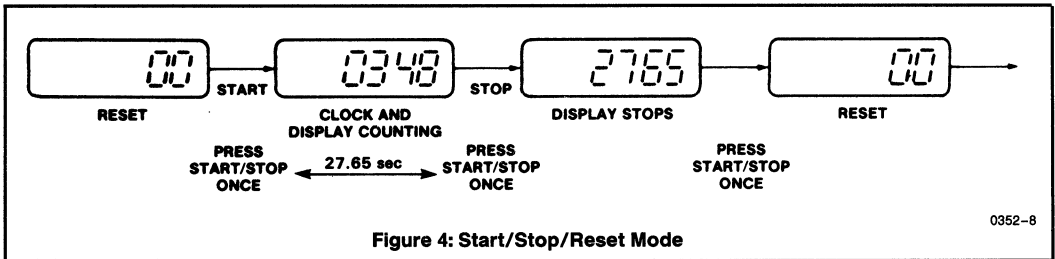
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



0352-6



0352-7



0352-8

DETAILED DESCRIPTION
FUNCTIONAL OPERATION

Turning on the stopwatch will bring up the reset state with the fractional seconds displaying 00 and the other digits blanked. This display always indicates that the stopwatch is ready to go.

The display can be turned off in any mode by connecting the CHIP ENABLE input to V_{DD} .

START/STOP/RESET MODE

When the MODE input is floating and the DISPLAY input is floating or connected to V_{DD} the circuit is in the Start/Stop/Reset mode. (Figure 4).

The Start/Stop/Reset mode can be used for single event timing in a one-button stopwatch; an additional switch can be used to provide an instant reset. To time another event, the display must be reset before the start of the event. Seconds will be displayed after one second, minutes after one minute. The range of the stopwatch is 59 minutes 59.99 seconds, and if an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.

TAYLOR OR SEQUENTIAL MODE

When the MODE input is connected to V_{SS} , the stopwatch is in the Taylor or Sequential mode. (Figure 5).

Each split time is measured from zero in the Taylor mode; i.e., after stopping the watch, the counters reset momentarily and start counting the next interval. The time displayed is that elapsed since the last activation of START/STOP. The display is stationary after the first interval unless the display unlock is used, by connecting the DISPLAY input to V_{SS} , to show the running clock. RESET can be used at any time.

SPLIT MODE

When the MODE input is connected to V_{DD} the stopwatch is in the Split mode. (Figure 6).

The Split mode differs from the Taylor in that the lap times are cumulative in the Split mode. The counters do not reset or stop after the first start until RESET is activated. Time displayed is the cumulative time elapsed since the first start after reset. Display unlock can be used, by connecting the DISPLAY input to V_{SS} , to let the display 'catch up' with the clock, and RESET can be used at any time.

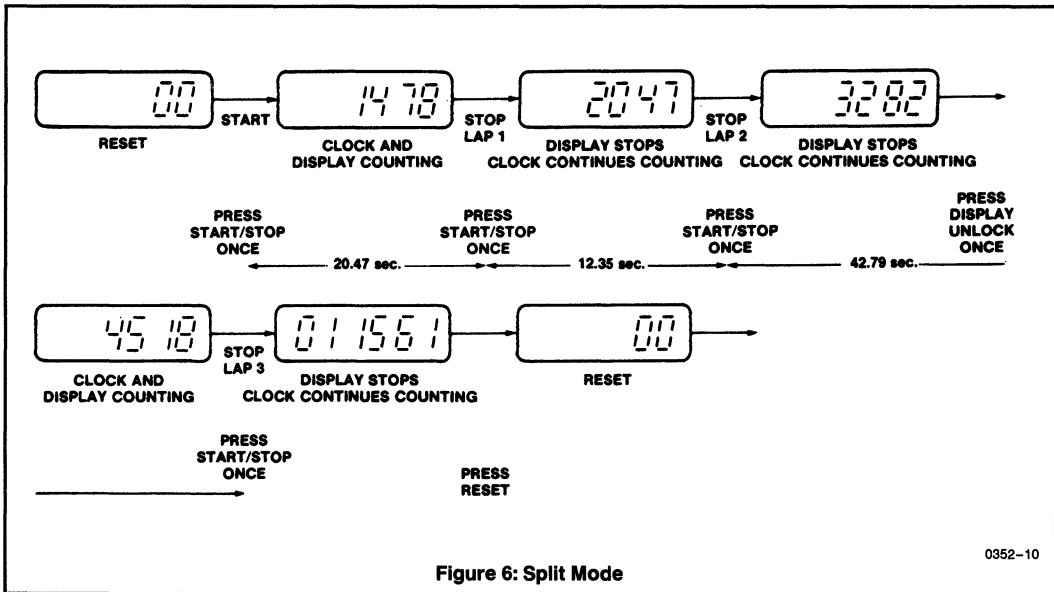
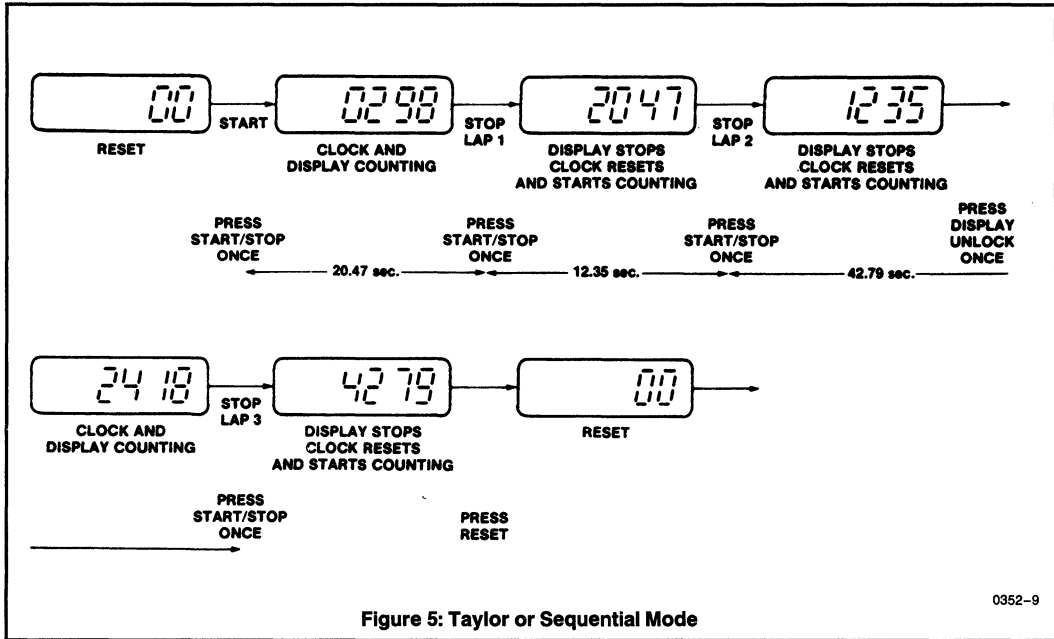
TIME OUT MODE

When the MODE input is floating and the DISPLAY input is tied to V_{SS} , the stopwatch is in the Time-out mode. (Figure 7).

In the Time-out mode the clock and display alternately start and stop with activations of the START/STOP switch. RESET can be used at any time. The display unlock button is bypassed in this mode.

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NOTE: All typical values have been characterized but are not tested.



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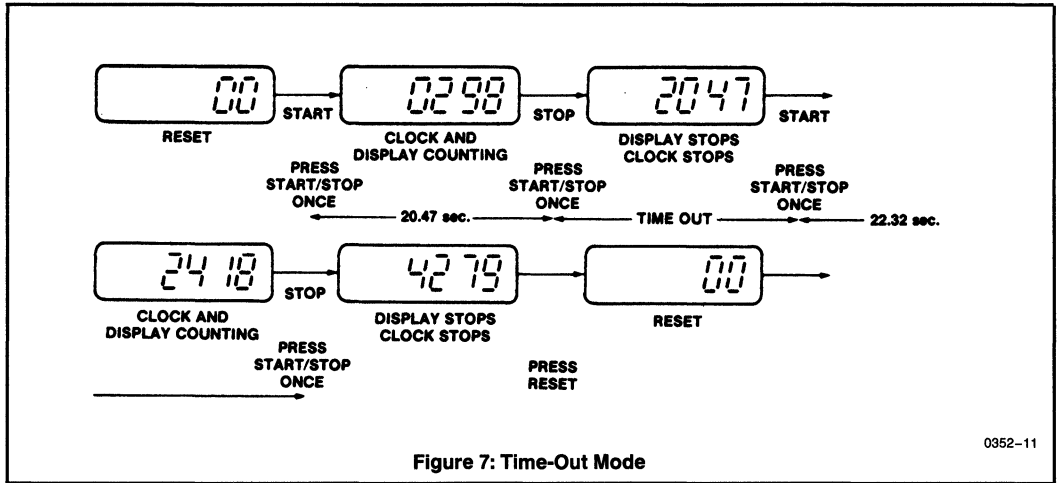


Figure 7: Time-Out Mode

0352-11

APPLICATION NOTES
LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers which will typically source 2mA of current. The threshold voltage is approximately 2.5 volts at room temperature. Normal AA type batteries will provide many hours of accurate timekeeping after the indicator comes on, however the wide voltage spread between the LBI threshold voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

CHIP ENABLE

The CHIP ENABLE input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the CHIP ENABLE input is floating or connected to V_{SS}, the display is enabled, and when the tied to V_{DD} the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the Taylor mode. The circuit, Figure 8, shows how the user can obtain lap and cumulative readings of the same event.

SWITCH CHARACTERISTICS

The ICM7215 is designed for use with SPST switches throughout. On the DISPLAY and RESET inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any length of time however short. Switch bounce on these inputs does not need to be specified. The START/STOP input, however, responds to an edge and so requires a switch with less than 15ms of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.

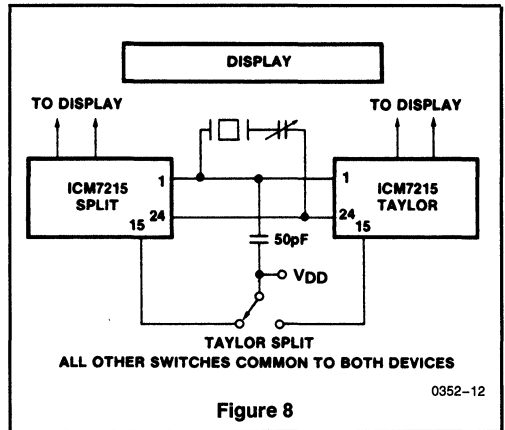


Figure 8

0352-12

LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to the 7215. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

OSCILLATOR DESIGN

The oscillator of the ICM7215 includes all components on chip except the 3.2768MHz crystal and the trimming capacitor. The oscillator input capacitance has a nominal value of 30pF, and the circuit is designed to work with a crystal with a load capacitance of approximately 15pF. If the crystal has

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NOTE: All typical values have been characterized but are not tested.

characteristics as shown in the Typical Performance Characteristics, an 8 – 40pF trimming capacitor will be adequate for a tuning tolerance of ± 30 PPM on the crystal. If the crystal's static capacitance is significantly lower, a narrower trimming range may be selected.

After deciding on a crystal and a nominal load capacitance, take the worst case values of C_{in} , C_{out} and R_S and calculate the g_m required by:

$$g_m = \omega^2 C_{in} C_{out} R_S \left[1 + \frac{C_o (C_{in} + C_{out})}{C_{in} C_{out}} \right]^2$$

C_o = static capacitance

R_S = series resistance

C_{in} = input capacitance

C_{out} = output capacitance

$\omega = 2\pi \times$ crystal frequency

The resulting g_m should be less than half the g_m specified for the device. If it is not, a lower value of crystal series resistance and/or load capacitance should be specified.

OSCILLATOR TUNING

Tuning can be accomplished by using the 10th or 100th seconds with the device reset. The frequency on the cath-

ode should be tuned to 1066.667Hz, which is equivalent to a period of 937.5 microseconds. Note that a frequency counter cannot be connected directly to the oscillator because of possible loading.

TEST

The TEST input is used for high speed testing of the device. When the input is pulsed low, a latch is set which speeds up counting by a factor of 32; each pulse on the TEST input rapidly advances both minutes and seconds in a parallel mode. To accurately rapid advance the signal applied to the TEST input must be free of switch bounce. The circuit is taken out of the test mode by using either RESET or START/STOP.

REPLACING THE ICM7205 WITH THE ICM7215

The ICM7215 is designed to be compatible with circuits using the ICM7205. If the 7205 is used only in the Split mode no changes are required. If the 7205 is used in the Taylor mode and the Split-Taylor input (pin 21) is left open, a jumper from pin 21 to V_{SS} must be added when converting to the 7215. A jumper may also be needed if the 7205 is used with a Split/Taylor switch. Once the jumper has been added the board can be used with either device.

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NOTE: All typical values have been characterized but are not tested.

ICM7216A/B/C/D

8-Digit Multi-Function Frequency Counter/Timer



GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Timer Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μ s resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in μ s. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7216AII	-25°C to +85°C	28 pin CERDIP
ICM7216BII	-25°C to +85°C	28 pin PLASTIC DIP
ICM7216BIJ	-25°C to +85°C	28 pin CERDIP
ICM7216CIJ	-25°C to +85°C	28 pin CERDIP
ICM7216DII	-25°C to +85°C	28 pin PLASTIC DIP
ICM7216DIJ	-25°C to +85°C	28 pin CERDIP

FEATURES

ALL VERSIONS:

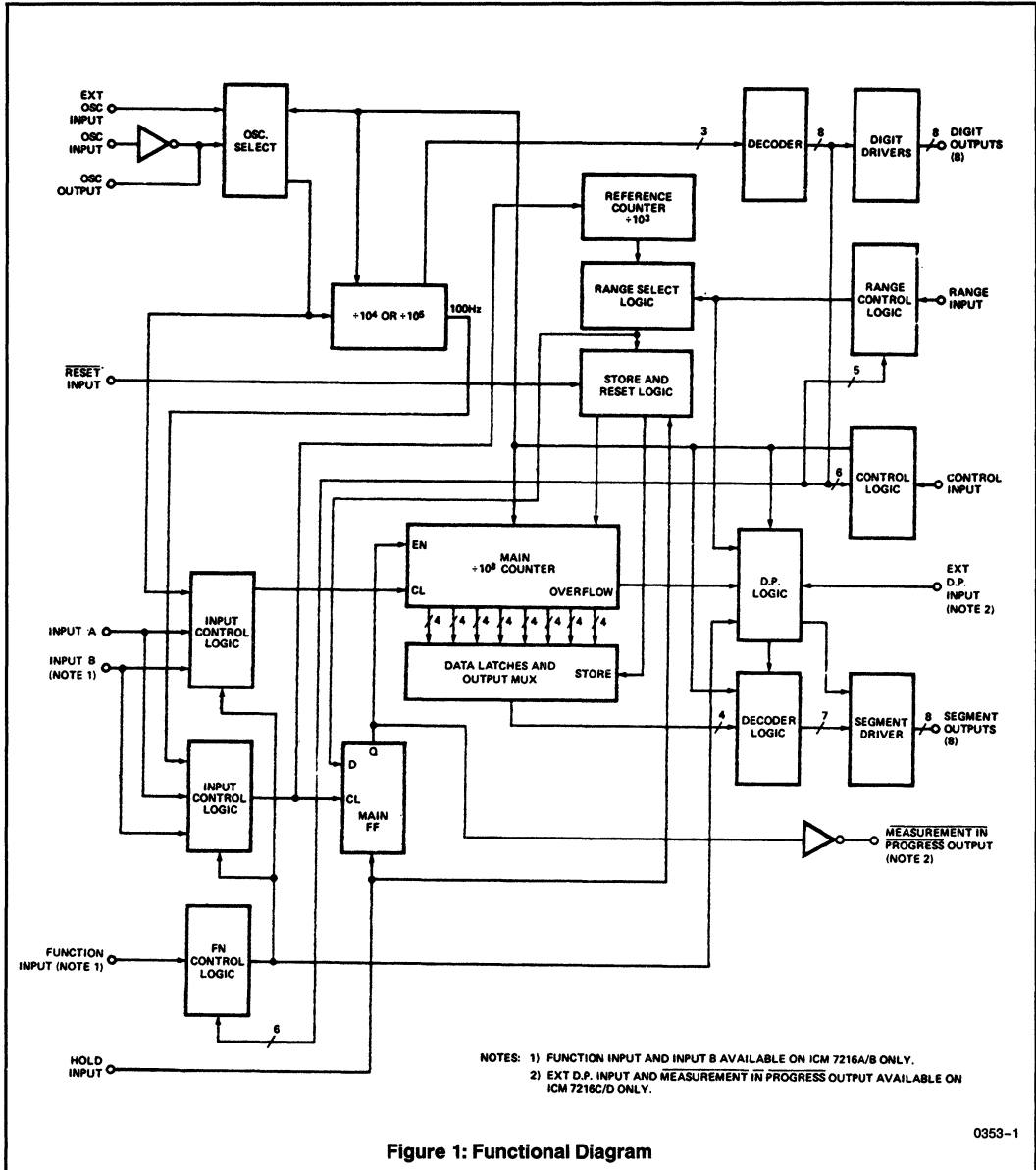
- Functions as a Frequency Counter (DC to 10MHz)
- Four Internal Gate Times: 0.01 Sec, 0.1 Sec, 1 Sec, 10 Sec in Frequency Counter Mode
- Directly Drives Digits and Segments of Large Multiplexed LED Displays (Common Anode and Common Cathode Versions)
- Single Nominal 5V Supply Required
- Highly Stable Oscillator, Uses 1MHz or 10MHz Crystal
- Internally Generated Decimal Points, Interdigit Blanking, Leading Zero Blanking and Overflow Indication
- Display Off Mode Turns Off Display and Puts Chip Into Low Power Mode
- Hold and Reset Inputs for Additional Flexibility

ICM7216A AND ICM7216B

- Functions Also as a Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter
- 1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes
- Measures Period From 0.5 μ s to 10s

ICM7216C AND ICM7216D

- Decimal Point and Leading Zero Blanking May Be Externally Selected



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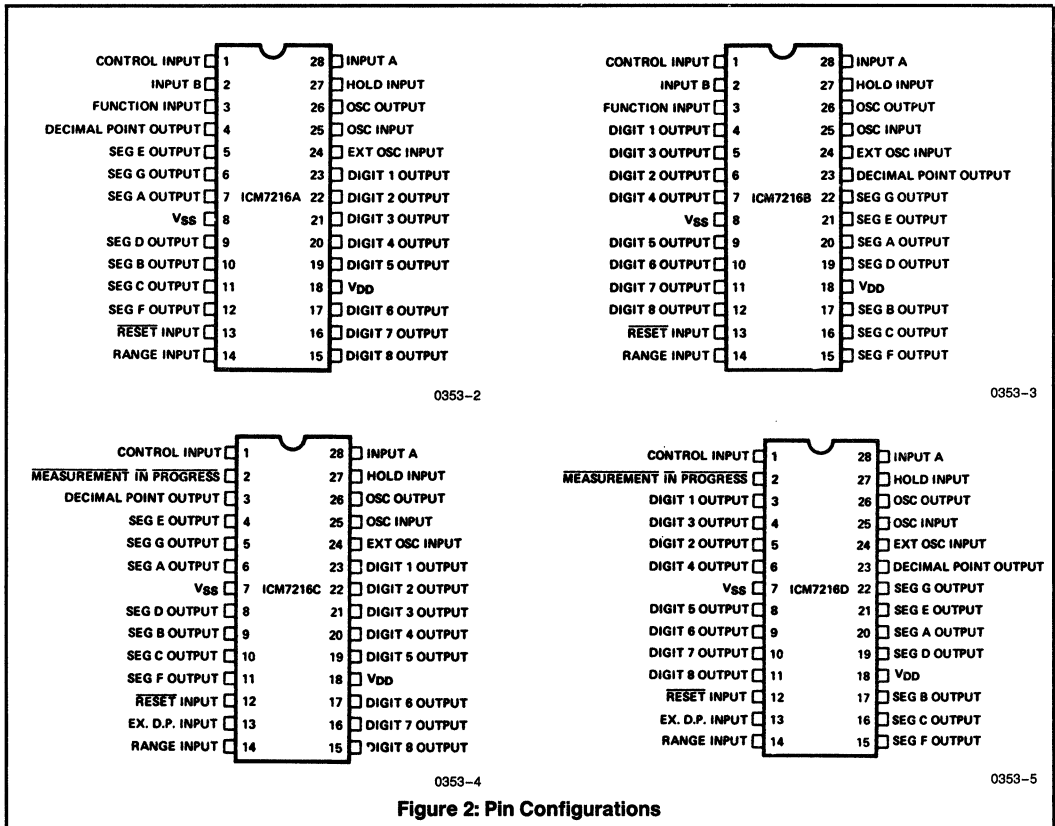
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V_{DD} - V_{SS}$)	6.5V
Maximum Digit Output Current	400mA
Maximum Segment Output Current	60mA
Voltage On Any Input or Output Terminal[1]	($V_{DD} + 0.3V$) to ($V_{SS} - 0.3V$)
Maximum Power Dissipation at 70°C	1.0W (ICM7216A & C) 0.5W (ICM7216B & D)
Operating Temperature Range	-25°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V_{DD} to V_{SS} by more than 0.3 volts.



EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIJL (Common Anode LED Display), a 10MHz

quartz crystal, eight 7 segment 0.3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (ICM7216A/B)

($V_{DD}=5.0V$, $V_{SS}=0$, $T_A=25^{\circ}C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216A/B						
I_{DD}	Operating Supply Current	Display Off, Unused Inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range ($V_{DD}-V_{SS}$)	INPUT A, INPUT B Frequency at f_{max}	4.75		6.0	V
$f_{A(max)}$	Maximum Frequency INPUT A, Pin 28	Figure 3, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5			MHz MHz
$f_{B(max)}$	Maximum Frequency INPUT B, Pin 2	Figure 4	2.5			MHz
	Minimum Separation INPUT A to INPUT B Time Interval Function	Figure 5	250			ns
f_{osc}	Maximum Osc. Freq. and Ext. Osc. Frequency		10			MHz
f_{osc}	Minimum Ext. Osc. Freq.				100	kHz
g_m	Oscillator Transconductance	$V_{DD}=4.75V$, $T_A=+85^{\circ}C$	2000			μs
f_{mux}	Multiplex Frequency	$f_{osc}=10MHz$		500		Hz
	Time Between Measurements	$f_{osc}=10MHz$		200		ms
V_{INL} V_{INH}	Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage		3.5		1.0	V V
R_{IN}	Input Resistance to V_{DD} Pins 13,24	$V_{IN}=V_{DD}-1.0V$	100	400		k Ω
I_{ILK}	Input Leakage Pin 27,28,2				20	μA
dV_{IN}/dt	Input Range of Change	Supplies Well Bypassed		15		mV/ μs
ICM7216A						
I_{OH} I_{OL}	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	$V_{OUT}=V_{DD}-2.0V$ $V_{OUT}=V_{SS}+1.0V$	-140	-180 0.3		mA mA
I_{OL} I_{OH}	Segment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	$V_{OUT}=V_{SS}+1.5V$ $V_{OUT}=V_{DD}-2.5V$	20	35 -100		mA μA
V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V_{SS}	$V_{IN}=V_{SS}+1.0V$	2.0 50	100	0.8	V V k Ω

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ELECTRICAL CHARACTERISTICS (ICM7216A/B)

 ($V_{DD}=5.0V$, $V_{SS}=0$, $T_A=25^{\circ}C$, unless otherwise specified.) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216B						
I_{OL} I_{OH}	Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	$V_{OUT}=V_{SS}+1.3V$ $V_{OUT}=V_{DD}-2.5V$	50	75 -100		mA μA
I_{OH} I_{SLK}	Segment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	$V_{OUT}=V_{DD}-2.0V$ $V_{OUT}=V_{DD}-2.5V$	-10		10	mA μA
V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V_{DD}	$V_{IN}=V_{DD}-2.5V$	$V_{DD}-0.8$ 100	360	$V_{DD}-2.0$	V V k Ω

ELECTRICAL CHARACTERISTICS (ICM7216C/D)

 ($V_{DD}=5.0V$, $V_{SS}=0$, $T_A=25^{\circ}C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216C/D						
I_{DD}	Operating Supply Current	Display Off, Unused Inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range ($V_{DD}-V_{SS}$)	INPUT A Frequency at f_{max}	4.75		6.0	V
$f_{A(max)}$	Maximum Frequency INPUT A, Pin 28	Figure 3	10			MHz
f_{osc}	Maximum Osc. Freq. and Ext. Osc. Frequency		10			MHz
f_{osc}	Minimum Ext. Osc. Freq.				100	kHz
g_m	Oscillator Transconductance	$V_{DD}=4.75V$, $T_A=+85^{\circ}C$	2000			μs
f_{mux}	Multiplex Frequency	$f_{osc}=10MHz$		500		Hz
	Time Between Measurements	$f_{osc}=10MHz$		200		ms
V_{INL} V_{INH}	Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage		3.5		1.0	V V
R_{IN}	Input Resistance to V_{DD} Pins 12,24	$V_{IN}=V_{DD}-1.0V$	100	400		k Ω
I_{ILK}	Input Leakage Pin 27, Pin 28				20	μA
I_{OL}	Output Current	$V_{OL}=+.4V$	0.36			mA
I_{OH}	Pin 2	$V_{OH}=V_{DD}-0.8V$	265			μA
dV_{IN}/dt	Input Rate of Change	Supplies Well Bypassed		15		mV/ μs

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NOTE: All typical values have been characterized but are not tested.

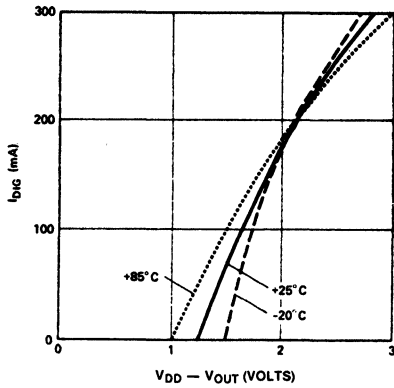
ELECTRICAL CHARACTERISTICS (ICM7216C/D)

($V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = 25^\circ C$, unless otherwise specified.) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216C						
I_{OH} I_{OL}	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	$V_{OUT} = V_{DD} - 2.0V$ $V_{OUT} = V_{SS} + 1.0V$	-140	-180 0.3		mA mA
I_{OL} I_{OH}	Segment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	$V_{OUT} = V_{SS} + 1.5V$ $V_{OUT} = V_{DD} - 2.5V$	20	30 -100		mA μA
V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V_{SS}	$V_{IN} = +1.0V$	2.0 50	100	0.8	V V k Ω
ICM7216D						
I_{OL} I_{OH}	Digit Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	$V_{OUT} = +1.3V$ $V_{OUT} = V_{DD} - 2.5V$	50	75 100		mA μA
I_{OH} I_{SLK}	Segment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	$V_{OUT} = V_{DD} - 2.0V$ $V_{OUT} = V_{DD} - 2.5V$	10	15	10	mA μA
V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V_{DD}	$V_{IN} = V_{DD} - 1.0V$	$V_{DD} - 0.8$ 100	360	$V_{DD} - 2.0$	V V k Ω

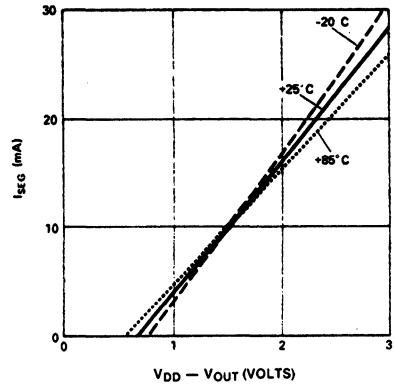
TYPICAL PERFORMANCE CHARACTERISTICS

ICM7216A & C Typical I_{DIG} vs. $V_{DD} - V_{OUT}$, $4.5 \leq V_{DD} \leq 6.0V$



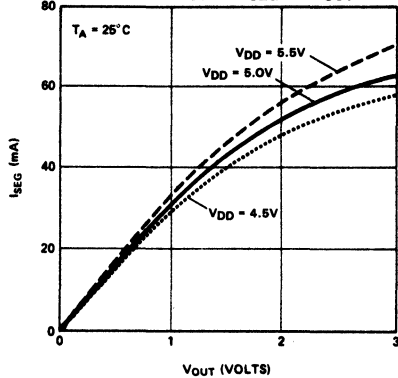
0353-6

ICM7216B & D Typical I_{SEG} vs. $V_{DD} - V_{OUT}$, $4.5 \leq V_{DD} \leq 6.0V$



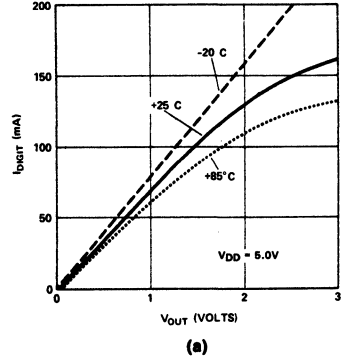
0353-7

ICM7216A & C Typical I_{SEG} vs. V_{OUT}

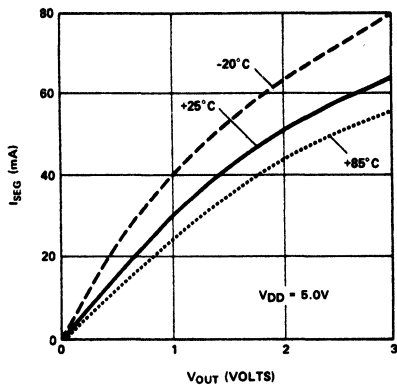


0353-8

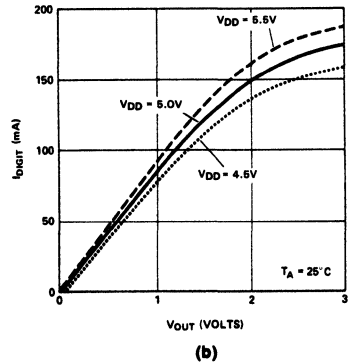
ICM7216B & D Typical I_{DIGIT} vs. V_{OUT}



(a)



0353-9

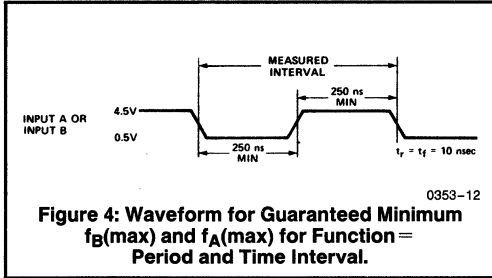
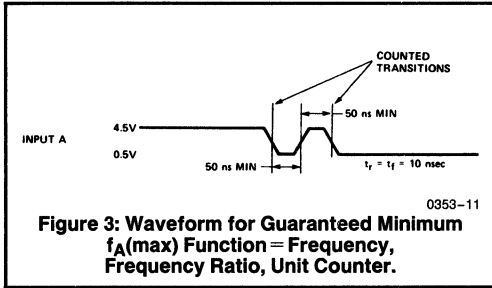


(b)

0353-10

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NOTE: All typical values have been characterized but are not tested.



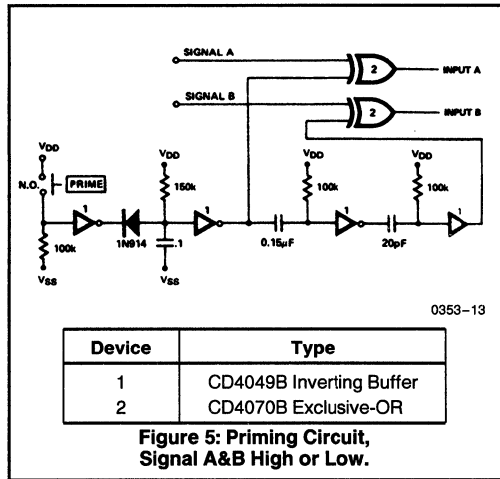
TIME INTERVAL MEASUREMENT

The ICM7216A/B can be used to accurately measure the time interval between two events. With a 10MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7216A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

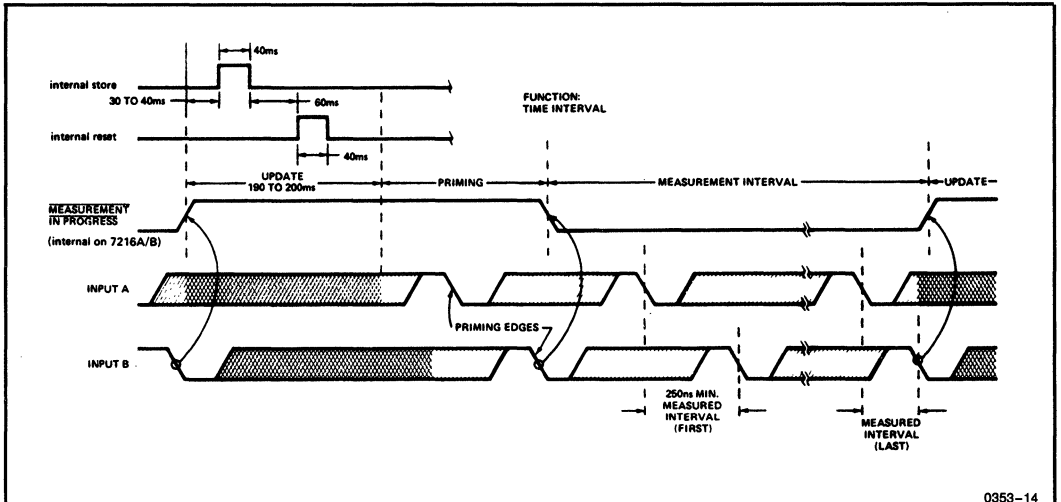
This can be easily accomplished with the following circuit: (Figure 5).



Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A/B as the first alternating signal states automatically prime the device. See Figure 5.

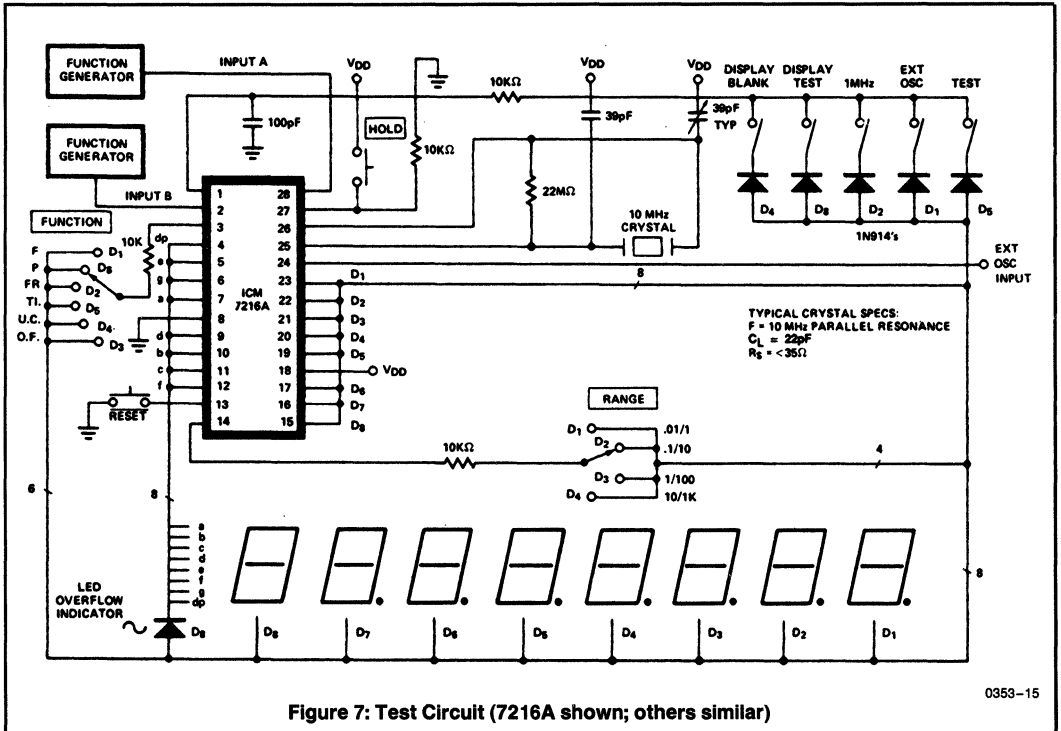
During any time interval measurement cycle, the ICM7216A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.



0353-14

NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

Figure 6: Waveforms for Time Interval Measurement (Others are similar, but without priming phase).

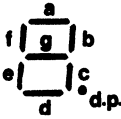


0353-15

Figure 7: Test Circuit (7216A shown; others similar)

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0353-16

Overflow will be indicated on the decimal point output of digit 8.
A separate LED overflow indicator can be connected as follows:



0353-17

	Cathode	Anode
ICM7216A/C	DEC. PT.	D ₈
ICM7216B/D	D ₈	DEC. PT.

Figure 8: Segment Identification and Display Font

DETAILED DESCRIPTION

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A/B).

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125µs). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

CONTROL INPUT Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Blank Display is selected at the same time.

Display Off — To disable the drivers, it is necessary to tie D₄ to the CONTROL INPUT and have the HOLD input at V_{DD}. The chip will remain in this "Display Off" mode until HOLD is switched back to V_{SS}. While in the "Display Off" mode, the segment and digit driver outputs are open, the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal, and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V_{SS}. Segment and Digit Drive outputs may thus be bussed to drive a common display (up to 6 circuits).

1MHz Select — The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in µs increments rather than 0.1µs increments.

External Oscillator Enable — In this mode the EXTERNAL OSCILLATOR INPUT is used instead of the on-chip oscillator for Timebase input and Main Counter input in **period** and **time interval modes**. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself to enable the on-chip oscillator. OSCillator INPUT (pin 25) must also be connected to EXT.OSC. input when using EXT.OSC. input.

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to EXTERNAL DECIMAL POINT input is active. Leading Zero Blanking will be disabled for all digits following the decimal point (7216C/D only).

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NOTE: All typical values have been characterized but are not tested.

RANGE INPUT

The RANGE INPUT selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except **unit counter** a change in the RANGE INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

Table 1: Multiplexed Input Functions

	Function	Digit
FUNCTION INPUT Pin 3 (ICM7216A & B Only)	Frequency	D ₁
	Period	D ₈
	Frequency Ratio	D ₂
	Time Interval	D ₅
	Unit Counter	D ₄
	Oscillator Frequency	D ₃
RANGE INPUT Pin 14	.01 sec/1 Cycle	D ₁
	.1 sec/10 Cycles	D ₂
	1 sec/100 Cycles	D ₃
	10 sec/1K Cycles	D ₄
CONTROL INPUT Pin 1	Blank Display	D ₄ and Hold
	Display Test	D ₈
	1 MHz Select	D ₂
	External Oscillator Enable	D ₁
	External Decimal Point Enable	D ₃
EXT. D.P. INPUT Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

FUNCTION INPUT

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency**. This input is available on the ICM7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the Reference Counter, as shown in Table 2. In all cases, only 1 → 0 transitions are counted or timed. In **time interval**, a flip-flop is toggled first by a 1 → 0 transition of INPUT A and then by a 1 → 0 transition of INPUT B. The oscillator is gated into the Main Counter from the time INPUT A toggles the flip-flop until INPUT B toggles it. In **unit counter** mode, the main counter contents are continuously displayed. A change in the FUNCTION INPUT will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed.

Table 2: 7216A/B Input Routing

Description	Main Counter	Reference Counter
Frequency (f_A)	Input A	100 Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A → B)	Osc • (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator $\div 10^5$ or 10^4)

EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected this input is active. Any of the digits, except D₈, can be connected to this point. D₈ should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

HOLD Input — Except in the **unit counter** mode, when the HOLD Input is at V_{DD}, any measurement in progress (before STORE goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

RESET Input — The **RESET** input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244 μ s. An interdigit blanking time of 6 μ s is used to prevent ghosting between digits. The decimal point and leading zero blanking assume right hand decimal point displays, and zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows. Overflow is indicated by the decimal point on digit 7 turning on.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. The Typical Performance Characteristics curves show the digit and segment currents as a function of output voltage.

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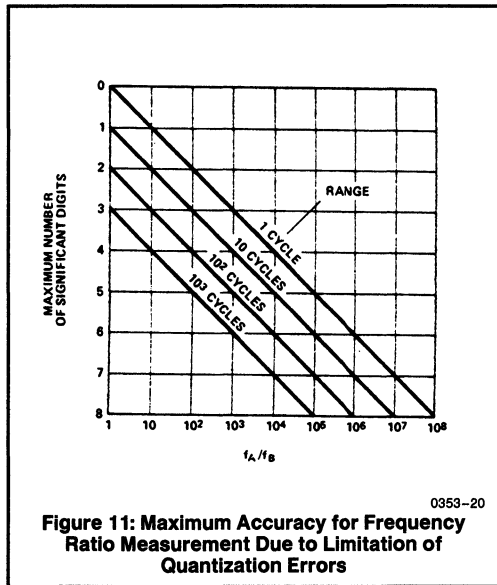
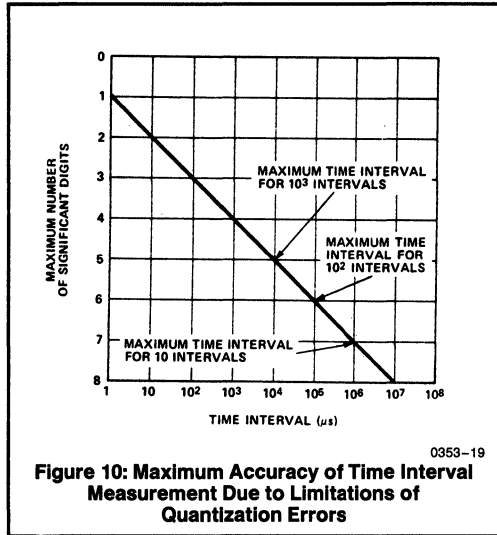
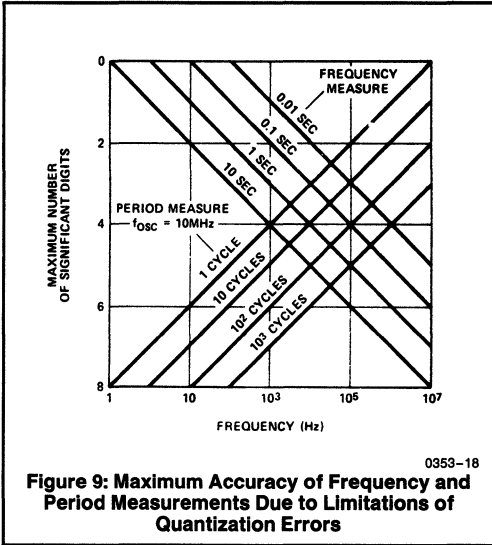
To get additional brightness out of the displays, V_{DD} may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

ACCURACY

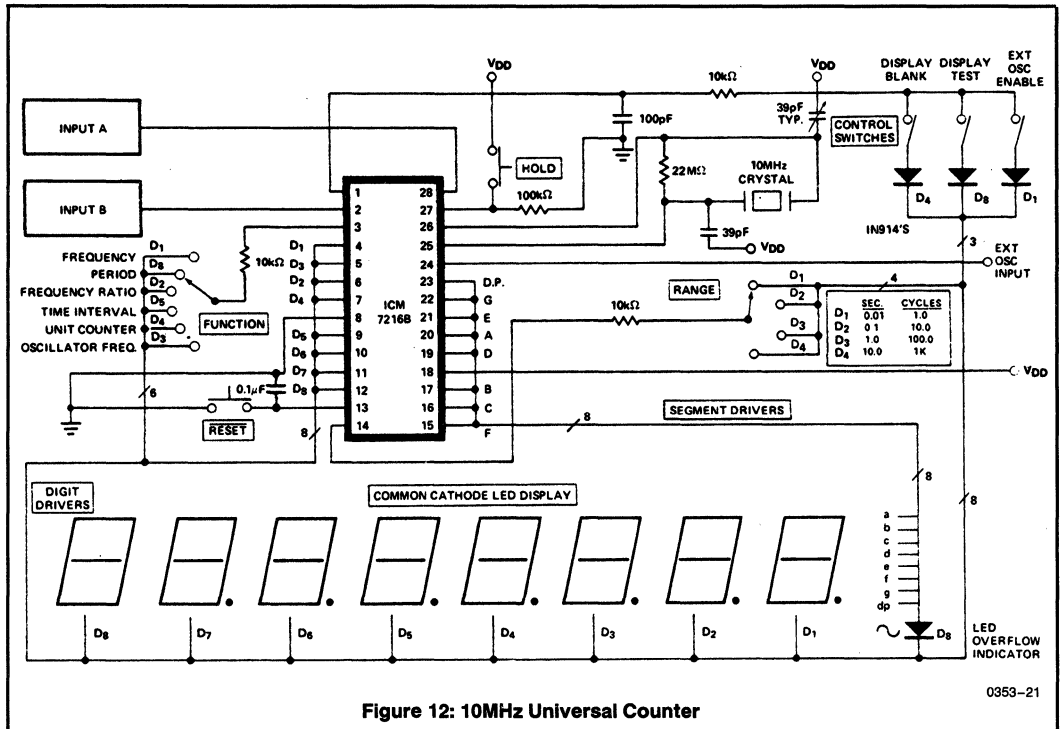
In a Universal Counter crystal drift and quantization effects cause errors. In **frequency**, **period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ± 1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 9, the least accuracy will be obtained at 10kHz. In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 10. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 11.



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NOTE: All typical values have been characterized but are not tested.



CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, pre-scalers will be required to reduce the input frequencies to under 10MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysteresis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 12. This circuit can use input frequencies up to 10MHz at INPUT A and 2MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74LS121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ns in duration.

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NOTE: All typical values have been characterized but are not tested.

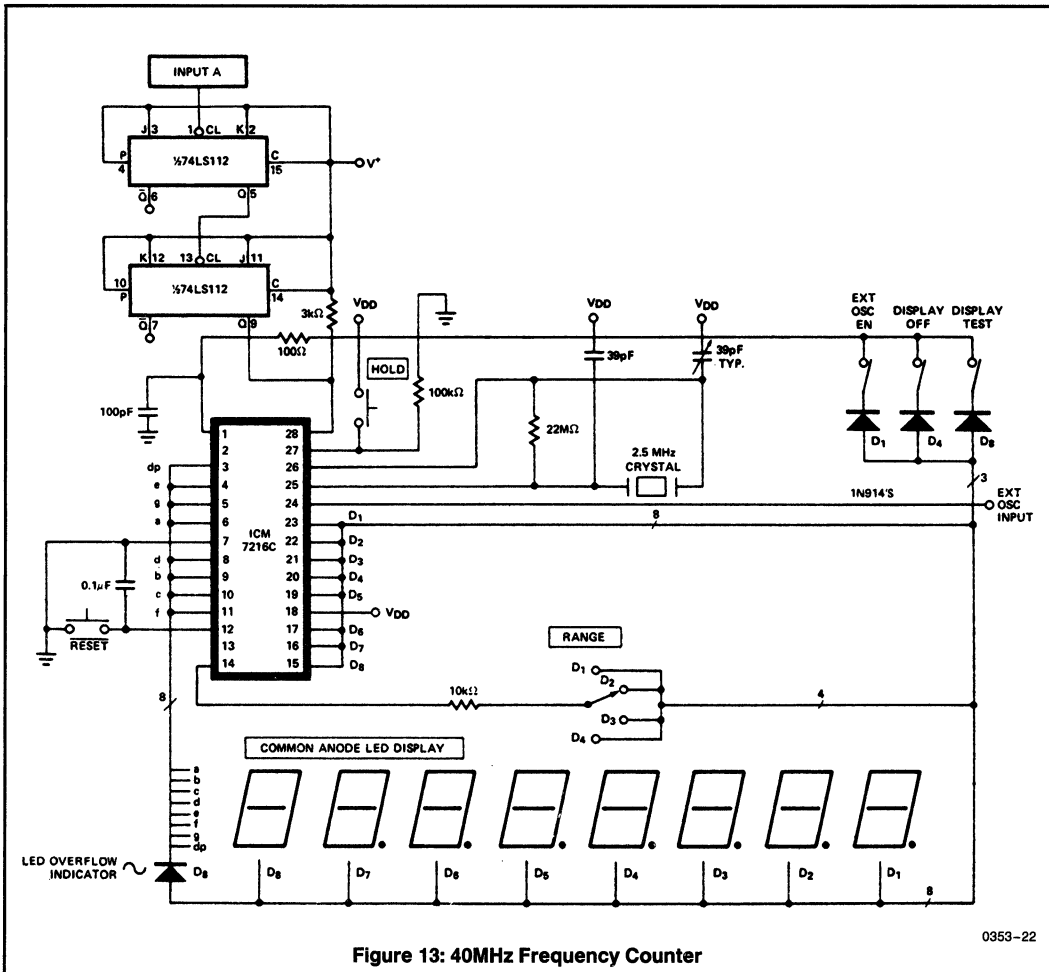


Figure 13: 40MHz Frequency Counter

0353-22

To measure frequencies up to 40MHz the circuit of Figure 13 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1MHz, but the decimal point must be moved one digit to the right. Figure 14 shows a frequency counter with a ÷10 prescaler and an ICM7216C. Since

there is no external decimal point control with the ICM7216A/B, the decimal point may be controlled externally with additional drivers as shown in Figure 15. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 16 additional logic has been added to count the input directly in **period** mode for maximum accuracy. In Figures 14 through 16, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

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NOTE: All typical values have been characterized but are not tested.

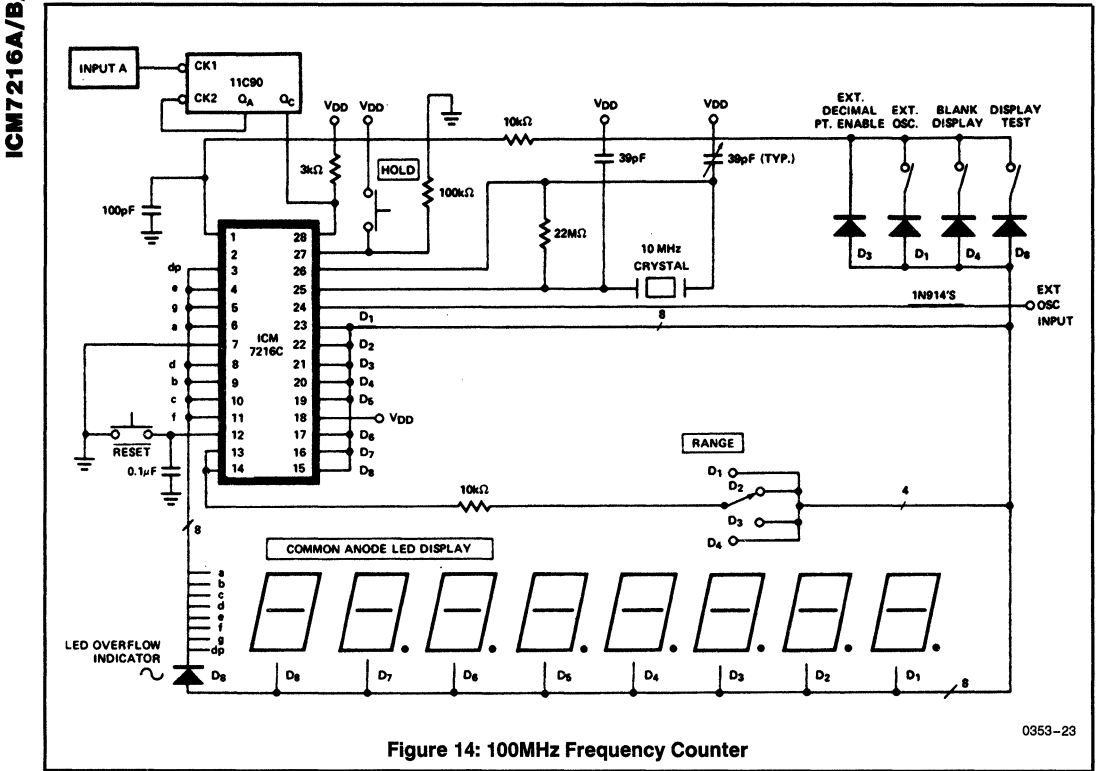


Figure 14: 100MHz Frequency Counter

0353-23

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain CMOS inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required gm can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} R_s \left(1 + \frac{C_O}{C_L} \right)^2$$

where $C_L = \left(\frac{C_{in} C_{out}}{C_{in} + C_{out}} \right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{in} = Input Capacitance

C_{out} = Output Capacitance

$$\omega = 2\pi f$$

The required gm should not exceed 50% of the gm specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to

C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10MHz or 1MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is

$$f_{mux} = \frac{f_{osc}}{2 \times 10^4} \text{ for 10MHz mode and } f_{mux} = \frac{f_{osc}}{2 \times 10^3} \text{ for the 1MHz mode.}$$

The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.

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NOTE: All typical values have been characterized but are not tested.

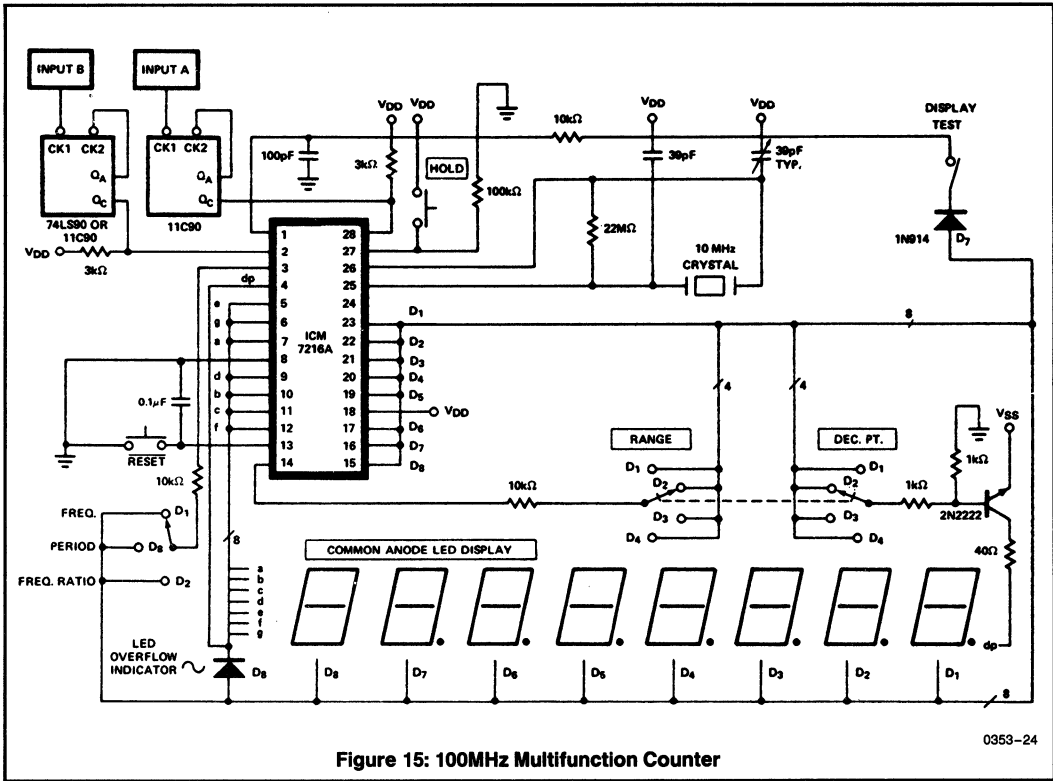


Figure 15: 100MHz Multifunction Counter

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NOTE: All typical values have been characterized but are not tested.

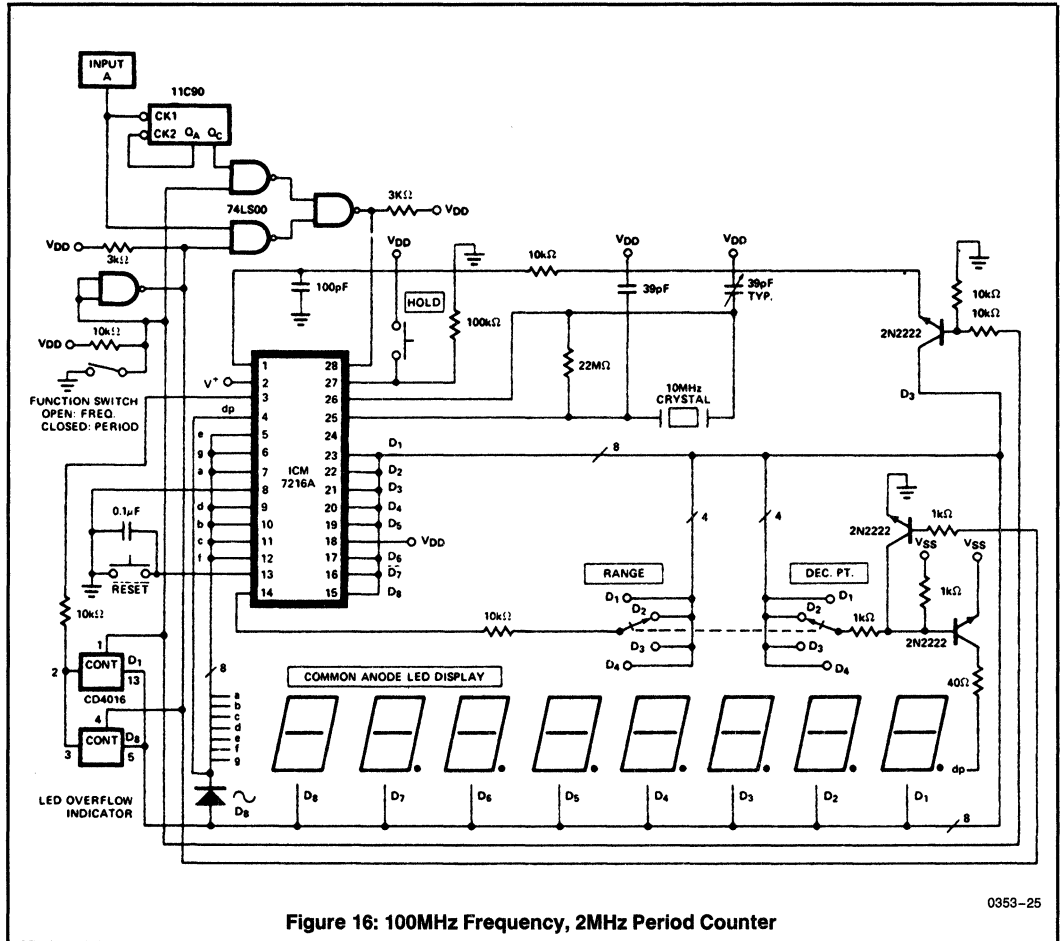
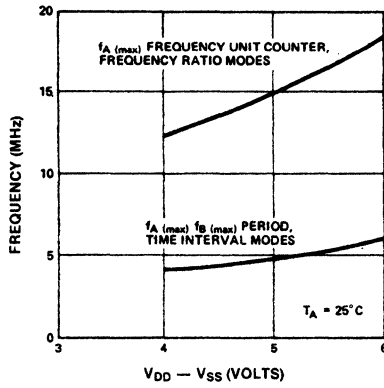


Figure 16: 100MHz Frequency, 2MHz Period Counter

0953-25

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NOTE: All typical values have been characterized but are not tested.



0353-26

f_A(max), f_B(max) as a Function of V_{DD}

Figure 17: Typical Operating Characteristics

ICM7217/ICM7227

4-Digit LED Display Programmable Up/Down Counter



GENERAL DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where pre-setting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

FEATURES

- Four Decade, Presettable Up-Down Counter With Parallel Zero Detect
- Settable Register With Contents Continuously Compared to Counter
- Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays
- On-Board Multiplex Scan Oscillator
- Schmitt Trigger On Count Input
- TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs
- Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW
- All Terminals Fully Protected Against Static Discharge
- Single 5V Supply Operation

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a ZERO output, which indicates when the count is zero, and an EQUAL output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, EQUAL, ZERO outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz. Counting and comparing (EQUAL output) will typically run 750kHz maximum.

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Option	Count Option Max Count
ICM7217JI	-25°C to +85°C	28 Lead CERDIP	Common Anode	Decade/9999
ICM7217AIPI	-25°C to +85°C	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7217BIJI	-25°C to +85°C	28 Lead CERDIP	Common Anode	Timer/5959
ICM7217CIPI	-25°C to +85°C	28 Lead PLASTIC	Common Cathode	Timer/5959
ICM7227JI	-25°C to +85°C	28 Lead CERDIP	Common Anode	Decade/9999
ICM7227AIPI	-25°C to +85°C	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7227BIJI	-25°C to +85°C	28 Lead CERDIP	Common Anode	Timer/5959
ICM7227CIPI	-25°C to +85°C	28 Lead PLASTIC	Common Cathode	Timer/5959

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NOTE: All typical values have been characterized but are not tested.

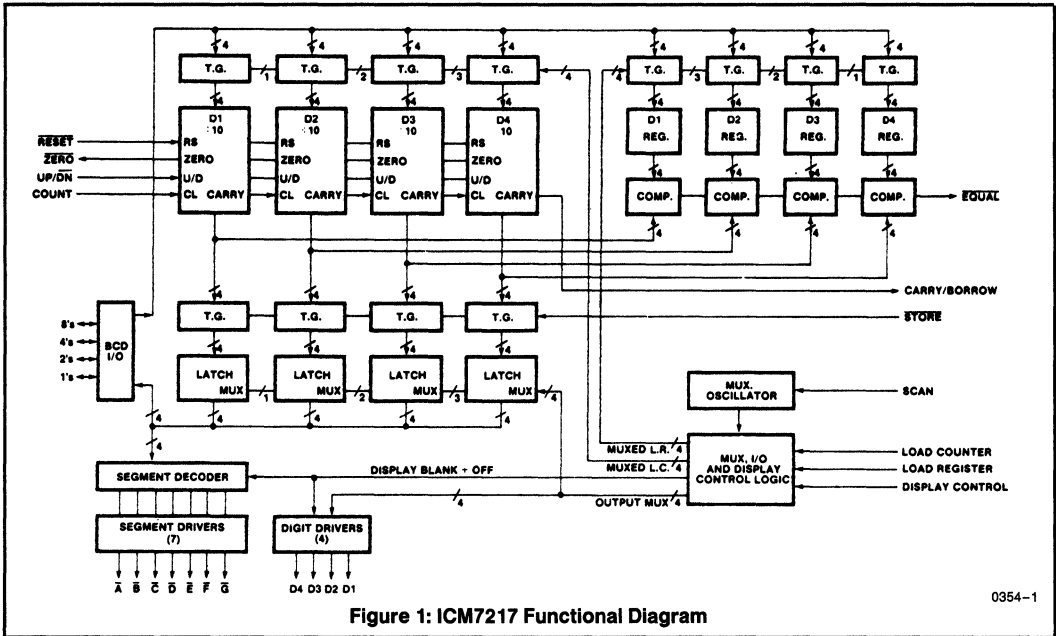


Figure 1: ICM7217 Functional Diagram

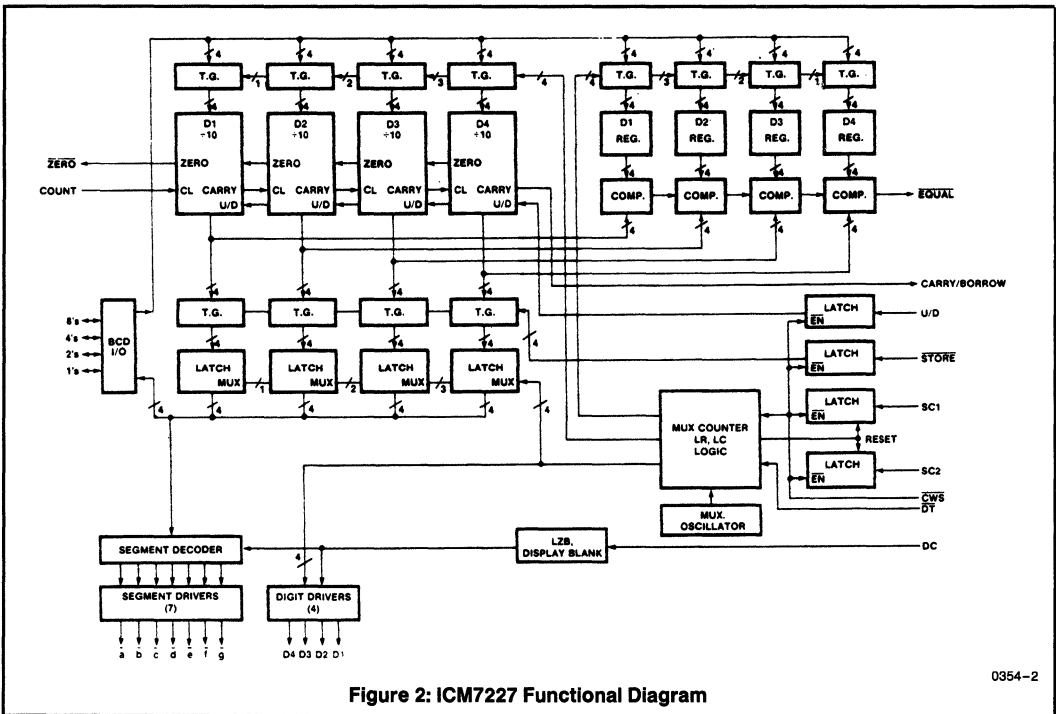


Figure 2: ICM7227 Functional Diagram

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ICM7217/ICM7227

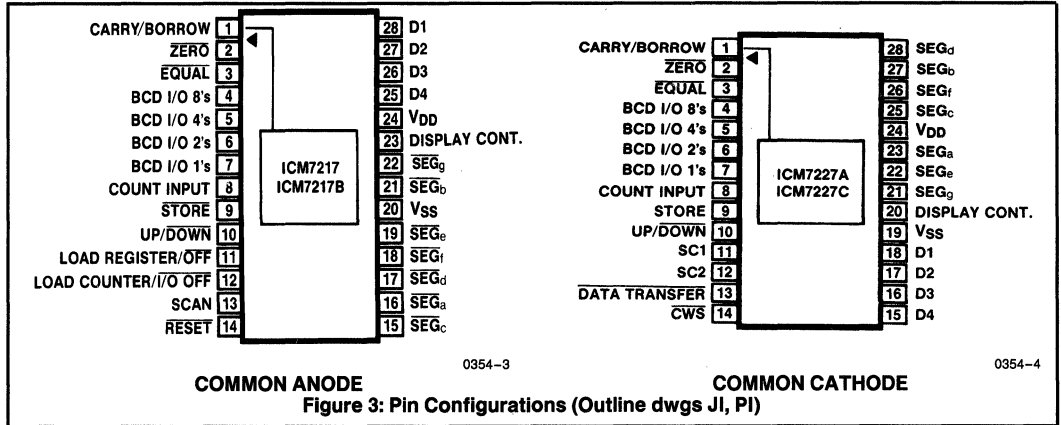


ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
 Input Voltage (any terminal) ($V_{DD} + 0.3V$ to $V_{SS} - 0.3V$) Note 2
 Power Dissipation (common anode/Cerdip) 1W Note 1

Power Dissipation (common cathode/Plastic) 0.5W
 Note 1
 Operating Temperature Range $-25^{\circ}C$ to $+85^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10sec) $300^{\circ}C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS ($V_{DD} = 5V, V_{SS} = 0V, T_A = 25^{\circ}C$, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD} (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)		350	500	μA
I_{DD} (7227)	Supply current (Lowest power mode)	Display off (Note 3)		300	500	μA
I_{OP}	Supply Current OPERATING	Common Anode, Display On, all "8's"	140	200		mA
		Common Cathode, Display On, all "8's"	50	100		mA
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DIG}	Digit Driver output current	Common anode, $V_{OUT} = V_{DD} - 2.0V$	140	200		mA peak
I_{SEG}	SEGment driver output current	Common anode, $V_{OUT} = +1.5V$	-20	-35		mA peak
I_{DIG}	Digit Driver output current	Common cathode, $V_{OUT} = +1.0V$	-50	-75		mA peak
I_{SEG}	SEGment driver output current	Common cathode $V_{OUT} = V_{DD} - 2V$	9	12.5		mA peak
I_P	$\overline{ST}, \overline{RS}, UP/\overline{DN}$ input pullup current	$V_{OUT} = V_{DD} - 2V$ (See Note 3)	5	25		μA
Z_{IN}	3 level input impedance		40		350	k Ω

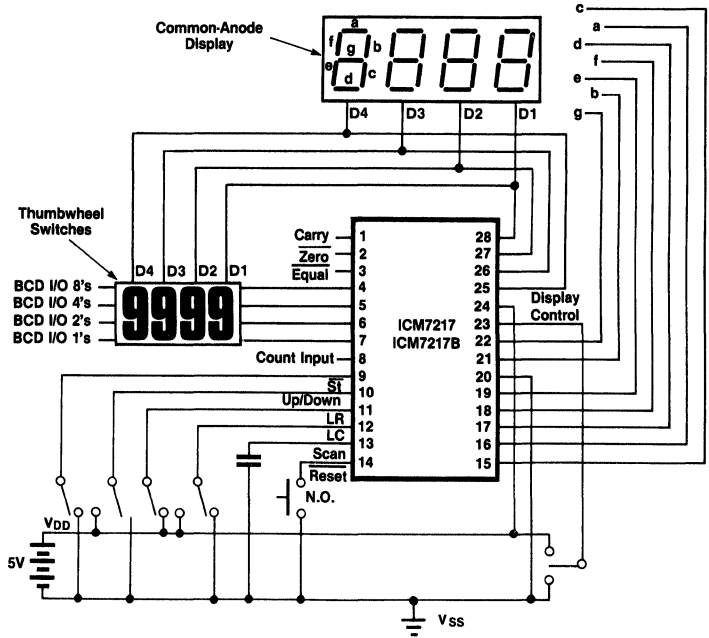
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NOTE: All typical values have been characterized but are not tested.

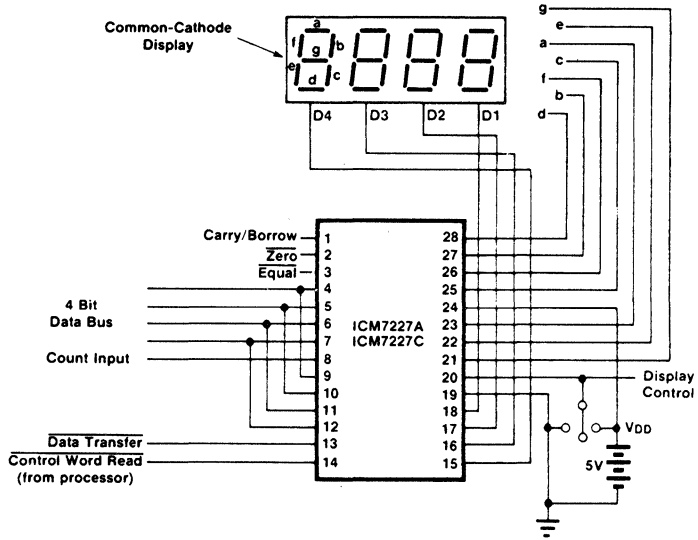
ELECTRICAL CHARACTERISTICS (Continued) ($V_{DD} = 5V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BIH}	BCD I/O input high voltage	ICM7217 common anode (Note 4)	1.5			V
		ICM7217 common cathode (Note 4)	4.40			V
		ICM7227 with 50pF effective load	3			V
V_{BIL}	BCD I/O input low voltage	ICM7217 common anode (Note 4)			0.60	V
		ICM7217 common cathode (Note 4)			3.2V	V
		ICM7227 with 50pF effective load			1.5	V
I_{BPU}	BCD I/O input pullup current	ICM7217 common cathode $V_{IN} = V_{DD} - 2V$ (Note 3)	5	25		μA
I_{BPD}	BCD I/O input pulldown current	ICM7217 common anode $V_{IN} = +2V$ (Note 3)	5	25		μA
V_{OH}	BCD I/O, ZERO, EQUAL Outputs output high voltage	$I_{OH} = 100\mu A$	3.5			V
V_{OL}	BCD I/O, CARRY/BORROW ZERO, EQUAL Outputs output low voltage	$I_{OL} = -1.6mA$			0.4	V
f_{in}	Count input frequency (Guaranteed)	$-20^\circ C < T_A < +70^\circ C$	0	5	2	MHz
V_{TH}	Count input threshold	(Note 5)		2		V
V_{HYS}	Count input hysteresis	(Note 5)		0.5		V
V_{CIL}	Count input LO				0.40	V
V_{CIH}	Count Input HI		3.5			V
f_{ds}	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)			10	kHz

- NOTES:**
- These limits refer to the package and will not be obtained during normal operation.
 - Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.
 - In the ICM7217 the UP/DOWN, STORE, RESET and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA . The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.
 - These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.
 - Parameters not tested (Guaranteed by Design).



0354-5



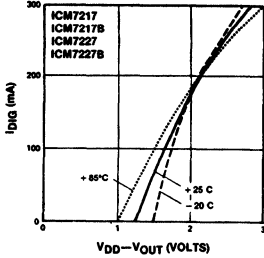
0354-6

Figure 4: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

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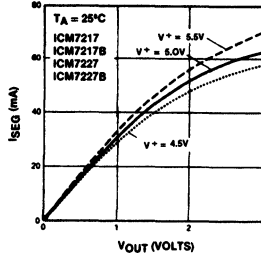
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (DIGIT AND SEGMENT DRIVERS)

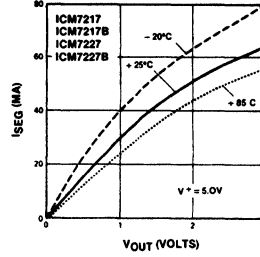


0354-7

Typical I_{DIG} vs. V_+
- V_{OUT} , $4.5V \leq V_+ \leq 6.0V$

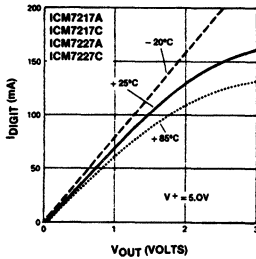


0354-8



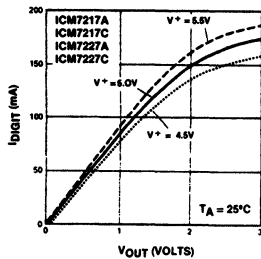
0354-9

Typical I_{SEG} vs. V_{OUT}

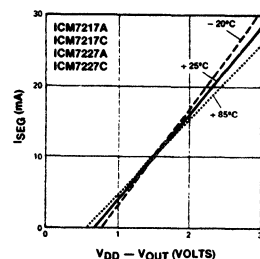


0354-10

Typical I_{DIGIT} vs. V_{OUT}



0354-11



0354-12

Typical I_{SEG} vs. $V_{DD} - V_{OUT}$,
 $4.5 \leq V_{DD} - V_{SS} \leq 6.0V$

Table 2: Control Input Definitions ICM7217

Input	Terminal	Voltage	Function
STORE	9	V_{DD} (or floating) V_{SS}	Output latches not updated Output latches updated
UP/DOWN	10	V_{DD} (or floating) V_{SS}	Counter counts up Counter counts down
RESET	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ I/O OFF	12	Unconnected V_{DD} V_{SS}	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ OFF	11	Unconnected V_{DD} V_{SS}	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTROL (DC)	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment drivers disabled Leading zero blanking inhibited

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NOTE: All typical values have been characterized but are not tested.

Table 3: Control Input Definitions ICM7227

Input		Terminal	Voltage	Function
DATA TRANSFER		13	V _{DD} V _{SS}	Normal Operation Causes transfer of data as directed by select code
Control Word Port	STORE	9	V _{DD} (During $\overline{\text{CWS}}$ Pulse) V _{SS}	Output latches updated Output latches not updated
	UP/DOWN	10	V _{DD} (During $\overline{\text{CWS}}$ Pulse) V _{SS}	Counter counts up Counter counts down
	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V _{DD} = "1" V _{SS} = "0"	SC1, SC2 control:— 00 Change store and up/down latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
$\overline{\text{Control Word Strobe (CWS)}}$		14	V _{DD} V _{SS}	Normal operation Causes control word to be written into control latches
DISPLAY CONTROL (DC)		23 Common Anode 20 Common Cathode	Unconnected V _{DD} V _{SS}	Normal operation Display drivers disabled Leading zero blanking inhibited

DETAILED DESCRIPTION

OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The EQUAL output assumes a negative level when the contents of the counter and register are equal.

The ZERO output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, EQUAL and ZERO outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA @ 0.4V (on resistance 250Ω), and for a logic one, the outputs will source >60μA. A 10kΩ pull-up resistor to V_{DD} on the EQUAL or ZERO outputs is recommended for

highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 5 shows the multiplex timing, while Figure 6 shows the Output Timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are inhibited, and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 4.

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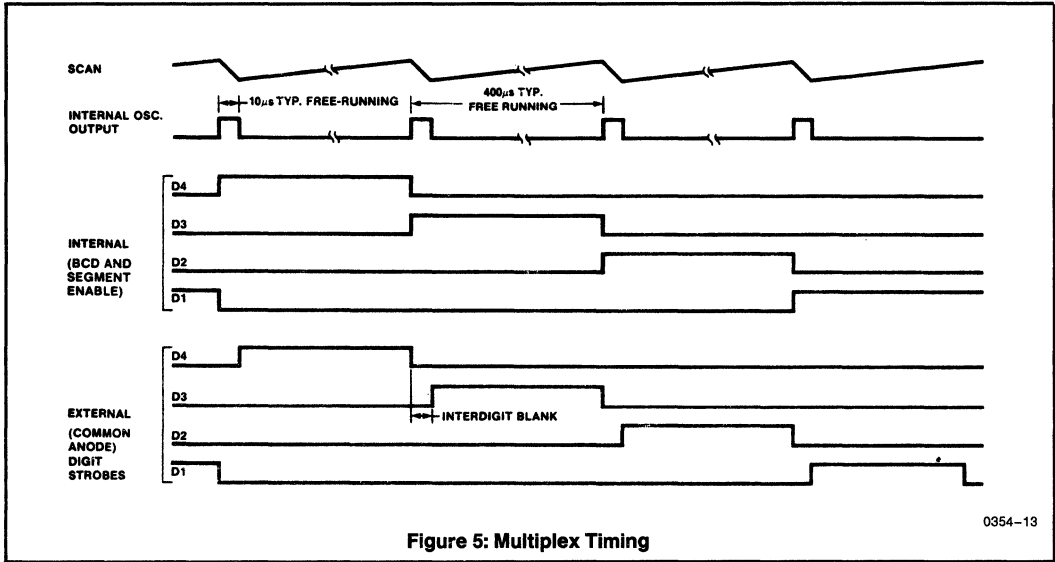


Figure 5: Multiplex Timing

0354-13

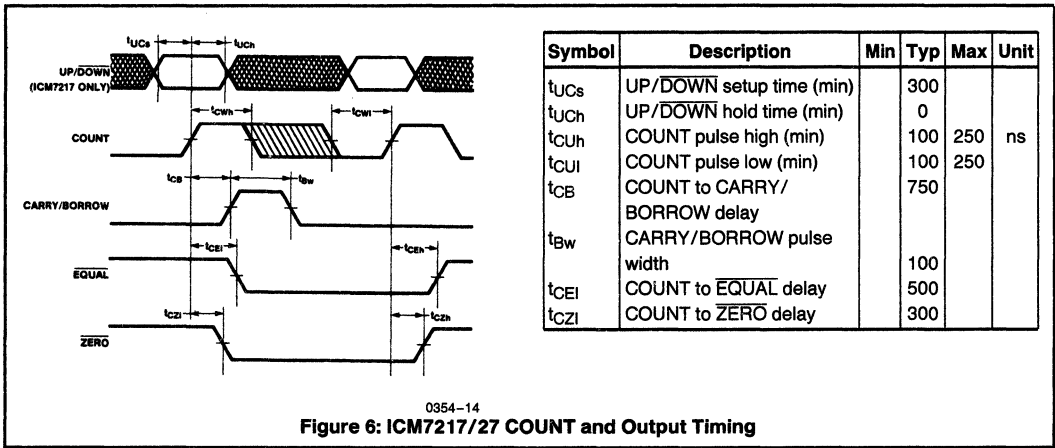


Figure 6: ICM7217/27 COUNT and Output Timing

Symbol	Description	Min	Typ	Max	Unit
tUCs	UP/DOWN setup time (min)	300			
tUCh	UP/DOWN hold time (min)	0			
tCUh	COUNT pulse high (min)	100	250		ns
tCUI	COUNT pulse low (min)	100	250		
tCB	COUNT to CARRY/BORROW delay	750			
tBw	CARRY/BORROW pulse width		100		
tCEI	COUNT to EQUAL delay	500			
tCZI	COUNT to ZERO delay	300			

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply (ICM7217 only). Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby pro-

viding inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplexed Rate Control

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time (4 digits)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

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NOTE: All typical values have been characterized but are not tested.

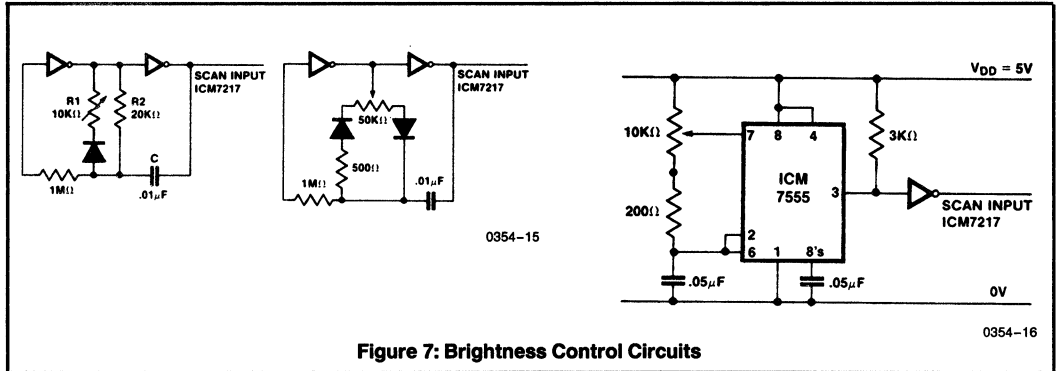


Figure 7: Brightness Control Circuits

During load counter and load register operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2 μ s. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 7 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control

As shown in Figure 6, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/DOWN is high. It is decremented when UP/DOWN is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and load counter operations.

The STORE pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the STORE pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the RESET pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the RESET input is low, the register will also be set to zero. The STORE, RESET and UP/DOWN pins are provided with pull-up resistors of approximately 75k Ω .

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

LOADING the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately $\frac{1}{2}V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD} , the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD} , the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD} , the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 7). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the

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preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 8). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, EQUAL, ZERO, UP/DOWN, RESET and STORE functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Figure 8. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

Output and Input Restrictions

The CARRY/BORROW output is not valid during load counter and reset operations.

The EQUAL output is not valid during load counter or load register operations.

The ZERO output is not valid during a load counter operation.

The RESET input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the RESET input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the RESET input is shown below.

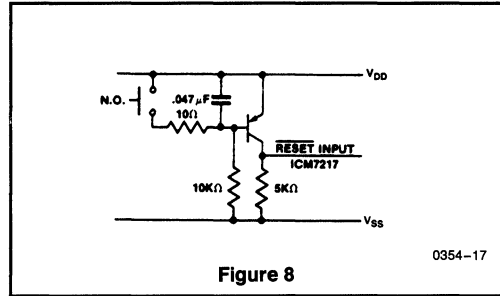


Figure 8

When using the circuit as a programmable divider (\div by n with equal outputs) a short time delay (about 1μs) is needed from the EQUAL output to the RESET input to establish a pulse of adequate duration. (See Figure 9)

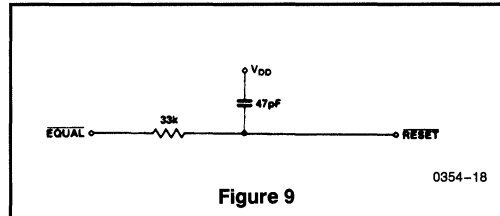


Figure 9

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching EQUAL), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. RESET will not clear the register.

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NOTE: All typical values have been characterized but are not tested.

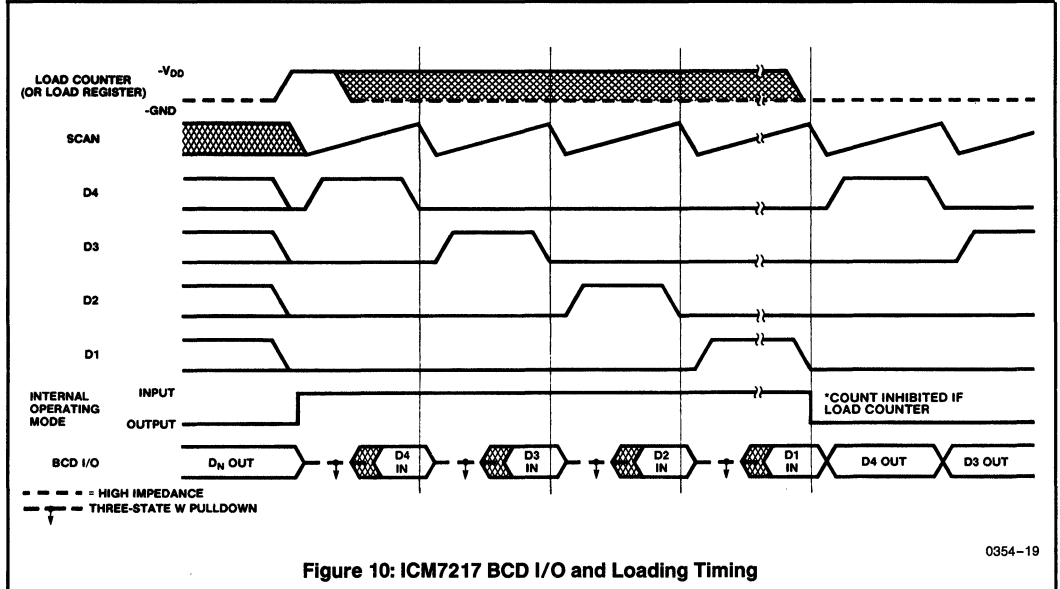


Figure 10: ICM7217 BCD I/O and Loading Timing

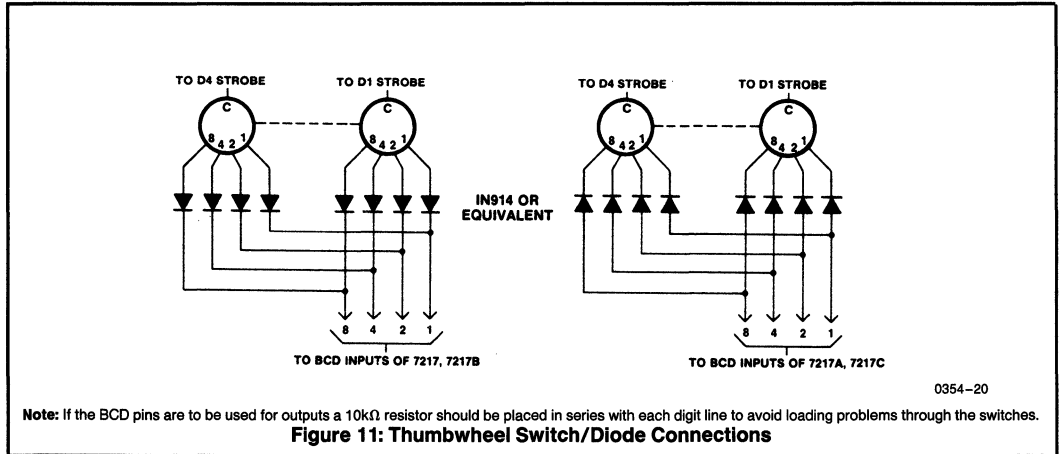


Figure 11: Thumbwheel Switch/Diode Connections

Note: If the BCD pins are to be used for outputs a 10kΩ resistor should be placed in series with each digit line to avoid loading problems through the switches.

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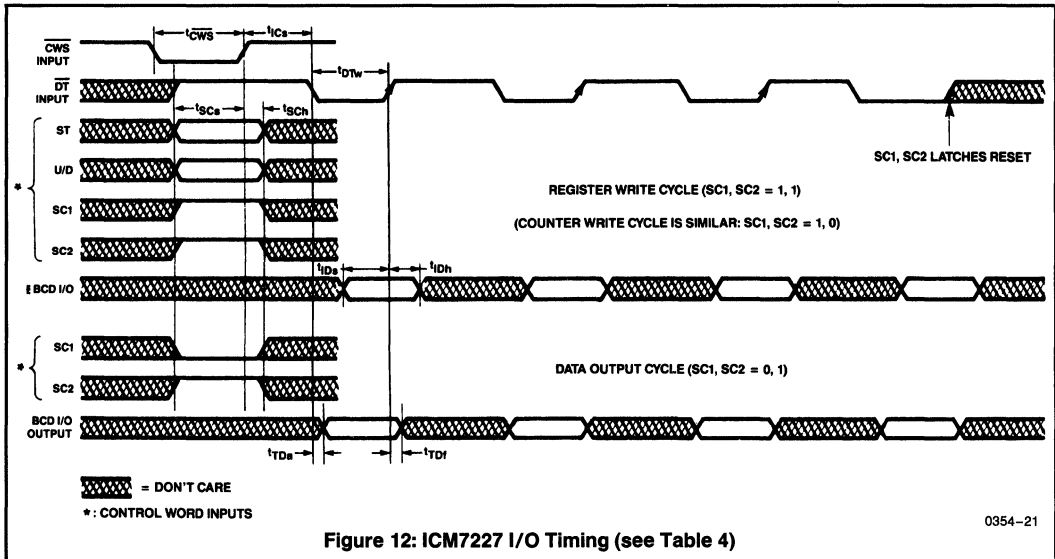


Figure 12: ICM7227 I/O Timing (see Table 4)

CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit micro-processor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/DOWN, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the CWS (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/Down latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/Down latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/Down latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a **data transfer** operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the **DATA TRANSFER** pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while DT is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first DT pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first DT pulse, the data for D3 must be valid during the second DT pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth DT pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Figure 12 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

Symbol	Description	Min	Typ	Max	Units
t_{CWS}	Control Word Strobe Width (min)		275		ns
t_{ICs}	Internal Control Set-up (min)		2.5	3	μ s
t_{DTW}	DATA TRANSFER pulse width (min)		300		ns
t_{SCs}	Control to Strobe setup (min)	300			ns
t_{SCh}	Control to Strobe hold (min)	300			ns
t_{IDs}	Input Data setup (min)	300			ns
t_{IDh}	Input Data Hold (min)	300			ns
t_{Dacc}	Output Data access		300		ns
t_{Df}	Output Transfer to Data float		300		ns

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ICM7217/ICM7227



APPLICATIONS

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Performance Characteristics for a similarly operating multi-digit connection.

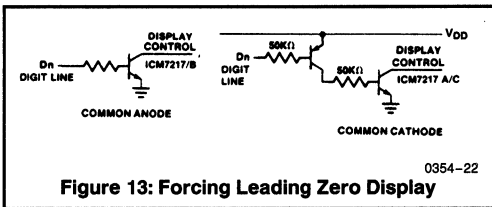


Figure 13: Forcing Leading Zero Display

DRIVING LARGER DISPLAYS

For displays requiring more current than the ICM7217/7227 can provide, the circuits of Figure 14 can be used.

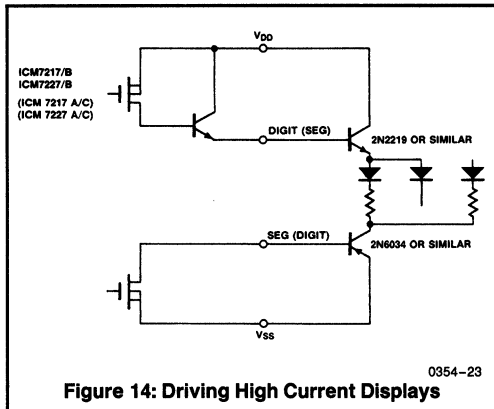


Figure 14: Driving High Current Displays

LCD DISPLAY INTERFACE

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 15. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10–20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

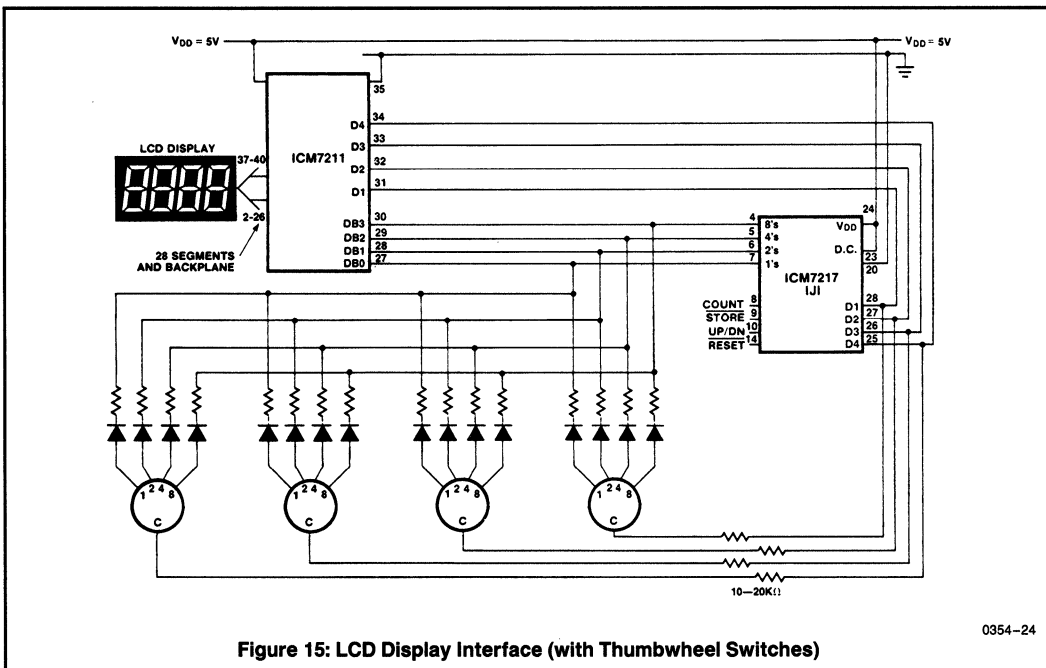


Figure 15: LCD Display Interface (with Thumbwheel Switches)

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UNIT COUNTER WITH BCD OUTPUT

The simplest application of the ICM7217 is a 4 digit unit counter (Figure 16). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

INEXPENSIVE FREQUENCY COUNTER/TACHOMETER

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, STORE and RESET signals as shown in Figure 17. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A , R_B and C to provide an output that is positive for approximately one second and negative for approximately $300 - 500\mu s$. The positive waveform time is given by $t_{wp} = 0.693 (R_A + R_B)C$ while the negative waveform is given by $t_{wn} = 0.693 R_B C$. The system is calibrated by using a $5M\Omega$ potentiometer for R_A as a "coarse" control and a $1k\Omega$ potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.

TAPE RECORDER POSITION INDICATOR/CONTROLLER

The circuit in Figure 18 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the EQUAL or ZERO outputs, and serve as a numerical display for the processor.

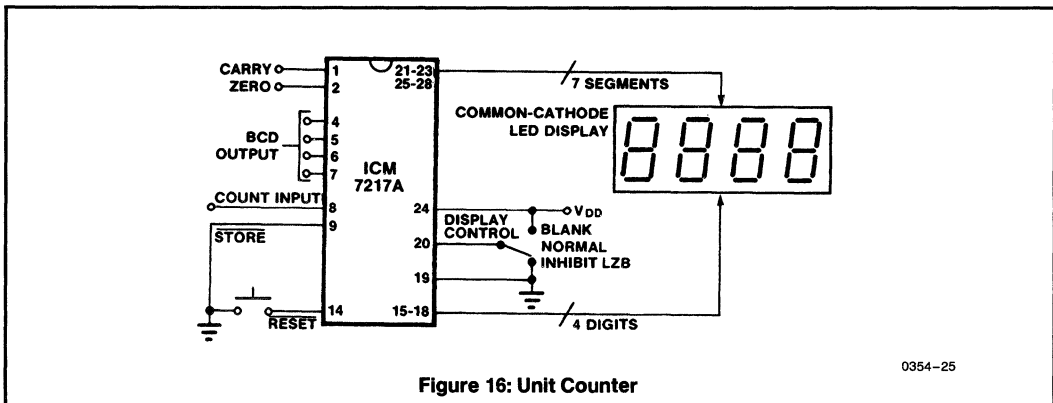
In the tape recorder application, the LOAD REGISTER, EQUAL and ZERO outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the EQUAL output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the ZERO output to be used to stop the recorder on rewind, leaving the leader on the reel.

The $1M\Omega$ resistor and $.0047\mu F$ capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

PRECISION ELAPSED TIME/COUNTDOWN TIMER

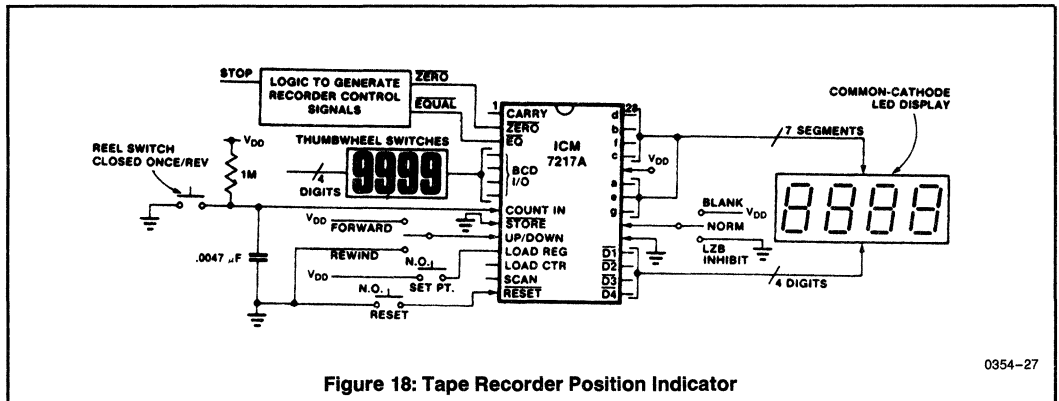
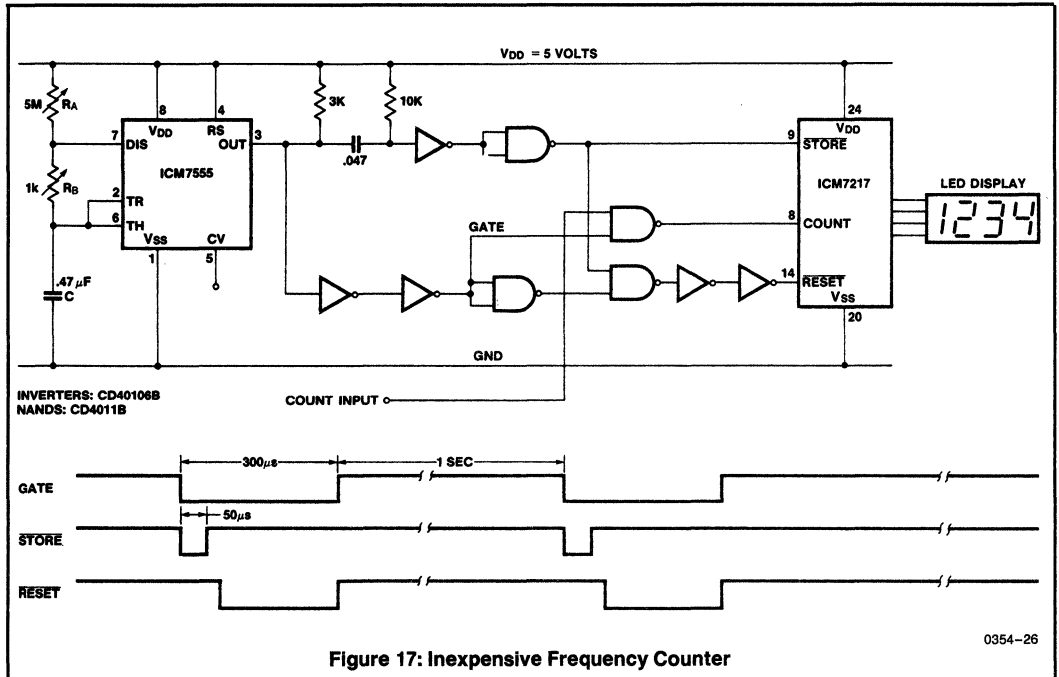
The circuit in Figure 19 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the EQUAL output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.



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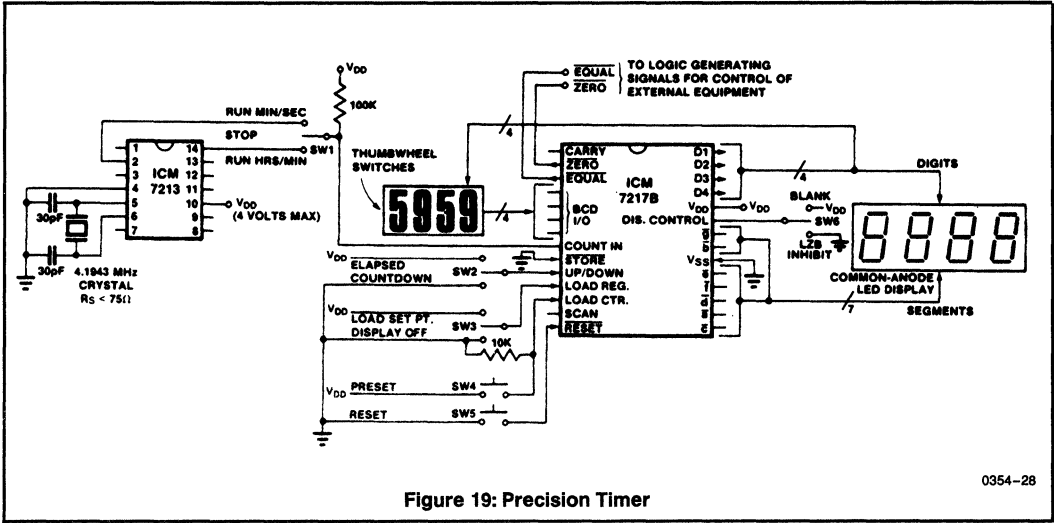


Figure 19: Precision Timer

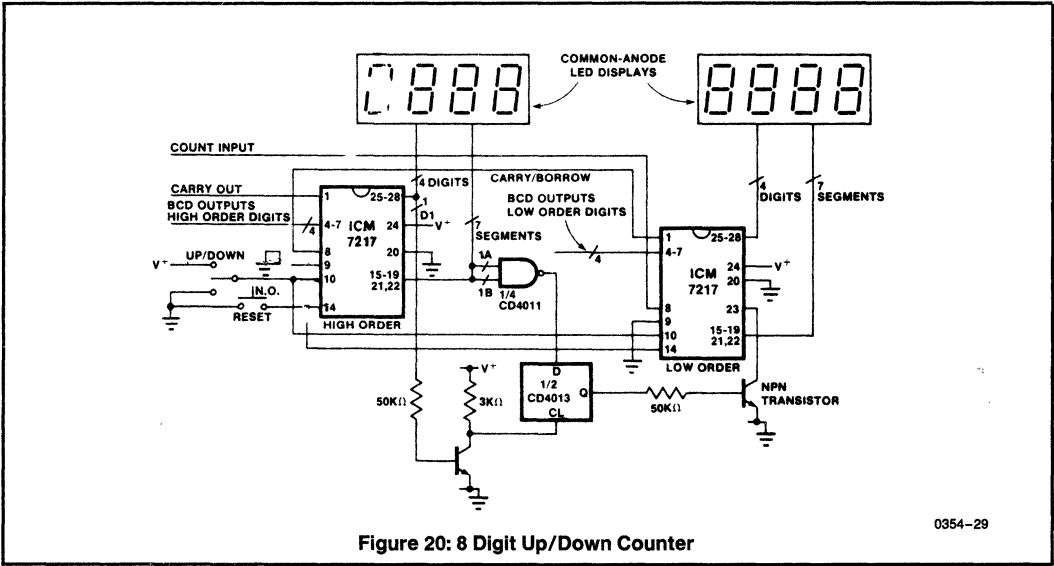
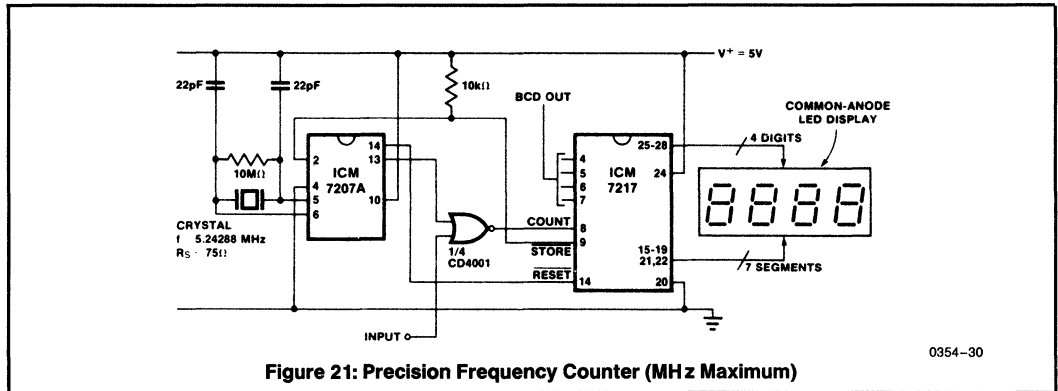


Figure 20: 8 Digit Up/Down Counter

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This technique may be used on any 3-level input. The 100k Ω pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 17 to generate a 1Hz reference.

8-DIGIT UP/DOWN COUNTER

This circuit (Figure 20) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments \bar{a} or \bar{b} is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

PRECISION FREQUENCY COUNTER/TACHOMETER

The circuit shown in Figure 21 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the STORE and RESET signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD} , the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01 second gating with Pin 11 connected to V_{DD} , and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-detector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the EQUAL and ZERO outputs, to count in SYNC with an ICL7109 A/D Converter as shown in Figure 22. By RESETING the ICM7217 on a "tare" value conversion, and STORE-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7109 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.

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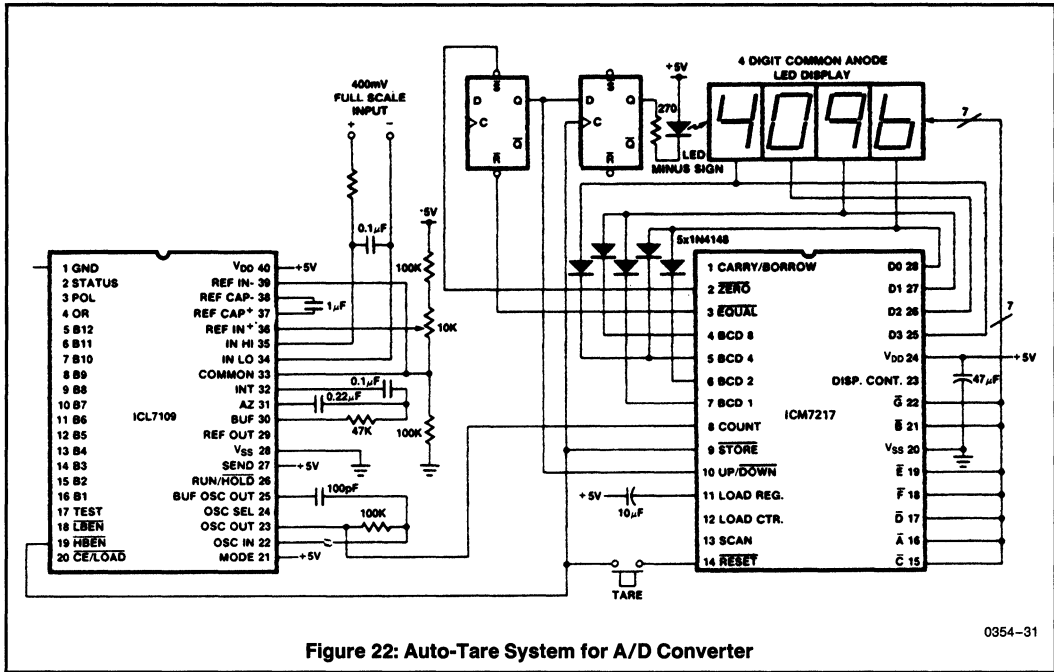


Figure 22: Auto-Tare System for A/D Converter

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ICM7224/ICM7225

4 1/2-Digit LCD/LED Display Counter



GENERAL DESCRIPTION

The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ± 10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In common-anode LED systems, the BRighTness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic or CERDIP package, or in dice.

ORDERING INFORMATION

Part Number	Display Type	Count Option
ICM7224IPL	LCD	19999
ICM7225IPL	LED	19999

Evaluation Kits, order ICM7224 EV/Kit or ICM7225 EV/Kit

FEATURES

- High Frequency Counting — Guaranteed 15MHz, Typically 25MHz at 5V
- Low Power Operation — Typically Less Than 100µW Quiescent
- STORE and RESET Inputs Permit Operation as Frequency or Period Counter
- True COUNT INHIBIT Disables First Counter Stage
- CARRY Output for Cascading Four-Digit Blocks
- Schmitt-Trigger On The COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs
- Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices
- LCD Devices Provide Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May Be Disabled Allowing Segments to be Slaved to A Master Backplane Signal
- LED Devices Provide BRighTness Input Which Can Function Digitally As A Display Enable or As A Continuous Display Brightness Control With A Single Potentiometer

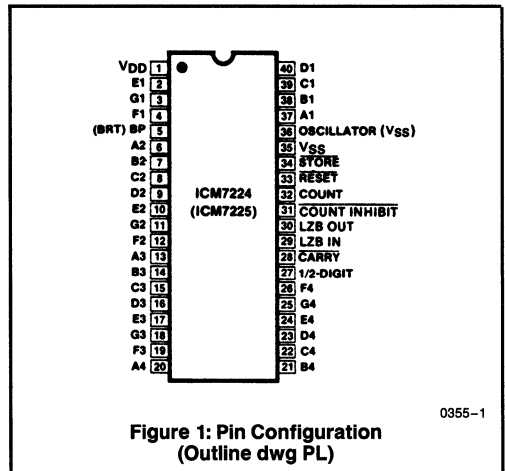
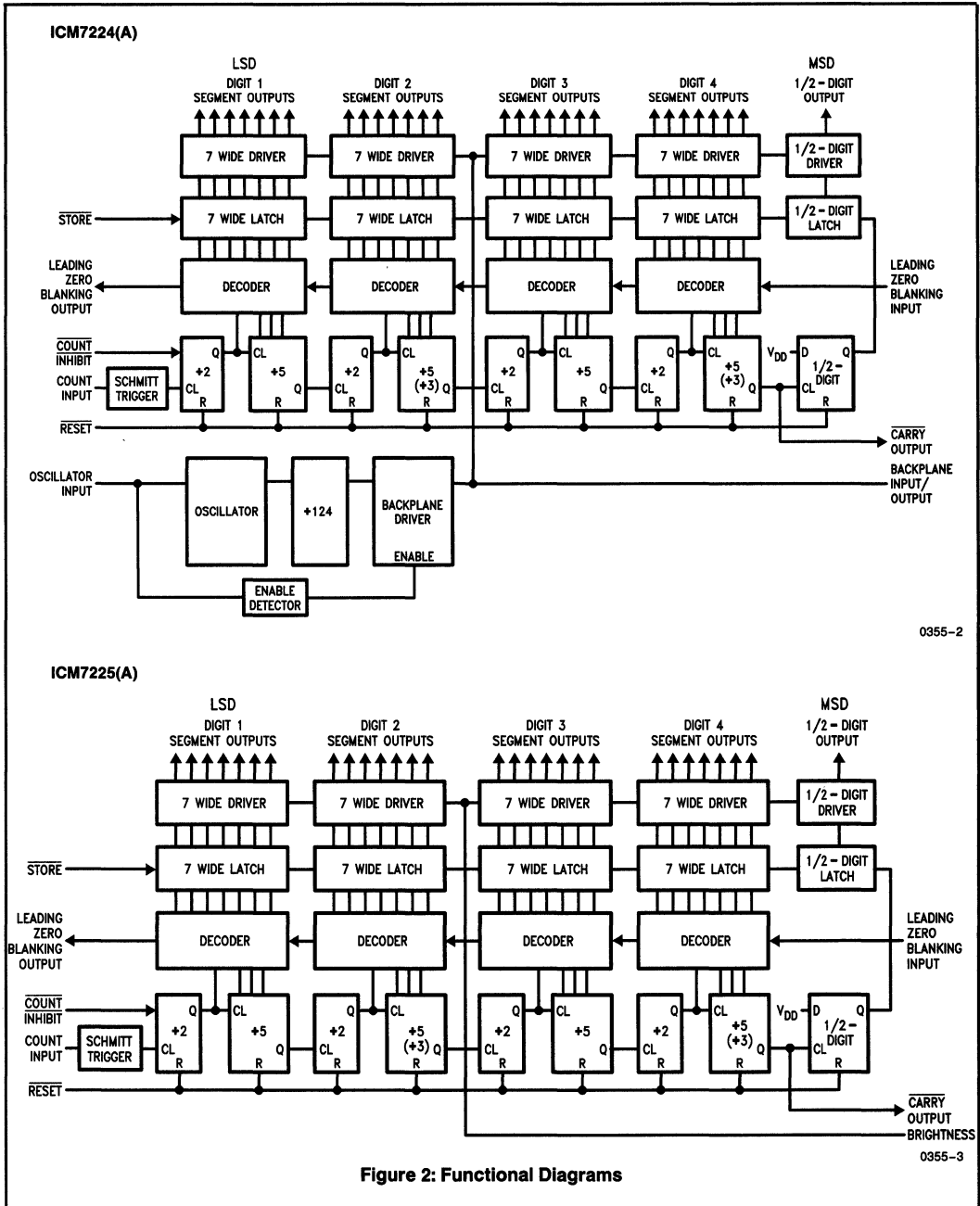


Figure 1: Pin Configuration (Outline dwg PL)

0955-1

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NOTE: All typical values have been characterized but are not tested.



0355-2

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Figure 2: Functional Diagrams

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NOTE: All typical values have been characterized but are not tested.

ICM7224/ICM7225



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
 Input Voltage (Any Terminal) (Note 2) ($V_{DD} + 0.3V$) to ($V_{SS} - 0.3V$)
 Power Dissipation (Note 1) 0.5W @ 70°C

Operating Temperature Range -25°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5V, V_{SS} = 0V, T_A = 25^\circ C$, unless otherwise indicated)

ICM7224 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating current	Test circuit, Display blank		10	50	μA
V_{SUPPLY}	Operating supply voltage range ($V_{DD} - V_{SS}$)		3		6	V
I_{OSCI}	OSCILLATOR input current	Pin 36		± 2	± 10	μA
$t_{R, tF}$	Segment rise/fall time	$C_{load} = 200pF$		0.5		μs
$t_{R, tF}$	BackPlane rise/fall time	$C_{load} = 5000pF$		1.5		
f_{OSC}	Oscillator frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane frequency	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{STBY}	Operating current display off	Pin 5 (BRIGHtness) at V_{SS} Pins 29, 31-34 at V_{DD}		10	50	μA
V_{SUPP}	Operating supply voltage range ($V_{DD} - V_{SS}$)		4		6	V
I_{DD}	Operating current	Pin 5 at V_{DD} , Display 18888		200		mA
I_{SLK}	Segment leakage current	Segment Off		± 0.01	± 1	μA
I_{SEG}	Segment on current	Segment On, $V_{out} = +3V$	5	8		mA
I_H	Half-digit on current	Half-digit on, $V_{out} = +3V$	10	16		

FAMILY CHARACTERISTICS

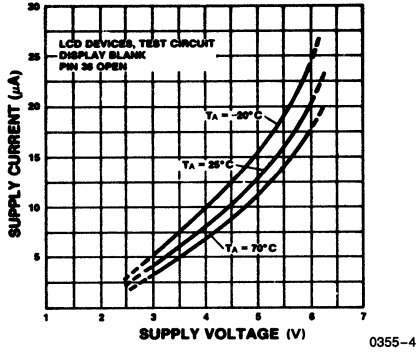
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_P	Input Pullup Currents	Pins 29, 31, 33, 34 $V_{out} = V_{DD} - 3V$		10		μA
V_{IH}	Input High Voltage	Pins 29, 31, 33, 34	3			V
V_{IL}	Input Low Voltage	Pins 29, 31, 33, 34			1	
V_{CT}	\overline{COUNT} Input Threshold			2		
V_{CH}	\overline{COUNT} Input Hysteresis			0.5		
I_{OH}	Output High Current	\overline{CARRY} Pin 28 Leading Zero Blanking OUT Pin 30 $V_{out} = V_{DD} - 3V$	350	500		μA
I_{OL}	Output Low Current	\overline{CARRY} Pin 28 Leading Zero Blanking Out Pin 30 $V_{out} = +3V$	350	500		
f_{COUNT}	Count Frequency	$4.5V < V_{DD} < 6V$	0		15	MHz
$t_{S, tR}$	STORE, RESET Minimum Pulse Width		3			μs

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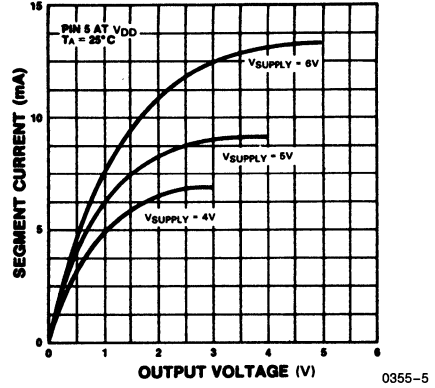
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

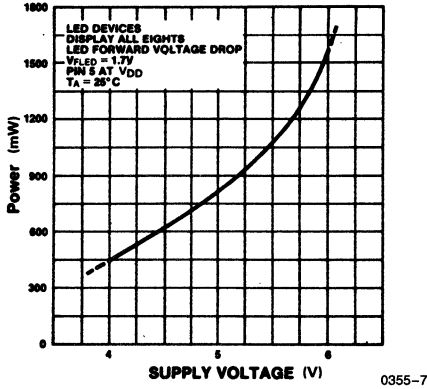
7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



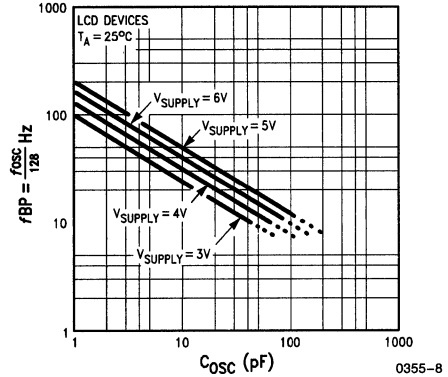
7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



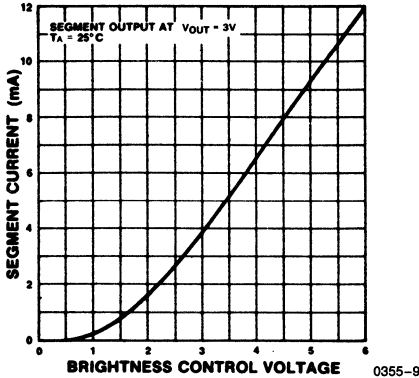
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



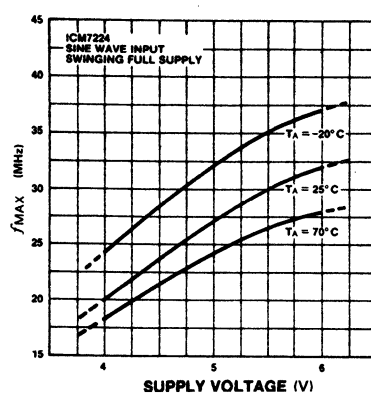
7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}



7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

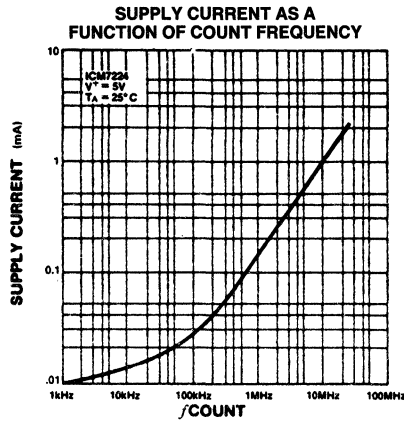


MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE



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NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)


0355-11

TABLE I: Control Input Definitions

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking Input	29	V_{DD} or Floating V_{SS}	Leading Zero Blanking Enabled Leading Zeroes Displayed
COUNT INHIBIT	31	V_{DD} or Floating V_{SS}	Counter Enabled Counter Disabled
RESET	33	V_{DD} or Floating V_{SS}	Inactive Counter Reset to 0000
STORE	34	V_{DD} or Floating V_{SS}	Output Latches not Updated Output Latches Updated

CONTROL INPUT DEFINITIONS

In Table I, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

DETAILED DESCRIPTION**LCD Devices**

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional $4\frac{1}{2}$ -digit by seven segment LCD displays. They include 29 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any D.C. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to V_{SS} . This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external

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NOTE: All typical values have been characterized but are not tested.

source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption, is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding $5\mu s$ (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external backplane signal should be capable of driving very large capacitive loads with short ($1-2\mu s$) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscilla-

tor free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V_{DD} ; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving $4\frac{1}{2}$ -digit by seven segment common-anode LED displays. They include 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value ($100k\Omega$ to $1M\Omega$) to minimize power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when at V_{DD} , the display is fully on, and at V_{SS} , fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for V_{SS} ; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at $25^{\circ}C$, derated linearly above $35^{\circ}C$ to 500mW at $70^{\circ}C$ ($15mW/^{\circ}C$ above $35^{\circ}C$). Power dissipation for the device is given by:

$$P = (V_{DD} - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

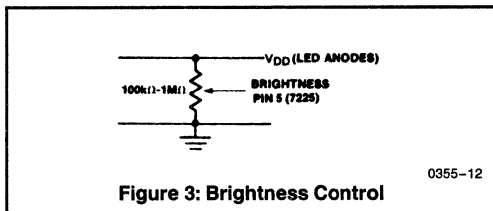


Figure 3: Brightness Control

0355-12

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a CARRY output. Also included is an extra D-type flip-flop, clocked by the CARRY signal which controls the half-digit segment driver. This output driver can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, while the CARRY output provides a negative-going edge following the count which increments the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the RESET terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent CARRY outputs will not be affected.

A negative level at the COUNT INHIBIT input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

Each decade of the counter directly drives a four-to-seven segment decoder which develops the required output data. The output data is latched at the driver. When the STORE pin is low, these latches are updated, and when it is high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When it is low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

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NOTE: All typical values have been characterized but are not tested.

ICM7224/ICM7225



The STORE, RESET, COUNT INHIBIT, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The CARRY and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 to ICM7225 devices in four-digit blocks.

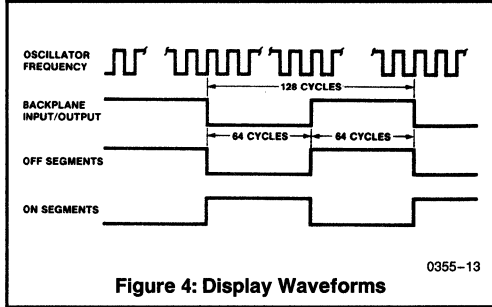


Figure 4: Display Waveforms

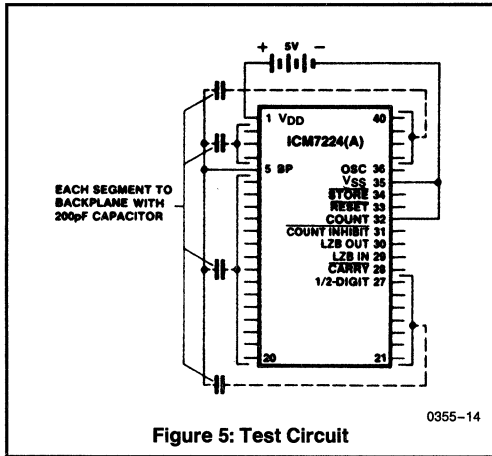


Figure 5: Test Circuit

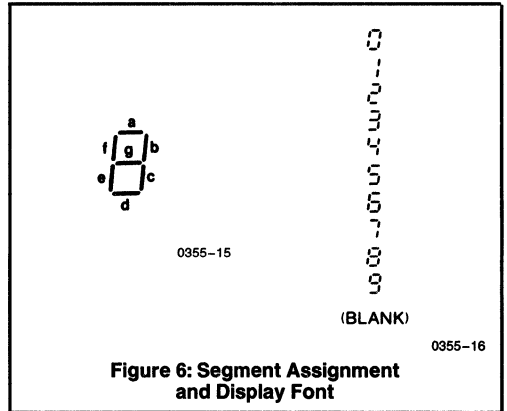


Figure 6: Segment Assignment and Display Font

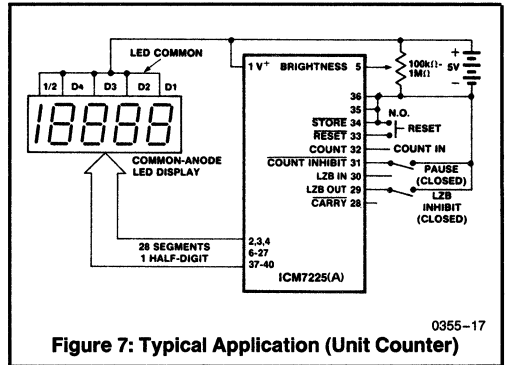
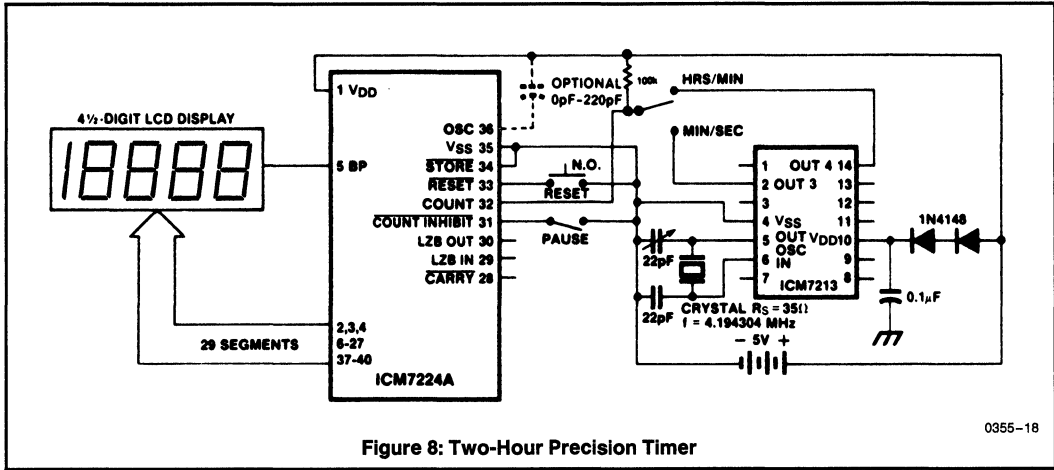


Figure 7: Typical Application (Unit Counter)

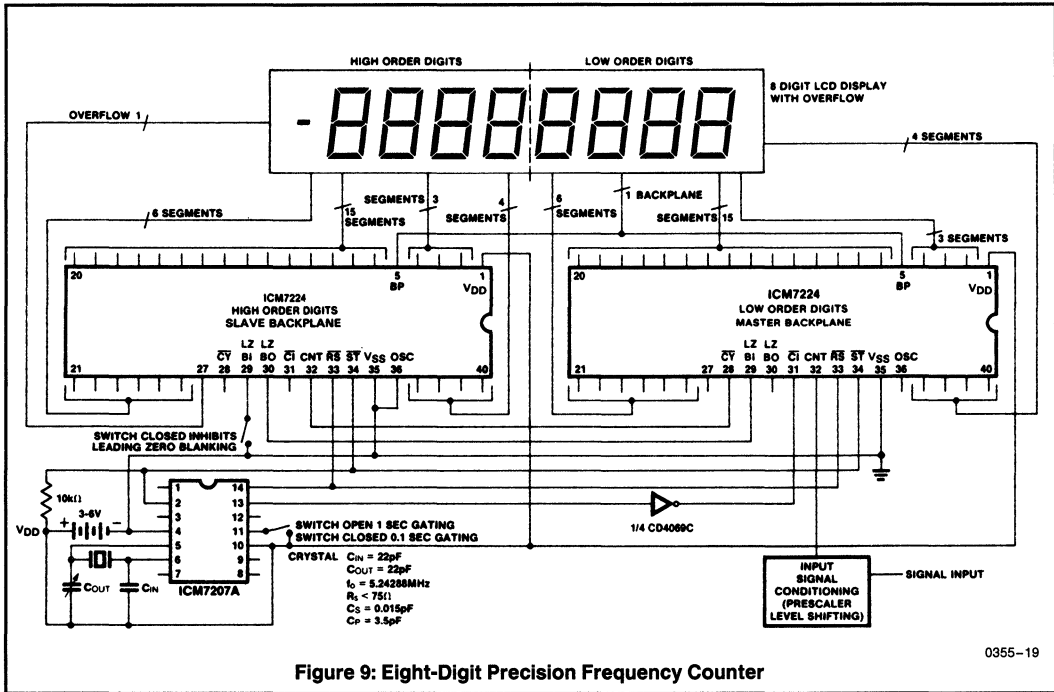
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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS



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NOTE: All typical values have been characterized but are not tested.

ICM7226A/B

8-Digit Multi-Function Frequency Counter/Timer



GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in **frequency** and **unit counter** modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval**, the 10MHz timebase gives a 0.1 μ s resolution. In **period average** and **time interval average**, the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μ s. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

FEATURES

- CMOS Design for Very Low Power
- Output Drivers Directly Drive Both Digits and Segments of Large 8 Digit LED Displays. Both Common Anode and Common Cathode Versions Are Available
- Measures Frequencies From DC to 10MHz; Periods From 0.5 μ s to 10s
- Stable High Frequency Oscillator Uses Either 1MHz or 10MHz Crystal
- Control Signals Available for External Systems Operation
- Multiplexed BCD Outputs

APPLICATIONS

- Frequency Counter
- Period Counter
- Unit Counter
- Frequency Ratio Counter
- Time Interval Counter

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7226AIJL	-25°C to 85°C	40 pin Cerdip
ICM7226BIJL	-25°C to +85°C	40 pin Cerdip
ICM7226BIPL	-25°C to 85°C	40 pin PLASTIC DIP

NOTE: An evaluation kit is available for these devices—order ICM7226AEV/KIT.

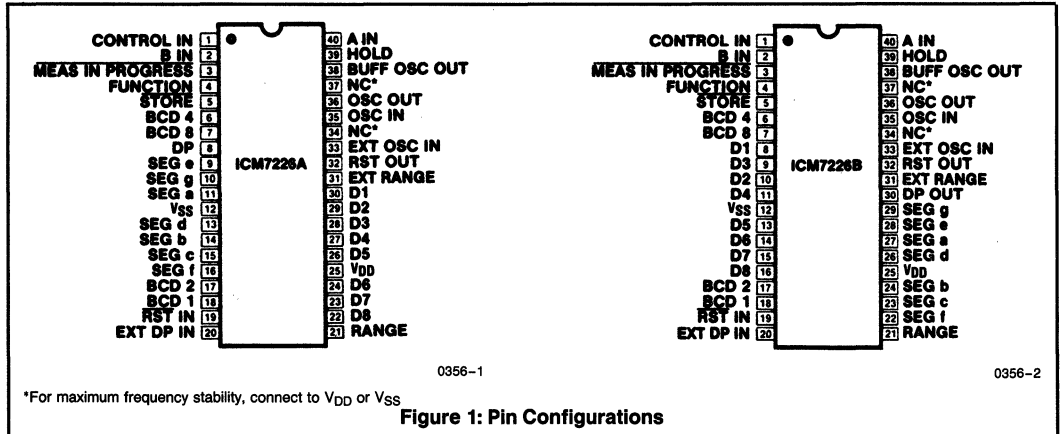


Figure 1: Pin Configurations

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V_{DD} - V_{SS}$)	6.5V
Maximum Digit Output Current	400mA
Maximum Segment Output Current	60mA
Voltage on any Input or Output Terminal (Note 1)	($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
Maximum Power Dissipation at 70°C (Note 2)	
ICM7226A	1.0W
ICM7226B	0.5W
Operating Temperature Range	-25°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (Soldering, 10sec)	300°C

*Note 1: Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V_{DD} or V_{SS} by 0.3V.

2: Assumes all leads soldered or welded to PC board and free air flow.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

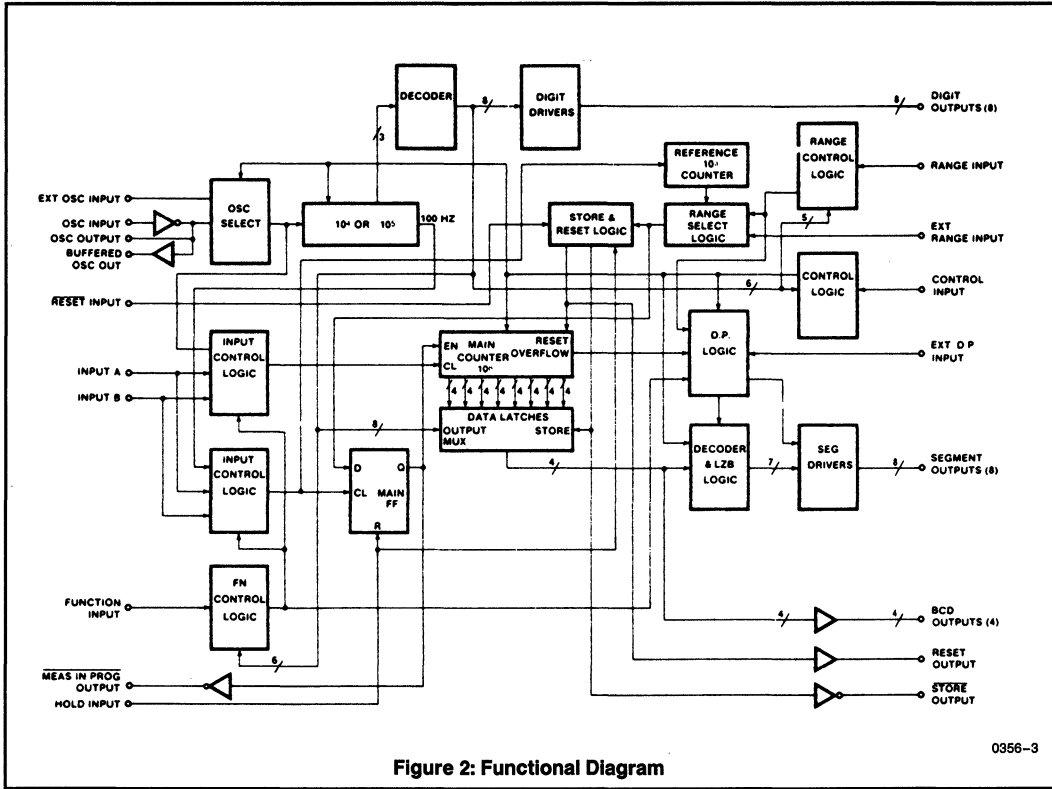


Figure 2: Functional Diagram

0356-3

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0V$, $T_A = 25^\circ C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current	Display Off Unused inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range $V_{DD} - V_{SS}$	$-25^\circ C < T_A < 85^\circ C$ Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
$f_{A(max)}$	Maximum Guaranteed Frequency Input A, Pin 40	$-25^\circ C < T_A < 85^\circ C$ $4.75V < V_{DD} < 6.0V$ Figure 4 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5	14		MHz
$f_{B(max)}$	Maximum Frequency Input B, Pin 2	$-25^\circ C < T_A < 85^\circ C$ $4.75V < V_{DD} < 6.0V$ Figure 5	2.5			
	Minimum Separation Input A to Input B Time Interval Function	$-25^\circ C < T_A < 85^\circ C$ $4.75V < V_{DD} < 6.0V$ Figure 6	250			ns
f_{OSC}	Osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	$-25^\circ C < T_A < 85^\circ C$ $4.75V < V_{DD} < 6.0V$	10 (0.1)			MHz
g_m	Oscillator Transconductance	$V_{DD} = 4.75V$ $T_A = +85^\circ C$	2000			μS
f_{mux}	Multiplex Frequency	$f_{osc} = 10MHz$		500		Hz
	Time Between Measurements	$f_{osc} = 10MHz$		200		ms
dV_{in}/dt	Input Rate of Charge	Inputs A, B		15		mV/ μs
V_{IL}	INPUT VOLTAGES PINS 2, 19, 33, 39, 40, 35 input low voltage	$-25^\circ C < T_A < +85^\circ C$			1.0	V
V_{IH}	input high voltage			3.5		
I_{ILK}	PIN 2, 39, 40 INPUT LEAKAGE, A, B				20	μA
R_{IN}	Input resistance to V_{DD} PINS 19,33	$V_{IN} = V_{DD} - 1.0V$	100	400		k Ω
R_{IN}	Input resistance to V_{SS} PIN 31	$V_{IN} = +1.0V$	50	100		
I_{OL}	Output Current PINS 3,5,6,7,17,18,32,38	$V_{OL} = +0.4V$	400			μA
I_{OH}	PINS 5,6,7,17,18,32	$V_{OH} = +2.4V$	100			μA
I_{OH}	PINS 3,38	$V_{OH} = V_{DD} - 0.8V$	265			
I_{OH}	ICM7226A PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER high output current	$V_O = V_{DD} - 2.0V$	150	180		mA
I_{OL}		low output current	$V_O = +1.0V$		-0.3	
I_{OL}	SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	$V_O = +1.5V$	25	35		mA
I_{OH}		high output current	$V_O = V_{DD} - 1.0V$		100	

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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0V$, $T_A = 25^\circ C$, unless otherwise specified.) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage				0.8	V
			2.0			
V_{IH}	input high voltage					
R_{IN}	input resistance to V_{SS}	$V_{IN} = +1.0V$	50	100		$k\Omega$
I_{OL}	ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	$V_O = +1.0V$	50	75		mA
		$V_O = V_{DD} - 2.5V$			100	
I_{OH}	high output current					
I_{OH}	SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30 high output current	$V_O = V_{DD} - 2.0V$	10	15		mA
		$V_O = V_{SS}$			10	μA
I_L	leakage current					
V_{IL}	MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage				$V_{DD} - 2.0$	V
			$V_{DD} - 0.8$			
V_{IH}	input high voltage					
R_{IN}	input resistance to V_{DD}	$V_{IN} = V_{DD} - 1.0V$	100	360		$k\Omega$

NOTE: Typical values are not tested.

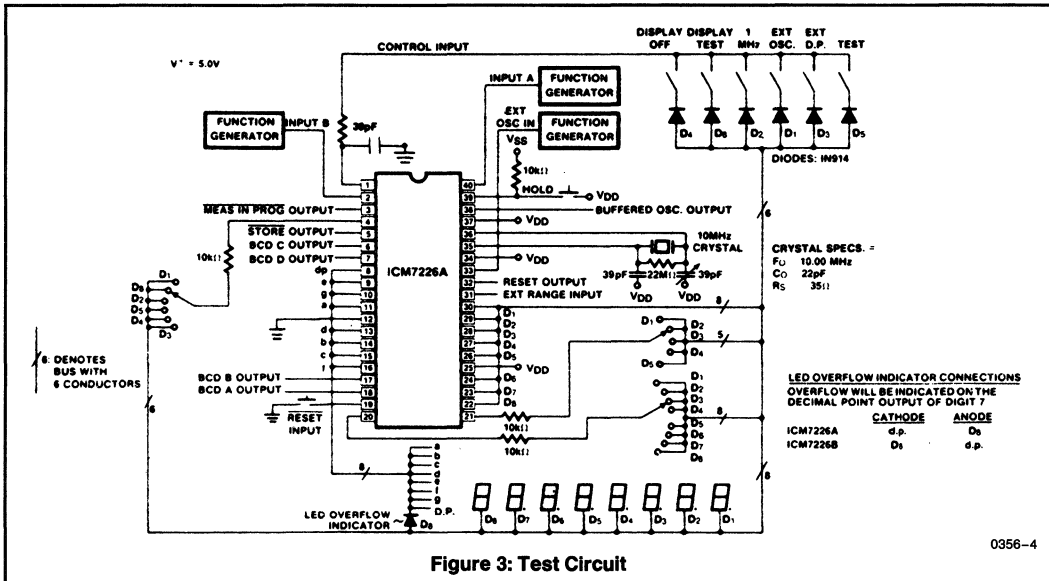


Figure 3: Test Circuit

0356-4

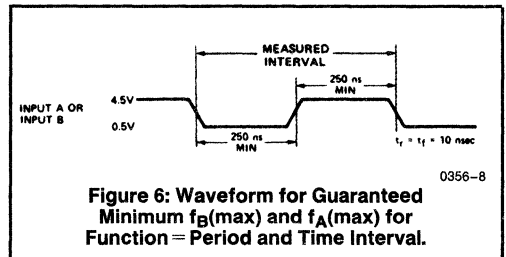
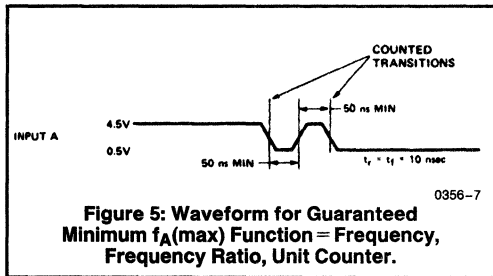
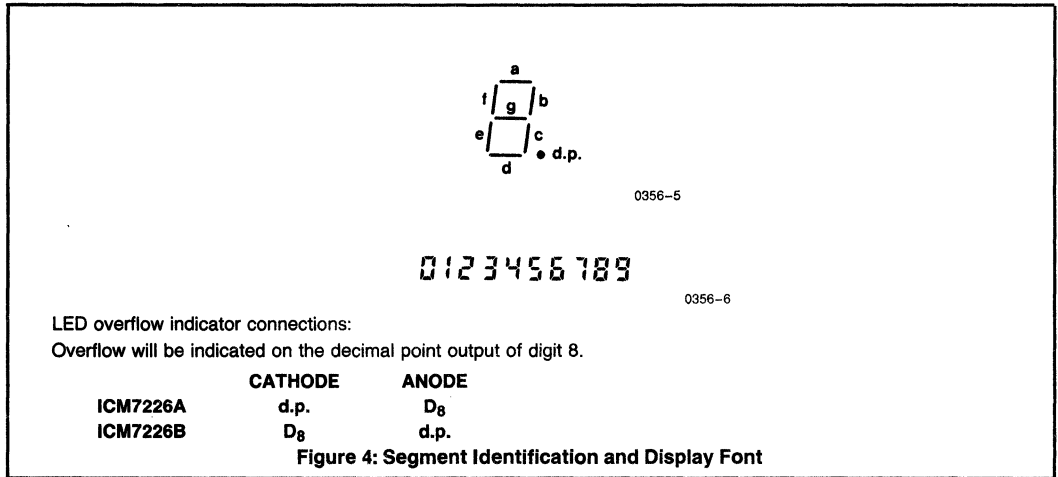
EVALUATION KIT

An evaluation kit is available for the ICM7226A. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226A. With the help of this kit, an engineer or techni-

cian can have the ICM7226A "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AJL, a 10MHz quartz crystal, eight each 7-segment 0.3" LEDs, PC board, resistors, capacitors, diodes, switches and IC socket. Order Number ICM7226AEV/Kit.

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NOTE: All typical values have been characterized but are not tested.



TIME INTERVAL MEASUREMENT

The ICM7226A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the **time interval** mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A/B as the first alternating signal states automatically prime the device. See Figure 7.

During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

DETAILED DESCRIPTION

INPUTS A & B

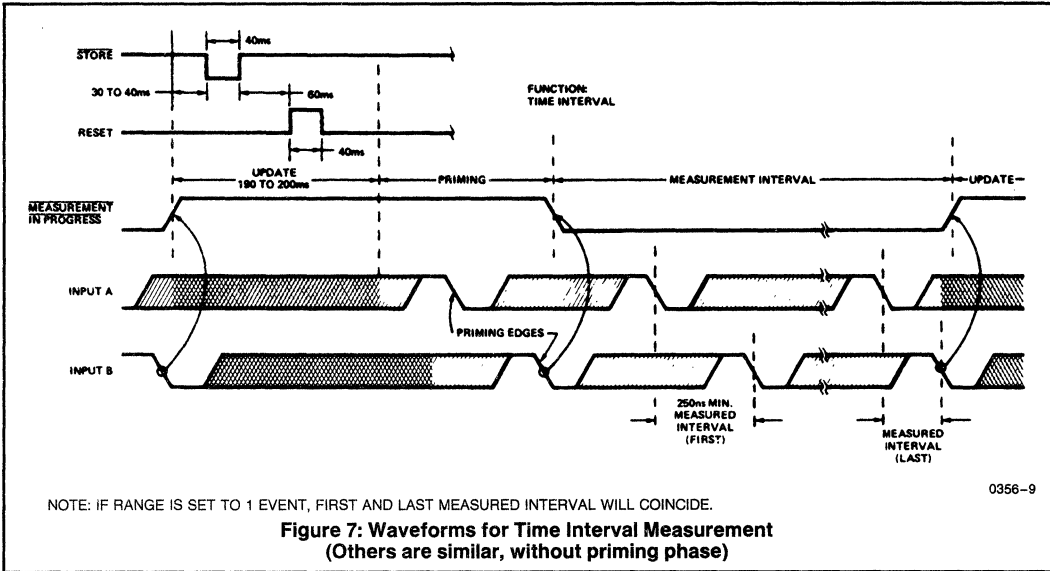
The signal to be measured is applied to INPUT A in **frequency period, unit counter, frequency ratio and time interval** modes. The other input signal to be measured is applied to INPUT B in **frequency ratio and time interval**. f_A should be higher than f_B during **frequency ratio**.

Both inputs are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V and input impedance of 250kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pull-up resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

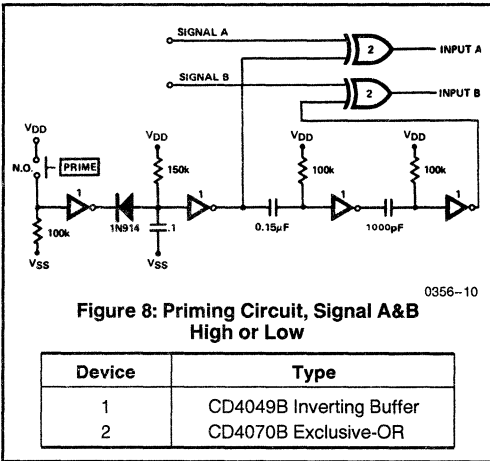
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This can be easily accomplished with the following circuit: (Figure 8).



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MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125µs). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Table 1: Multiple Input Control

FUNCTION INPUT	Function	Digit
Pin 4	Frequency	D ₁
	Period	D ₈
	Frequency Ratio	D ₂
	Time Interval	D ₅
	Unit Counter	D ₄
PIN 21	Oscillator Frequency	D ₃
	0.01 Sec/1 Cycle	D ₁
	0.1 Sec/10 cycles	D ₂
	1 Sec/100 Cycles	D ₃
	10 Sec/1k Cycles	D ₄
PIN 31	Enable External Range Input	D ₅
CONTROL INPUT PIN 1	Display Off	D ₄ & Hold
	Display Test	D ₈
	1MHz Select	D ₂
	External Oscillator Enable	D ₁
	External Decimal Point Enable	D ₃
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

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NOTE: All typical values have been characterized but are not tested.

CONTROL INPUTS

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if **display off** is selected at the same time.

Display Off — To enable the **display off** mode it is necessary to tie D_4 to the CONTROL input and have the HOLD input at V_{DD} . The chip will remain in this mode until HOLD is switched low. While in the **display off** mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5mA with a 10MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter.)

1MHz Select — The **1MHz select** mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in **period** and **time interval**, since the least significant digit will be in $1\mu s$ increments rather than $0.1\mu s$.

External Oscillator Enable — In this mode, the EXTERNAL OSCillator INput is used, rather than the on-chip oscillator, for the Timebase and Main Counter inputs in **period** and **time interval** modes. The on-chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to both OSC IN (pin 35) and EXT OSC IN (pin 33), or provide crystal for "default" oscillation, to avoid hang-up problems if an external OSC or TXCO will always be used, AC couple to OSC IN.

External Decimal Point Enable — When **external decimal point** is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

RANGE INPUT

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter, or if the EXTERNAL RANGE INput determines the measurement time. In all functional modes except **unit counter**, a change in the RANGE input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

FUNCTION INPUT

Six functions can be selected. They are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency**.

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In **time interval** a flip flop is set first by a $1 \rightarrow 0$ transition at INPUT A and then reset by a $1 \rightarrow 0$ transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement

in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow indication is output on the Decimal Point Output during D_8 .

Table 2: Input Routing

Description	Main Counter	Reference Counter
Frequency (f_A)	Input A	100 Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A \rightarrow B)	Osc ON Gate	Osc OFF Gate
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator $\div 10^5$ or 10^4)

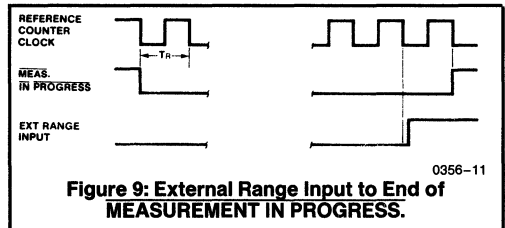
EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected, this input is active. Any of the digits, except D_8 , can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input — Except in the **unit counter** mode, when the HOLD input is at V_{DD} , any measurement in progress (before \overline{STORE} goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD} , the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

RESET Input — The \overline{RESET} Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTERNAL RANGE Input — The EXTERNAL RANGE Input is used to select other ranges than those provided on the chip. Figure 9 shows the relationship between MEASUREMENT IN PROGRESS and EXTERNAL RANGE Input.



MEASUREMENT IN PROGRESS, STORE AND RESET

Outputs — These Outputs are provided to facilitate external interfacing. Figure 10 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The MEASUREMENT IN PROGRESS output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.

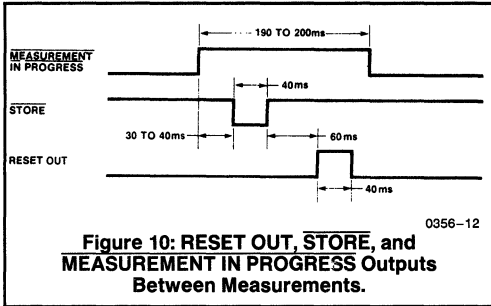


Figure 10: RESET OUT, STORE, and MEASUREMENT IN PROGRESS Outputs Between Measurements.

BCD Outputs — The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A—Common Anode) or negative going (ICM7226B — Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

Table 3: Truth Table BCD Outputs

Number	BCD 8 Pin 7	BCD 4 Pin 6	BCD 2 Pin 17	BCD 1 Pin 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFFERed OSCillator OUTPUT — The BUFFERed OSCillator OUTPUT has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244 μ s, and an interdigit blanking time of 6 μ s to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the

Main Counter overflows. The internal decimal point control displays frequency in kHz and time in μ s.

The ICM7226A is designed to drive common anode LED displays at a peak current of 25mA/segment, using displays with $V_F=1.8V$ at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with $V_F=1.8V$ at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 11, 12, 13 and 14 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

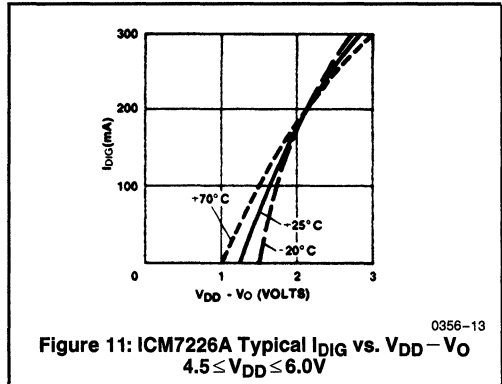


Figure 11: ICM7226A Typical I_{DIG} vs. $V_{DD} - V_O$ $4.5 \leq V_{DD} \leq 6.0V$

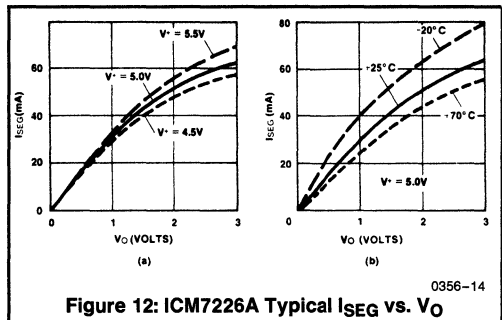


Figure 12: ICM7226A Typical I_{SEG} vs. V_O

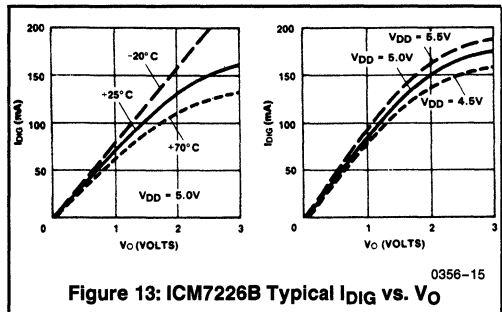
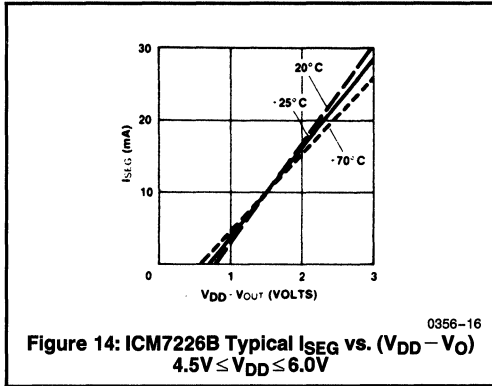


Figure 13: ICM7226B Typical I_{DIG} vs. V_O

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NOTE: All typical values have been characterized but are not tested.



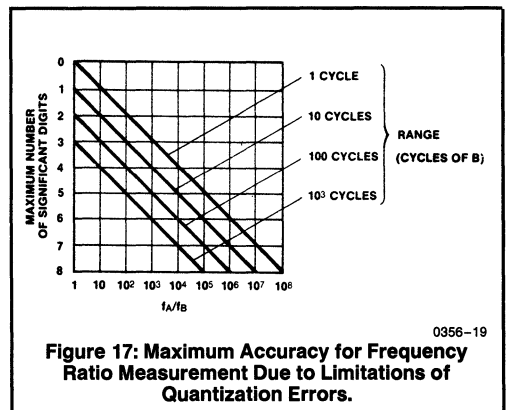
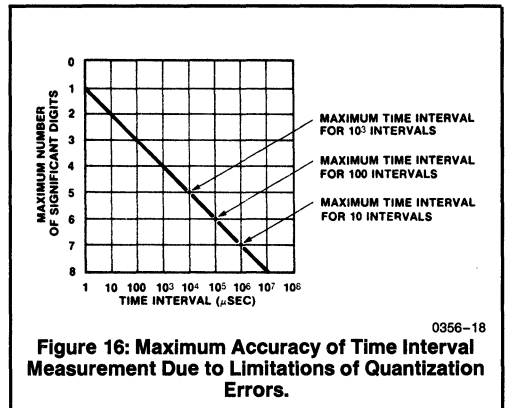
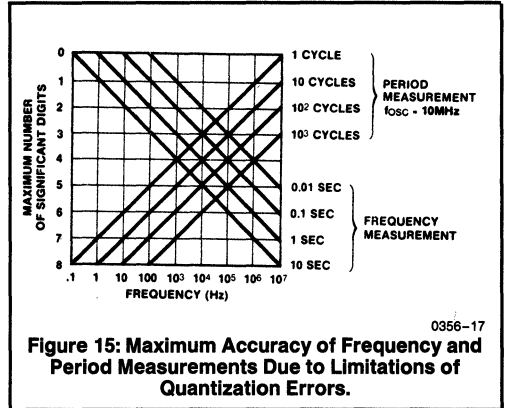
To increase the light output from the displays, VDD may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

ACCURACY

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency**, **period** and **time interval** modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode, maximum accuracy is obtained with high frequency inputs, and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 15, the least accuracy will be obtained at 10kHz. In **time interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 16. In **frequency ratio** measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 17.



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CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V_{DD} should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in Figure 18.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **frequency and period counter**. To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 20 shows use of a $\div 10$ prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy. Note that A IN comes from Q_C rather than Q_D , to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74LS121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.

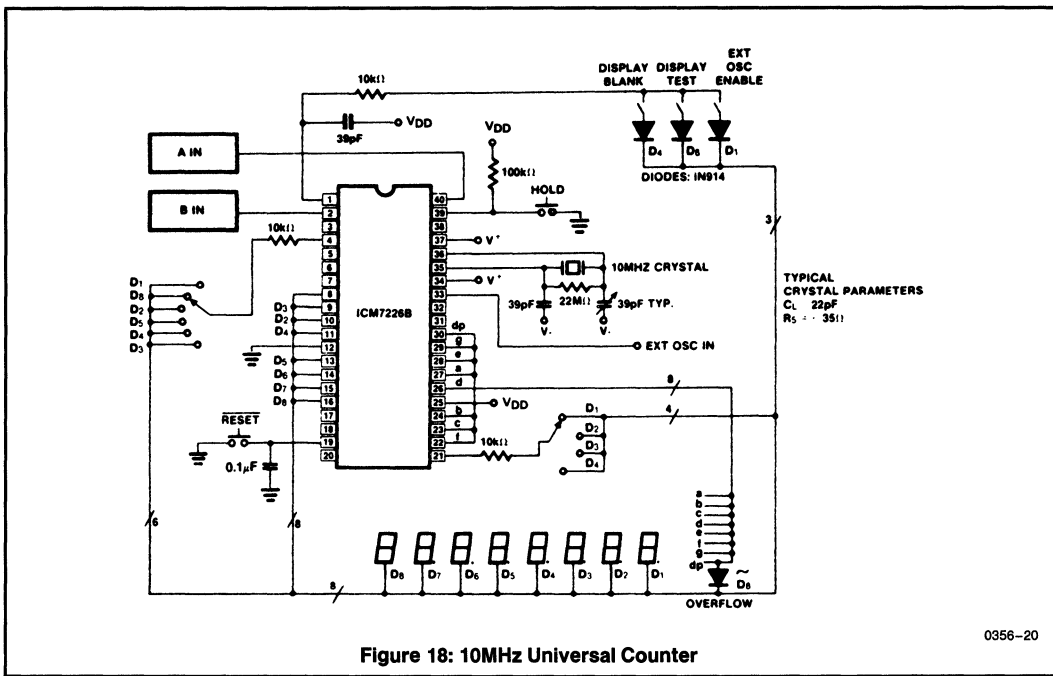
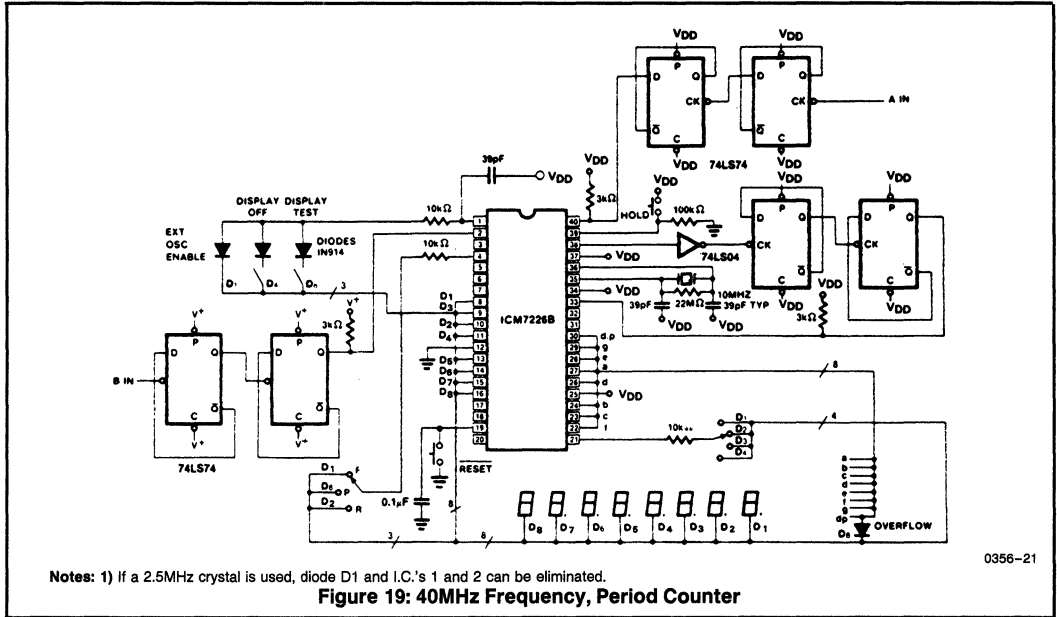


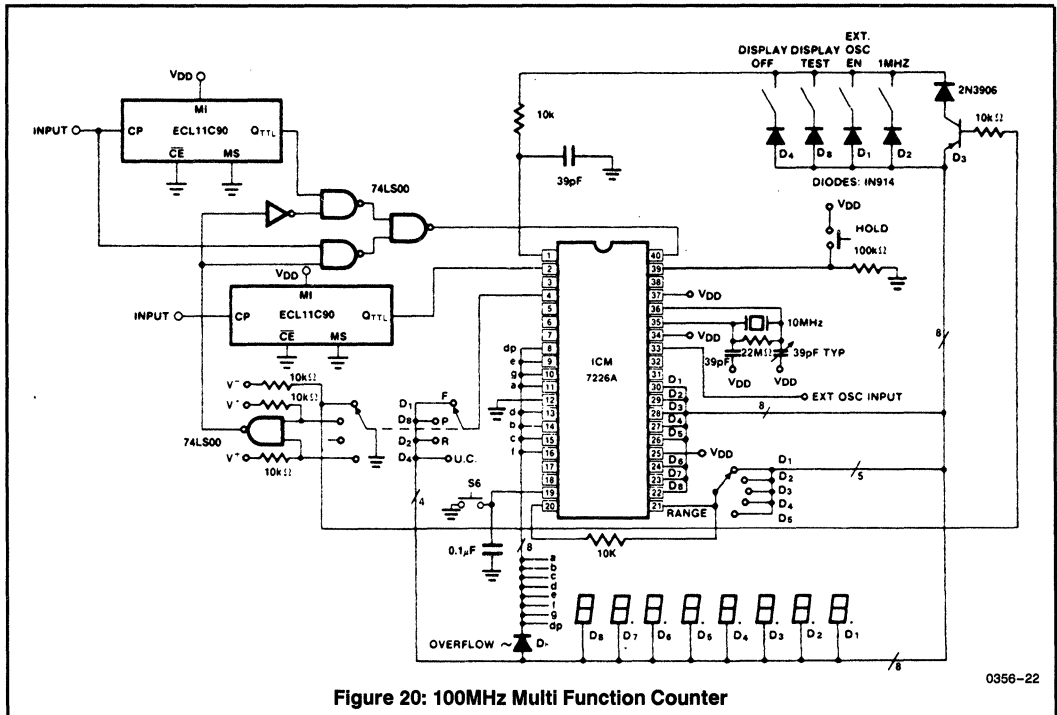
Figure 18: 10MHz Universal Counter

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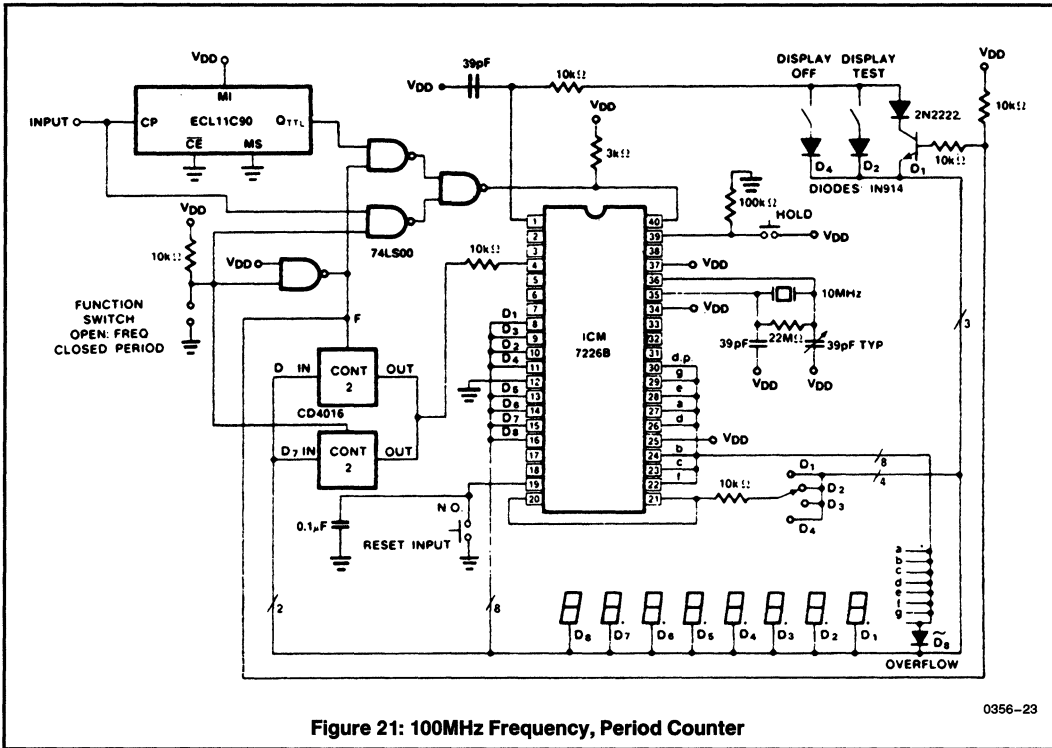
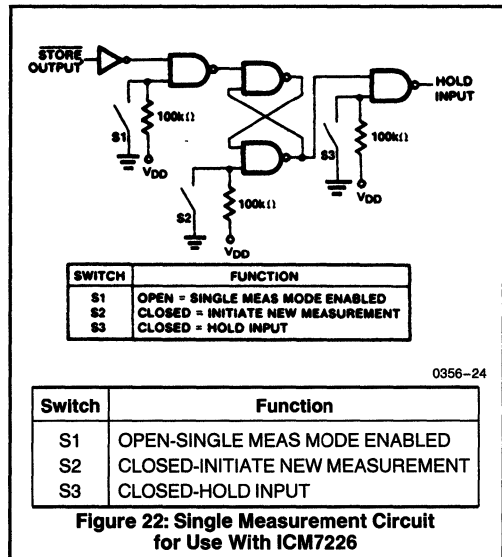


Figure 21: 100MHz Frequency, Period Counter

0356-23

Figure 21 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74LS153 or 74LS251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

The circuit shown in Figure 22 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the STORE output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in Figure 23 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 23 on the circuit shown in Figure 19 will reduce the time between measurements from 1600ms to 800ms.



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Figure 22: Single Measurement Circuit for Use With ICM7226

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NOTE: All typical values have been characterized but are not tested.

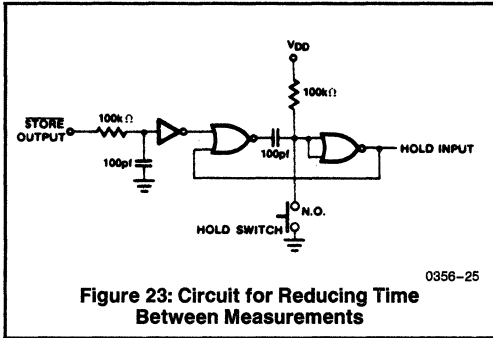


Figure 23: Circuit for Reducing Time Between Measurements

0356-25

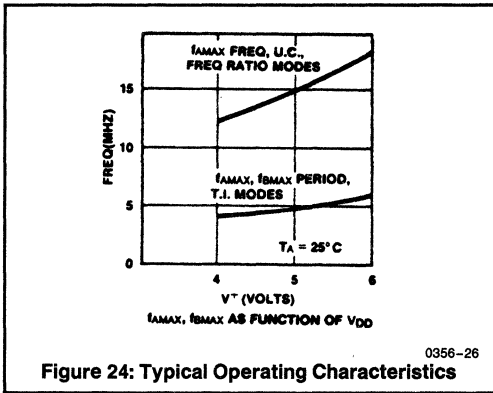


Figure 24: Typical Operating Characteristics

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Figure 25 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive two ICM7211 display drivers. The ICM7226 EV/Kit may easily be interfaced to 2 ICM7211 EV/Kits in this way. A similar arrangement can be used for driving vacuum fluorescent displays with the ICM7235.

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a load capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required gm can be calculated as follows:

$$g_m = \omega^2 C_{IN} C_{OUT} R_s \left(1 + \frac{C_0}{C_L} \right)^2$$

- where
- C_L = $\left(\frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}} \right)$
 - C_0 = Crystal static capacitance
 - R_s = Crystal Series Resistance
 - C_{in} = Input Capacitance
 - C_{out} = Output Capacitance
 - ω = $2\pi f$

The required gm should not exceed 50% of the gm specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4pF to CIN and COUT. For maximum frequency stability, CIN and COUT should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10MHz nor 1MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate is

$$f_{mux} = \frac{f_{osc}}{2 \times 10^4} \text{ for 10MHz mode and } f_{mux} = \frac{f_{osc}}{2 \times 10^3} \text{ for the 1MHz mode.}$$

The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in

the 10MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1MHz mode. The buff-

ered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to VDD.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFFered OSCillator OUTPUT and EXTERNAL OSCillator INPUT to the OSCillator OUTPUT or OSCillator INPUT can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to VDD or VSS and these two signals should be kept away from the oscillator circuit.

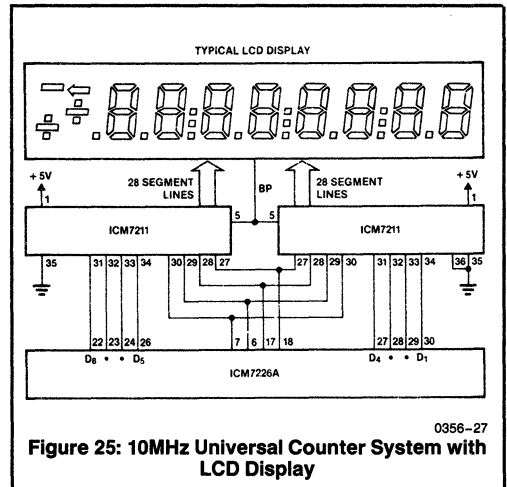


Figure 25: 10MHz Universal Counter System with LCD Display

0356-27

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NOTE: All typical values have been characterized but are not tested.

ICM7236

4½-Digit Counter/Vacuum Fluorescent Display Driver



ICM7236

GENERAL DESCRIPTION

The ICM7236 and ICM7236A devices are high-performance CMOS 4½-digit counters. They include 7-segment decoders, output latches, count inhibit, reset, and leading zero blanking circuitry, as well as twenty-nine high-voltage open drain P-channel transistor outputs suitable for driving non-multiplexed (static) vacuum fluorescent displays.

The ICM7236 is a decade counter, providing a maximum count of 19999, while the ICM7236A is intended for timing purposes, and provides a maximum count of 15959.

The counter section of the two devices in the ICM7236 family provides direct static counting from DC to 15MHz guaranteed (with a 5V ± 10% supply) over the operating temperature range. At normal room temperatures, the device will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger for operation in noisy environments and allows correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allow a direct interface to the ICM7207 devices. This results in a low cost, low power frequency counter with minimum component count.

These devices also incorporate features intended to simplify cascading in four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INPUT and OUTPUT allow correct leading zero blanking between four-decade blocks.

The ICM7236 and ICM7236A are packaged in a standard 40-pin dual-in-line plastic and CERDIP packages.

ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7236iJL	-40°C to +85°C	40-PIN CERDIP
ICM7236AiJL	-40°C to +85°C	40-PIN CERDIP
ICM7236iPL	-40°C to +85°C	40-PIN PLASTIC DIP
ICM7236AiPL	-40°C to +85°C	40-PIN PLASTIC DIP
ICM7236/D	-40°C to +85°C	DICE
ICM7236A/D	-40°C to +85°C	DICE
ICM7236EV/KIT		EVALUATION KIT

FEATURES

- High Frequency Counting — Guaranteed 15MHz, Typically 25MHz at T_A = 25°C
- Low Power Operation — Less Than 100µW Quiescent
- Direct 4½-Digit Seven-Segment Display Drive for Non-Multiplexed Vacuum Fluorescent Displays
- STORE and RESET Inputs Permit Operation As Frequency or Period Counter
- True COUNT INHIBIT Disables First Counter Stage
- CARRY Output for Cascading Four-Digit Blocks
- Schmitt-Trigger On COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs
- Leading Zero Blanking INPUT and OUTPUT for Correct Leading Zero Blanking With Cascaded Devices

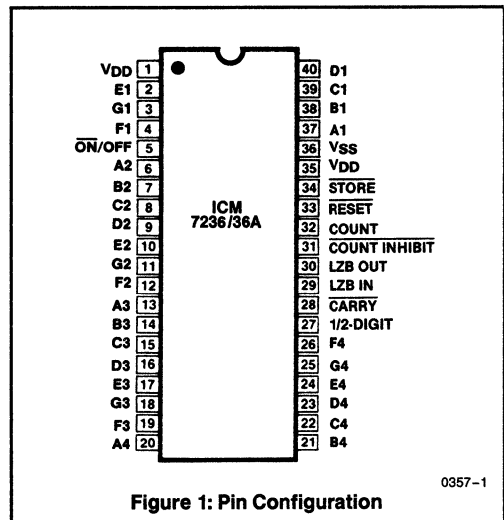


Figure 1: Pin Configuration

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) 0.5W @ + 70°C
 Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
 Display Voltage (Note 3) $V_{DD} - 3V$
 Input Voltage ($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)

Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10sec) 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

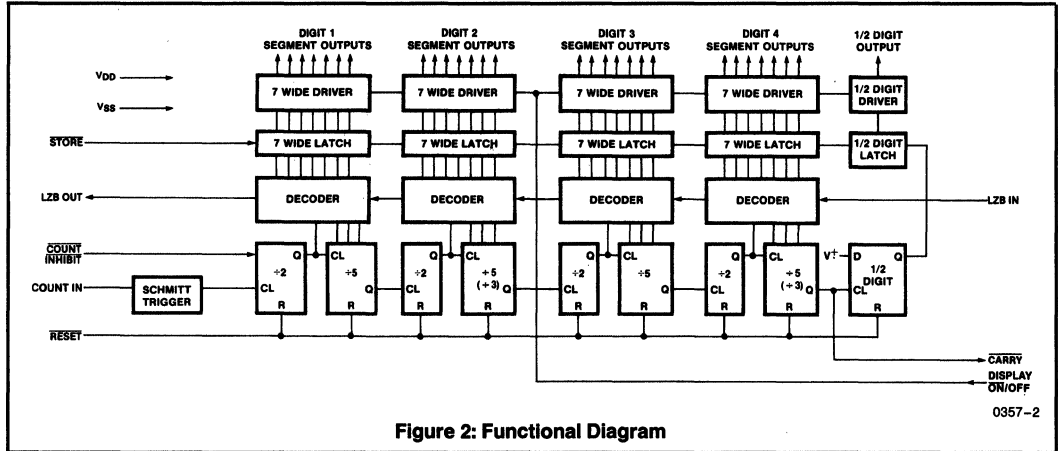


Figure 2: Functional Diagram

0357-2

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5V, V_{SS} = 0V, T_A = 25^\circ C$, unless otherwise indicated).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD} - V_{SS}$)		3	5	6	V
I_{DD}	Operating Current	Test circuit, Display blank		10	50	μA
V_{DISP}	Display Voltage				30	V
I_{DLK}	Display Output Leakage	Output OFF, $V_{DISP} = V_{DD} - 30V$		0.1	10	μA
I_p	Input Pullup Currents	Pins 29, 31, 33, 34 $V_{IN} = V_{DD} - 3V$		10		μA
V_{IH}	Input High Voltage	Pins 29, 31, 33, 34	3			V
V_{IL}	Input Low Voltage	Pins 29, 31, 33, 34			2	V
V_{CT}	COUNT Input Threshold			2		V
V_{CH}	COUNT Input Hysteresis			0.5		V
I_{OH}	Output High Current	\bar{CARRY} (Pin 28), LZB OUT (Pin 30) $V_{OUT} = V_{DD} - 3V$.	350	500		μA
I_{OL}	Output Low Current	\bar{CARRY} (Pin 28), LZB OUT (Pin 30) $V_{OUT} = +3V$.	350	500		μA
f_{count}	Count Frequency	$4.5V < V_{DD} < 6V$	0	25	15	MHz
t_s, t_w	STORE, RESET Minimum Pulse Width		3			μs

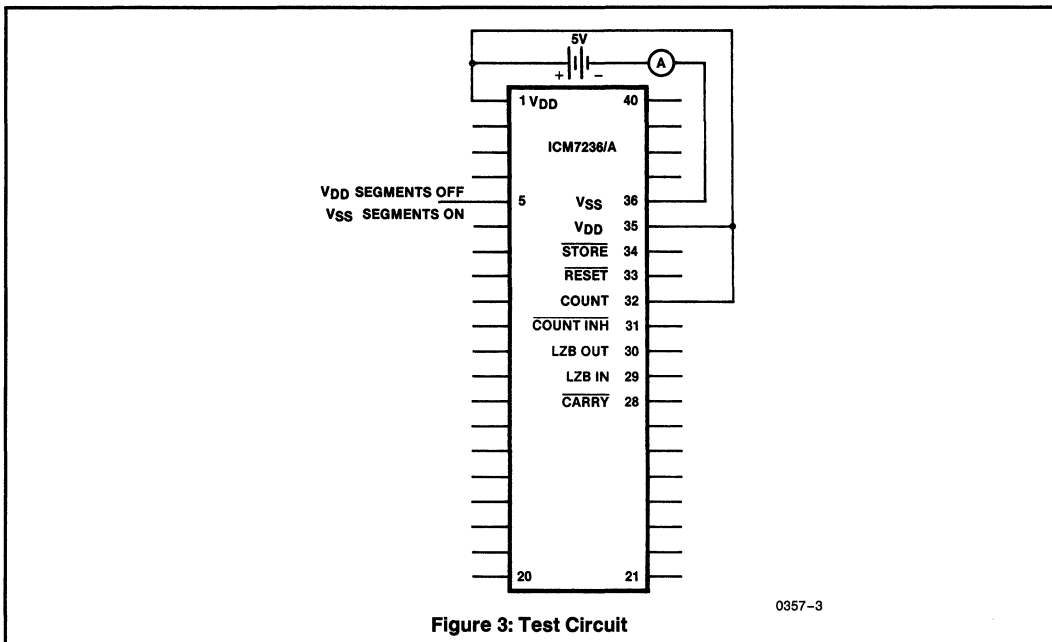
- NOTES:**
- This limit refers to that of the package and will not occur during normal operation.
 - Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V_{DD} or less than ground may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7236/7236A be turned on first.
 - This limit refers to the display output terminals only.

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NOTE: All typical values have been characterized but are not tested.

OPERATING CHARACTERISTICS

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking Input (LZB IN)	29	V _{DD} or Floating V _{SS}	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V _{DD} or Floating V _{SS}	Counter Enabled Counter Disabled
RESET	33	V _{DD} or Floating V _{SS}	Inactive Counter Reset to 0000
STORE	34	V _{DD} or Floating V _{SS}	Output Latches Not Updated Output Latches Updated
Display $\overline{\text{ON}}$ /OFF	5	V _{DD} V _{SS}	Display Outputs Disabled Display Outputs Enabled

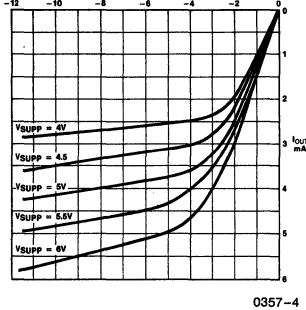


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NOTE: All typical values have been characterized but are not tested.

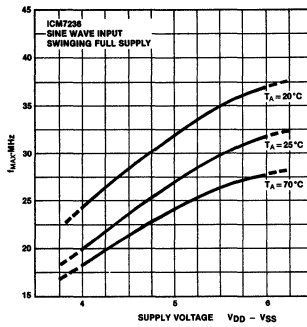
TYPICAL PERFORMANCE CHARACTERISTICS

Output Characteristics
V₀



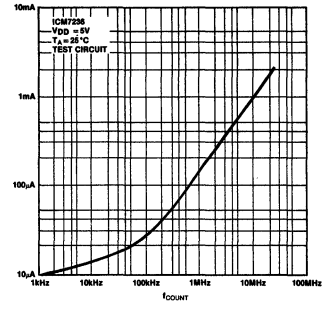
0357-4

Maximum Count Frequency (Typical)
as a Function of Supply Voltage



0357-5

Supply Current as a Function of
Count Frequency



0357-6

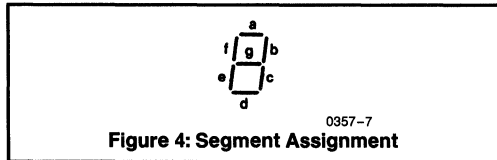
DESCRIPTION OF OPERATION

Both devices in the ICM7236 family provide twenty-nine outputs suitable for directly driving the anode terminals of 4½ digit seven-segment non-multiplexed (static) vacuum-fluorescent displays. Each display output is the drain of a high-voltage low-leakage P-channel transistor, capable of withstanding typically greater than -35 volts with respect to V_{DD}. The output characteristics are shown graphically under "Typical Characteristics."

These chips also provide a display $\overline{\text{ON}}$ /OFF input which may be used to disable all the segment outputs and thus blank the display. This input may also be used to control the display brightness by varying the duty cycle of a signal at the input swinging between V_{DD} and V_{SS}.

Note that these circuits have two terminals for V_{DD}; both of these pins should be connected to the power supply positive terminal. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

These chips may also be used to directly drive non-multiplexed common-cathode LED displays, where each segment of the display is driven by one ICM7236 output, and the common cathode is connected to ground. With a 5V power supply and a 1.7V LED diode forward voltage drop, the current in an "ON" segment will be typically 3mA. This should provide sufficient brightness in displays up to about 0.3" character height.



0357-7

Figure 4: Segment Assignment

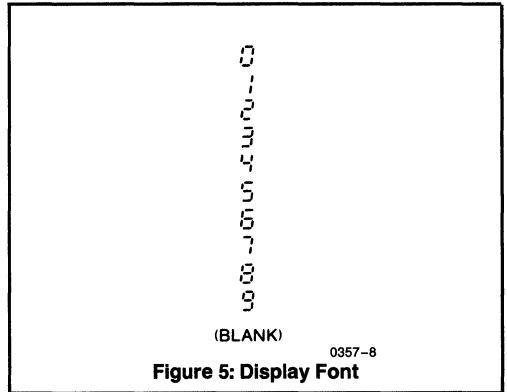


Figure 5: Display Font

COUNTER SECTION

The devices in the ICM7236 family implement a four-digit ripple-carry resettable counter, including a Schmitt trigger COUNT input and a CARRY output. Also included is an extra D-type flip-flop, clocked by the carry signal, which controls the half-digit segment driver. This can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, and the CARRY output will provide a negative-going edge following the count which increments the counter from 9999 (or 5959) to 10000. Once half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the RESET terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent CARRY outputs will not be affected.

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NOTE: All typical values have been characterized but are not tested.

A negative level at the **COUNT INHIBIT** disables the first divide-by-two flip-flop in the counter chain without affecting its clock. This provides a true **count** inhibit which is not sensitive to the state of the **COUNT** input, and prevents false counts which can result from a normal logic gate forcing the state of the clock to prevent counting.

Each decade is fed directly into a four-to-seven line decoder which generates the seven-segment output code. Each decoder output corresponds to one-segment terminal of the device. The output data is latched at the driver. When the **STORE** pin is at a negative level, the latches are updated, and when the pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating, or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the Leading Zero Blanking INput is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, and can

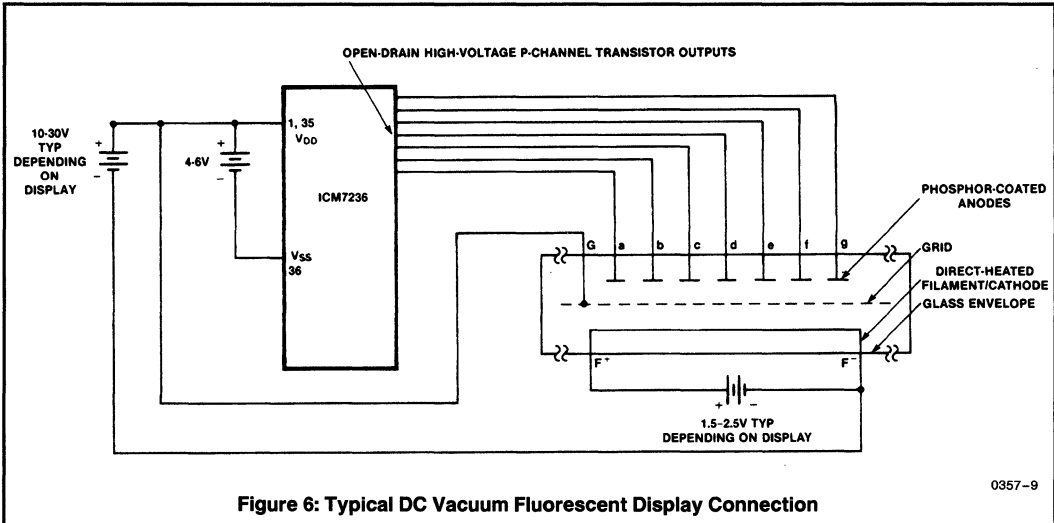
only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, on an eight-decade counter with overflow using two ICM7236 devices, the Leading Zero Blanking OUTput of the high-order digit device would be connected to the Leading Zero Blanking INput of the low-order digit device. This will assure correct leading zero blanking for all eight digits.

The **STORE**, **RESET**, **COUNT INHIBIT**, and Leading Zero Blanking INputs are provided with internal pullup devices, so that they may be left open when a positive level is desired. The **CARRY** and Leading Zero OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7236 devices in four-digit blocks.

CONTROL INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.



VACUUM FLUORESCENT DISPLAYS (4½-DIGIT):

N.E.C. Electronics, Inc.
Model FIP5F8S

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NOTE: All typical values have been characterized but are not tested.

ICM7240/ICM7250

Programmable Timer



GENERAL DESCRIPTION

The ICM7240/50 is a family of CMOS Timer/Counter circuits intended to replace Intersil's ICM8240/50 and the 2240 in most applications. Together with the ICM7555/56 (CMOS versions of the SE/NE 555/6), they provide a complete line of RC oscillators/timers/counters offering lower supply currents, wider supply voltage ranges, higher operating frequencies, lower component counts and a wider range of timing components. They are intended to simplify the selection of various time delays or frequency outputs from a fixed RC oscillator circuit.

Each device consists of a counter section, control circuitry, and an RC oscillator requiring an external resistor and capacitor. For counter/divider applications, the oscillator may be inhibited and an input clock applied to the TB terminal. The ICM7240 is intended for straight binary counting or timing, whereas the ICM7250 is optimized for decimal counting or timing. Both devices use open drain output transistors, thereby allowing wire AND-ing. Manual programming is easily accomplished by the use of standard thumbwheel switches or hardwired connections. The ICM7240/50 are packaged in 16 pin Cerdip packages.

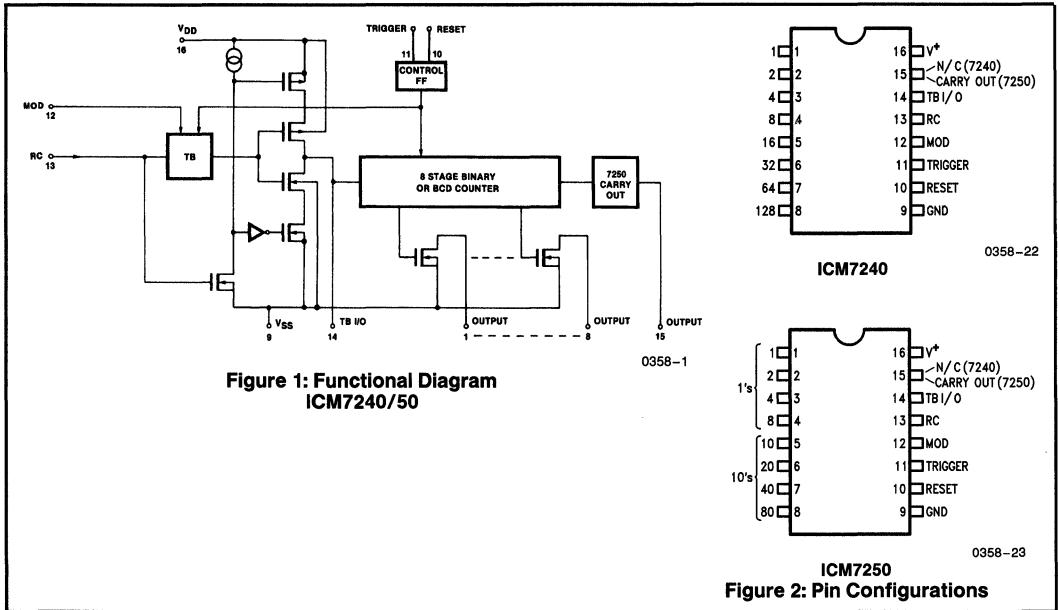
Applications include programmable timing, long delay generation, cascadeable counters, programmable counters, low frequency oscillators, and sequence timing.

FEATURES

- Replaces 8240/50, 2240 in Most Applications
- Timing From Microseconds to Days
- May Be Used As Fixed or Programmable Counter
- Programmable With Standard Thumbwheel Switches
- Select Output Count From
1RC to 255RC (ICM7240)
1RC to 99RC (ICM7250)
- Monostable or Astable Operation
- Low Supply Current: 115 μ A @ 5 Volts
- Wide Supply Voltage Range: 2 - 16 Volts
- Cascadeable

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7240JE	-25°C to +85°C	16 Lead Cerdip
ICM7250JE	-25°C to +85°C	16 Lead Cerdip



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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 18V
 Input Voltage^[1]
 Terminals 10,11,12,13,14 $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
 Maximum continuous output
 current (each output) 50mA

Power Dissipation^[2] 200mW
 Operating Temperature Range $-25^{\circ}C$ to $+85^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10sec) $300^{\circ}C$

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7240/50 be turned on first.

2. Derate at $-2mW/^{\circ}C$ above $25^{\circ}C$.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

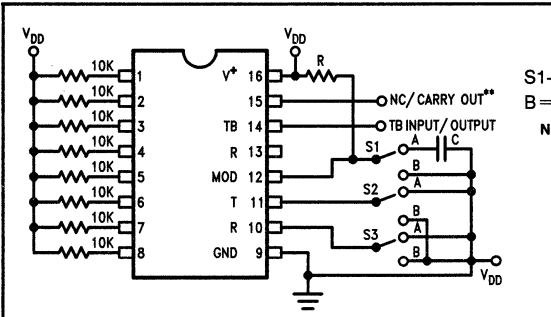
($V_{DD}=5V$, $V_{SS}=0V$, $T_A = +25^{\circ}C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Guaranteed Supply Voltage ($V_{DD}-V_{SS}$)		2		16	V
I_{DD}	Supply Current	Reset Operating, $R = 10k\Omega$, $C = 0.1\mu F$ Operating, $R = 1M\Omega$, $C = 0.1\mu F$ TB Inhibited, RC Connected to GND		125 300 120 125	800 600	μA μA μA μA
	Timing Accuracy			5		%
$\Delta f/\Delta T$	RC Oscillator Frequency Temperature Drift	(Exclusive of RC Drift)		250		ppm/ $^{\circ}C$
V_{OTB}	Time Base Output Voltage	$I_{SOURCE} = 100\mu A$ $I_{SINK} = 1.0mA$		3.50 0.40		V
I_{TBLK}	Time Base Output Leakage Current	RC = Ground			25	μA
V_{MOD}	Mod Voltage Level	$V_{DD} = 5V$ $V_{DD} = 15V$		3.5 11.0		V V
V_{TRIG}	Trigger Input Voltage	$V_{DD} = 5V$ $V_{DD} = 15V$		1.6 3.5	2.0 4.5	V V
V_{RST}	Reset Input Voltage	$V_{DD} = 5V$ $V_{DD} = 15V$		1.3 2.7	2.0 4.0	V V
f_t	Max Count Toggle Rate 7240	$V_{DD} = 2V$ $V_{DD} = 5V$ $V_{DD} = 15V$ } Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}	2	1 6 13		MHz MHz MHz
f_t	Max Counter Toggle Rate 7250	$V_{DD} = 5V$ (Counter/Divider Mode)	2	5		MHz
f_t	Max Count Toggle Rate	Programmed Timer — Divider Mode			100	kHz
V_{SAT}	Output Saturation Voltage	All Outputs except TB Output $V_{DD} = 5V$, $I_{OUT} = 3.2 mA$		0.22	0.4	V
I_{OLK}	Output Leakage Current	$V_{DD} = 5V$, per Output			1	μA
C_t	MIN Timing Capacitor (Note 1)		10			pF
R_t	Timing Resistor Range (Note 1)	$V_{DD} \leq 5.5V$ $V_{DD} \leq 16V$	1K 1K		12M 12M	Ω Ω

NOTE: 1. For Design only, not tested.

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NOTE: All typical values have been characterized but are not tested.



0358-3

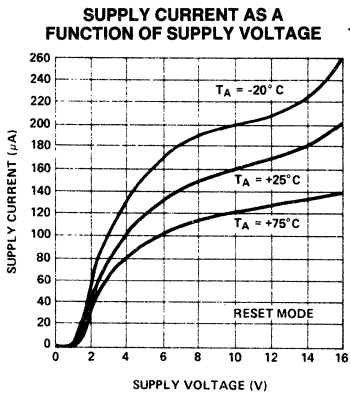
Figure 3: Test Circuit

S1-A = RC RUN S2-A = INACTIVE S3-A = INACTIVE
 B = T.B. INPUT RUN B = TRIGGER B = RESET

NOTE: S1-B INHIBITS THE TIMEBASE SECTION, ALLOWING TERMINAL 14 TO BECOME THE COUNTER INPUT.

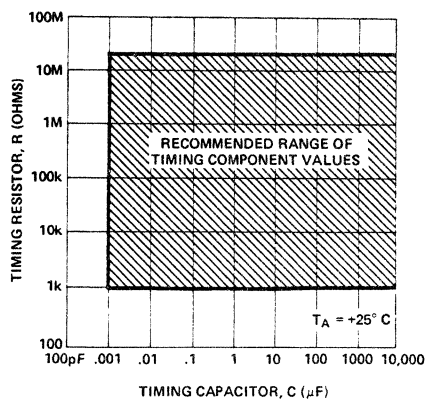
** TERMINAL 15 IS CARRY OUTPUT FOR 7250 DEVICES.

TYPICAL PERFORMANCE CHARACTERISTICS



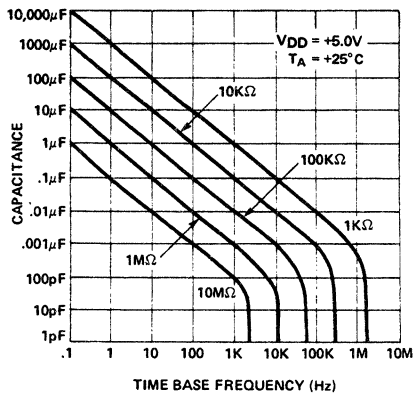
0358-4

RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



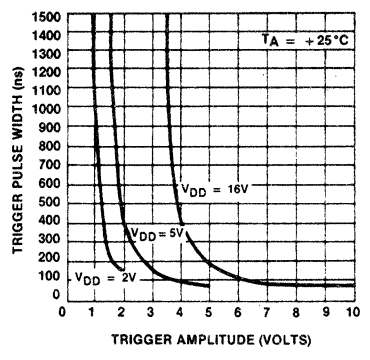
0358-5

TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



0358-6

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



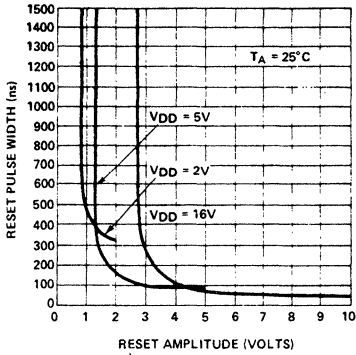
0358-7

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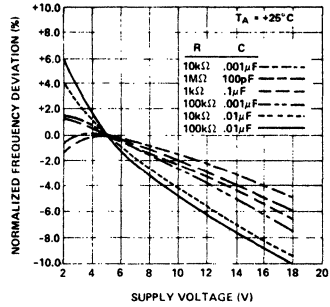
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE

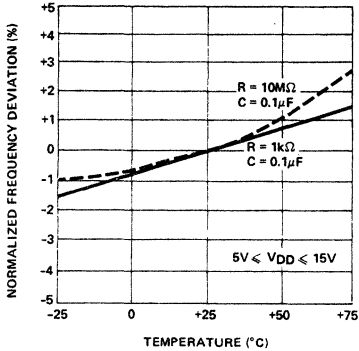


NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



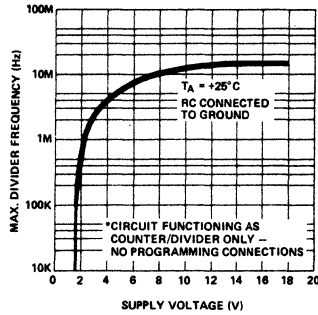
0358-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



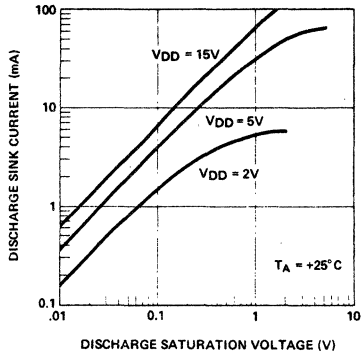
0358-8

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE*



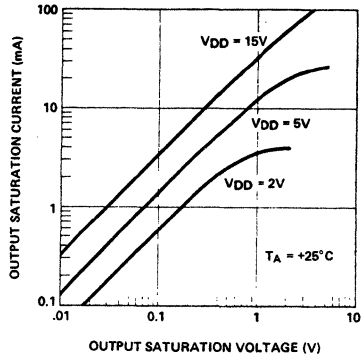
0358-11

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0358-10

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



0358-12

0358-13

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NOTE: All typical values have been characterized but are not tested.

CIRCUIT DESCRIPTION

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This pulse enables the counter section, sets all counter outputs to the LOW or ON state, and starts the time base oscillator. Then, external R is charged through external C from 20% to 70% of $V_{DD}-V_{SS}$, generating a timing waveform with period t , equal to $1RC$. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. These clock pulses are counted by the binary counter of the 7240 or by two cascaded Binary Coded Decimal (BCD) Counters in the 7250. The timing cycle terminates when a positive level is applied to RESET. When the circuit is at reset, both the time base and the counter sections are disabled and all the counter outputs are at a HIGH or OFF state. The carry-out is also HIGH. Both devices utilize an identical timebase, control flip-flops, and basic counters, with the outputs consisting of open drain n-channel transistors. Only the ICM7250 has CARRY outputs.

In most timing applications, one or more of the counter outputs are connected back to RESET, the circuit will start timing when a TRIGGER is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the RESET (switch S_1 open), the circuit operates in its astable, or free-running mode, after initial triggering.

DESCRIPTION OF PIN FUNCTIONS COUNTER OUTPUTS (PINS 1 THROUGH 8)

Each binary counter output is a buffered "open-drain" type. At reset condition, all the counter outputs are at a high, or non-conducting state. After a trigger input or when using the internal timebase, the outputs change state (see timing diagram, Figure 4). If an external clock input is used, the trigger input must overlap at least the first falling edge of the clock. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Programming section.

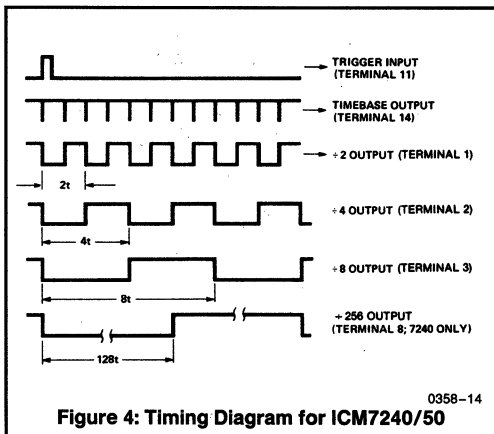


Figure 4: Timing Diagram for ICM7240/50

V_{SS} (PIN 9)

This is the return or most negative supply pin. It should have a very low impedance as the capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuits are reset or triggered by a positive level applied to pins 10 and 11, and once triggered they ignore additional trigger inputs until either the timing cycle is completed or a reset signal is applied. If both reset and trigger are applied simultaneously trigger overrides reset. Minimum input pulse widths are shown in the typical performance characteristics. Note that all devices feature power ON reset.

MODULATION AND SYNC INPUT (PIN 12)

The period, t , of the time base oscillator can be modulated by applying a DC voltage to this terminal. The time base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12.

TIMEBASE INPUT/OUTPUT PIN (PIN 14)

While this pin can be used as either a time base input or output terminal, it should only be used as an input if the RC pin is connected to V_{SS} .

If the counter is to be externally driven, care should be taken to ensure that fall times are fast (see Operating Limits section).

Under no conditions is a 300pF capacitor on this terminal useful and should be removed if a 7240/50 is used to replace an 8240/50 or 2240.

CARRY OUTPUT (PIN 15, ICM7250 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 7250 counter stage while still using all the counter outputs of the first. Thus, by cascading several 7250's a large BCD countdown can be achieved.

The basic timing diagrams for the ICM7240/50 are shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive level on the RESET terminal (if TRIGGER is low), a positive level on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states.

Note that for straight binary counting the outputs are symmetrical; that is, a 50% duty cycle HI-LO. This is not the case when using BCD counting. (See Figure 6.)

PROGRAMMING CAPABILITY

The counter outputs, pins 1 through 8, are open-drain N-channel FETs, and can be shorted together to a common pull-up resistor to form a "wired-AND" connection. The combined output will be LOW as long as **any one** of the outputs is low. Each output is capable of sinking ≈ 5 mA. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle (monostable mode) t_0 would be $32t$ for a 7240 and $20t$ for a 7250. Similarly, if pins, 1, 5, and 6 were

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NOTE: All typical values have been characterized but are not tested.

shorted to the output bus, the total time delay would be $t_o = (1 + 16 + 32)t$ for the 7240 or $(1 + 10 + 20)t$ for the 7250. Thus, by selecting the number of counter terminals connected to the output bus, the timing cycle can be programmed from:

$$1t \leq t_o \leq 255t \text{ (7240)}$$

$$1t \leq t_o \leq 99t \text{ (7250)}$$

Note that for the 7250, invalid count states (BCD values ≥ 10) will not be recognized and the counter will not stop.

The 7240/50 can be configured to initiate a controlled timing cycle upon power up, and also reset internally; see Figure 5. Applications for this could include lawn watering sprinkler timing, pump operation, etc.

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 5, the output of the 7240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 4, which shows the phase relations between the counter outputs. Figure 6 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

THUMBWHEEL SWITCHES

While the ICM7240 is frequently hard wired for a particular function, the ICM7250 can easily be programmed using thumbwheel switches. Standard BCD thumbwheel switches have one common and four inputs (1,2,4 and 8) which are connected according to the binary equivalent to the digits 0 through 9.

For a single ICM7250 two such switches would select a time of $1RC$ to $99RC$. Cascading two ICM7250's (using the carry out gate) would expand selection to $9999RC$.

NOTES ON THE COUNTER SECTION

Used as a straight binary counter (ICM7240), or as a $\div 100$ (ICM7250), both devices are significantly faster than their bipolar equivalents. However, when using these devices as *programmable* counters the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 (ICM7240), or 100 (ICM7250), the maximum input frequency must be limited to approximately 100kHz or less (with V_{DD} equal to +5 volts). The reason for this is two-fold:

- Since Ripple counters are used, there is a propagation delay between each individual $\div 2$ counter (8 counters for the ICM7240/50). Outputs from the individual $\div 2$ counters are AND'ed together to provide the output signal and the RESET/TRIGGER signal.
- There must be a delay of the positive going output to RESET, (pin 10) and TRIGGER (pin 11). The RESET signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The TRIGGER overrides RESET.

The delay between TRIGGER and RESET is generated by the signal RC network consisting of the 56k Ω resistor and the 330pF capacitor.

The delay caused by the counter ripple delays can be as long as 2 μ s (5 volt supply), and the delay between RESET and TRIGGER should be at least 2 μ s. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation. See Figure 7 and 8.

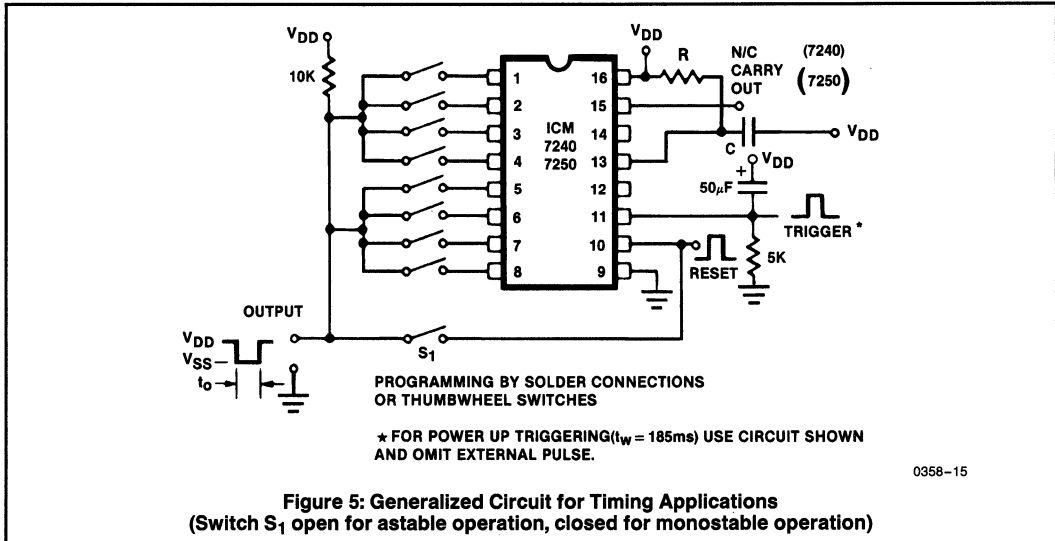


Figure 5: Generalized Circuit for Timing Applications
(Switch S_1 open for astable operation, closed for monostable operation)

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NOTE: All typical values have been characterized but are not tested.

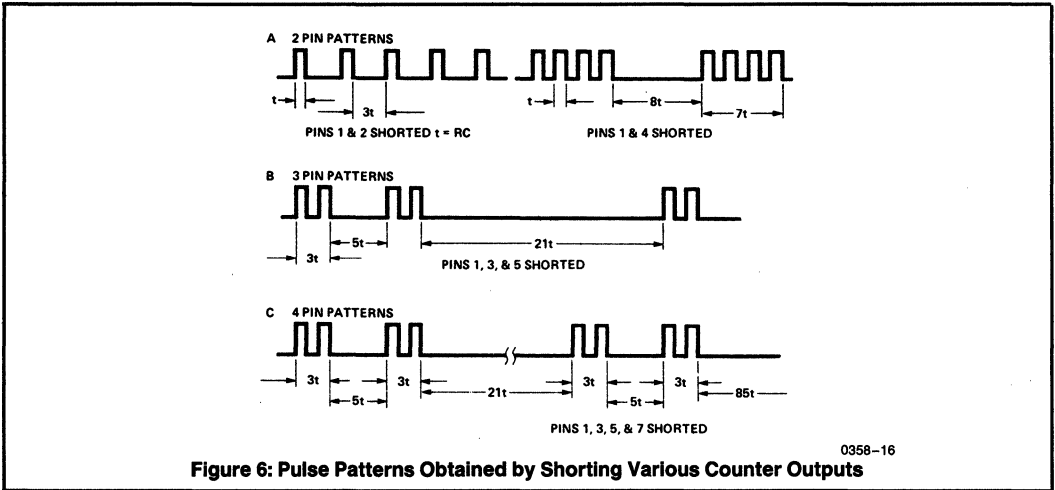


Figure 6: Pulse Patterns Obtained by Shorting Various Counter Outputs

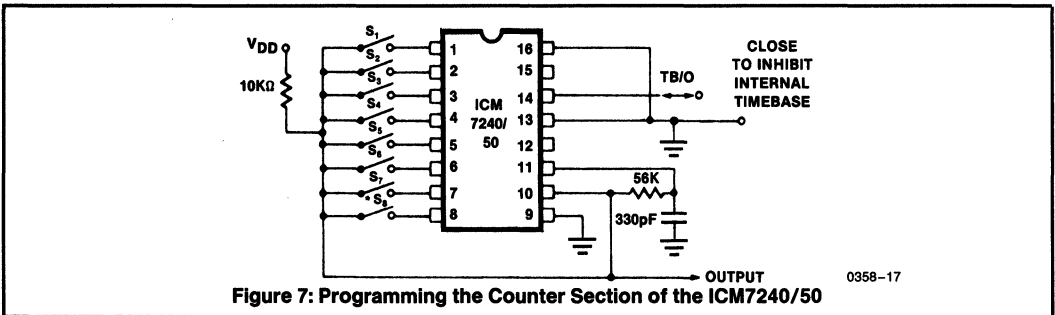


Figure 7: Programming the Counter Section of the ICM7240/50

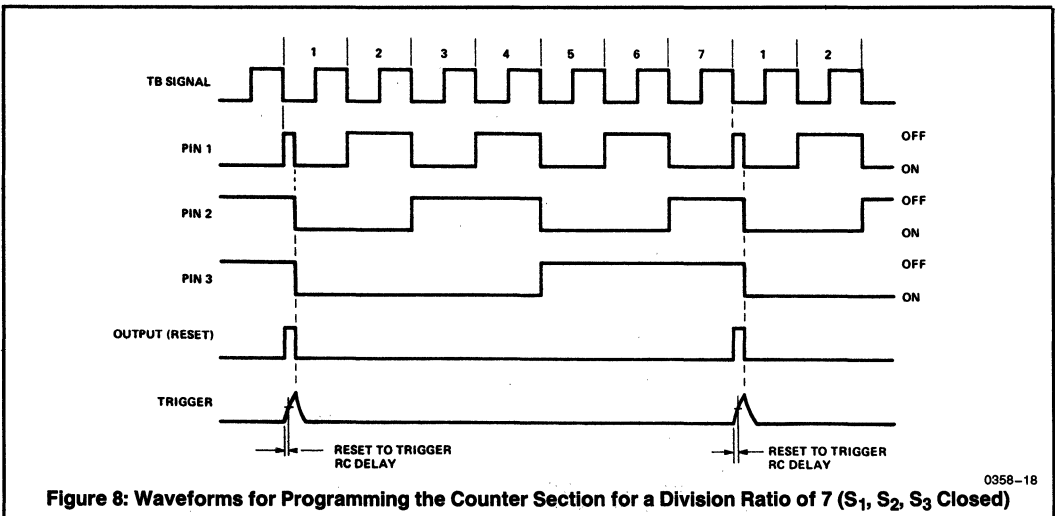


Figure 8: Waveforms for Programming the Counter Section for a Division Ratio of 7 (S_1, S_2, S_3 Closed)

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APPLICATIONS

GENERAL CONSIDERATIONS

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

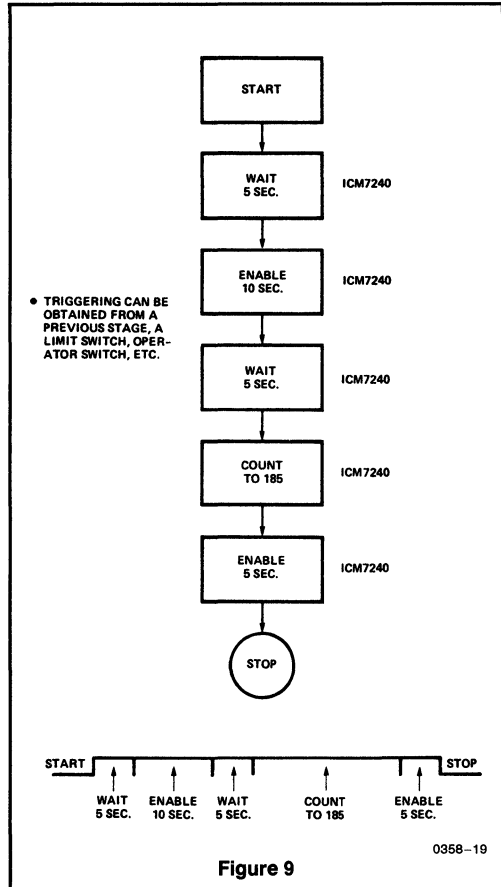
There is a limit of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under Typical Performance Characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform (rise/fall time $\leq 1\mu\text{s}$); this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM 7240/50.

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:



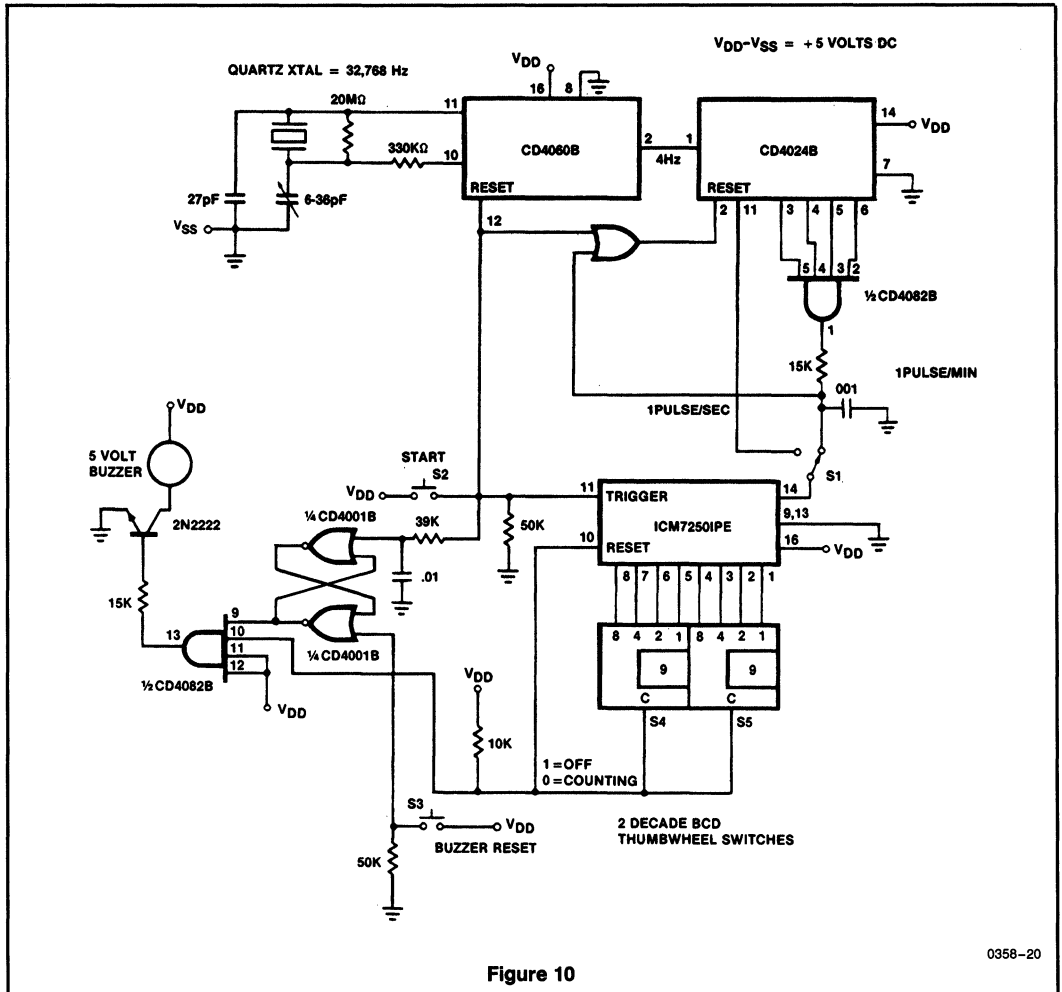


Figure 10

0358-20

CMOS PRECISION PROGRAMMABLE 0-99 SECONDS/MINUTES LABORATORY TIMER

The ICM7250 is well suited as a laboratory timer to alert personnel of the expiration of a preselected interval of time.

When connected as shown in Figure 10, the timer can accurately measure preselected time intervals of 0-99 seconds or 0-99 minutes. A 5 volt buzzer alerts the operator when the preselected time interval is over.

The circuit operates as follows:

The time base is first selected with S1 (seconds or minutes), then units 0-99 are selected on the two thumbwheel switches S4 and S5. Finally, switch S2 is depressed to start the timer. Simultaneously the quartz crystal controlled divider circuits are reset, the ICM7250 is triggered and counting begins. The ICM7250 counts until the pre-programmed value is reached, whereupon it is reset, pin 10 of the CD4082B is enabled and the buzzer is turned on. Pressing S3 turns the buzzer off.

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NOTE: All typical values have been characterized but are not tested.

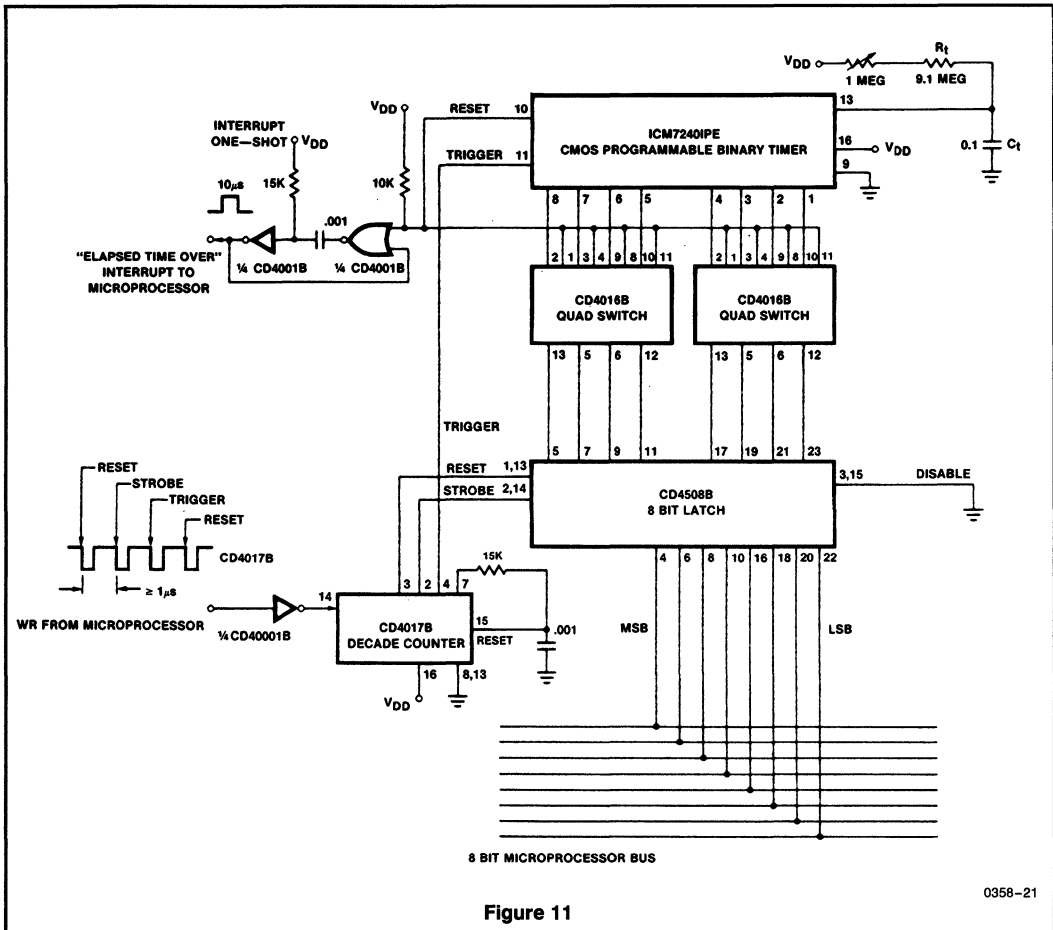


Figure 11

0358-21

LOW POWER MICROPROCESSOR PROGRAMMABLE INTERVAL TIMER

The ICM7240 CMOS programmable binary timer can be configured as a low cost microprocessor controlled interval timer with the addition of a few inexpensive CD4000 series devices.

With the devices connected as shown in Figure 11, the sequence of operation is as follows:

The microprocessor sends out an 8 bit binary code on its 8 bit I/O bus (the binary value needed to program the ICM7240), followed by four WRITE pulses into the CD4017B decade counter. The first pulse resets the 8 bit latch, the second strobes the binary value into the 8 bit

latch, the third triggers the ICM7240 to begin its timing cycle and the fourth resets the decade counter.

The ICM7240 then counts the interval of time determined by the R-C value on pin 13, and the programmed binary count on pins 1 through 8. At the end of the programmed time interval, the interrupt one-shot is triggered, informing the microprocessor that the programmed time interval is over.

With a resistor of approximately 10MΩ and capacitor of 0.1 μF, the time base of the ICM7240 is one second. Thus, a time of 1 – 255 seconds can be programmed by the microprocessor, and by varying R or C, longer or shorter time bases can be selected.

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NOTE: All typical values have been characterized but are not tested.

ICM7242

Long-Range Fixed Timer



GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7242IPA	-25°C to +85°C	8 pin MINI-DIP
ICM7242IJA	-25°C to +85°C	8 pin Cerdip
ICM7242CBA	0°C to +70°C	8 pin S.O.I.C.

FEATURES

- Replaces The 2242 in Most Applications
- Timing From Microseconds to Days
- Cascadeable
- Monostable or Astable Operation
- Wide Supply Voltage Range: 2 - 16 volts
- Low Supply Current: 115µA @ 5 volts

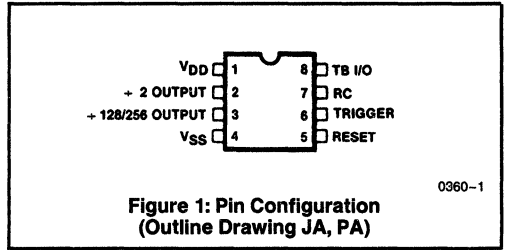


Figure 1: Pin Configuration (Outline Drawing JA, PA)

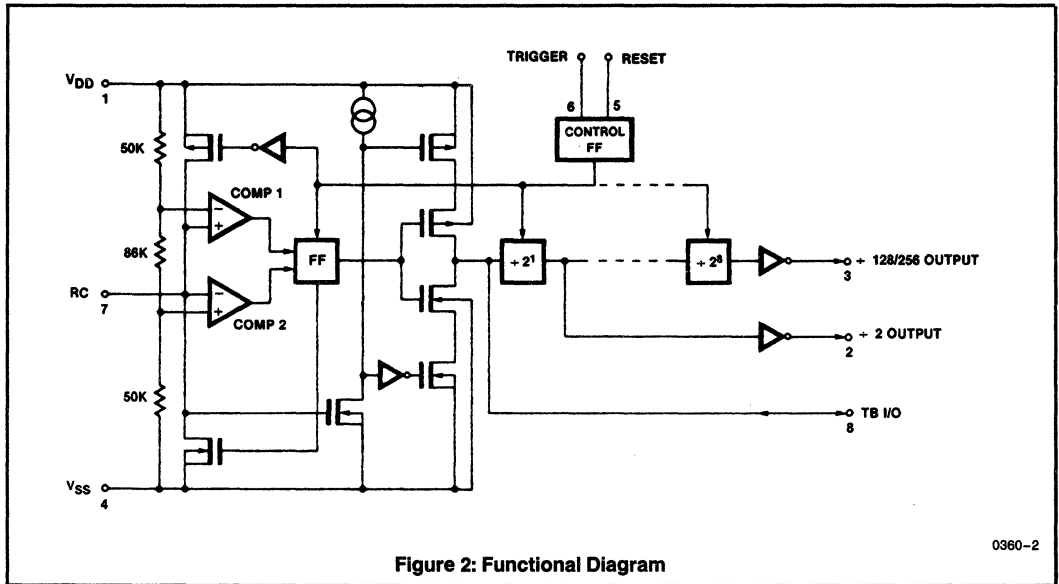


Figure 2: Functional Diagram

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS})	18V
Input Voltage [1]	
Terminals (Pins 5, 6, 7, 8)	($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
Maximum continuous output current (each output)	50mA
Power Dissipation [2]	200mW
Operating Temperature Range	
ICM7242I	-25°C to +85°C
ICM7242C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- NOTES:** 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. Derate at $-2mW/°C$ above 25°C.

ELECTRICAL CHARACTERISTICS

($V_{DD}=5V$, $T_A = +25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, $V_{SS}=0V$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Guaranteed Supply Voltage		2		16	V
I_{DD}	Supply Current	Reset Operating, $R = 10k\Omega$, $C = 0.1\mu F$ Operating, $R = 1M\Omega$, $C = 0.1\mu F$ TB Inhibited, RC Connected to V_{SS}		125 340 220 225	800 600	μA μA μA μA
	Timing Accuracy			5		%
$\Delta f/\Delta T$	RC Oscillator Frequency Temperature Drift	Independent of RC Components		250		ppm/°C
V_{OTB}	Time Base Output Voltage	$I_{SOURCE} = 100\mu A$ $I_{SINK} = 1.0mA$		3.5 0.40		V V
I_{TBLK}	Time Base Output Leakage Current	RC = Ground			25	μA
V_{TRIG}	Trigger Input Voltage	$V_{DD} = 5V$ $V_{DD} = 15V$		1.6 3.5	2.0 4.5	V V
V_{RST}	Reset Input Voltage	$V_{DD} = 5V$ $V_{DD} = 15V$		1.3 2.7	2.0 4.0	V V
I_{TRIG} , I_{RST}	Trigger/Reset Input Current			10		μA
f_t	Max Count Toggle Rate	$V_{DD} = 2V$ $V_{DD} = 5V$ $V_{DD} = 15V$ } Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and v_{SS}	2	1 6 13		MHz MHz MHz
V_{SAT}	Output Saturation Voltage	All Outputs except TB Output $V_{DD} = 5V$, $I_{OUT} = 3.2mA$		0.22	0.4	V
I_{SOURCE}	Output Sourcing Current 7242	$V_{DD} = 5V$ Terminals 2 & 3, $V_{OUT} = 1V$		300		μA
C_t	MIN Timing Capacitor (Note 1)		10			pF
R_t	Timing Resistor Range (Note 1)	$V_{DD} = 2-16V$	1K		22M	Ω

NOTE: 1. For Design only, not tested.

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NOTE: All typical values have been characterized but are not tested.

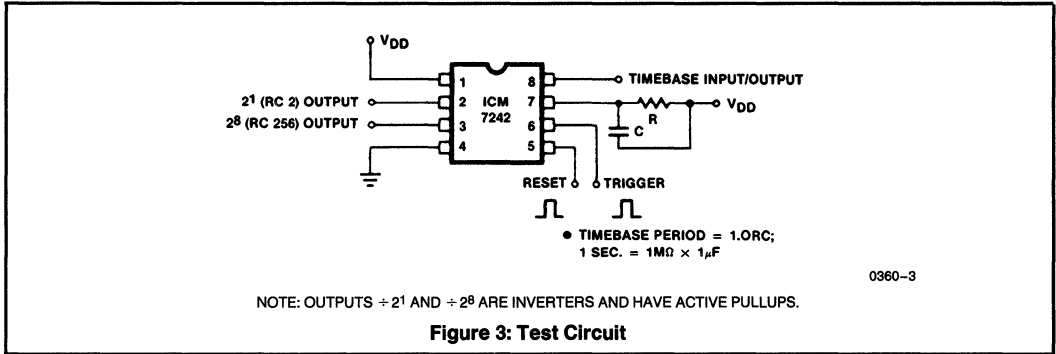
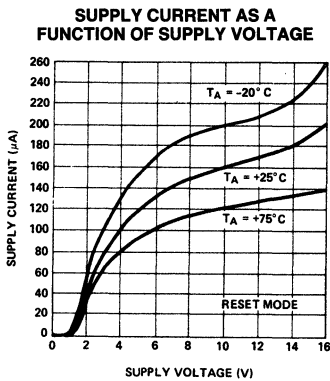


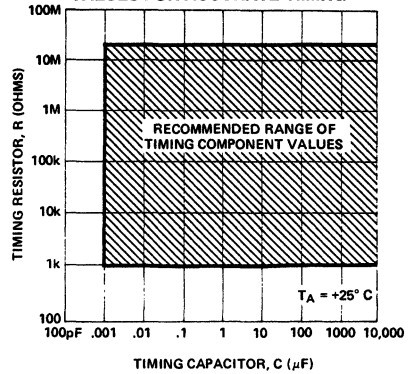
Figure 3: Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS



0360-4

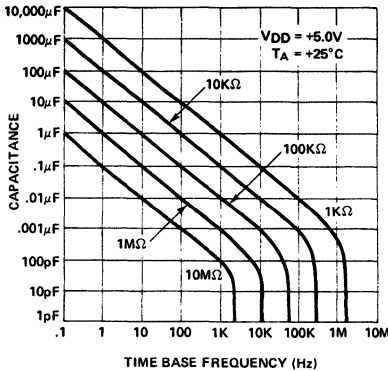
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



DIMENSIONS IN INCHES AND MILLIMETERS

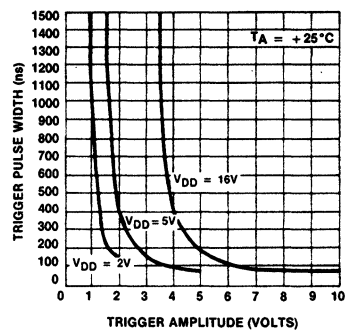
0360-5

TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



0360-6

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE



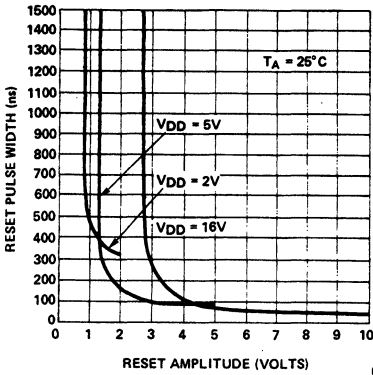
0360-7

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NOTE: All typical values have been characterized but are not tested.

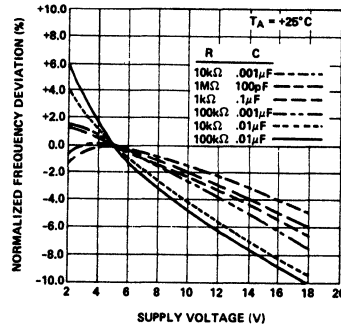
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



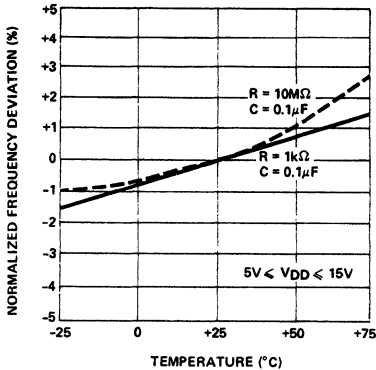
0360-8

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



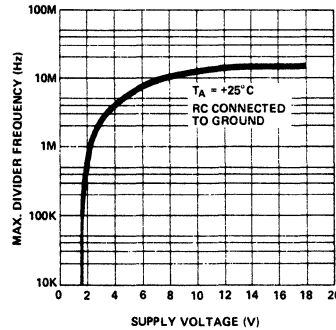
0360-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



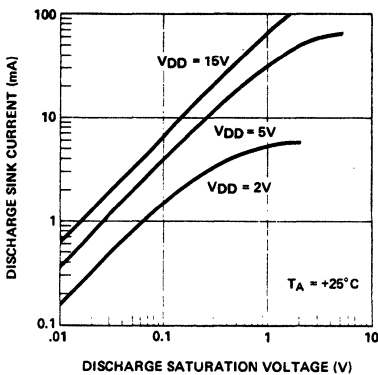
0360-10

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



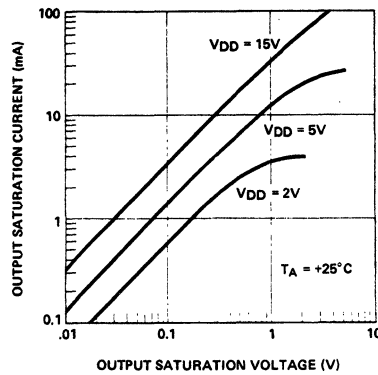
0360-11

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0360-12

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



0360-13

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NOTE: All typical values have been characterized but are not tested.

OPERATING CONSIDERATIONS

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200KHz.

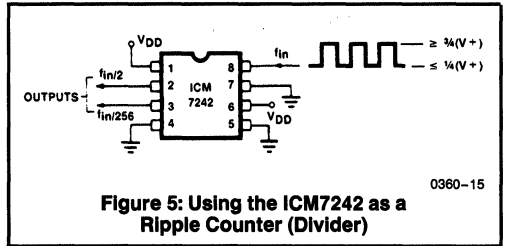
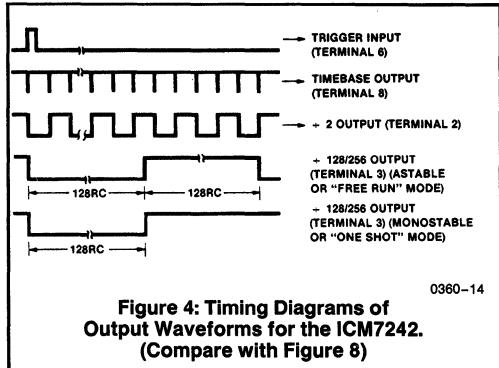
When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

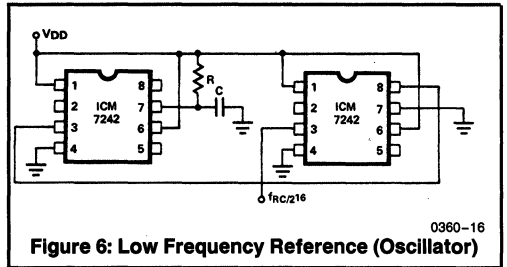
Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the ÷2⁸ output returns to the high state.

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.

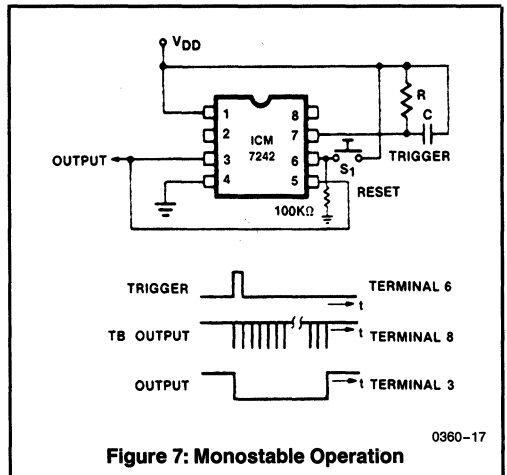


The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 6).



For monostable operation the ÷2⁸ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p-resistors have been used on the ICM7242 to provide the comparator timing points.



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NOTE: All typical values have been characterized but are not tested.

COMPARING THE ICM7242 WITH THE 2242

	ICM7242	2242
a. Operating Voltage	2 - 16V	4 - 15V
b. Operating Temp. Range	-25°C to +85°C	0°C to +70°C
c. Supply Current V _{DD} = 5V	0.7mA Max.	7mA Max.
d. Pullup Resistors		
TB Output	No	Yes
÷ 2 Output	No	Yes
÷ 256 Output	No	Yes
e. Toggle Rate	3.0MHz	0.5MHz
f. Resistor to Inhibit Oscillator	No	Yes
g. Resistor in Series with Reset for Monostable Operation	No	Yes
h. Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

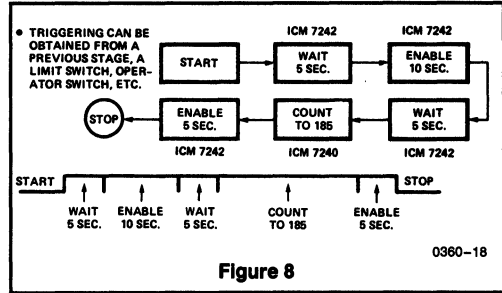


Figure 8

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

SEQUENCE TIMING

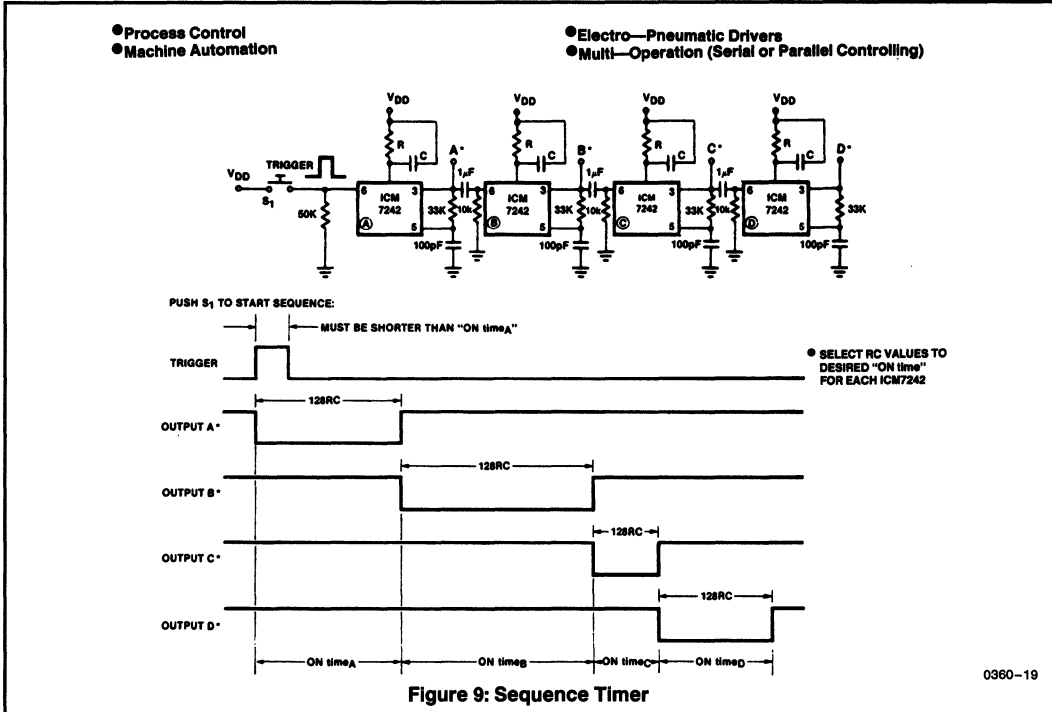


Figure 9: Sequence Timer

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NOTE: All typical values have been characterized but are not tested.

ICM7249

5 $\frac{1}{2}$ Digit LCD μ -Power Event/Hour Meter



GENERAL DESCRIPTION

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1 μ A during active timing or counting, due to Intersil's special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48-lead device, powered by a single DC voltage source and controlled by a 32.768kHz quartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard LCD segments. The chip is available in dice and in ceramic side-braced packages.

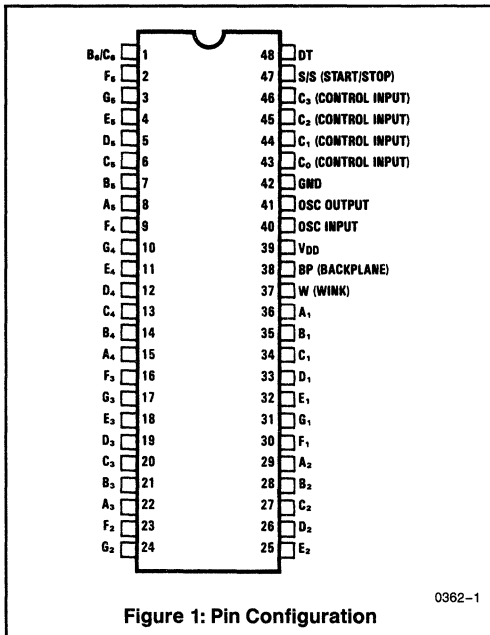


Figure 1: Pin Configuration

FEATURES

- Hour Meter Requires Only 4 Parts Total
- Micropower Operation: <1 μ A at 2.8V Typical
- 10 Year Operation On One Lithium Cell
- 2 $\frac{1}{2}$ Year Battery Life With Display Connected
- Directly drives 5 $\frac{1}{2}$ Digit LCD
- 14 Programmable Modes of Operation
- Times Hrs., 0.1 Hrs., .01 Hrs., .1 Mins.
- Counts 1's, 10's, 100's, 1000's
- Dual Function Input Circuit:
 - Selectable Debounce for Counter
 - High-Pass Filter for Timer
- Direct AC Line Triggering With Input Resistor
- Winking "Timer Active" Display Output
- Display Test Feature

APPLICATIONS

- AC or DC Hour Meters
- AC or DC Totalizers
- Portable Battery Powered Equipment
- Long Range Service Meters

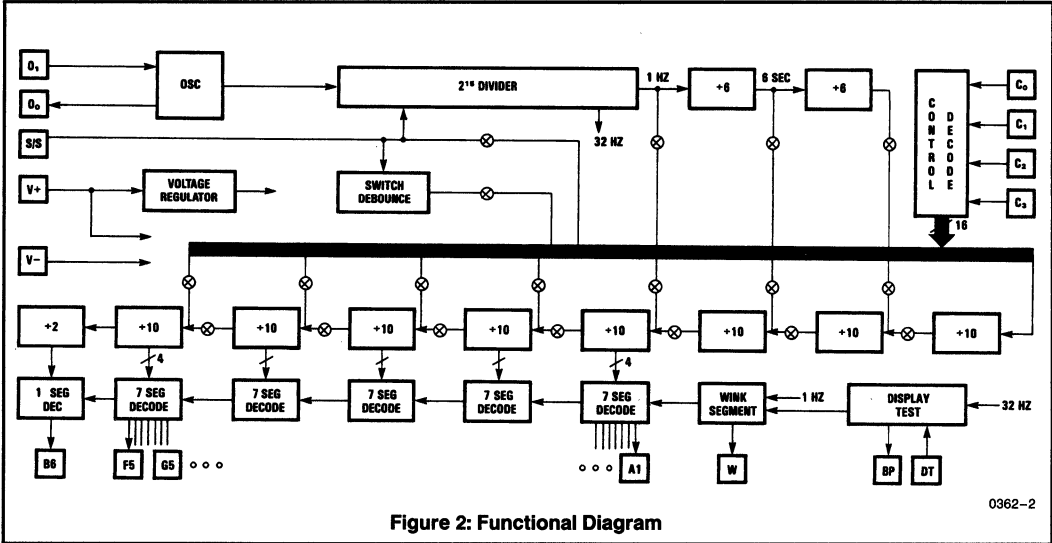
ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7249IDM	-40°C to +85°C	48-Pin Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V
Input Voltage	
Pins 43-48 (Note 1)	(V _{SS} - 0.3V) to (V _{DD} + 0.3V)
Power Dissipation (Note 2)	200mW
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS Temperature = -40°C to $+85^{\circ}\text{C}$, $V_{\text{DD}} = 2.5\text{V}$ to 5.5V , $V_{\text{SS}} = 0\text{V}$, unless otherwise noted. Typical specifications measured at temperature = 25°C and $V_{\text{DD}} = 2.8\text{V}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{DD}	Operating Voltage	Note 3	2.5		5.5	V
I_{DD}	Operating Current	Note 4, All inputs = V_{DD} or GND $V_{\text{DD}} = 2.8\text{V}$ $V_{\text{DD}} = 5.5\text{V}$		1.0 4.0	10.0 20.0	μA μA
I_{IN} I_{SS} I_{DT}	Input Current: C_0-C_3 , S/S DT	All Inputs V_{DD} or GND $V_{\text{DD}} = 2.8\text{V}$ Note 5	0.0 0.5 40.0	1.5	1 3.0 110	μA μA μA
V_{IL} V_{IH}	Input Voltage: C_0-C_3 , DT, S/S		0.7 V_{DD}		0.3 V_{DD}	V V
V_{OL} V_{OH}	Segment Output Voltage	$I_{\text{OL}} = 1\mu\text{A}$ $I_{\text{OH}} = 1\mu\text{A}$	$V_{\text{DD}} - 0.8$		0.8	V
V_{OL} V_{OH}	Backplane Output Voltage	$I_{\text{OL}} = 10\mu\text{A}$ $I_{\text{OH}} = 10\mu\text{A}$	$V_{\text{DD}} - 0.8$		0.8	V
—	Oscillator Stability: Temp. = 25°C , $V_{\text{DD}} = 2.5\text{V}$ to 5.5V Temp. = -40°C to $+85^{\circ}\text{C}$, $V_{\text{DD}} = 2.5\text{V}$ to 5.5V			0.1 5		ppm ppm
T_{HP} T_{DE} T_{DE}	S/S Pulse Width: High-pass Filter (Modes 0-3) Debounce (Modes 4, 6, 8, 10) w/o Debounce (Modes 5, 7, 9, 11)		5 10,000 5		10,000	μs μs μs

NOTES: 1. Due to the SCR structure inherent in junction-isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs or outputs before power is applied. If only inputs are affected, latchup also can be prevented by limiting the current into the input terminal to less than 1mA.

2. This limit refers to that of the package and will not occur during normal operation.

3. Internal reset to 00000 requires a maximum V_{DD} rise time of $1\mu\text{s}$. Longer rise times at power-up may cause improper reset.

4. Operating current is measured with the LCD disconnected, and input current I_{SS} and I_{DT} supplied externally.

5. Inputs C_0-C_3 are latched internally and draw no DC current after switching. During switching, a $90\mu\text{A}$ peak current may be drawn for 10 nanoseconds.

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NOTE: All typical values have been characterized but are not tested.

Table 1. Pin Assignment and Function

Pin	Name	Description
1	B ₆ /C ₆	Half-digit LCD segment output.
2	F ₅	Seven-segment LCD outputs.
3	G ₅	
4	E ₅	
5	D ₅	
6	C ₅	
7	B ₅	
8	A ₅	
9	F ₄	
10	G ₄	
11	E ₄	
12	D ₄	
13	C ₄	
14	B ₄	
15	A ₄	
16	F ₃	
17	G ₃	
18	E ₃	
19	D ₃	
20	C ₃	
21	B ₃	
22	A ₃	
23	F ₂	
24	G ₂	
25	E ₂	
26	D ₂	
27	C ₂	
28	B ₂	
29	A ₂	
30	F ₁	
31	G ₁	
32	E ₁	
33	D ₁	
34	C ₁	
35	B ₁	
36	A ₁	

Table 1. Pin Assignment and Function (Continued)

Pin	Name	Description
37	W	Wink-segment output.
38	BP	Backplane for LCD reference.
39	V+	Positive supply voltage.
40	OSC _I	Quartz Crystal connections
41	OSC _O	
42	GND	Chip GRouND.
43	C ₀	Mode-select control inputs.
44	C ₁	
45	C ₂	
46	C ₃	
47	S/S	Start / Stop
48	DT	Display Test

Table 2. Mode Select Table

Mode	Control Pin Inputs				Function
	C ₃	C ₂	C ₁	C ₀	
0	0	0	0	0	1 hour interval timer
1	0	0	0	1	0.1 hour interval timer
2	0	0	1	0	0.01 hour interval timer
3	0	0	1	1	0.1 minute interval timer
4	0	1	0	0	1's counter with debounce
5	0	1	0	1	1's counter
6	0	1	1	0	10's counter with debounce
7	0	1	1	1	10's counter
8	1	0	0	0	100's counter with debounce
9	1	0	0	1	100's counter
10	1	0	1	0	1000's counter with debounce
11	1	0	1	1	1000's counter
12	1	1	0	0	Test display digits
13	1	1	0	1	Internal test
14	1	1	1	0	Internal test
15	1	1	1	1	Reset

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

After power is applied, the ICM7249 requires a rise time of t_{R} to become active and for oscillation to begin, as seen in Figure 3. Initially the backplane output BP is a logic '1' level, but then changes after every 512 crystal oscillation cycles, giving BP a square-wave frequency of 32Hz. Segments are turned off when the voltage levels of the segment drive pins are the same as and in phase with BP. Segments are turned on by having the drive pin voltages out of phase with BP.

The 16 modes are selected by placing the binary equivalent of the mode number on inputs C_0-C_3 (Table 2). In the four timer modes, timing is controlled by the Start/Stop input S/S. Because of internal high-pass filtering, timing is active when either S/S is held high for more than 25ms, or the input signal has a frequency of at least 50Hz and less than 120kHz as shown in Figure 4. Driving S/S with an input

frequency between 40Hz and 50Hz has an indeterminate effect on the timing.

The timing intervals are different for each mode. For example, in Mode 0 the display is incremented every hour, while in Mode 3 the display is incremented every tenth of a minute.

While timing is active, the wink-segment output W will flash, as seen in Figure 1. On the upward transition of S/S, the wink output turns off. It remains off for 16 backplane cycles and turns back on for another 16 cycles. If timing is still active, the wink segment repeats this process, giving it a flash rate of 1Hz; otherwise the wink output remains on until timing begins again. In counting modes 4-11, the count is registered and latched on each positive transition of S/S.

The display is keyed to the specific counting mode. In the 1's counter mode, the display is incremented for each count; in the 10's counter mode, the display is incremented after every tenth count.

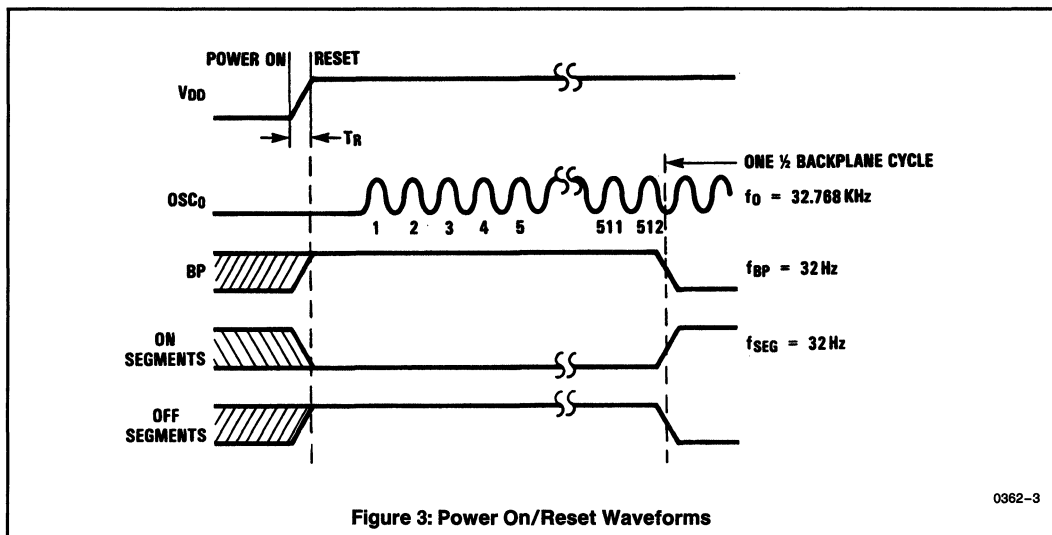
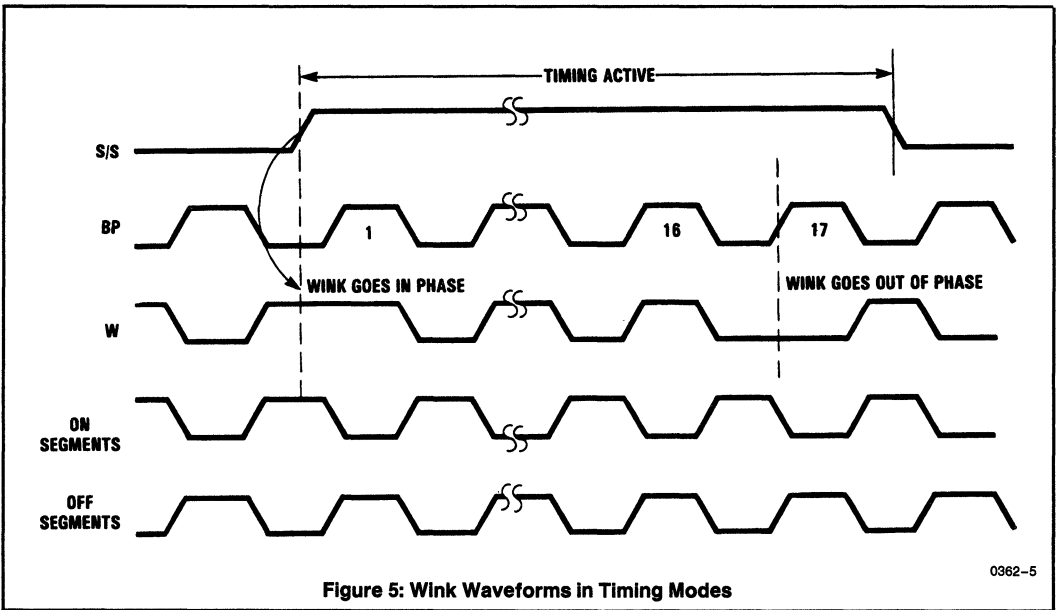
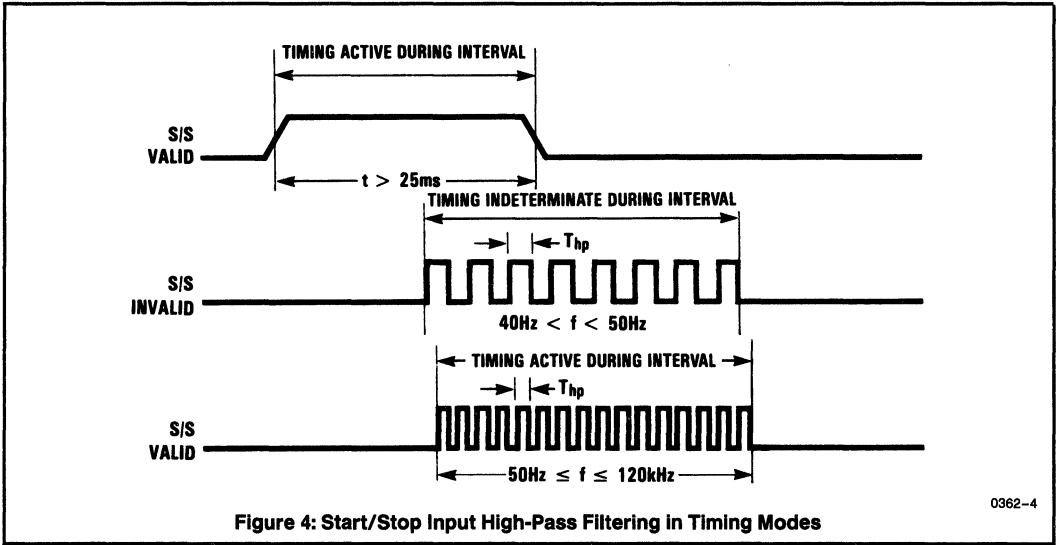


Figure 3: Power On/Reset Waveforms

0362-3

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

During counting, the display will wink off at each count input regardless of whether the display is incremented. When a count occurs, the wink segment output turns off at the end of the 16th BP cycle and turns back on at the end of the 32nd BP cycle, creating a half-second wink, as shown in Figure 6. If counting occurs more frequently than once a second, the wink output will default to a constant 1Hz flash rate.

In counter modes 4, 6, 8 and 10, the count pulse is subject to debounce filtering. Figure 7 shows that only pulses with a frequency of less than 40Hz are valid. Pulses with a frequency between 50Hz and 120kHz are ignored, while those with a frequency between 40Hz and 50Hz have an indeterminate effect on the count.

The display may be tested at any time without disturbing operation by pulsing DT high, as seen in Figure 8. On the next positive transition of BP, all the segments turn on and remain on until the end of the 16th BP cycle. This takes a half-second or less. All the segments then turn off for an additional 48 BP cycles (the end of the 64th cycle), after which valid data returns to the display. As long as DT is held high, the segments will remain on.

Additional display testing is provided by using mode 12. In this mode each displayed decade is incremented on each positive transition of S/S. Modes 13 and 14 are for manufacturer testing only.

Mode 15 resets all the decades and internal counters to zero, essentially bringing everything back to power-up status.

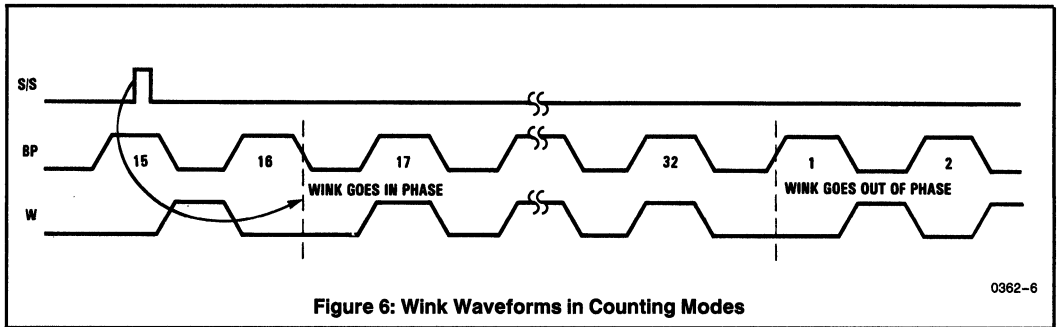


Figure 6: Wink Waveforms in Counting Modes

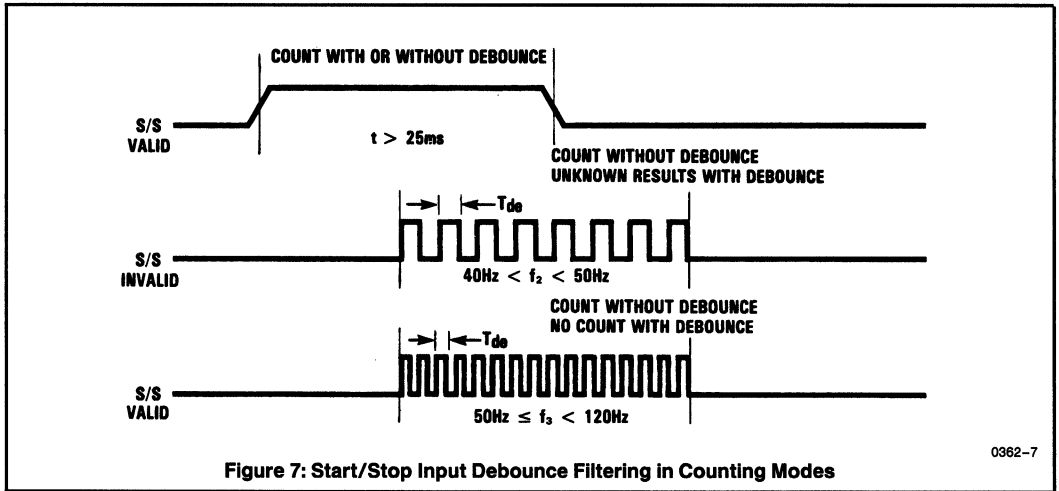


Figure 7: Start/Stop Input Debounce Filtering in Counting Modes

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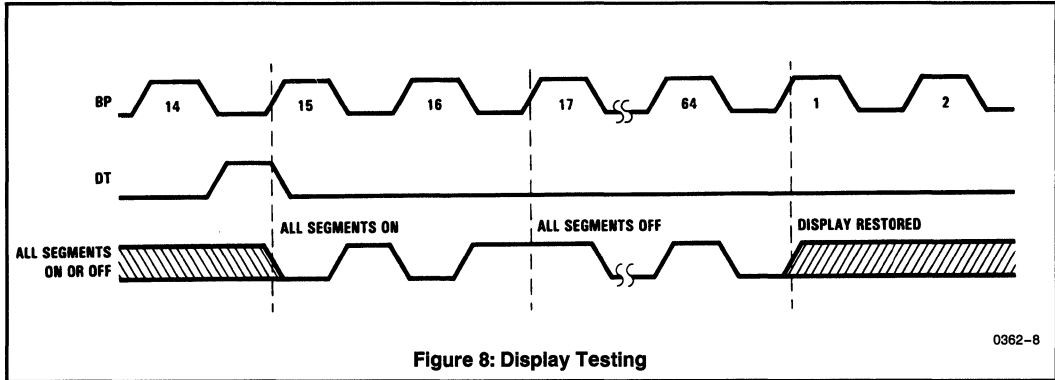


Figure 8: Display Testing

APPLICATION NOTES

A typical use of the ICM7249 is seen in Figure 9, the Motor Hour Meter. In this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The 20MΩ resistor and high-pass filtering allow AC line activation of the S/S input. This configuration, which is powered by a 3V lithium cell, will operate continuously for 2½ years. Without the display, which only needs to be connected when a reading is required, the span of operation is extended to 10 years.

When the ICM7249 is configured as an attendance counter, as shown in Figure 10, the display shows each increment. By using mode 2, external debouncing of the gate switch is unnecessary, provided the switch bounce is less than 35ms.

The 3V lithium battery can be replaced without disturbing operation if a suitable capacitor is connected in parallel with it. The display should be disconnected, if possible, during the procedure to minimize current drain. The capacitor should be large enough to store charge for the amount of time needed to physically replace the battery ($\Delta t = \Delta VC/I$). A 100μF capacitor initially charged to 3V will supply a current of 1.0μA for 50 seconds before its voltage drops to 2.5V, which is the minimum operating voltage for the ICM7249.

Before the battery is removed, the capacitor should be placed in parallel, across the V_{DD} and GND terminals. After the battery is replaced, the capacitor can be removed and the display reconnected.

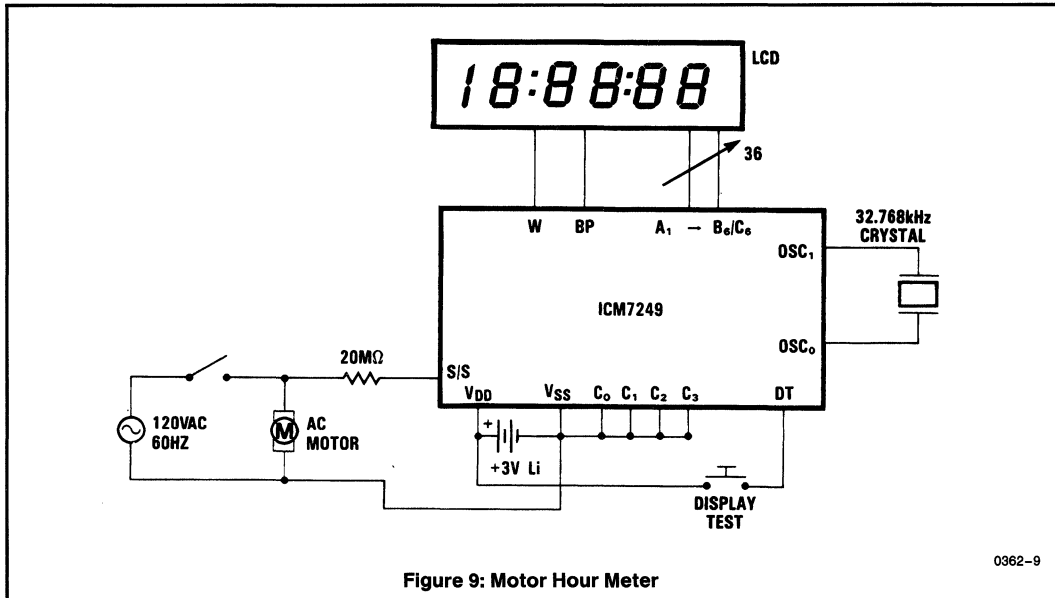
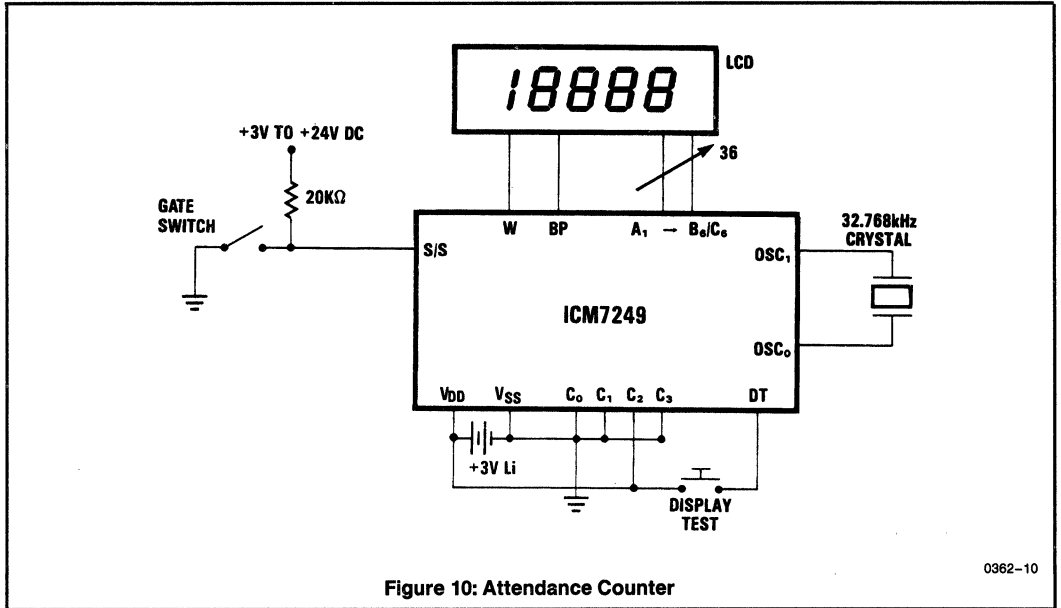


Figure 9: Motor Hour Meter

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NOTE: All typical values have been characterized but are not tested.



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NOTE: All typical values have been characterized but are not tested.

ICM7555/ICM7556

General Purpose Timer



ICM7555/ICM7556

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbaring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V⁺ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7555CBA	0°C to +70°C	8 Lead SOIC
ICM7555IPA	-25°C to +85°C	8 Lead MiniDip
ICM7555ITV	-25°C to +85°C	TO-99 Can
ICM7555MTV*	-55°C to +125°C	TO-99 Can
ICM7556IPD	-25°C to +85°C	14 Lead Plastic DIP
ICM7556MJD*	-55°C to +125°C	14 Lead Cerdip

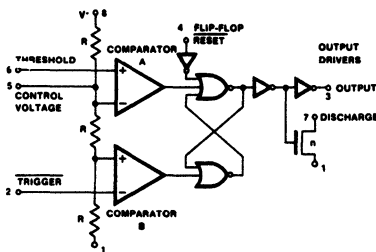
*Add /883B to part number if 883B processing is desired.

FEATURES

- Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556
- Low Supply Current — 60µA Typ. (ICM7555) 120µA Typ. (ICM7556)
- Extremely Low Trigger, Threshold and Reset Currents — 20pA Typical
- High Speed Operation — 1MHz Typical
- Wide Operation Supply Voltage Range Guaranteed 2 to 18 Volts
- Normal Reset Function — No Crowbaring of Supply During Output Transition
- Can Be Used With Higher Impedance Timing Elements Than Regular 555/6 for Longer RC Time Constants
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Output Source/Sink Driver Can Drive TTL/CMOS
- Typical Temperature Stability of 0.005% Per °C at 25°C
- Outputs Have Very Low Offsets, HI and LO

APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector



0363-1

This Functional Diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ±20% typ.

Figure 1: Functional Diagram

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NOTE: All typical values have been characterized but are not tested.

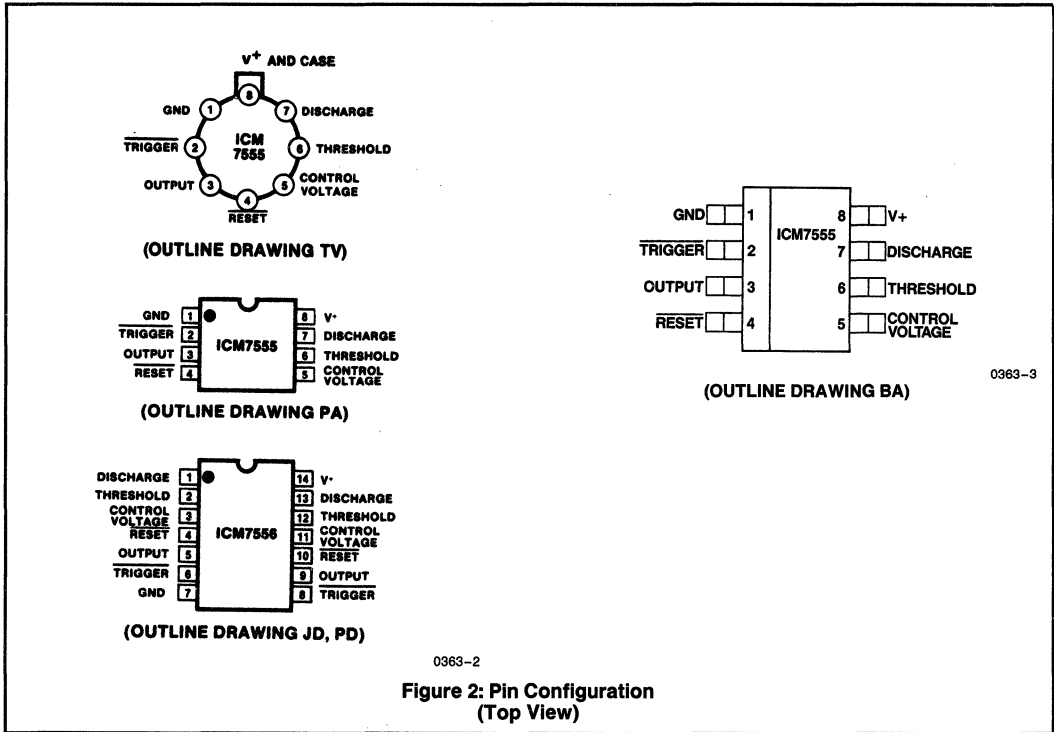
ICM7555/ICM7556



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+ 18 Volts
Input Voltage: Trigger, Reset	
Control Voltage, Threshold,	V+ + 0.3V to V- - 0.3V
Output Current	100mA
Power Dissipation ^[2] ICM7556	300mW
ICM7555	200mW
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Operating Temperature Range ^[2]	
ICM7555XC	0°C to +70°C
ICM7555XI	-25°C to +85°C
ICM7555XM	-55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0363-3

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NOTE: All typical values have been characterized but are not tested.

ICM7555 ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	ICM7555C,I,M			ICM7555M			Units
			T _A = 25°C			-55°C ≤ T _A ≤ +125°C			
			Min	Typ	Max	Min	Typ	Max	
I ⁺	Static Supply Current	V _{DD} = 5V		40	200			300	μA
		V _{DD} = 15V		60	300			300	μA
	Monostable Timing Accuracy	RA = 10k, C = 0.1μF, V _{DD} = 5V		2		858		1161	% μs
	Drift with Temp*	V _{DD} = 5V		150			150		ppm/°C
		V _{DD} = 10V		200			200		ppm/°C
		V _{DD} = 15V		250			250		ppm/°C
	Drift with Supply*	V _{DD} = 5 to 15V		0.5			0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1μF, V _{DD} = 5V		2		1717		2323	% μs
			Drift with Temp*	V _{DD} = 5V		150			150
	V _{DD} = 10V			200			200		ppm/°C
	V _{DD} = 15V			250			250		ppm/°C
	Drift with Supply*	V _{DD} = 5V to 15V		0.5			0.5		%/V
V _{TH}	Threshold Voltage	V _{DD} = 15V	62	67	71	61		72	% V _{DD}
V _{TRIG}	Trigger Voltage	V _{DD} = 15V	28	32	36	27		37	% V _{DD}
I _{TRIG}	Trigger Current	V _{DD} = 15V			10			50	nA
I _{TH}	Threshold Current	V _{DD} = 15V			10			50	nA
V _{CV}	Control Voltage	V _{DD} = 15V	62	67	71	61		72	% V _{DD}
V _{RST}	Reset Voltage	V _{DD} = 2 to 15V	0.4		1.0	0.2		1.2	V
I _{RST}	Reset Current	V _{DD} = 15V			10			50	nA
I _{DIS}	Discharge Leakage	V _{DD} = 15V			10			50	nA
V _{OL}	Output Voltage Drop	V _{DD} = 15V, I _{sink} = 20mA		0.4	1.0			1.25	V
		V _{DD} = 5V, I _{sink} = 3.2mA		0.2	0.4			0.5	V
V _{OH}	Output Voltage Drop	V _{DD} = 15V, I _{source} = 0.8mA	14.3	14.6		14.2			V
		V _{DD} = 5V, I _{source} = 0.8mA	4.0	4.3		3.8			V
V _{DIS}	Discharge Output Voltage Drop	V _{DD} = 5V, I _{SINK} = 15mA		0.2	0.4			0.6	V
		V _{DD} = 15V, I _{sink} = 15mA						0.4	V
V ⁺	Supply Voltage*	Functional Oper.	2.0		18.0	2.0		18.0	V
t _R	Output Rise Time*	RL = 10M, CL = 10pF, V _{DD} = 5V		75			75		ns
t _F	Output Fall Time*	RL = 10M, CL = 10pF, V _{DD} = 5V		75			75		ns
f _{MAX}	Oscillator Frequency*	V _{DD} = 5V, RA = 470Ω, RB = 270Ω, C = 200pF		1			1		MHz

*These parameters are based upon characterization data and are not tested.

ICM7555/ICM7556



ICM7556

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Test Conditions	ICM7556I,M			ICM7556M			Units
			$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			
			Min	Typ	Max	Min	Typ	Max	
I ⁺	Static Supply Current	V _{DD} = 5V V _{DD} = 15V		80	400			600	μA μA
				120	600			600	
	Monostable Timing Accuracy	RA = 10k, C = 0.1 μF , V _{DD} = 5V		2		858		1161	% μs
	Drift with Temp*	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		150			150		ppm/ $^\circ\text{C}$
			200			200		ppm/ $^\circ\text{C}$	
			250			250		ppm/ $^\circ\text{C}$	
	Drift with Supply*	V _{DD} = 5V to 15V		0.5			0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1 μF , V _{DD} = 5V		2		1717		2323	% μs
	Drift with Temp*	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		150			150		ppm/ $^\circ\text{C}$
			200			200		ppm/ $^\circ\text{C}$	
			250			250		ppm/ $^\circ\text{C}$	
	Drift with Supply*	V _{DD} = 5V to 15V		0.5			0.5		% V
V _{TH}	Threshold Voltage	V _{DD} = 15V	62	67	71	61		72	% V _{DD}
V _{TRIG}	Trigger Voltage	V _{DD} = 15V	28	32	36	27		37	% V _{DD}
I _{TRIG}	Trigger Current	V _{DD} = 15V			10			50	nA
I _{TH}	Threshold Current	V _{DD} = 15V			10			50	nA
V _{CV}	Control Voltage	V _{DD} = 15V	62	67	71	61		72	% V _{DD}
V _{RST}	Reset Voltage	V _{DD} = 2V to 15V	0.4		1.0	0.2		1.2	V
I _{RST}	Reset Current	V _{DD} = 15V			10			50	nA
I _{DIS}	Discharge Leakage	V _{DD} = 15V			10			50	nA
V _{OL}	Output Voltage Drop	V _{DD} = 15V, I _{sink} = 20mA V _{DD} = 5V, I _{sink} = 3.2mA		0.4	1.0			1.25	V
				0.2	0.4			0.5	V
V _{OH}	Output Voltage Drop	V _{DD} = 15V, I _{source} = 0.8mA V _{DD} = 5V, I _{source} = 0.8mA	14.3	14.6		14.2			V
			4.0	4.3		3.8			V
V _{DIS}	Discharge Output Voltage Drop	V _{DD} = 5V, I _{sink} = 15mA V _{DD} = 5V, I _{sink} = 15mA		0.2	0.4			0.6	V
								0.4	V
V ⁺	Supply Voltage*	Functional Oper.	2.0		18.0	2.0		18.0	V
t _R	Output Rise Time*	RL = 10M, CL = 10pF, V _{DD} = 5V		75			75		ns
t _F	Output Fall Time*	RL = 10M, CL = 10pF, V _{DD} = 5V		75			75		ns
f _{MAX}	Oscillator Frequency*	V _{DD} = 5V, RA = 470 Ω , RB = 270 Ω , C = 200pF		1			1		MHz

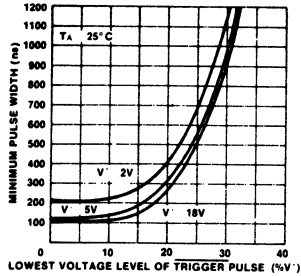
*These parameters are based upon characterization data and are not tested.

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NOTE: All typical values have been characterized but are not tested.

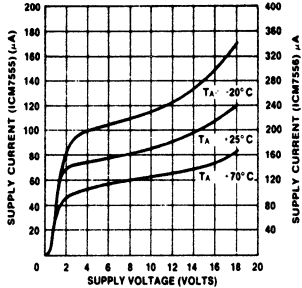
TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



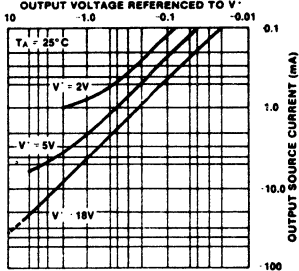
0363-4

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



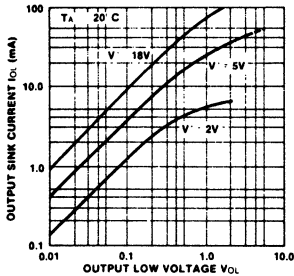
0363-5

OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



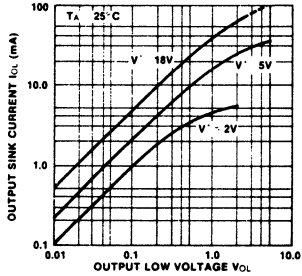
0363-6

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



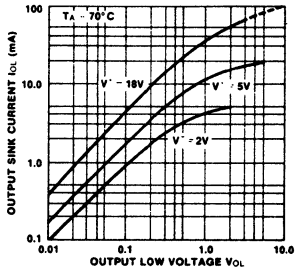
0363-7

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



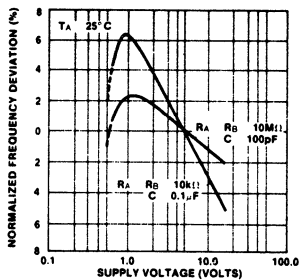
0363-8

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



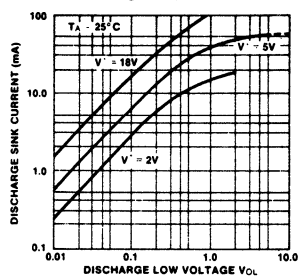
0363-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



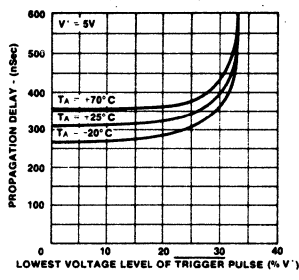
0363-10

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0363-11

PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



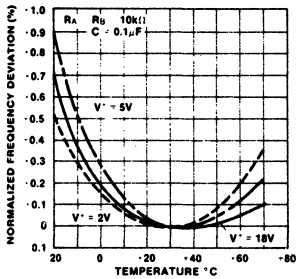
0363-12

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NOTE: All typical values have been characterized but are not tested.

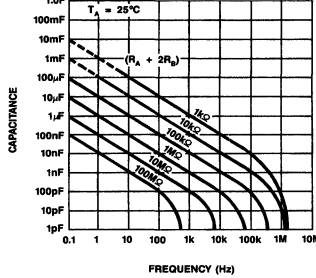
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



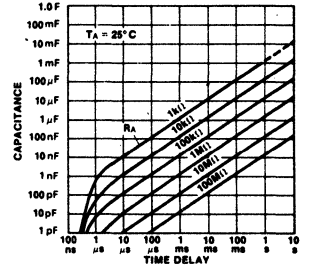
0363-13

FREE RUNNING FREQUENCY AS A FUNCTION OF RA, RB and C



0363-14

TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C

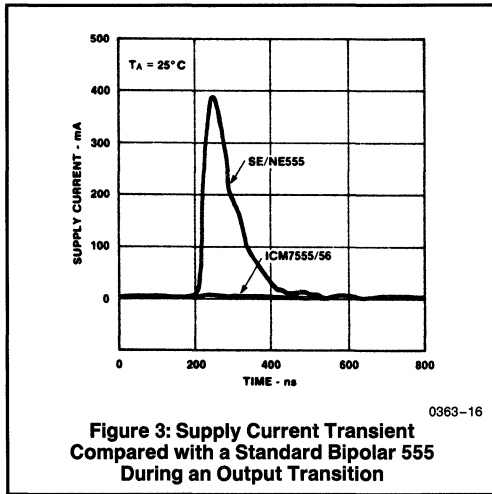


0363-15

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 3.



0363-16

Figure 3: Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4 and 5.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4 RC}$$

The timer can also be connected as shown in Figure 4b. In this circuit, the frequency is:

$$f = 1.44 / ((R_A + 2R_B)C)$$

The duty cycle is controlled by the values of RA and RB, by the equation:

$$D = (R_A + R_B) / (R_A + 2R_B)$$

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative TRIGGER pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_A C$. When the voltage across the capacitor equals $2/3 V+$, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. TRIGGER must return to a high state before the OUTPUT can return to a low state.

$$t_{output} = -\ln(1/3) R_A C = 1.1 R_A C$$

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NOTE: All typical values have been characterized but are not tested.

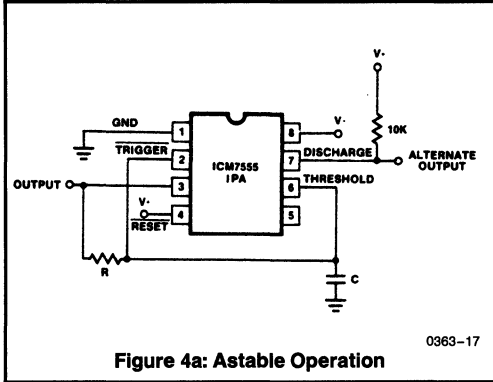


Figure 4a: Astable Operation

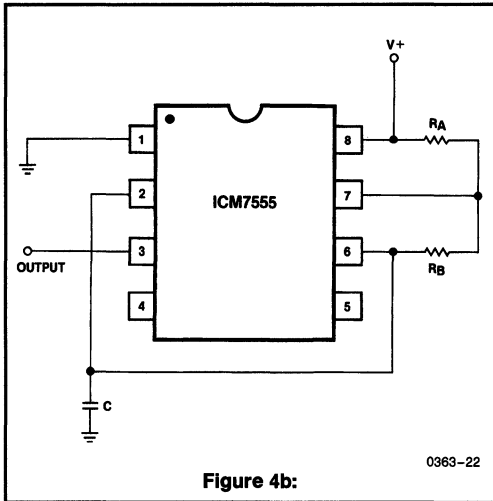


Figure 4b:

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the RESET function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

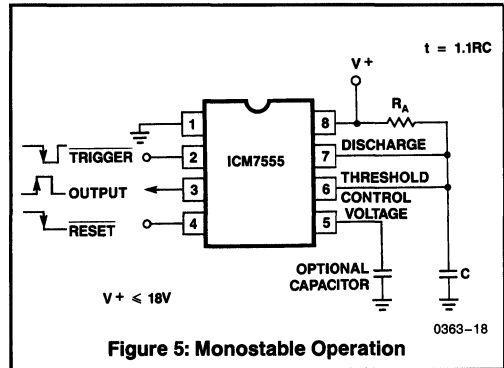


Figure 5: Monostable Operation

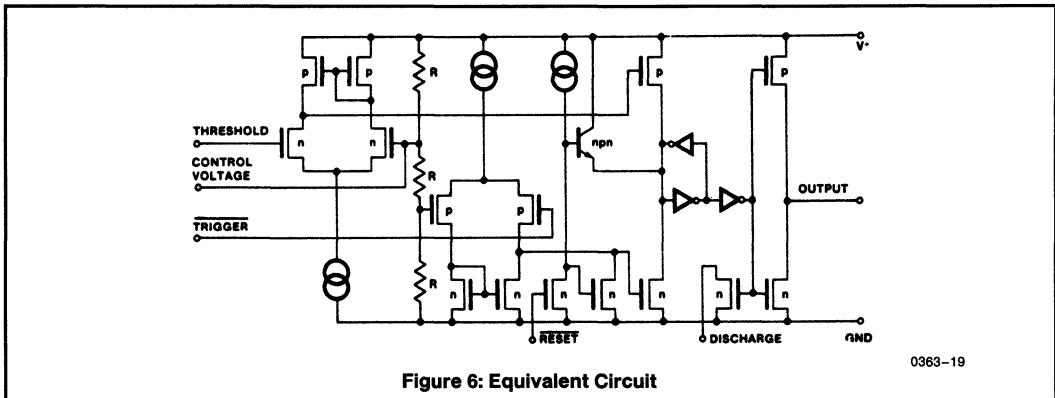


Figure 6: Equivalent Circuit

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NOTE: All typical values have been characterized but are not tested.

TRUTH TABLE

Threshold Voltage	Trigger Voltage	RESET	Output	Discharge Switch
DON'T CARE	DON'T CARE	LOW	LOW	ON
$> \frac{2}{3}(V^+)$	$> \frac{1}{3}(V^+)$	HIGH	LOW	ON
$< \frac{2}{3}(V^+)$	$> \frac{1}{3}(V^+)$	HIGH	STABLE	STABLE
DON'T CARE	$< \frac{1}{3}(V^+)$	HIGH	HIGH	OFF

NOTE: RESET will dominate all other inputs: TRIGGER will dominate over THRESHOLD.

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NOTE: All typical values have been characterized but are not tested.

Section 15 — High Reliability



HIGH-RELIABILITY/MILITARY PRODUCTS

100% INTEGRATED CIRCUIT PROCESSING

Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

HI-REL PROCESS OFFERINGS 38510 PRODUCTS

Intersil holds QPL1 status on a number of JAN MIL-M-38510 products. As required by JAN specifications, these products are fabricated, assembled, and 100% processed within the United States and are fully compliant with all the requirements, procedures, and methods as given in MIL-M-38510 and MIL-STD-883.

MILITARY DRAWING PRODUCTS

Intersil offers a large and growing number of Military Drawing Products (previously referred to as Desc Drawings). These are processed in full compliance with MIL-STD-883 Rev C and carry electrical specifications standardized and controlled by Desc.

883 CLASS B PRODUCTS

The 883 Class B flow diagram represents product processed in accordance with Method 5004 and Method 5005 of MIL-STD-883 Rev. C, Class B. Many products herein are available as compliant to paragraph 1.2 of MIL-STD-883 Rev. C while others are available only as non-compliant at this time. Check with Intersil Customer Service as to the compliant status of individual product offerings at any point in time.

HR PRODUCTS

The HR flow diagram, newly offered by Intersil, represents high reliability hermetic product utilizing many, but not necessarily all, of the test methods and requirements of MIL-STD-883 Rev. C, to be used in high reliability applications where some deviations from Rev. C may be justified and economic advantages realized. Such product may not be branded /883B but may be branded /HR or a special brand as required by purchase order.

BR PRODUCTS

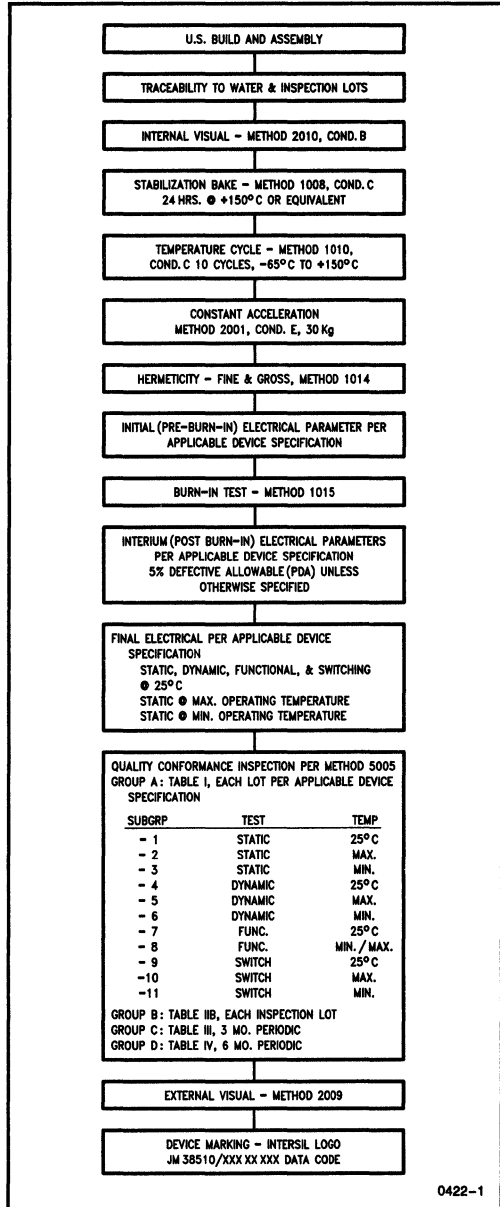
The BR flow diagram, newly offered by Intersil, represents hermetic or plastic encapsulated product intended for application in the computer, industrial, or hi-rel commercial marketplace. In addition to 100% burn-in, many other reliability processing steps are included to enhance quality levels on shipped parts and to improve long term reliability characteristics. Such product may be branded /BR or as required by purchase order.

Contact Product Marketing for availability and pricing on 883B, HR and BR products.

100% DISCRETE DEVICE PROCESSING

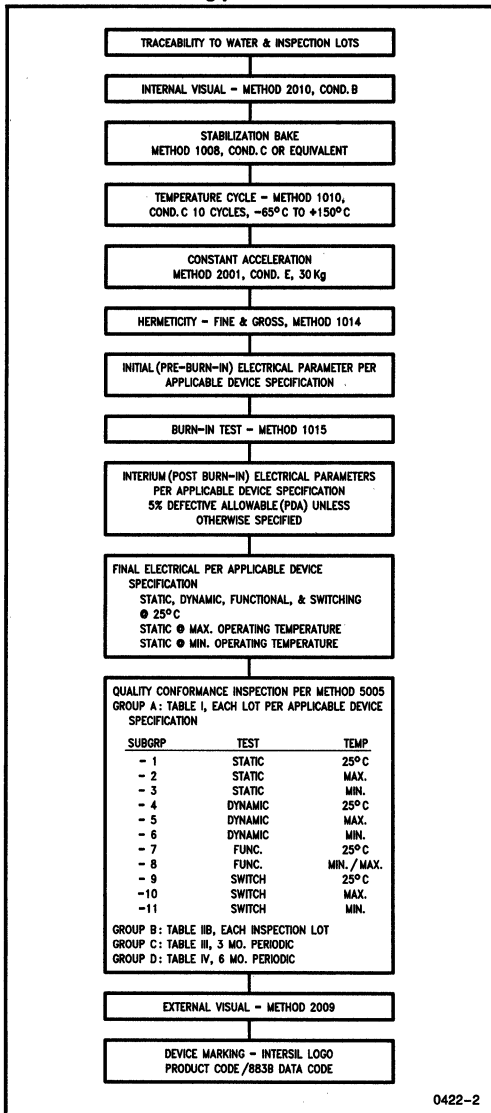
Intersil also offers several QPL-approved discrete products carrying the JAN, JTX, and JTXV designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

38510 Per MIL-M-38510 Slash Sheet

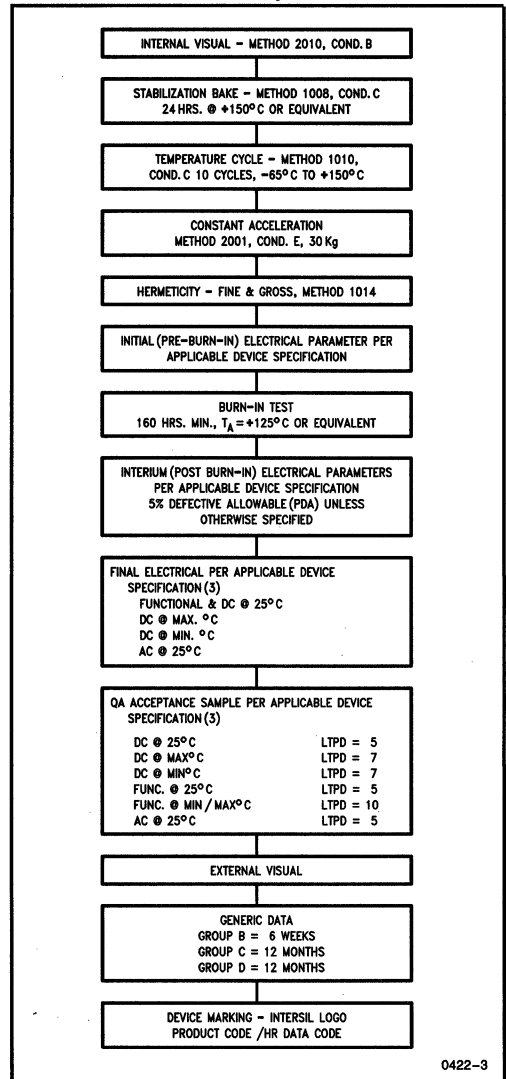


0422-1

**883 Class B (1, 2, 4)
Per MIL-STD-883 Rev. C
Screening per Method 5004**



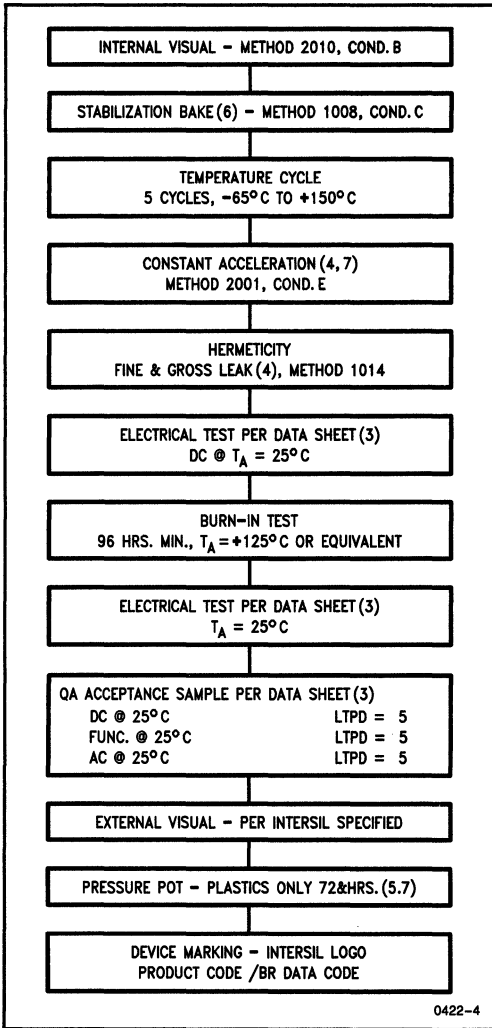
**HR (1, 2, 4)
In-House Hi Rel Processing
Flows Performed 100% Unless
Otherwise Noted Applies to
IC's and Hybrids**



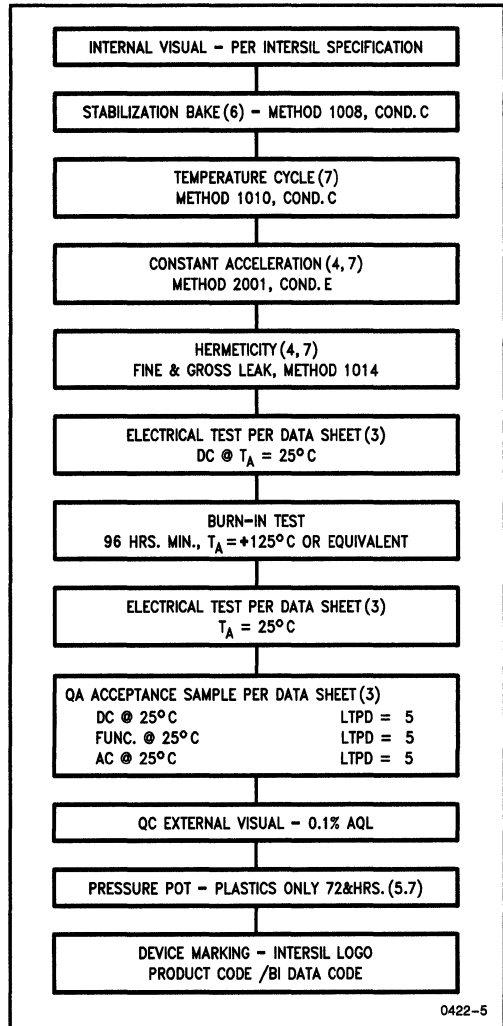
FOOTNOTES:

- (1) Governing Document, Order of Precedence
 - A. Purchase Order Contract
 - B. Detail Specification
 - C. This Flow
- (2) Where test methods are indicated, the test will be performed to MIL-STD-883.
- (3) With exception of parameters guaranteed by basic design, not tested.

BR (1, 2)
Performed 100% Unless Otherwise Noted
APPLIES TO IC'S AND HYBRIDS



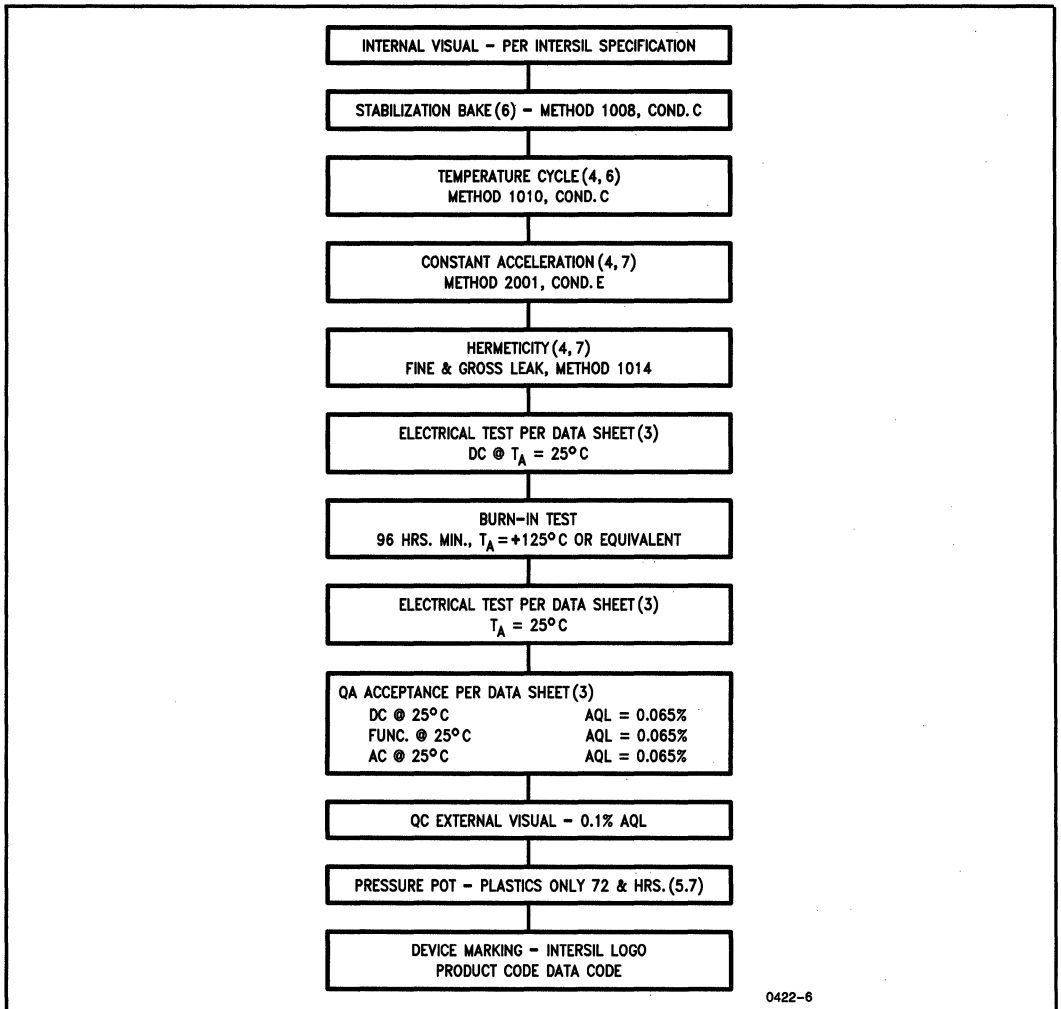
B1 (1, 2)
Performed 100% Unless Otherwise Noted
APPLIES TO IC'S ANY HYBRIDS AND
TRANSISTORS



FOOTNOTES:

- (1) Governing Document, Order of Precedence
 - A. Purchase Order Contract
 - B. Detail Specification
 - C. This Flow
- (2) Where test methods are indicated, the test will be performed to MIL-STD-883.
- (3) With exception of parameters guaranteed by basic design, not tested.
- (4) Does not apply to plastic packages.
- (5) May be performed any time after encapsulation.
- (6) For Plastic Packages, stabilization bake is accomplished during the encapsulation curing cycle.
- (7) Weekly Reliability Monitor.

**Standard Product (1, 2)
Performed 100% Unless Otherwise Noted
APPLIES TO IC'S AND HYBRIDS AND TRANSISTORS**

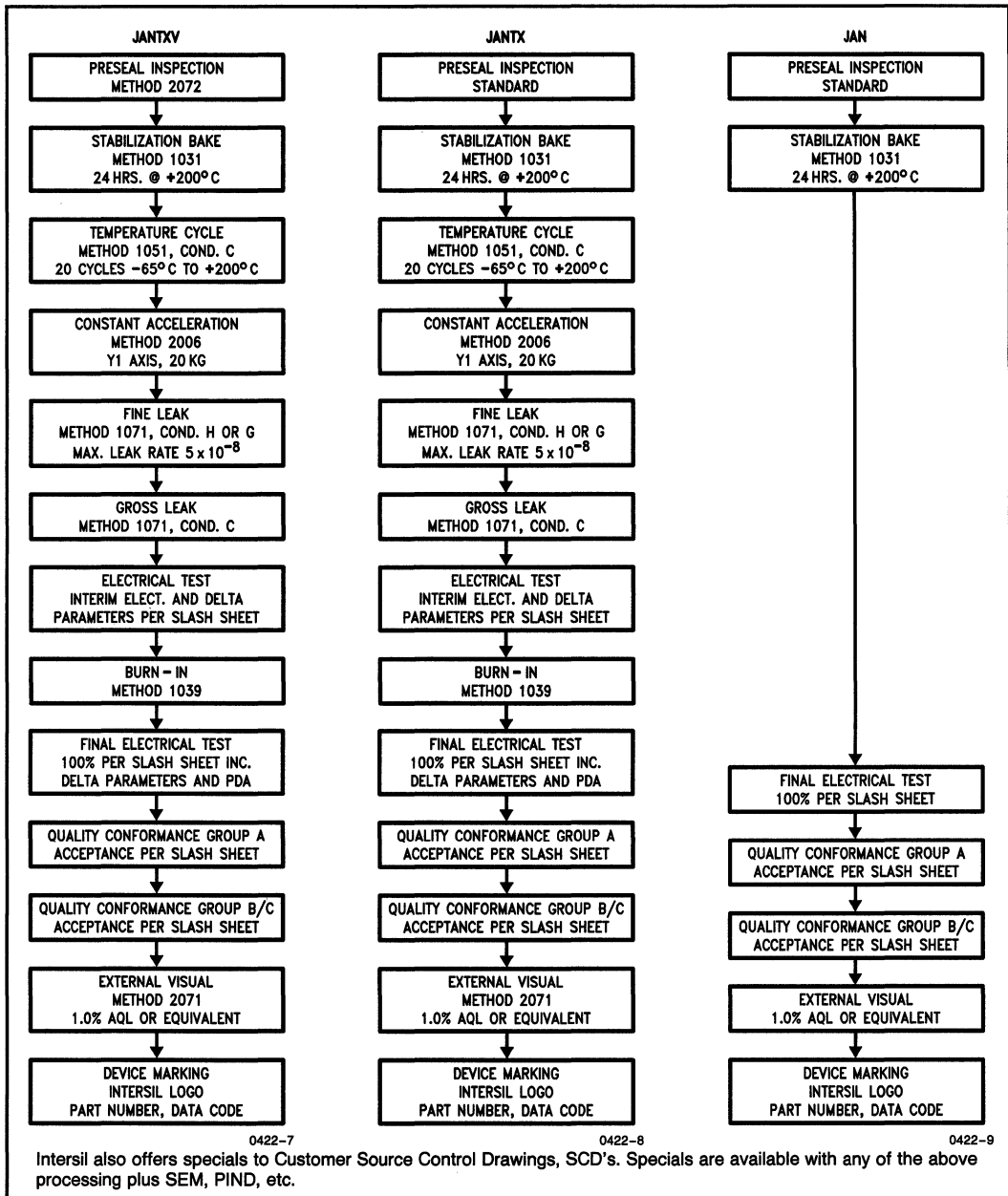


0422-6

FOOTNOTES:

- (1) Governing Document, Order of Precedence
 - A. Purchase Order Contract
 - B. Detail Specification
 - C. This Flow
- (2) Where test methods are indicated, the test will be performed to MIL-STD-883.
- (3) With exception of parameters guaranteed by basic design, not tested.
- (4) Does not apply to plastic packages.
- (5) May be performed any time after encapsulation.
- (6) For Plastic Packages, stabilization bake is accomplished during the encapsulation curing cycle.
- (7) Weekly Reliability Monitor.

**High-Reliability/Military Products
Discrete Products JAN, JANTX and JANTXV
Per MIL-S-19500 and MIL-STD-750
Performed 100% unless otherwise noted**



**HIGH RELIABILITY PROCESSING
PROCESS FLOW SELECTION GUIDE
- STANDARD IC PROCESS FLOWS -**

	39510	883B	HERMETIC PLASTIC				HERMETIC PLASTIC		HERMETIC	PLASTIC	NOTES
	JAN	REV. C.	HR	BR	BR	BI	BI	STANDARD	STANDARD		
ON-SHORE BUILD	X										
WAFER LOT											
TRACEABILITY	X	X								2	
PRE-CAP VISUAL M2010B	X	X	X	X	X						
STABILIZATION BAKE	X	X	X	X	X	X	X	X	X		
TEMPERATURE CYCLE	X	X	X	X	X	S	S	S	S	3	
CENTRIFUGE	X	X	X	S		S		S			
HERMETICITY	X	X	X	X		S		S			
ELECTRICAL TEST	X	X	X	X	X	X	X				
BURN-IN	X	X	X	X	X	X	X				
ELECTRICAL TEST	X	X	X	X	X	X	X	X	X		
POST BURN-IN PDA	X	X									
D.C. ELECT. @ 3 TEMPS.	X	X	X								
A.C. ELECT. @ 25°C	X	X	X								
GROUP A SAMPLE											
INSPECTION	X	X	X	X	X	X	X	X	X		
GROUP B EAC INSP. LOT	X	X	S							3	
STRICT DOCUMENTATION	X	X									
GROUP C & D INSPECTION	S	S	G	G						3	

**HIGH RELIABILITY PROCESSING
PROCESS FLOW SELECTION GUIDE
- STANDARD TRANSISTOR PROCESS FLOWS -**

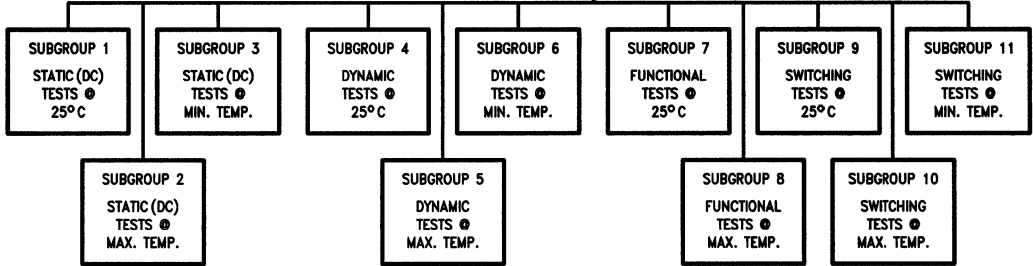
	HERMETIC PLASTIC			HERMETIC PLASTIC		HERMETIC STANDARD	PLASTIC STANDARD	NOTES
	JANTXV	JANTX	JAN	BI	BI			
ON-SHORE BUILD		X						
INSPECTION LOT TRACEABILITY	X	X	X					2
PRE-CAP VISUAL	X	X	X					
STABILIZATION BAKE	X	X	X	X	X	X	X	
TEMPERATURE CYCLE	X	X		S	S	S	S	3
CENTRIFUGE	X	X		S		S		
HERMETICITY	X	X		S		S		
ELECTRICAL TEST	X	X	X	X	X			
BURN-IN	X	X		X	X			
ELECTRICAL TEST	X	X						
POST BURN-IN PDA	X	X						
D.C. ELECT. @ 25°C	X	X	X	X	X	X	X	
A.C. ELECT. @ 25°C	X	X	X	X	X	X	X	
GROUP A	X	X	X	X	X	X	X	
GROUP B EACH INSP. LOT	X	X	S					3
STRICT DOCUMENTATION	X	X	X					
GROUP C INSPECTION	S	S	S					

- NOTE 1.** ONLY MAJOR TRANSISTOR PROCESSING DIFFERENCES ARE SHOWN HERE. SEE DETAIL FLOWS ON FOLLOWING PAGES FOR MORE SPECIFIC DATA. CHART IS FOR HERMETIC PACKAGES. ONLY MINIMUM REQUIREMENTS ARE SHOWN.
- 2.** WAFER LOT TRACEABILITY MAINTAINED AND AVAILABLE AT EXTRA CHARGE FOR OTHER PRODUCTS.
- 3.** S= SAMPLE TEST ON REGULAR BASIS.
X= PERFORMED 100%. G= GENERIC DATA.
- 4.** INTERSIL ALSO OFFERS "SPECIALS" TO SPECIFIC CUSTOMER SCD'S. SPECIALS ARE AVAILABLE WITH ANY OF THE ABOVE PROCESSING PLUS SEM, PIND, ETC.

MIL-STD-883 REV. C, CLASS B

METHOD 5005

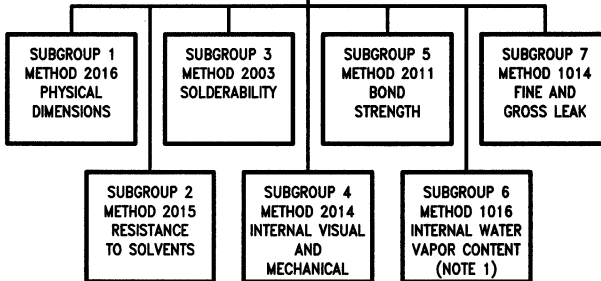
GROUP A
ELECTRICAL TESTS



0422-10

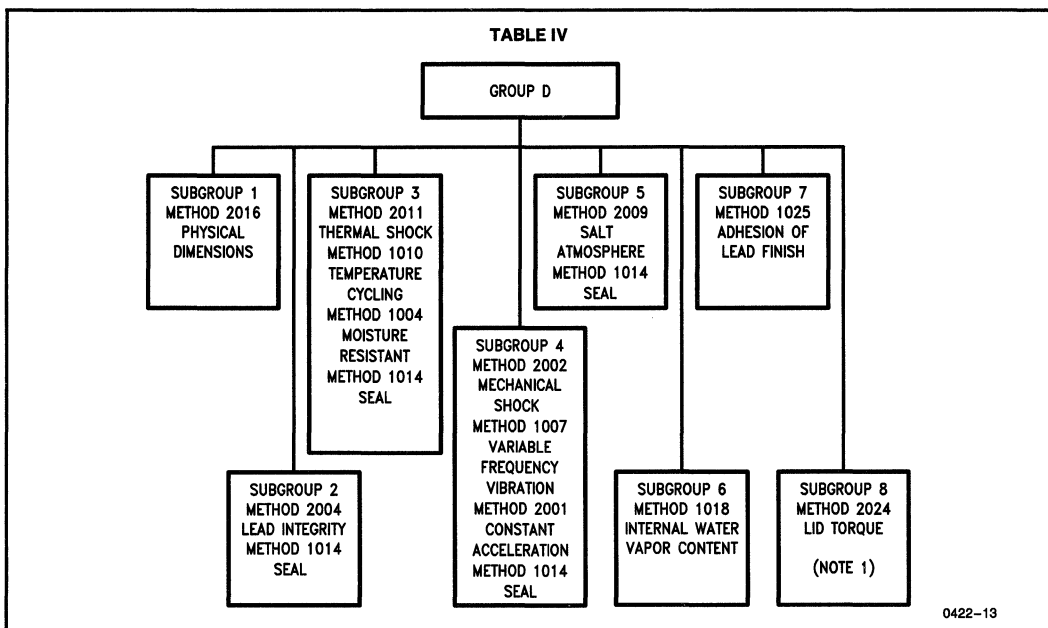
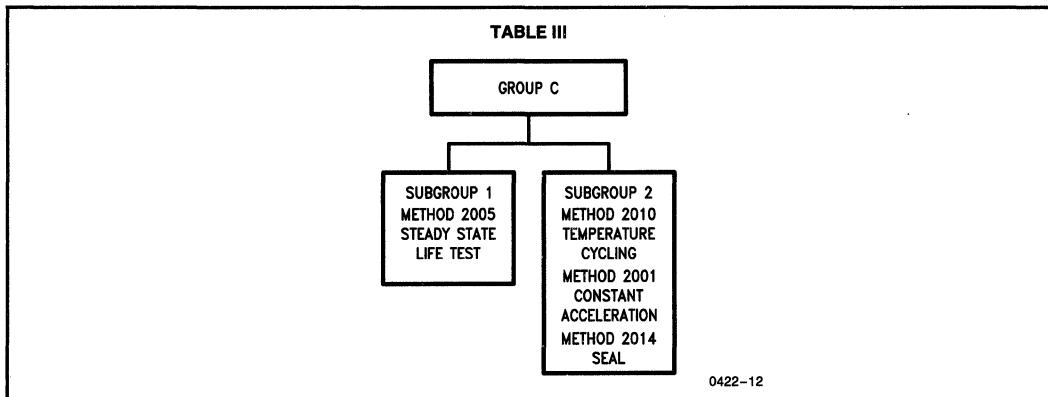
TABLE IIb

GROUP B



0422-11

Note 1: Required only if package contains a desiccant.



Note 1: Applies if package has a Frit-Seal.

INTERSIL QPL/Hi-REL DEVICES

Data Acquisition Products

JM38510

12702BEA	AD7520UD
12703BVA	AD7521UD
12704BVC	AD7541TD
12704BVA	AD7541TD

Analog Switch Products

JM38510

10501BEA	IH5040MDE
10501BEC	IH5040MDE
10502BEA	IH5041MDE
10502BEC	IH5041MDE
10503BEA	IH5042MDE
10503BEC	IH5042MDE
10504BEA	IH5043MDE
10504BEC	IH5043MDE
11101BAC	DG181AL
11101BCC	DG181AP
11101BIA	DG181AA
11101BIC	DG181AA
11101BCA	DG181AP
11102BIA	DG182AA
11102BAC	DG182AL
11102BCC	DG182AP
11102BIC	DG182AA
11102BCA	DG182AP
11103BAC	DG184AL
11103BEC	DG184AP
11103BEA	DG184AP
11104BAC	DG185AL
11104BEC	DG185AP
11104BEA	DG185AP
11105BAC	DG187AL
11105BCC	DG187AP
11105BIA	DG187AA
11105BIC	DG187AA
11105BCA	DG187AP
11106BAC	DG188AL
11106BCC	DG188AP
11106BIA	DG188AA
11106BIC	DG188AA
11106BCA	DG188AP
11107BAC	DG190AL
11107BEC	DG190AP
11107BEA	DG190AP
11107BAC	DG191AL

Data Acquisition Products

JM38510 (Continued)

11108BEC	DG191AP
11108BEA	DG191AP
11601BCC	DG300AAP
11601BCA	DG300AAP
11602BCC	DG301AAP
11602BCA	DG301AAP
11603BCC	DG302AAP
11603BCA	DG302AAP
11604BCC	DG303AAP
11604BCA	DG303AAP
12302BEA	DG201AP
12302BEC	DG201AP

Analog Switch Products

Military DWG. NO.

7705201EA	IH6108MJE
7705201EC	IH6108MDE
7705201EA	IH6108MDE
7705301EA	DG201AK
7705301EC	DG201AP
7705301EA	DG201AP
7801401CA	DG129AK
7801401CC	DG129AP
7801401CA	DG129AP
8100601AC	IH5040MFD
8100601EC	IH5040MDE
8100601EA	IH5040MDE
8100602AC	IH5041MFD
8100602EC	IH5041MDE
8100602EA	IH5041MDE
8100602IA	IH5041MTW
8100602IC	IH5041MTW
8100602IB	IH5041MTW
8100603AC	IH5042MFD
8100603EC	IH5042MDE
8100603EA	IH5042MDE
8100603IA	IH5042MTW
8100603IC	IH5042MTW
8100603IB	IH5042MTW
8100604AC	IH5043MFD
8100604EA	IH5043MJE
8100604EC	IH5043MDE
8100604EA	IH5043MDE
8100605AC	IH5044MFD
8100605EA	IH5044MJE

Analog Switch Products

Military DWG. NO. (Continued)

8100605EC	IH5044MDE
8100605EA	IH5044MDE
8100605IA	IH5044MTW
8100605IC	IH5044MTW
8100605IB	IH5044MTW
8100606AC	IH5045MFD
8100606EA	IH5045MJE
8100606EC	IH5045MDE
8100606EA	IH5045MDE
8100606IA	IH5045MTW
8100606IC	IH5045MTW
8100606IB	IH5045MTW
5962-8513104XA	IH5116MJI
5962-8513104XA	IH5116MDI
5962-8513104XC	IH5116MDI
5962-8513105XA	IH5216MJI
5962-8513105XA	IH5216MDI
5962-8513105XC	IH5216MDI
5962-8513106EA	IH5208MJE
5962-8513106EA	IH5208MDE
5962-8513106EC	IH5208MDE

MIL-S-19500 Transistors

2N3821JAN	2N4858JAN
2N3821JTX	2N4858JTX
2N3821JTXV	2N4858JTXV
2N3823JAN	2N4859JAN
2N3823JTX	2N4859JTX
2N3823JTXV	2N4859JTXV
2N4091JAN	2N4860JAN
2N4091JTX	2N4860JTX
2N4091JTXV	2N4860JTXV
2N4092JAN	2N4861JAN
2N4092JTX	2N4861JTX
2N4092JTXV	2N4861JTXV
2N4093JAN	2N5114JAN
2N4093JTX	2N5114JTX
2N4093JTXV	2N5114JTXV
2N4856JAN	2N5115JAN
2N4856JTX	2N5115JTX
2N4856JTXV	2N5115JTXV
2N4857JAN	2N5116JAN
2N4857JTX	2N5116JTX
2N4857JTXV	2N5116JTXV

INTERSIL MIL-STD-883B REV. C COMPLIANT DEVICES

Data Acquisition Products

883B Rev C.
 AD7520SD/883B
 AD7520TD/883B
 AD7520UD/883B
 AD7521SD/883B
 AD7521TD/883B
 AD7521UD/883B
 AD7533SD/883B
 AD7533TD/883B
 AD7533UD/883B
 AD7541SD/883B
 AD7541TD/883B
 ICL7134UJMJI/883B
 ICL7134UKMJI/883B
 ICL7134ULMJI/883B
 ICL7134BJMJI/883B
 ICL7134BKMJI/883B
 ICL7134BLMJI/883B

Special Analog Functions

883B Rev C.
 ICL7660MTV/883B
 ICL7662MTV/883B
 ICL7667MJA/883B
 ICL7667MTV/883B
 ICL8038AMJD/883B
 ICL8038BMJD/883B
 ICL8069CMSQ/883B
 ICL8069DMSQ/883B
 ICL8211MTY/883B
 ICL8212MTY/883B

Timer/Counter Circuits

883B Rev C.
 ICM7555MTV/883B
 ICM7556MJD/883B

Amplifiers-Operational
883B Rev C.
 ICL8021MTY/883B
 ICL8023MJE/883B

Analog Switch Products

883B Rev C.
 D123AK/883B
 D123AL/883B
 D125AK/883B
 D125AL/883B
 D129AK/883B
 D129AL/883B
 DG126AK/883B

Analog Switch Products

883B Rev C. (Continued)
 DG126AL/883B
 DG129AK/883B
 DG129AL/883B
 DG133AK/883B
 DG133AL/883B
 DG134AK/883B
 DG134AL/883B
 DG139AK/883B
 DG139AL/883B
 DG140AL/883B
 DG140AP/883B
 DG141AL/883B
 DG141AP/883B
 DG142AK/883B
 DG142AL/883B
 DG143AK/883B
 DG143AL/883B
 DG144AK/883B
 DG144AL/883B
 DG145AL/883B
 DG145AP/883B
 DG146AL/883B
 DG146AP/883B
 DG151AK/883B
 DG151AL/883B
 DG152AK/883B
 DG152AL/883B
 DG153AL/883B
 DG153AP/883B
 DG154AK/883B
 DG154AL/883B
 DG161AL/883B
 DG161AP/883B
 DG162AK/883B
 DG162AL/883B
 DG163AL/883B
 DG163AP/883B
 DG164AK/883B
 DG164AL/883B
 DG180AA/883B
 DG180AK/883B
 DG180AL/883B
 DG181AA/883B
 DG181AK/883B
 DG181AL/883B
 DG182AA/883B
 DG182AK/883B
 DG182AL/883B
 DG183AL/883B
 DG183AP/883B
 DG184AK/883B
 DG184AL/883B
 DG185AK/883B
 DG185AL/883B
 DG186AA/883B
 DG186AL/883B

Analog Switch Products

883B Rev C. (Continued)
 DG186AP/883B
 DG187AA/883B
 DG187AK/883B
 DG187AL/883B
 DG188AA/883B
 DG188AK/883B
 DG188AL/883B
 DG189AP/883B
 DG190AK/883B
 DG190AL/883B
 DG191AK/883B
 DG191AL/883B
 DG200AA/883B
 DG200AK/883B
 DG201AK/883B
 DG201AAK/883B
 DG202AK/883B
 DG300AAK/883B
 DG301AAA/883B
 DG301AAK/883B
 DG302AAK/883B
 DG303AAK/883B
 DGM181AA/883B
 DGM181AK/883B
 DGM182AA/883B
 DGM182AK/883B
 DGM184AK/883B
 DGM185AK/883B
 DGM190AK/883B
 DGM191AK/883B
 IH5009MJD/883B
 IH5010MJD/883B
 IH5011MJE/883B
 IH5012MJE/883B
 IH5013MJD/883B
 IH5014MJD/883B
 IH5015MJE/883B
 IH5016MJE/883B
 IH5017MJD/883B
 IH5018MJD/883B
 IH5019MJE/883B
 IH5020MJE/883B
 IH5021MJD/883B
 IH5022MJD/883B
 IH5023MJE/883B
 IH5024MJE/883B
 IH5040MFD/883B
 IH5040MJE/883B
 IH5041MFD/883B
 IH5041MJE/883B
 IH5042MFD/883B
 IH5042MJE/883B
 IH5043MFD/883B
 IH5043MJE/883B
 IH5044MFD/883B
 IH5044MJE/883B

Analog Switch Products

883B Rev C. (Continued)
 IH5045MFD/883B
 IH5045MJE/883B
 IH5046MFD/883B
 IH5046MJE/883B
 IH5047MFD/883B
 IH5047MJE/883B
 IH5052MJE/883B
 IH5053MJE/883B
 IH5108MJE/883B
 IH5116MJI/883B
 IH5140MFD/883B
 IH5140MJE/883B
 IH5141MFD/883B
 IH5141MJE/883B
 IH5142MFD/883B
 IH5142MJE/883B
 IH5143MFD/883B
 IH5143MJE/883B
 IH5144MFD/883B
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 IH5150MFD/883B
 IH5150MJE/883B
 IH5151MFD/883B
 IH5151MJE/883B
 IH5208MJE/883B
 IH5216MJI/883B
 IH5341MTW/883B
 IH5352MJE/883B
 IH6108MJE/883B
 IH6116MJI/883B
 IH6201MJE/883B
 IH6208MJE/883B
 IH6216MJI/883B

Microcontrollers, Microperipherals, Memory

883B Rev C.
 ICM7170MDG/883B
 IM6402-1MJL/883B
 IM6402AJL/883B
 IM6402AMJL/883B
 IM6402IJL/883B
 IM6653AMJG/883B
 IM6653MJG/883B
 IM6654-1IJG/883B
 IM6654AMJG/883B
 IM6654MJG/883B
 IM6654IJG/883B

High Reliability Processing

GLOSSARY OF MILITARY/AEROSPACE HI-REL DEFINITIONS/TERMINOLOGY

ACCELERATED BURN-IN — Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150°C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA — Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE — Technique used to define manufacturing and test processes at time of order placement. Baseline usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs.

BURN-IN — A screening operation. Devices are subjected to high temperature (typically 125°C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

CLASS S AND B INTEGRATED CIRCUITS — These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-STD-883. Classes, S and B are sometimes referred to as "Levels S and B." The Classes cover:

CLASS S — For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.

CLASS B — For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap visual, etc.

CORRECTIVE ACTION — Those actions which a given supplier (or user) agrees to perform so that a detected problem does not reoccur.

DESC — Defense Electronic Supply Center, located in Dayton, Ohio.

DESC LINE CERTIFICATION — The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

DPA — Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

GENERIC DATA — Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order.

GROUP A — Sample electrical test which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

GROUP B — For Integrated Circuits, Package-Related Environmental Tests are performed for Class B Products per MIL-STD-883, Method 5005 (For Revision Products) or per the "HR" program. For Class S, Group B includes Additional Processing, including steady state life test.

For Diodes and Transistors, both environmental and life test are performed per MIL-S-19500.

GROUP C — For Class B or "HR" program I.C.'s, Die-Related Tests are performed. Not required for Class S I.C.'s. Group C includes life testing temperature cycling and constant acceleration per MIL-M-38510. For diodes transistors, Group C includes both environmental and life tests per MIL-S-19500.

GROUP D — Additional Package-Related Environmental Test for I.C.'s for Class B or Class S products or per the "HR" program.

JAN — "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX — A JAN-qualified diode or transistor which has been subjected to additional screening and burn-in tests. MIL-S-19500 only.

JAN TXV — A JAN-qualified diode or transistor which, in addition to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits. MIL-S-19500 only. LTPD-Lot Tolerance Percent Defective is a sampling plan measurement criteria.

MIL-M-38510 — The general military specification for integrated circuits.

M38510/XXX — Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-S-19500 — The general military specifications for diodes and transistors.

MIL-S-19500/XXX — Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 — Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

MIL-STD-883 — Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, hermeticity, storage life, etc.

NPFC — Naval Publications and Forms Center, Philadelphia Printing and distribution source for military specifications.

NON-STANDARD PARTS — In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL — Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

HIGH RELIABILITY PROCESSING

OPERATING LIFE TEST — Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA — Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA — Percent Defective Allowable. Criteria sometimes applied to burn-in screening. MIL-STD-883 and MIL-M-38510 typically require either a 5% or 10% PDA. A 10% PDA means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

PDS — Parameter Drift Screening. Measures the changes (Δ s) in electrical parameters through burn-in. Common for Class S devices.

PIND — Particle Impact Noise Detection. This is an audio screening test to locate and eliminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY — The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL — A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY — Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABILITY — Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours) or MTBF (mean time between failure in hours). MTBF is the reciprocal of Failure Rate.

QPL — Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist for MIL-M-38510:

PART II QPL — This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided after 90 days whenever any one supplier is granted a PART I QPL.

PART I QPL — A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QUALIFYING ACTIVITY — Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING — Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D per MIL-STD-883. For diodes and transistors, this usually means testing to Groups A, B and C per MIL-STD-750.

QUALITY CONFORMANCE TESTING — These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

RADC — Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA — Same as variable data.

REWORK PROVISION — For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), re-marking, and cleaning.

SCREENING — Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc.

SEM INSPECTION — Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects.

SERIALIZATION — The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs — Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

SOURCE INSPECTION — Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can typically occur at one or more points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection.

TRACEABILITY — A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA — Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.

Section 16 — Ordering and Marking Information

ORDERING INFORMATION

Device Family Prefixes

AD	—Analog Devices Alternate Source
D	—Driver/Level Translator IC
DG	—Siliconix Analog Switch Alternate Source
DGM	—Monolithic DG Analog Switch Replacement
ICL	—Linear IC
ICM	—Microperipheral IC
ICH	—Hybrid IC
IM	—Microcontroller IC
LH	—National Semiconductor Hybrid Alternate Source
LM	—National Semiconductor Alternate Source
MM	—High Voltage Analog Switch
NE	—Signetics Alternate Source
SE	—Signetics Alternate Source
2N	—Industry Standard Discrete Transistor
3N	—Industry Standard Discrete Transistor
IT	—Discrete Transistor
ITE	—Discrete Transistor
J	—Discrete Transistor
M	—Discrete Transistor
NF	—Discrete Transistor
P	—Discrete Transistor
PN	—Discrete Transistor
U	—Discrete Transistor
VCR	—Discrete Transistor
ID	—Low Leakage Diodes
G	—Siliconix Analog Gate Alternate Source
IH	—Analog Switch Family
ADC	—National Semiconductor A/D Alternate Source
μa	—Fairchild Linear Alternate Source

Temperature Range Designators

C	—Commercial: 0°C to +70°C
I	—Industrial: Either –25°C to +85°C or –40°C to +85°C (Specified on Datasheet)
M	—Military: –55°C to +125°C

Package Type Designators

A	—TO-237
B	—Small Outline IC (SOIC)
C	—TO-220
D	—Ceramic Dual-In-Line
E	—Small TO-8
F	—Ceramic Flat Pack
H	—TO-66
I	—16 Pin (0.6 x 0.7 Pin Spacing) Hermetic Hybrid Dip
J	—CERDIP Dual-In-Line
K	—TO-3
L	—Leadless, Ceramic
P	—Plastic Dual-In-Line
S	—TO-52
T	—TO-5 Type (Also TO-78, TO-99, TO-100)
U	—TO-72 Type (Also TO-18, TO-71)
V	—TO-39
Z	—TO-92

EXCEPTIONS TO PACKAGE TYPE DESIGNATORS

DG & DGM Series

A	—10 Pin Metal Can
L	—14 Pin Flatpack
P	—Ceramic DIP (Special Order Only)
K	—CERDIP

AD Series

H	—TO-52
D	—CERDIP Ceramic DIP
N	—Epoxy DIP
R	—TO-92

ORDERING INFORMATION

Pin Count Designator

A	8	P	20
B	10	Q	2
C	12	R	3
D	14	S	4
E	16	T	6
F	22	U	7
G	24	V	8 (0.200" pin circle, isolated case)
H	42		
I	28	W	10 (0.230" pin circle, isolated case)
J	32		
K	35	Y	8 (0.200" pin circle, case to pin 4)
L	40		
M	48	Z	10 (0.230" pin circle, case to pin 5)
N	18		

EXCEPTIONS TO PIN COUNT DESIGNATORS

DG & DGM Series

A	—10 Pin Metal Can
L	—14 Pin Flatpack
P	—Ceramic DIP (Special Order Only)
K	—CERDIP

AD Series

D	—20, 18, 16 or 14
H	—3 Pin
N	—20, 18, 16 or 14

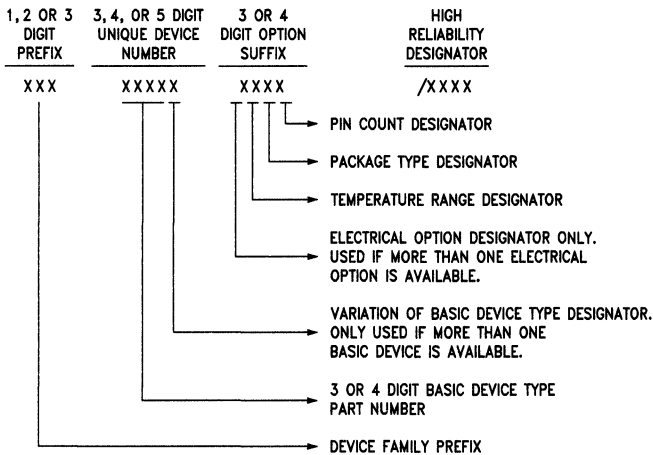
HIGH RELIABILITY DESIGNATOR

/883B	—MIL-STD-883B Screened Device
/HR	—High-Reliability Device
/BR	—Cost Effective High-Reliability Device
/BI	—Burn-in Only Process Flow

ORDERING INFORMATION

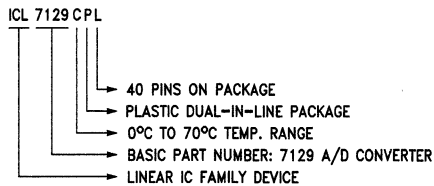
Part Numbering System

All Intersil Part Numbers consist of a Device Family Prefix, a Basic Numeric Part Number, and an Option Suffix, as follows:



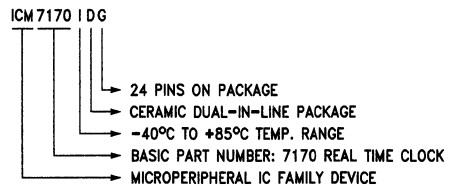
0424-1

Part Number Systems Examples



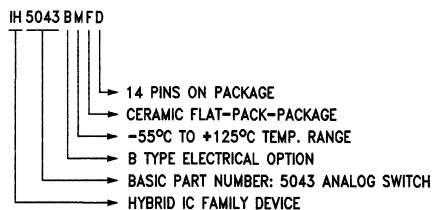
0424-2

Example 1



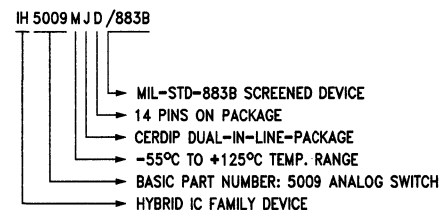
0424-3

Example 2



0424-4

Example 3

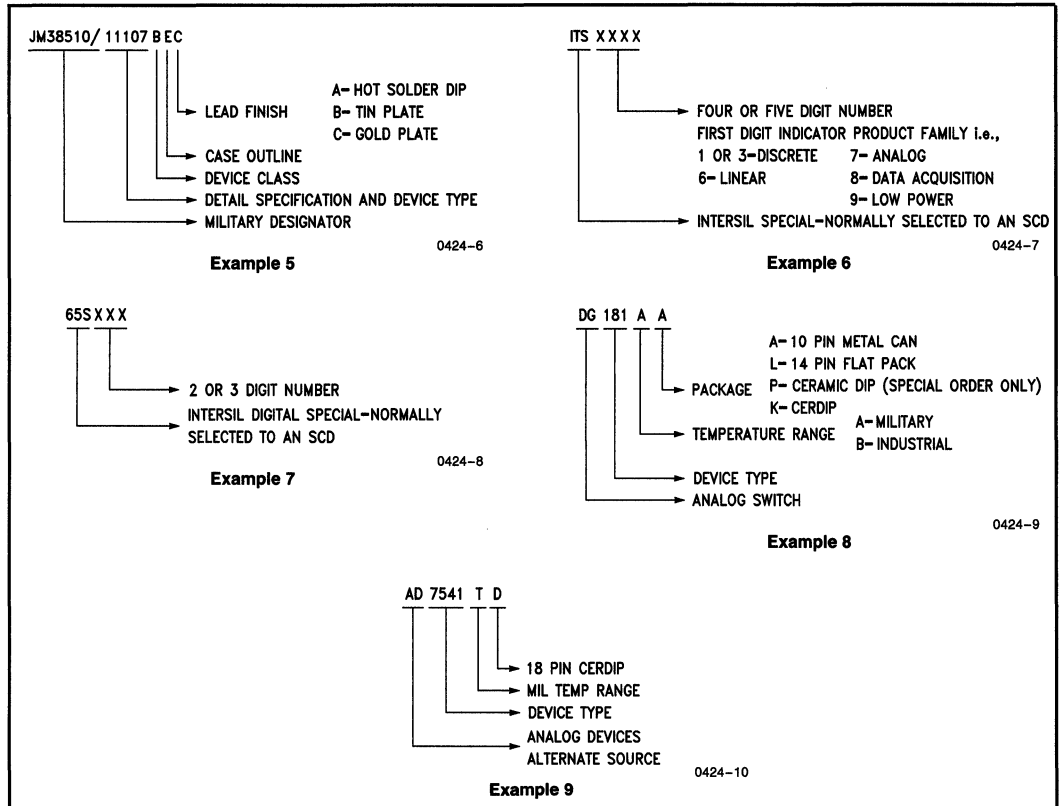


0424-5

Example 4

ORDERING INFORMATION

Part Number Systems Examples (Continued)



Intersil Code and FSCM Number Information

CDPR — Letter Code for Intersil Assigned by the U.S. Government

32293 — Intersil FSCM Number Assigned by the U.S. Government

EVALUATION KITS

Product Description	Part Number	Contents
Power Amplifier Kits	ICH8510IEV/KIT	ICH8510i + Socket + Heat Sink
	ICH8520IEV/KIT	ICH8520i + Socket + Heat Sink
3½ Digit LCD Panel Meter Kit	ICL7106EV/KIT	ICL7106 + PC Card + All Passive Components
3½ Digit LED Panel Meter Kit	ICL7107EV/KIT	ICL7107 + PC Card + All Passive Components
3½ Digit Low Power LCD Panel Meter Kit	ICL7126EV/KIT	ICL7126 + PC Card + All Passive Components
4½ Digit A/D Converter Kit	ICL7129EV/KIT	ICL7129 + 4½ Digit LCD Display + ICL8069 + PC Card + Active, Passive Components
4½ Digit LCD Display Driver Kit	ICM7211EV/KIT	ICM7211 + 4½ Digit LCD Display + PC Card + Active, Passive Components
8 Character Multiplexed LCD Display Driver Kit	ICM7233AEV/KIT	2 of ICM7233A + PC Card + 8 Character Triplexed LCD Display
8 Character Multiplexed LED Display Driver Kit	ICM7243BEV/KIT	ICM7243B + PC Card + 8 Character LED
4½ Digit LCD Display Counter Kit	ICL7224EV/KIT	ICM7224 + ICM7207A + 5.24288MHz Crystal + 4½ Digit LCD Display + PC Card + Passive Components
4½ Digit LED Display Counter Kit	ICM7225EV/KIT	ICM7225 + ICM7207A + 5.24288MHz Crystal + 4½ Digit LED Display + PC Card + Passive Components
Touch Tone Encoder		
One contact per key	ICM7206EV/KIT	ICM7206 + 3.579545MHz Crystal
Two contacts per key, common to positive supply	ICM7206AEV/KIT	ICM7206A + 3.579545MHz Crystal
Common to negative supply, oscillator enabled when key depressed	ICM7206BEV/KIT	ICM7206B + 3.579545MHz Crystal
8 Digit Frequency/Period Counter		
5 Function	ICM7226AEV/KIT	ICM7226A + 10MHz Crystal + PC Card + LEDs + All Passive Components

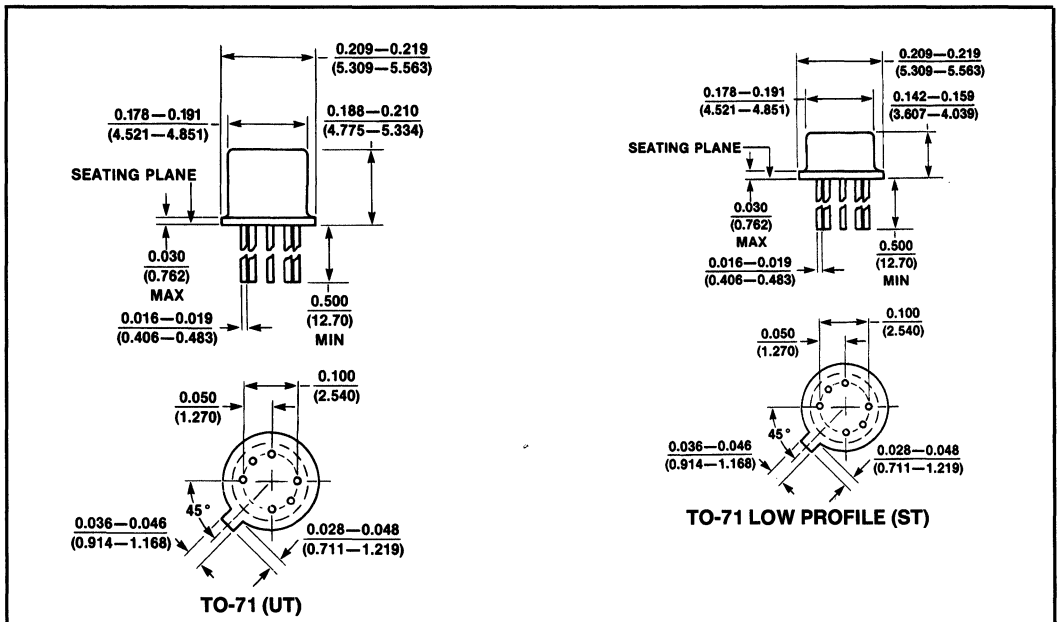
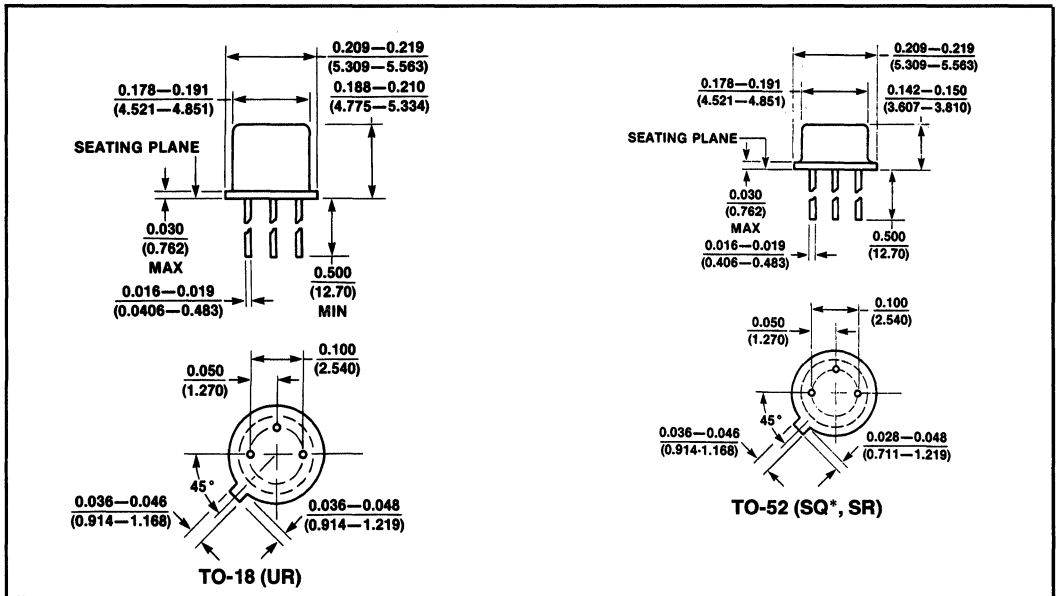
APPLICATION NOTE SUMMARY

The following are brief descriptions of current Intersil Application notes.

- A003 UNDERSTANDING AND APPLYING THE ANALOG SWITCH**
Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET+driver), J-FET "virtual ground" and J-FET "positive signal" types. Application information included.
- A004 IH5009 LOW COST ANALOG SWITCH SERIES**
Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.
- A005 THE 8007 — A HIGH PERFORMANCE FET INPUT OP AMP**
Compares the 8007 with the 741, which is pin compatible and suggests applications such as logantilog amplifier, sample and hold circuit, photometer, peak detector, etc.
- A007 USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER**
Describes in detail the operation of the 8048 logarithmic amplifier, and its counterpart, the 8049 antilog amp.
- A011 A PRECISION FOUR QUADRANT MULTIPLIER — THE 8013**
Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.
- A013 EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038**
This note includes 17 of the most asked questions regarding the use of the 8038.
- A015 DESIGN FOR A BATTERY OPERATED FREQUENCY COUNTER**
Describes a low cost battery operated frequency/period counter using the 7207A and 7208. Includes specifications, schematics, PC layout, etc.
- A016 SELECTING A/D CONVERTERS**
Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.
- A017 THE INTEGRATING A/D CONVERTER**
Provides an explanation of integrating A/D converters, together with a detailed error analysis.
- A018 DO'S AND DONT'S OF APPLYING A/D CONVERTERS**
An analysis of proper design techniques using D/A converters.
- A019 4½ DIGIT PANEL METER DEMONSTRATION/INSTRUMENTATION BOARDS**
Describes two typical PC board layouts using the 8052A/7103A 4½ digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.
- A020 A COOKBOOK APPROACH TO HIGH SPEED DATA ACQUISITION AND MICROPROCESSOR INTERFACING**
Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.
- A021 POWER D/A CONVERTERS USING THE ICH 8510**
Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc. Also see A026.
- A022 A NEW J-FET STRUCTURE — THE VARAFET**
Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built-in.
- A023 LOW COST DIGITAL PANEL METER DESIGNS**
Provides a detailed explanation of the 7106 and 7107 3½ digit panel meter IC's, and describes two of the evaluation kits available from Intersil.
- A026 DC SERVO MOTOR SYSTEMS USING THE ICH8510**
This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.
- A027 POWER SUPPLY DESIGN USING THE ICL8211 AND ICL8212**
Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbar, power supply window detector, etc.
- A028 BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR**
This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a $\pm 4\frac{1}{2}$ digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.
- A029 POWER OP AMP HEAT SINK KIT**
Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.
- A030 THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS**
Describes in detail the operation of the 7104. Includes in digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.
- A031 COIL DRIVE ALARM DESIGN CONSIDERATIONS**
Explains the procedure used when using watch circuits to drive piezoelectric transducers.
- A032 UNDERSTANDING THE AUTO-ZERO AND COMMON MODE PERFORMANCE OF THE ICL7106/7107/7109 FAMILY**
Explains in detail the operation of the ICL7106/7/9 family of A/D Converters.

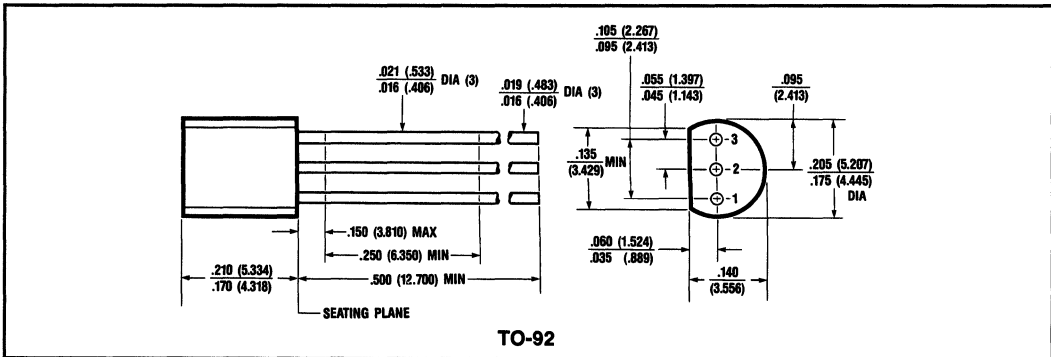
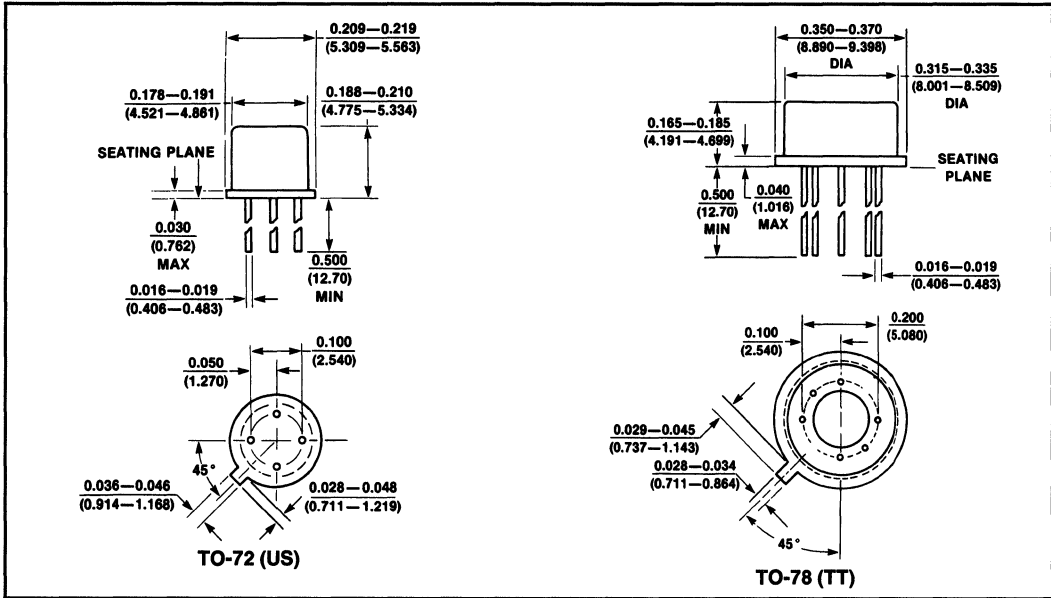
- A046 BUILDING A BATTERY OPERATED AUTO RANGING DVM WITH THE ICL7106**
Explains principles of auto ranging, problems and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.
- A047 GAMES PEOPLE PLAY WITH A/D CONVERTERS**
Describes 25 different integrating A/D converter applications. Input circuits, conversion modifications, display and microprocessor interfaces are shown in detail.
- A050 USING THE IT500 FAMILY TO IMPROVE THE INPUT BIAS CURRENT OF BIFET OP AMPS**
A brief description of a preamplifier for BIFET OP AMPS.
- A051 PRINCIPLES AND APPLICATIONS OF THE ICL7660 CMOS VOLTAGE CONVERTER**
Describes internal operation of the ICL7660. Includes a wide range of possible applications.
- A052 TIPS FOR USING SINGLE CHIP 3½ DIGIT A/D CONVERTERS**
Answers frequently asked questions regarding the operation of 3½ digit single chip A/D converters. Included are sections on power supplies, displays, timing and component selection.
- A053 THE ICL7650 A NEW ERA IN GLITCH-FREE CHOPPER STABILIZER AMPLIFIERS**
A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.
- A054 DISPLAY DRIVER FAMILY COMBINES CONVENIENCE OF USE WITH MICROPROCESSOR INTERFACEABILITY**
Compares and describes the various display drivers. Includes design examples for 7 segment, Alpha-numeric, and bargraph systems.

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

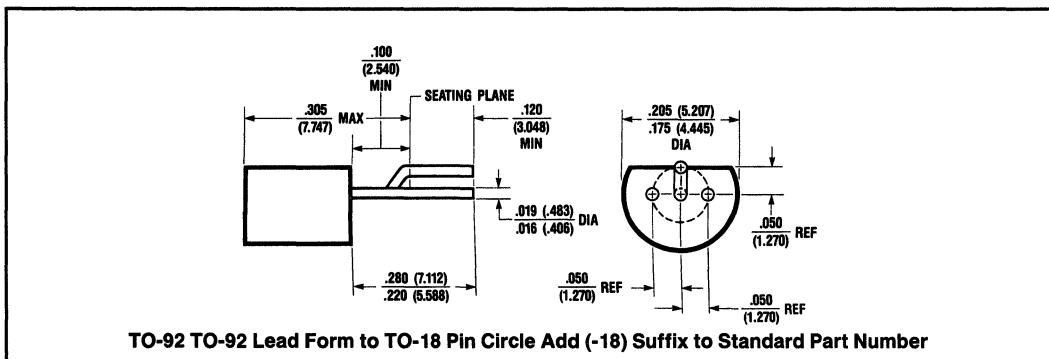
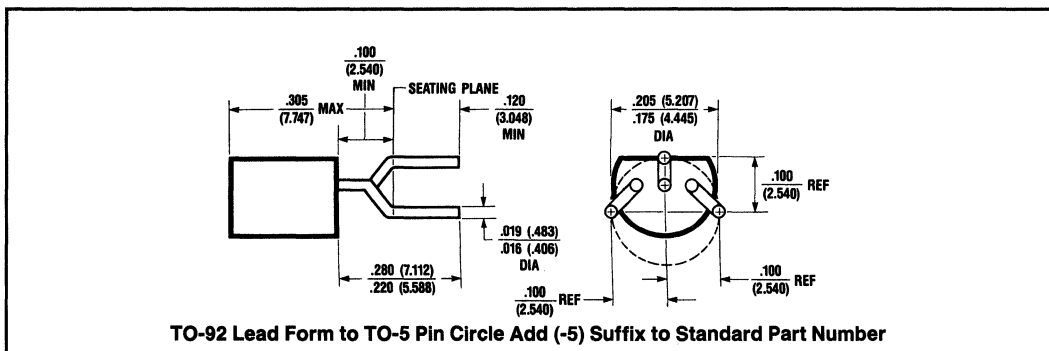
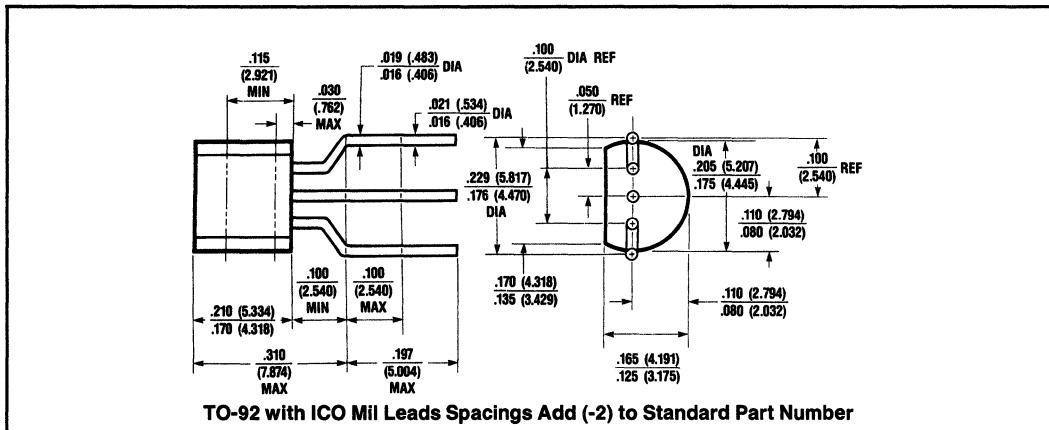


SQ* denotes a two lead package; center lead missing.

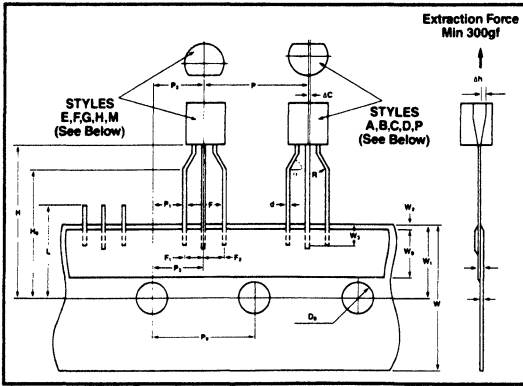
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



PACKAGE OUTLINES All dimensions given in inches and (millimeters).



TO-92 TAPING SPECIFICATIONS AND WINDING STYLES



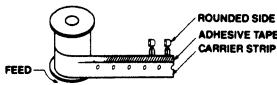
(EIA STD RS468)

P	12.7 ± 0.5	H ₀	16 ± 0.5
P ₀	12.7 ± 0.2	F	5 ^{+0.02} _{-0.02}
P ₁	3.85 ± 0.5	F ₁ - F ₂	± 0.3
P ₂	6.35 ± 0.5	D ₀	4 ± 0.2
P ₃	6.35	t	0.7 ± 0.2
W	8 ^{+1.0} _{-0.5}	Δ _H	0 ± 1
W ₀	6 ± 1	d	0.050 ^{+0.005} _{-0.005} dia.
W ₁	9 ± 0.5	R	0.8
W ₂	Max. 0.5	α	45°C - 60°C
W ₃	Min. 4.5	L	Max. 11
H	19.5 ± 0.5	Δ _C	0 ± 0.5

All Dimensions in Millimeter

STYLE A

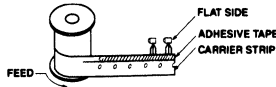
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ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

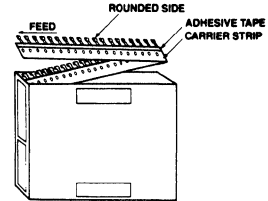
STYLE E

STYLE E IS A PREFERRED STYLE



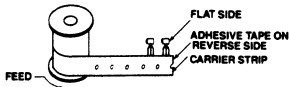
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE P



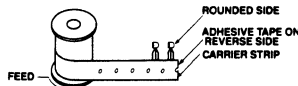
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE
 STYLE P IS EQUIVALENT TO STYLES A, B, C, D OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

STYLE B



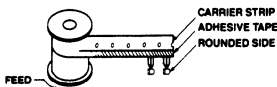
FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE (ADHESIVE TAPE ON REVERSE SIDE)

STYLE F



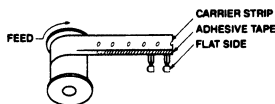
ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE (ADHESIVE TAPE ON REVERSE SIDE)

STYLE C



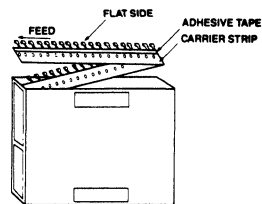
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE G



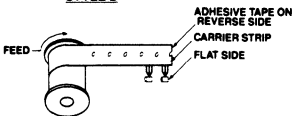
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

STYLE M



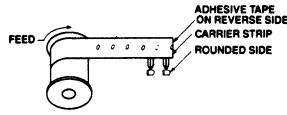
FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE
 STYLE M AMMO PACK IS EQUIVALENT TO STYLES E, F, G, H OF REEL PACK DEPENDING ON WHICH BOX-FLAP IS OPENED AND WHICH END OF THE BOX THE DEVICES ARE FED FROM.

STYLE D



FLAT SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE (ADHESIVE TAPE ON REVERSE SIDE)

STYLE H



ROUNDED SIDE OF TRANSISTOR AND CARRIER STRIP VISIBLE (ADHESIVE TAPE ON REVERSE SIDE)

0424-11

ORDERING INFORMATION

TO-92 Standard Lead Forms

Lead Form	Suffix
TO-18 Pin Circle	-18
TO-5 Pin Circle	-5
100-Mil Leads Spacing	-Z

Typical Quantities

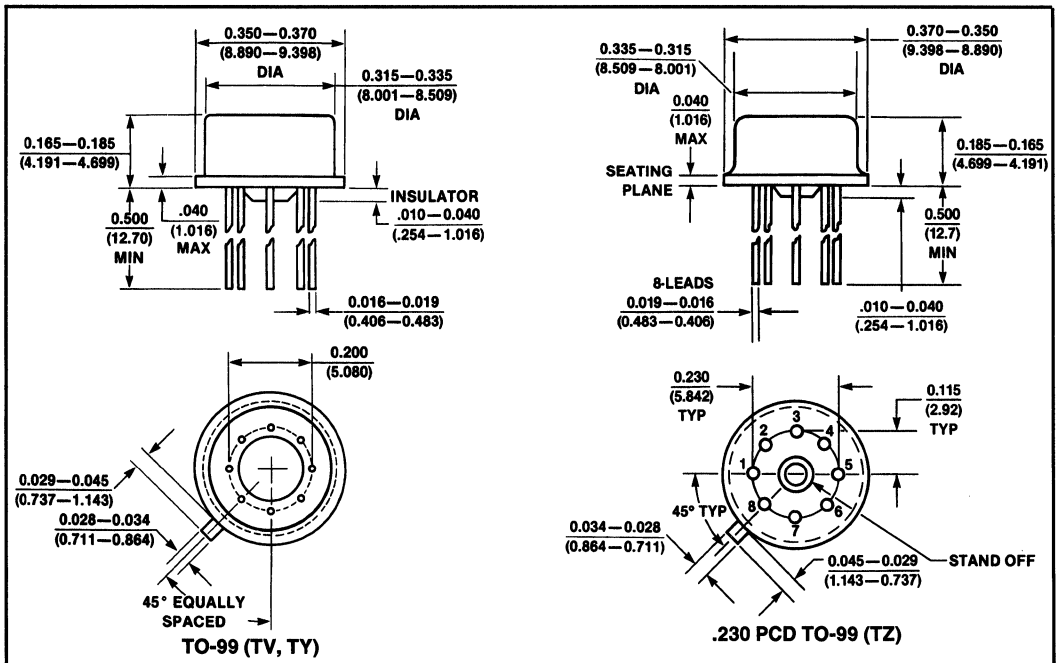
1800 Units Per Reel
3000 Units Per Ammo Box

TO-92 Taping Specifications and Winding Styles

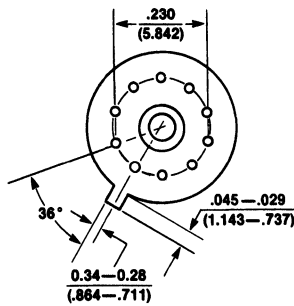
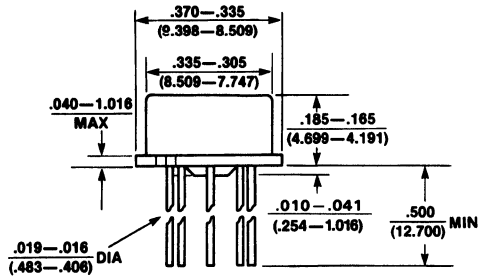
Style	Packaging	Suffix
A	Reel	-TA
B	Reel	-TB
C	Reel	-TC
D	Reel	-TD
E	Reel	-TE
F	Reel	-TF
G	Reel	-TG
H	Reel	-TH
P	Ammo Box	-TP
M	Ammo Box	-TM

PACKAGE OUTLINES

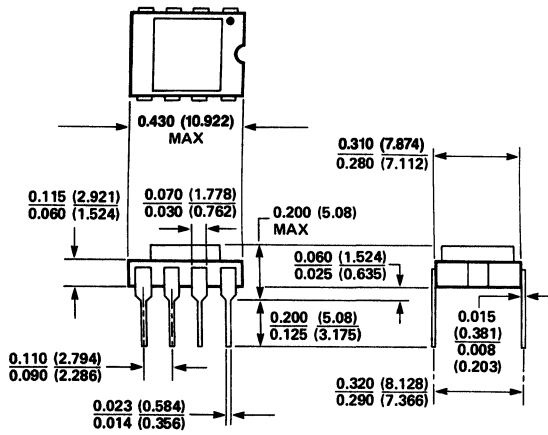
All dimensions given in inches and (millimeters).



PACKAGE OUTLINES All dimensions given in inches and (millimeters).

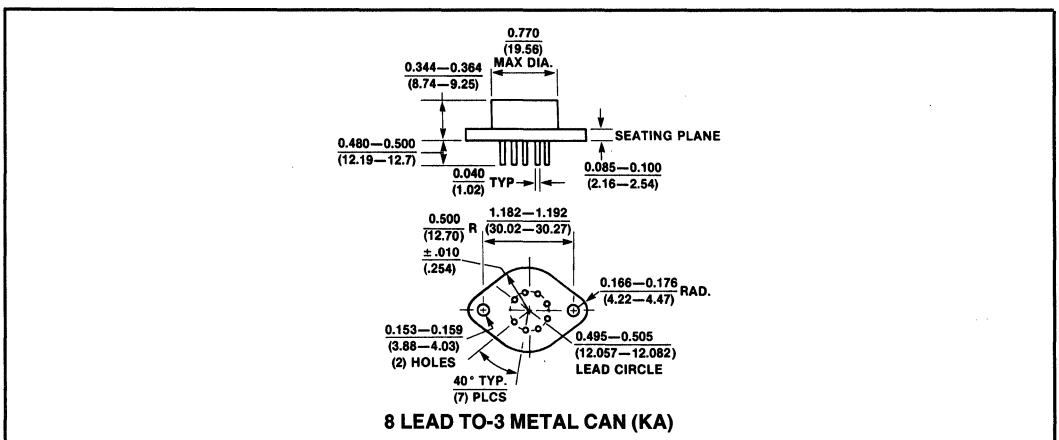
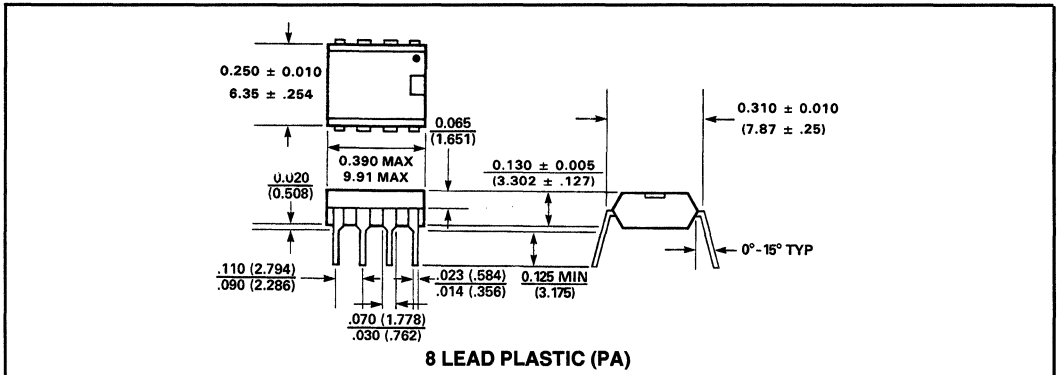
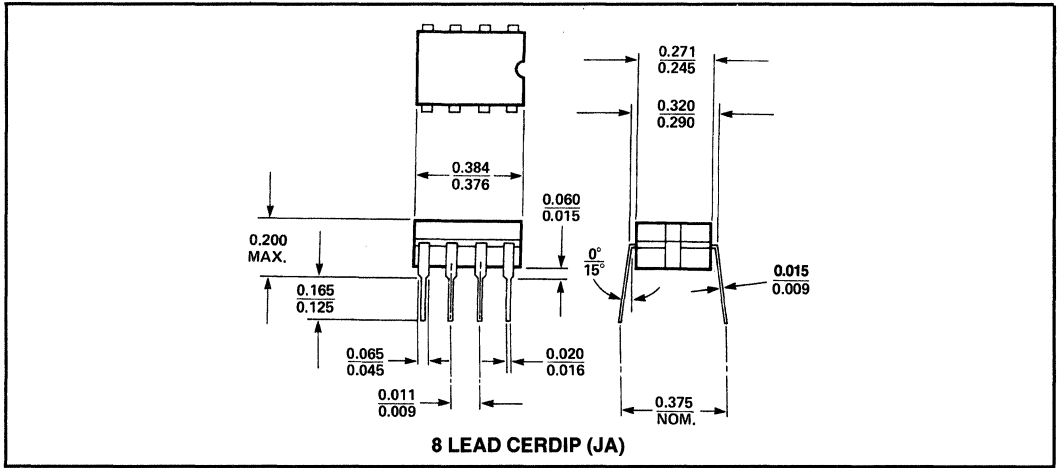


TO-100 (TW, TX)

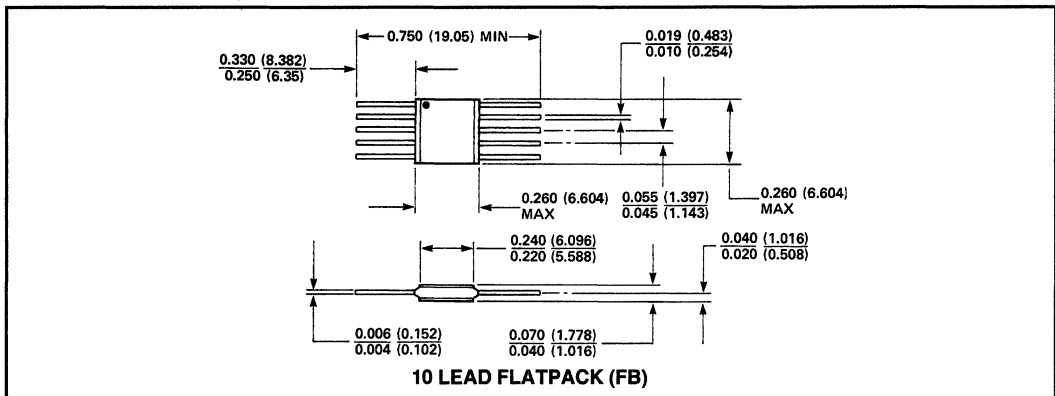
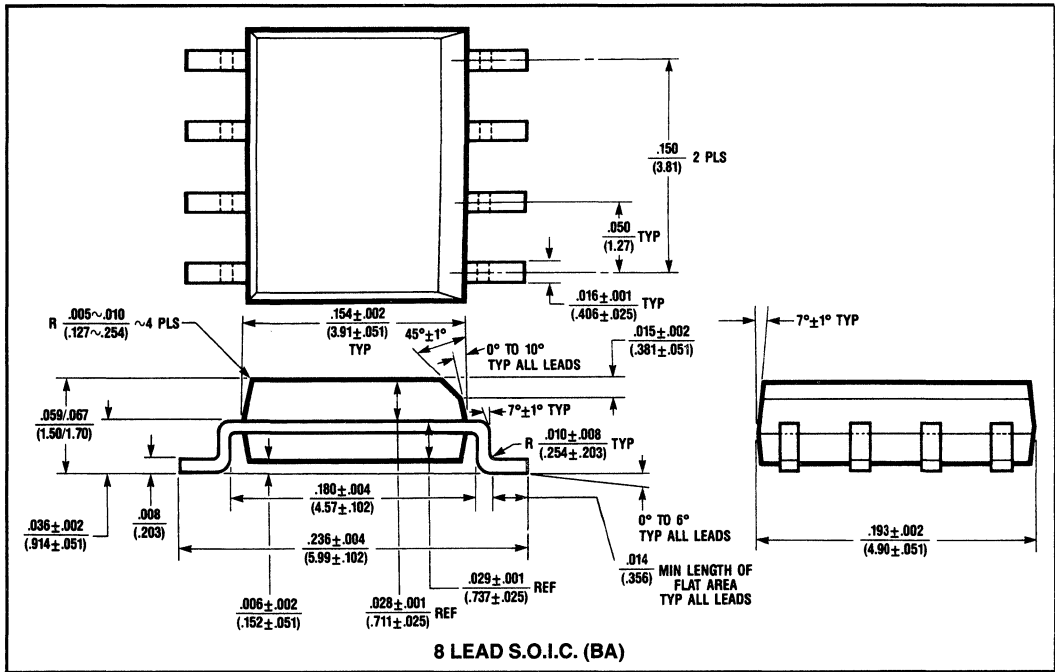


8 LEAD CERAMIC (DA)

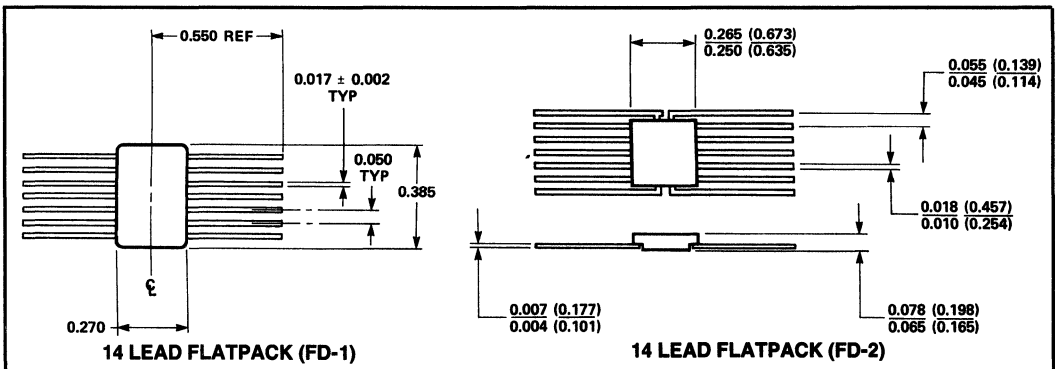
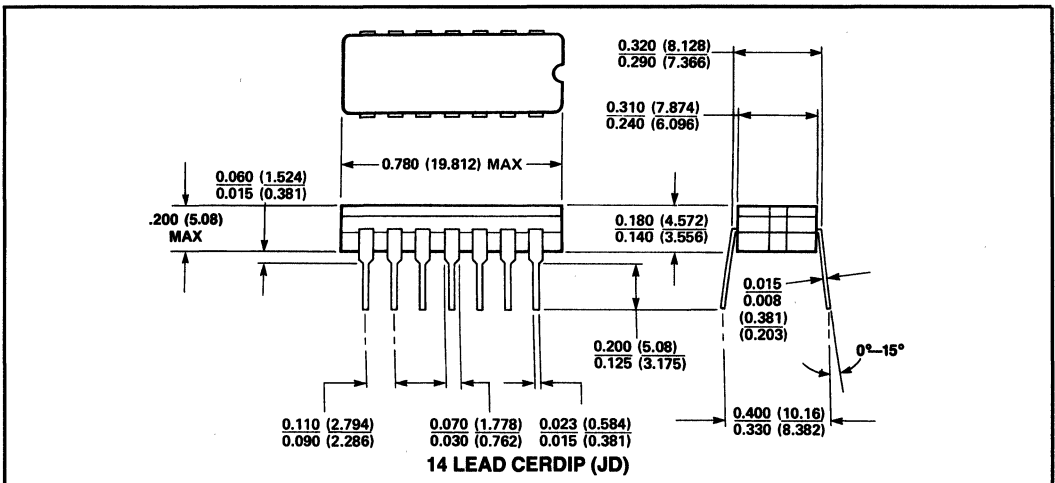
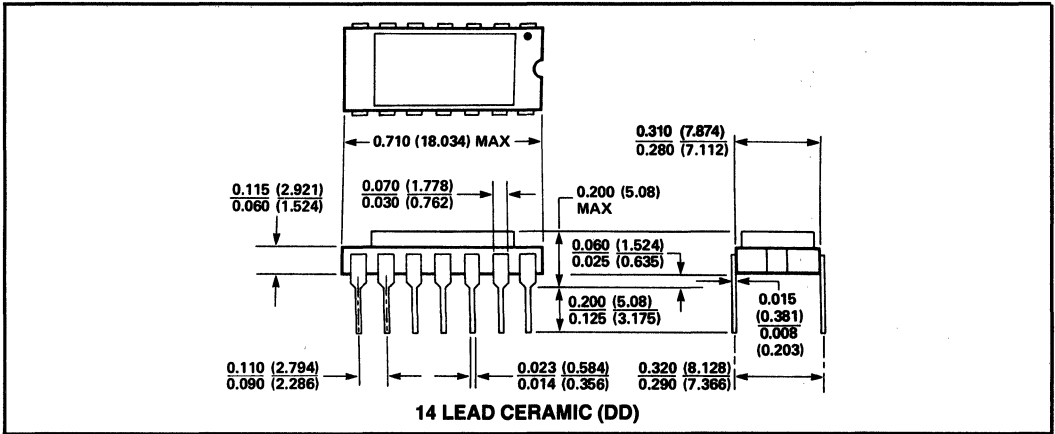
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



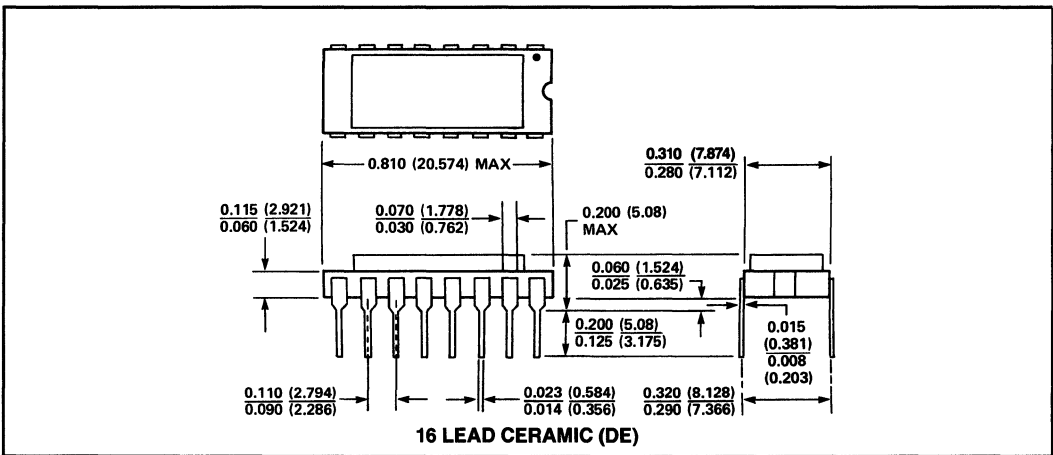
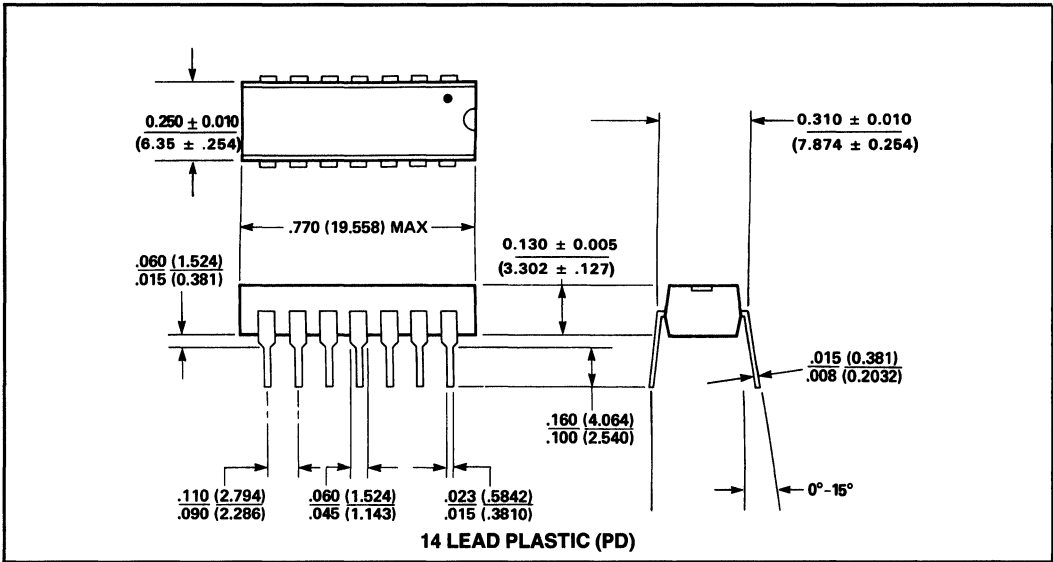
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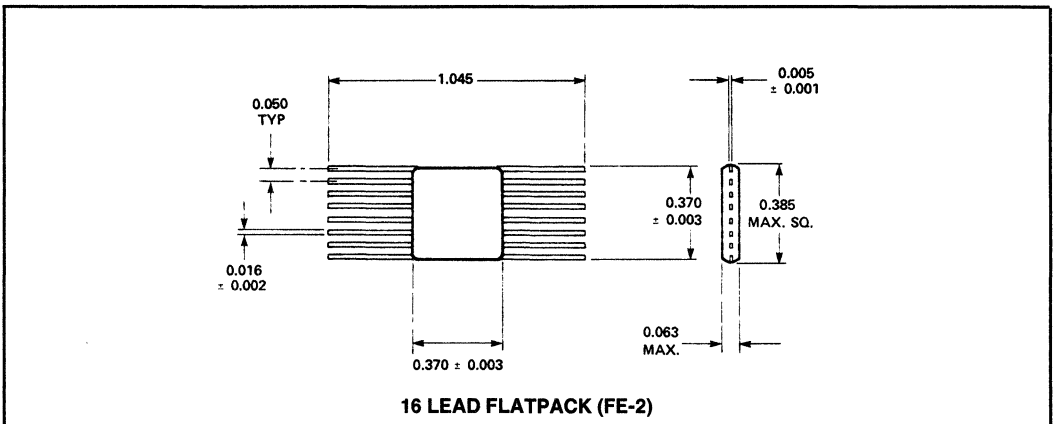
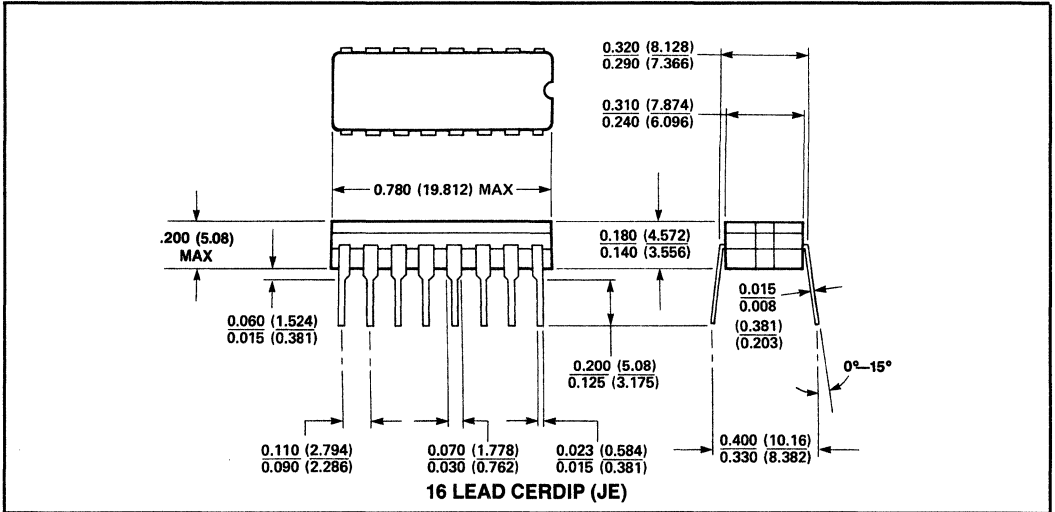
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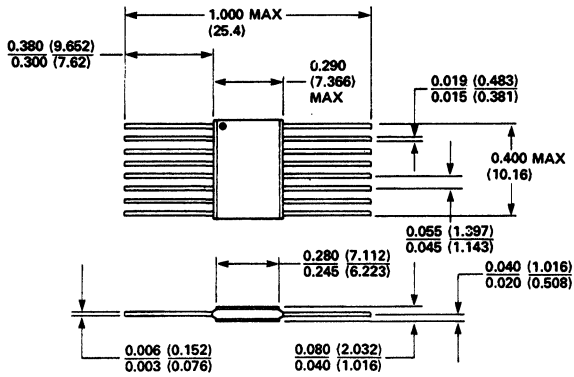
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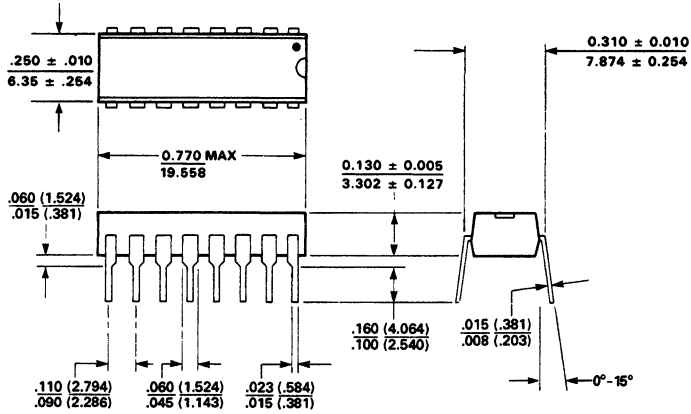
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PACKAGE OUTLINES All dimensions given in inches and (millimeters).

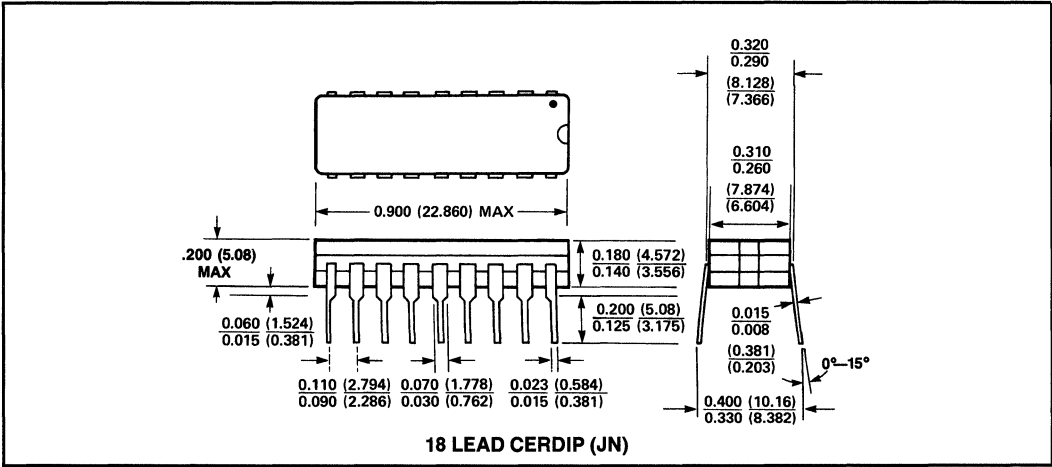
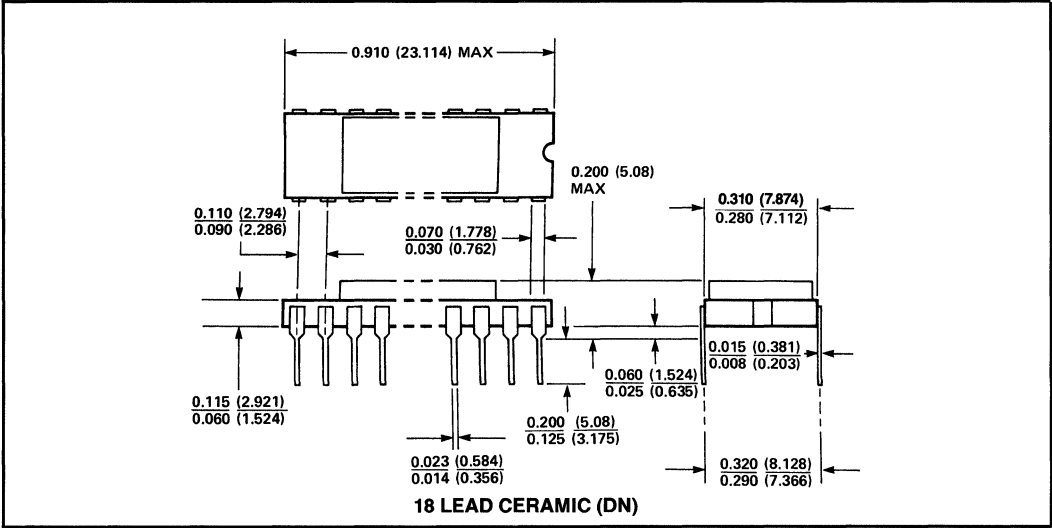


16 LEAD FLATPACK (FE-1)

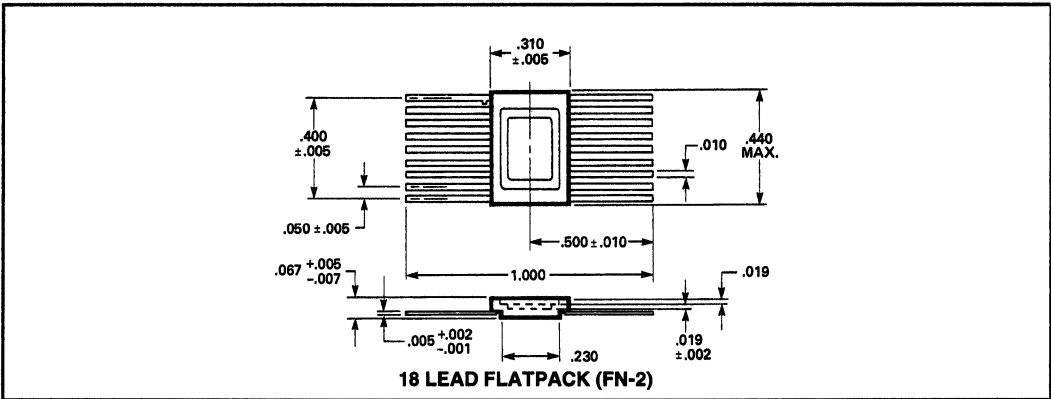
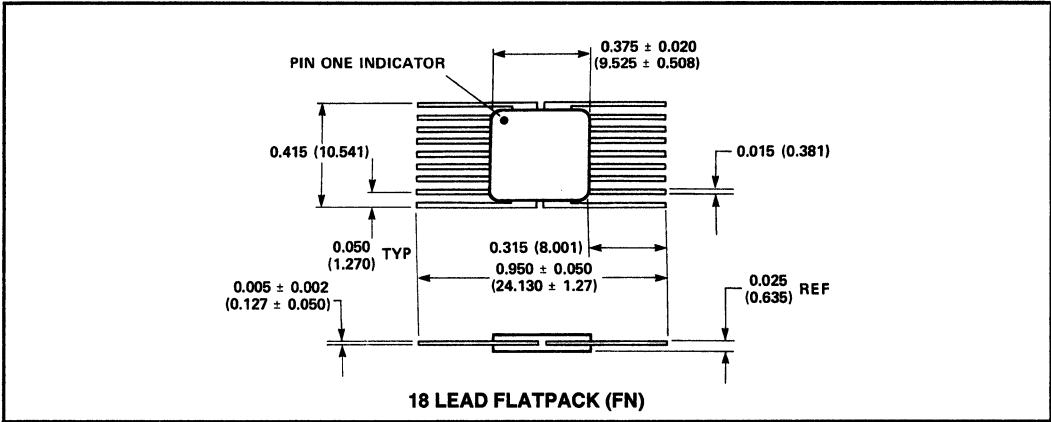


16 LEAD PLASTIC (PE)

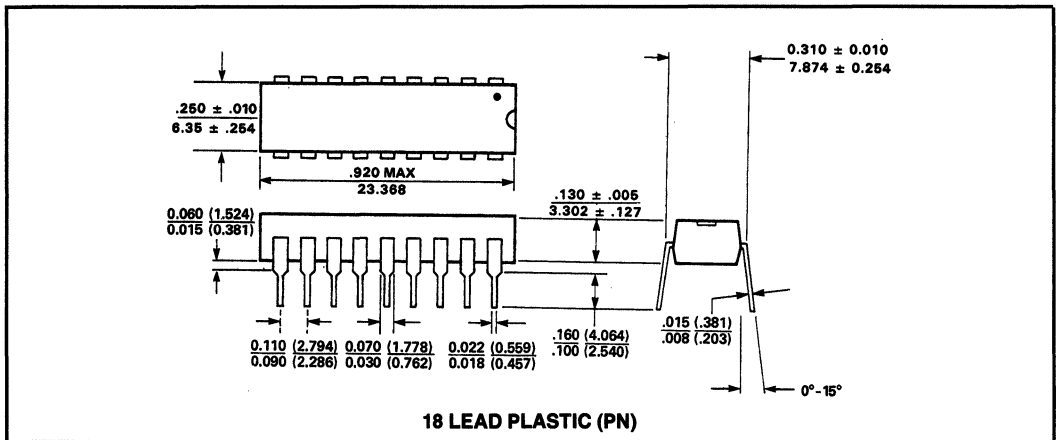
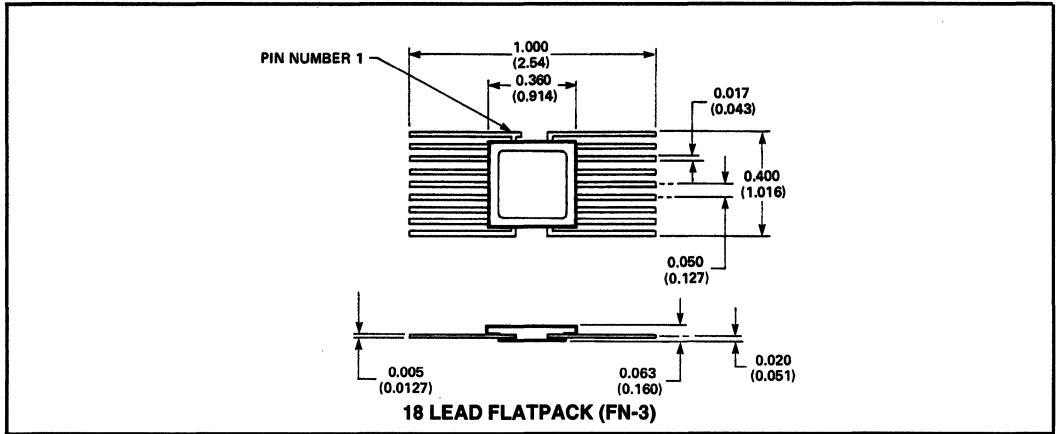
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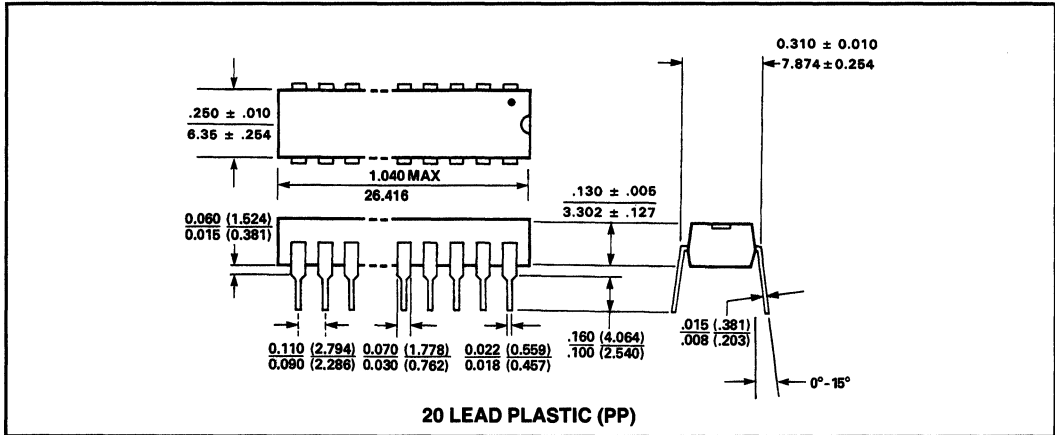
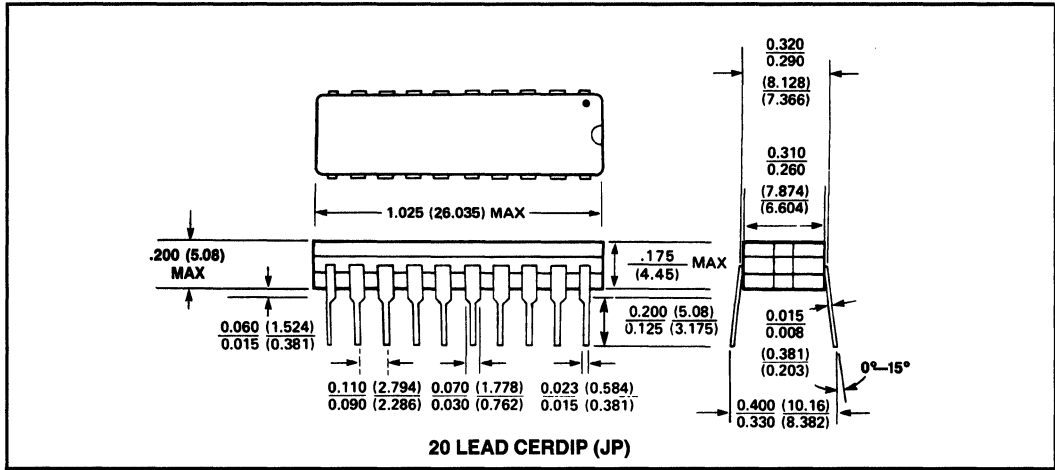
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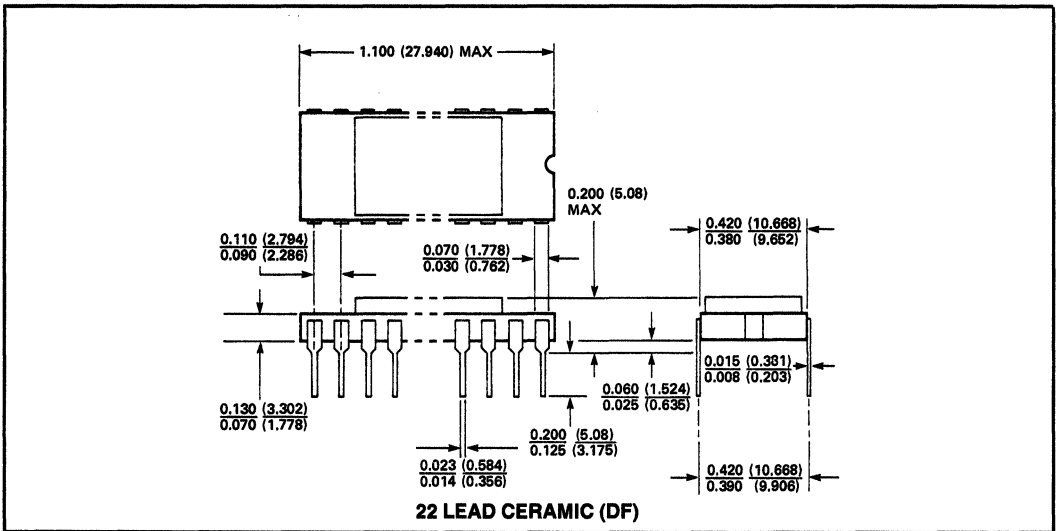
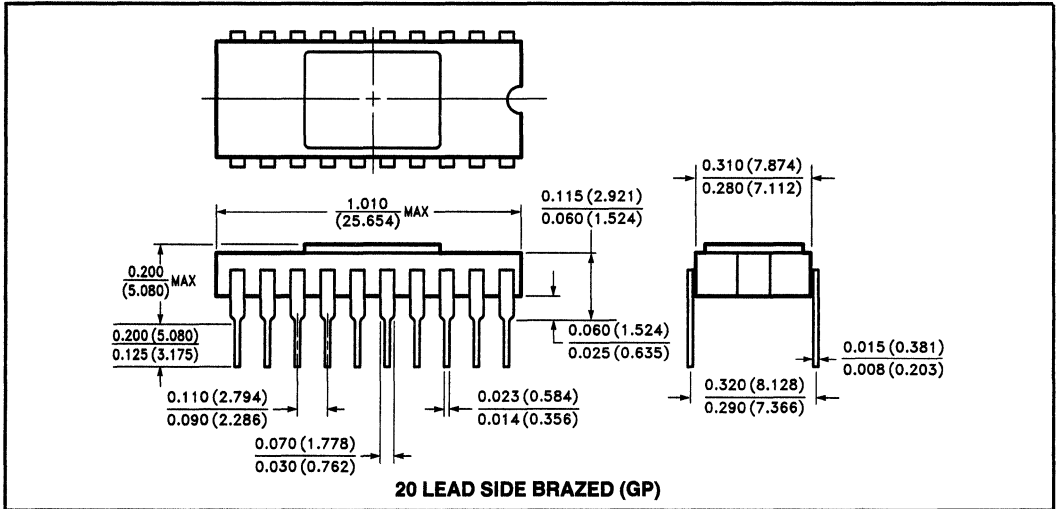
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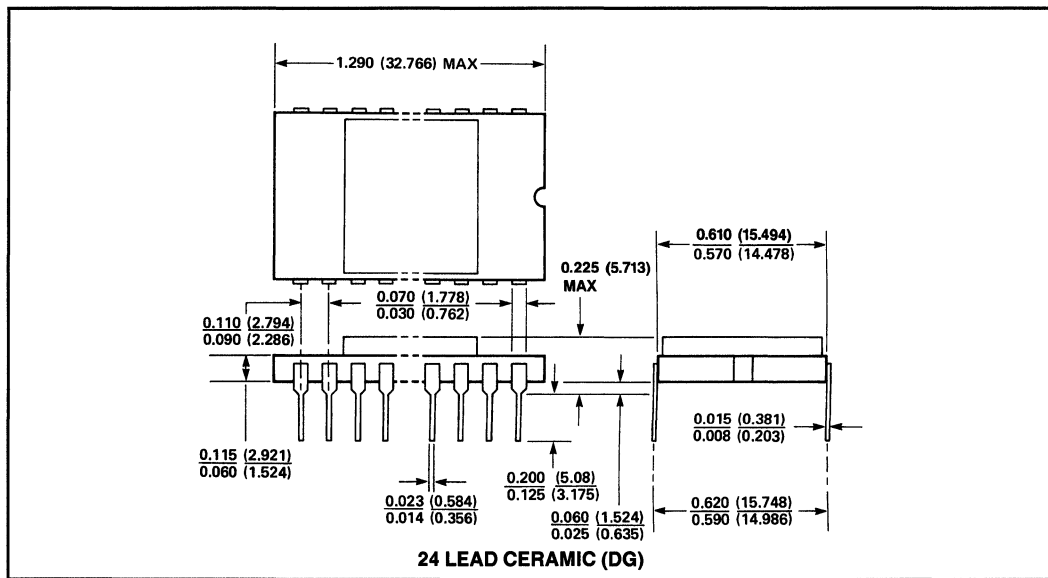
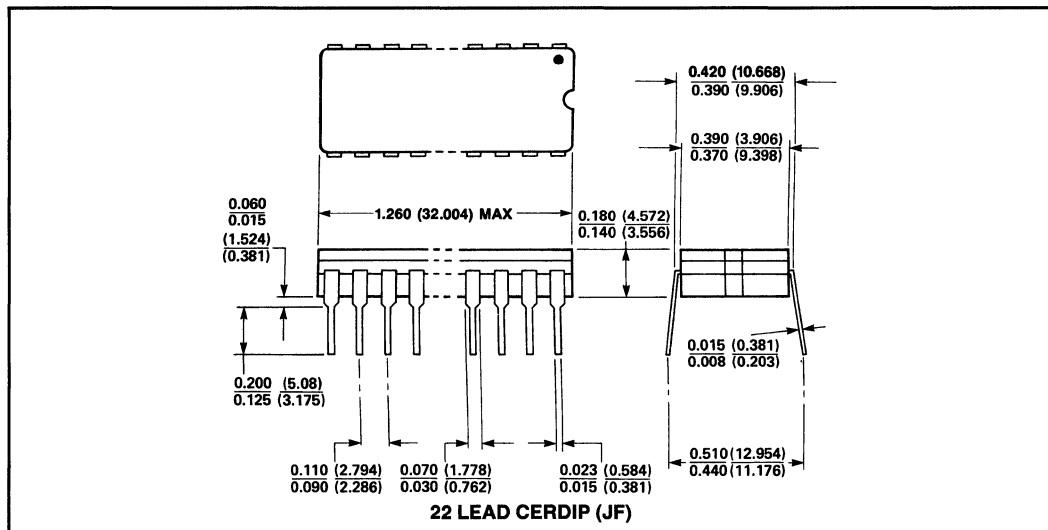
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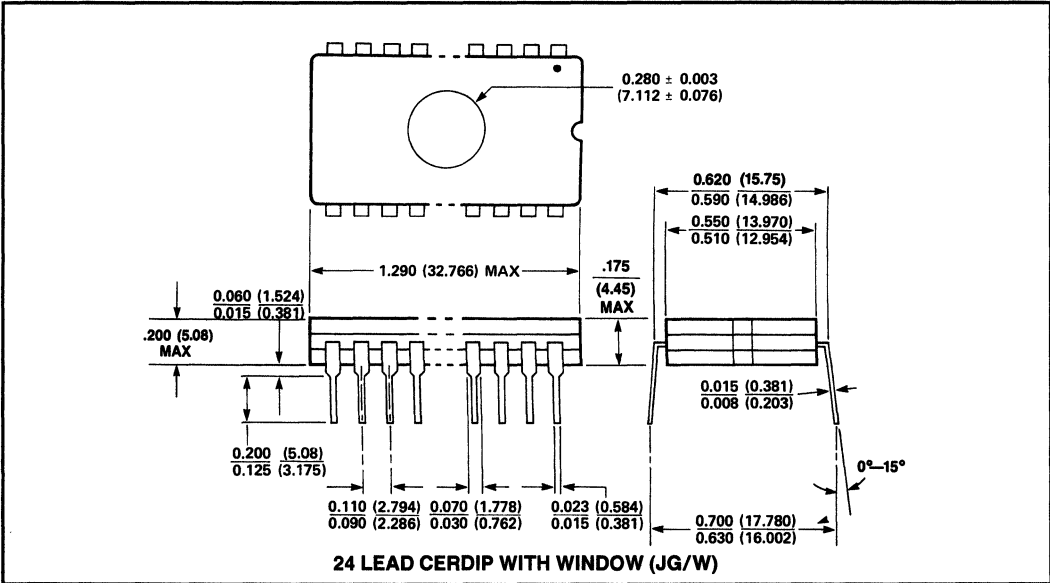
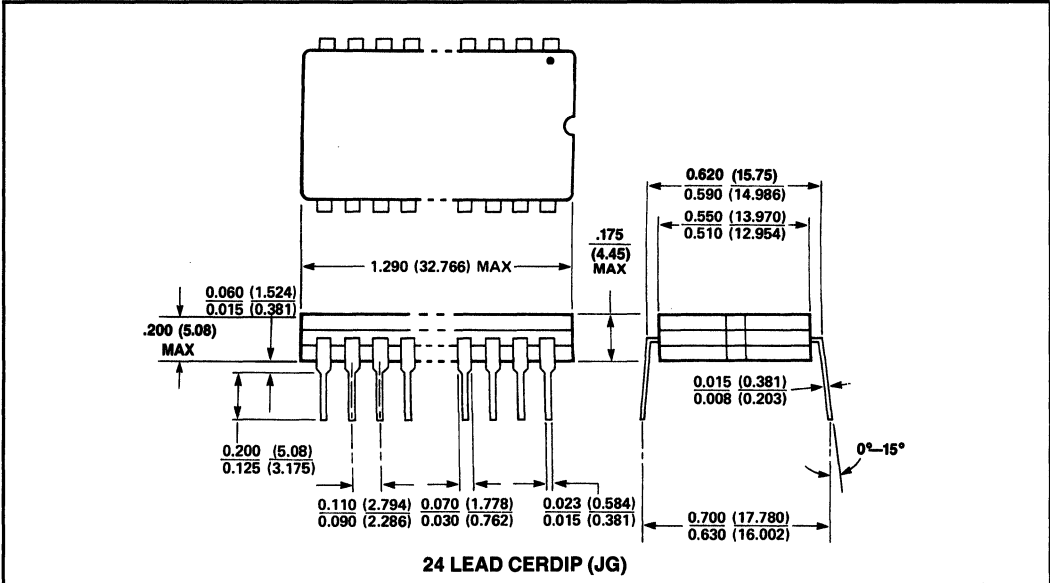
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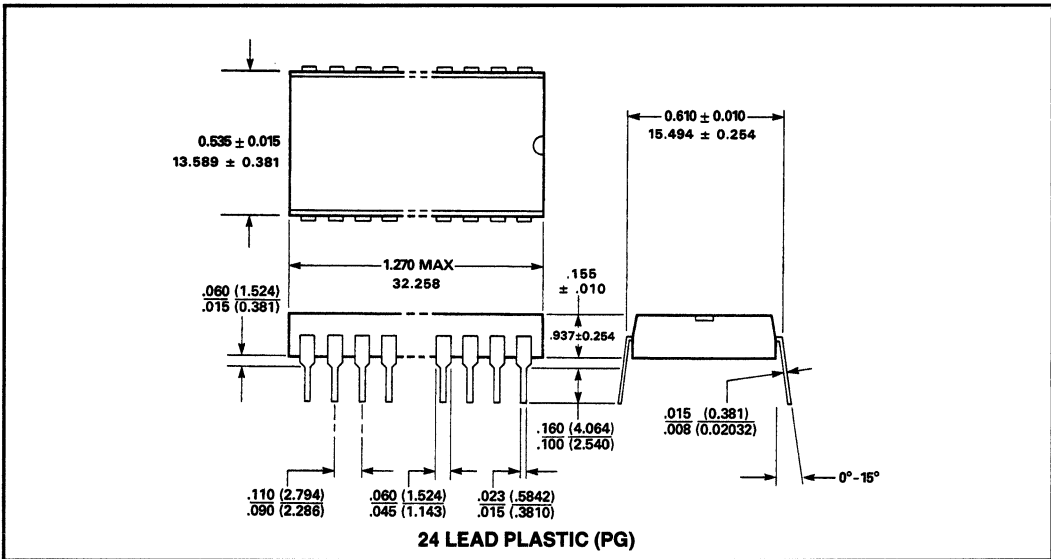
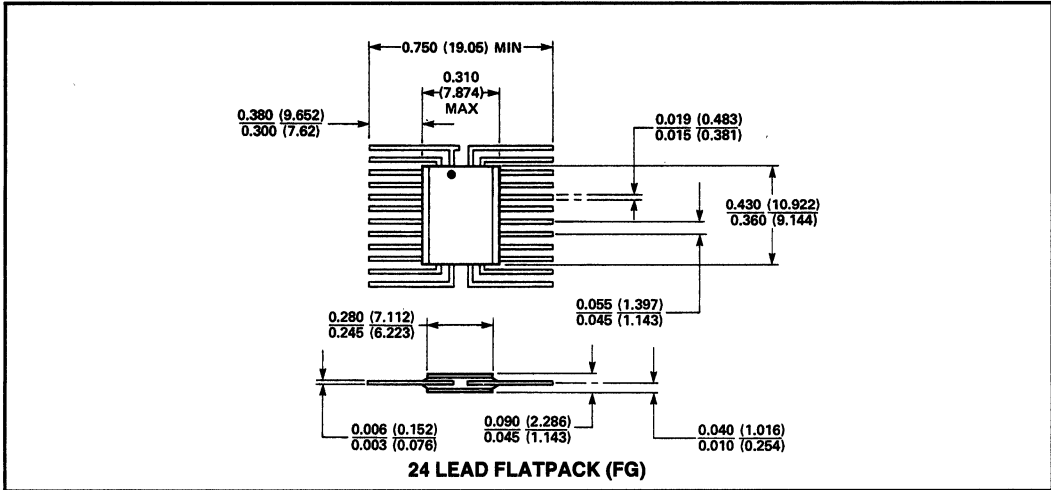
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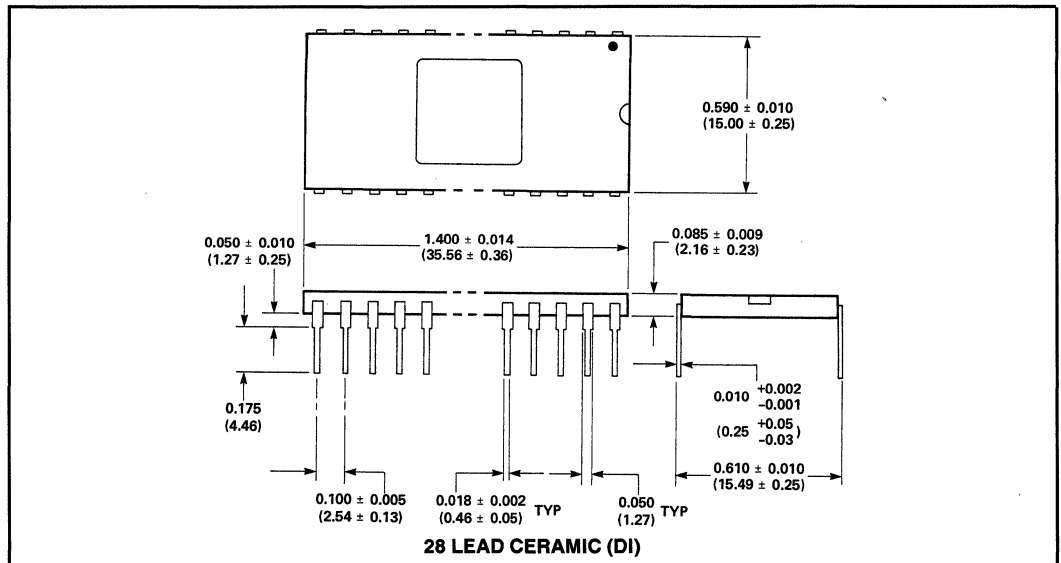
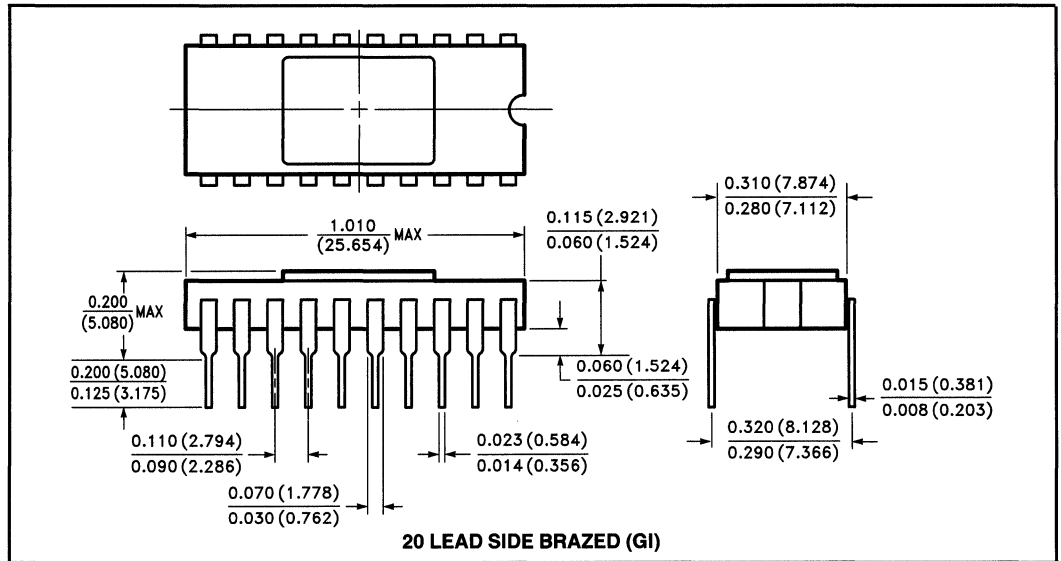
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



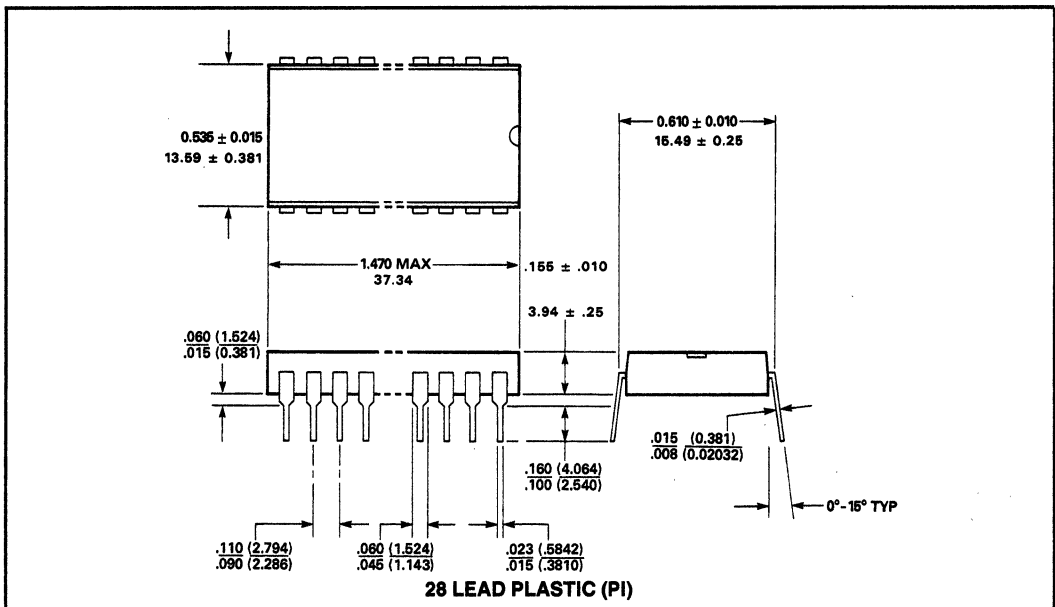
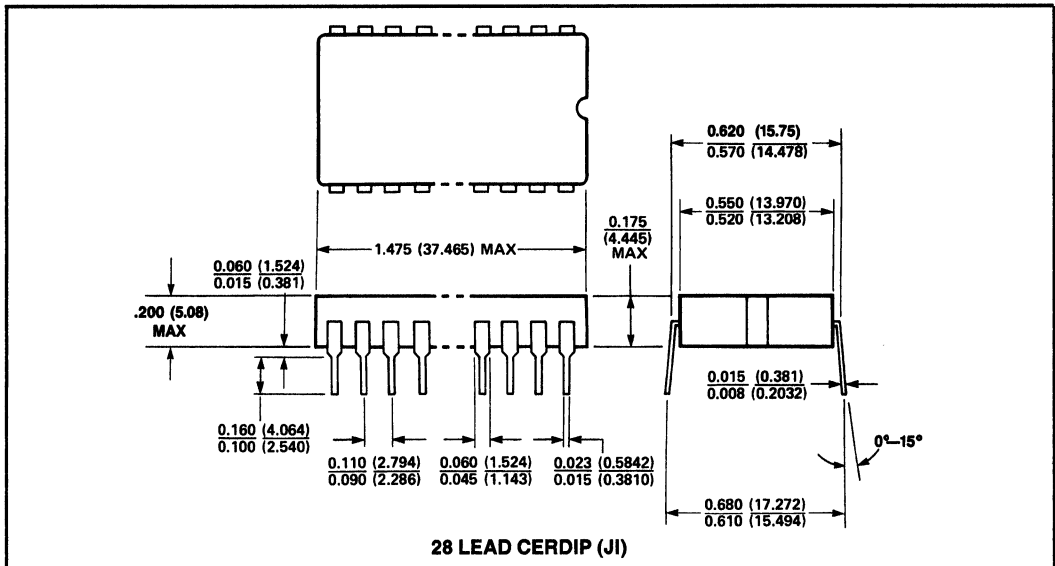
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



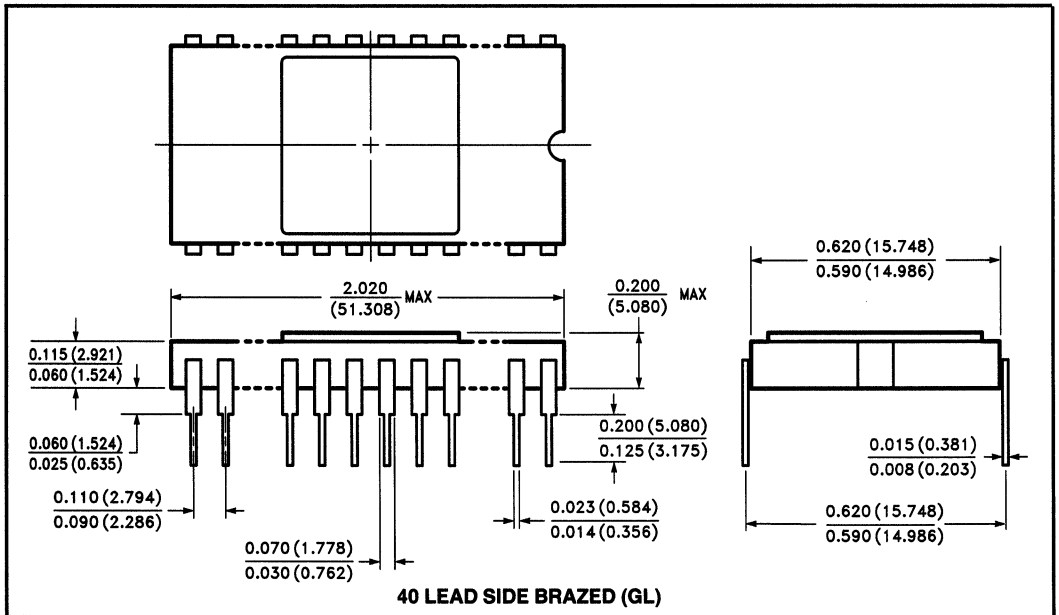
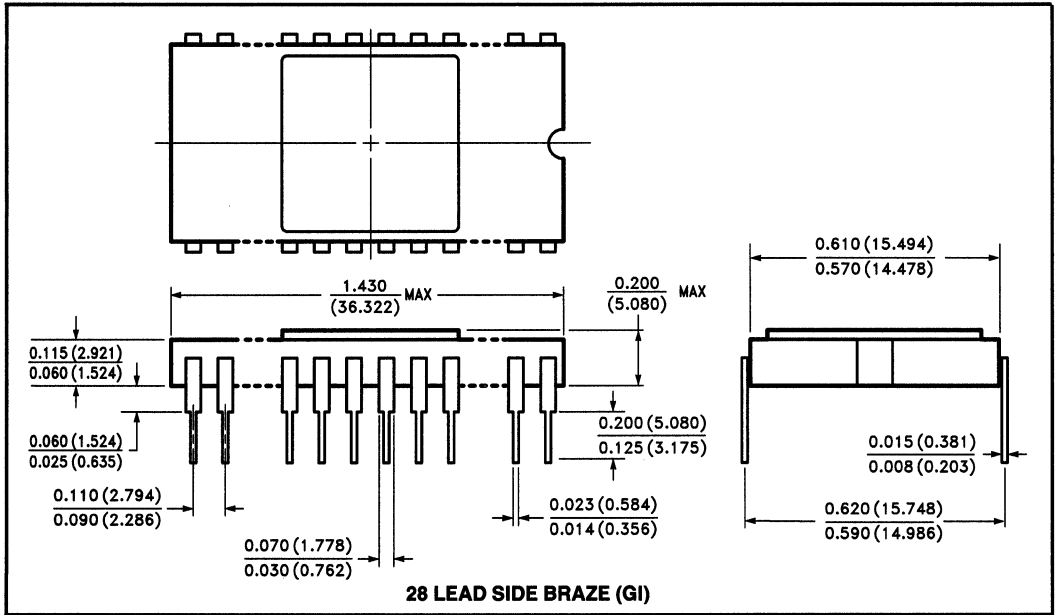
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



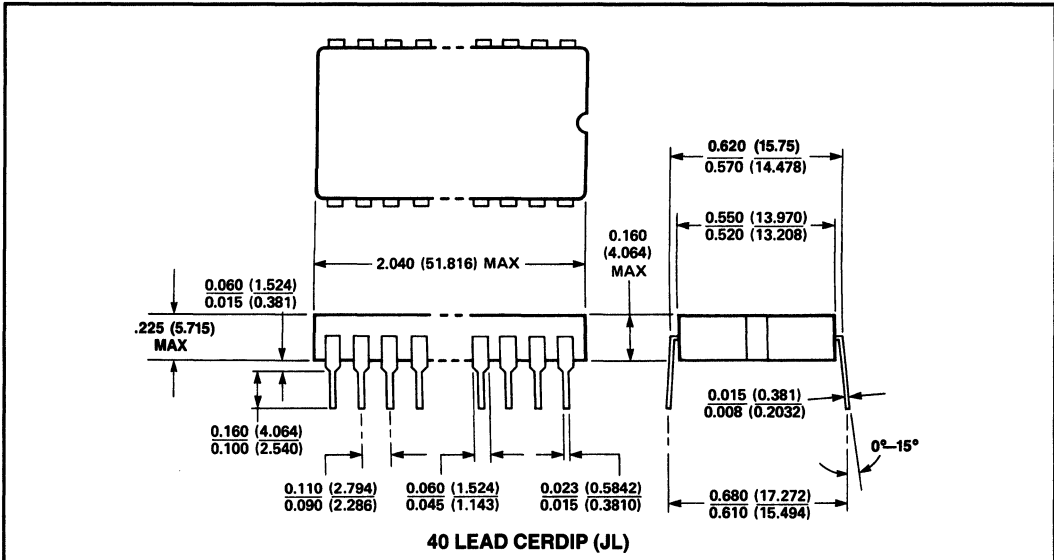
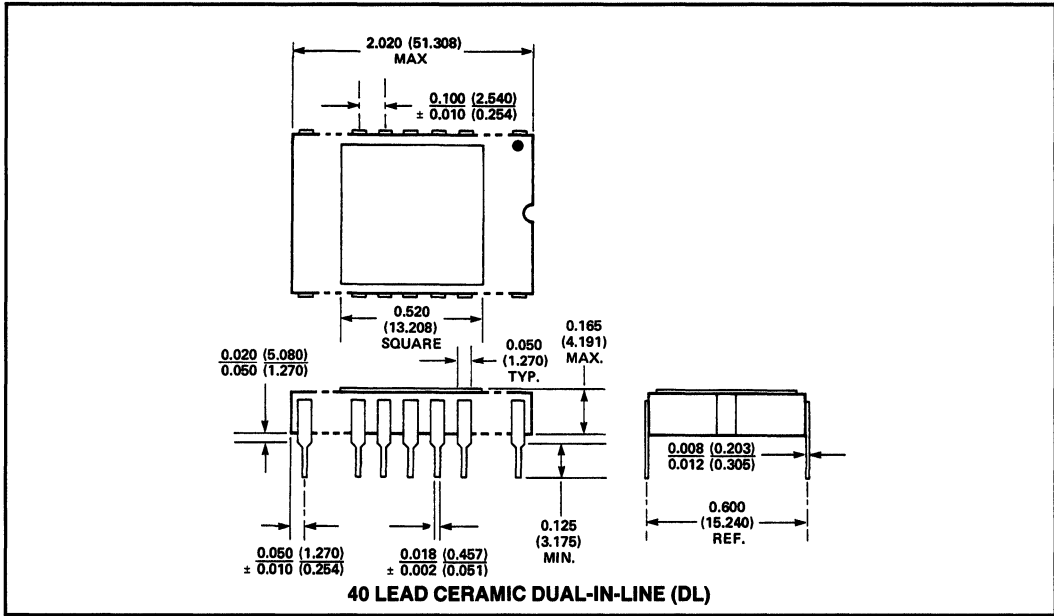
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



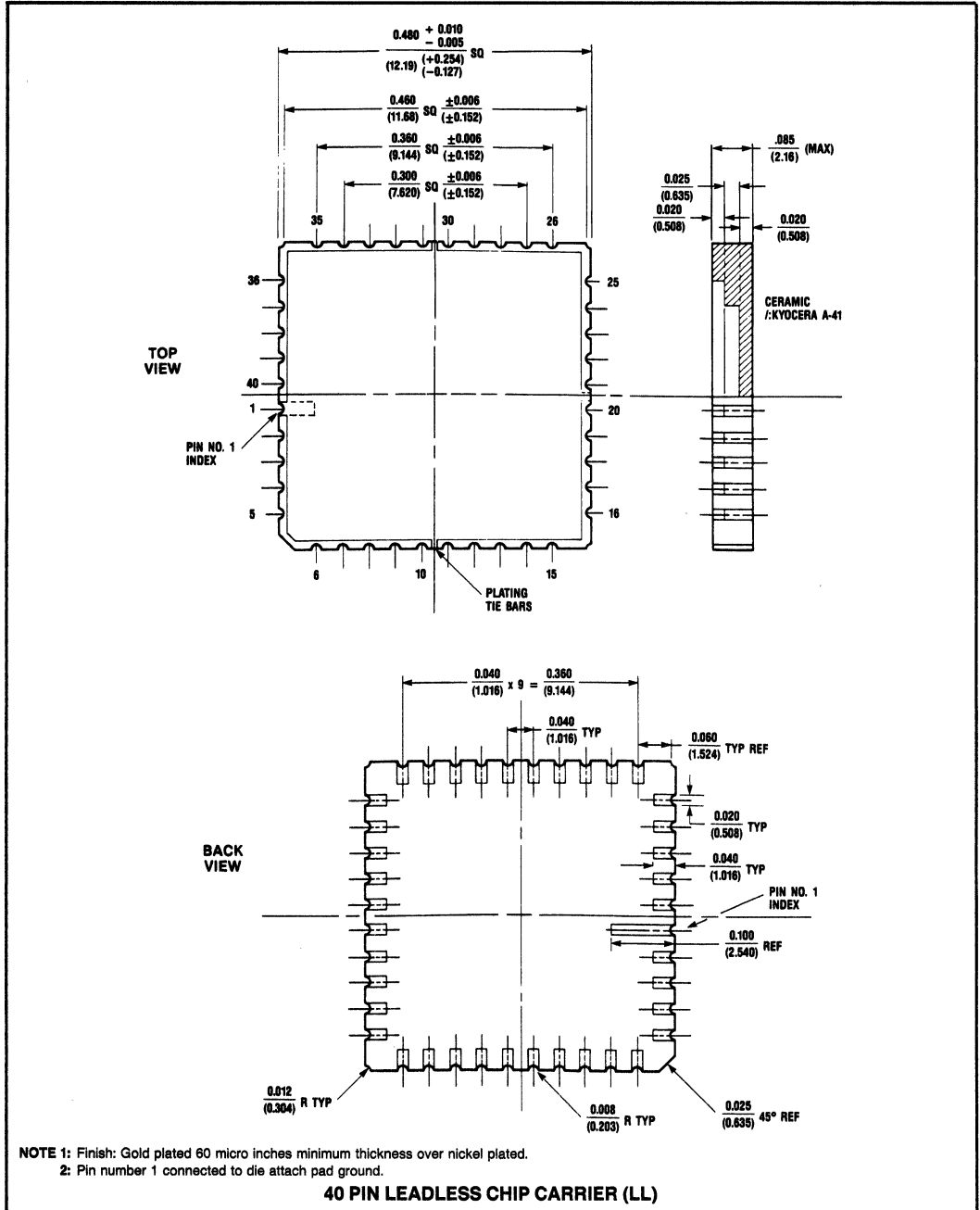
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



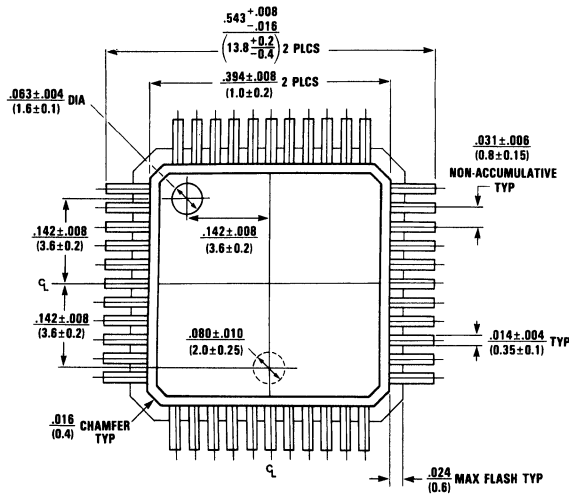
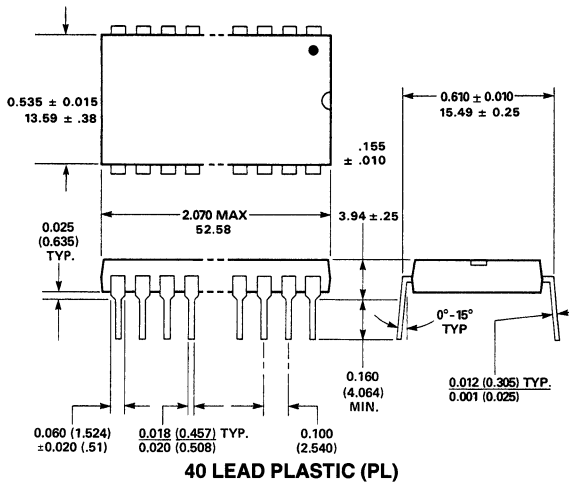
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



PACKAGE OUTLINES All dimensions given in inches and (millimeters).



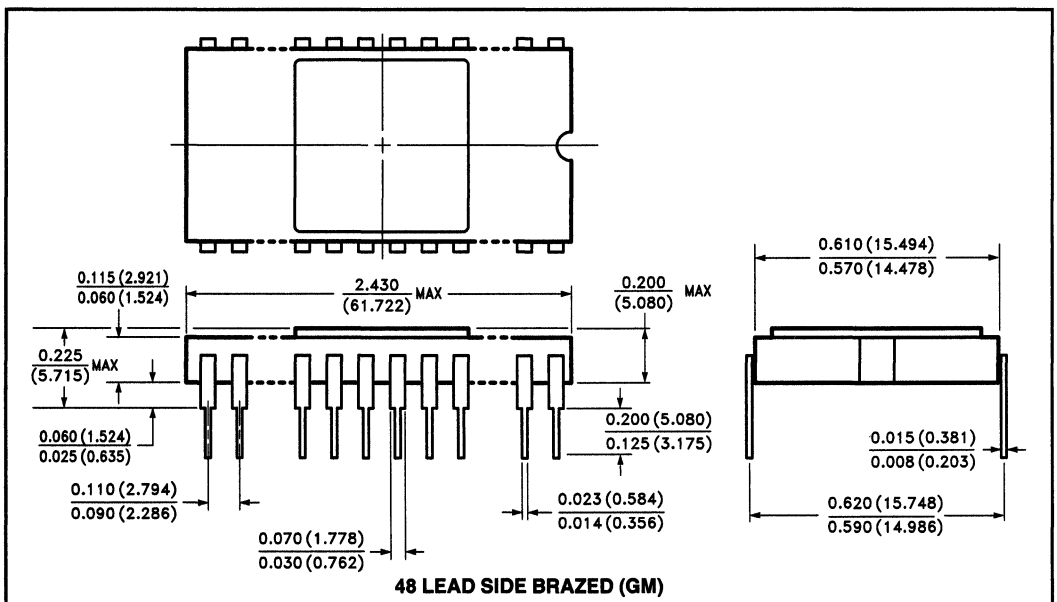
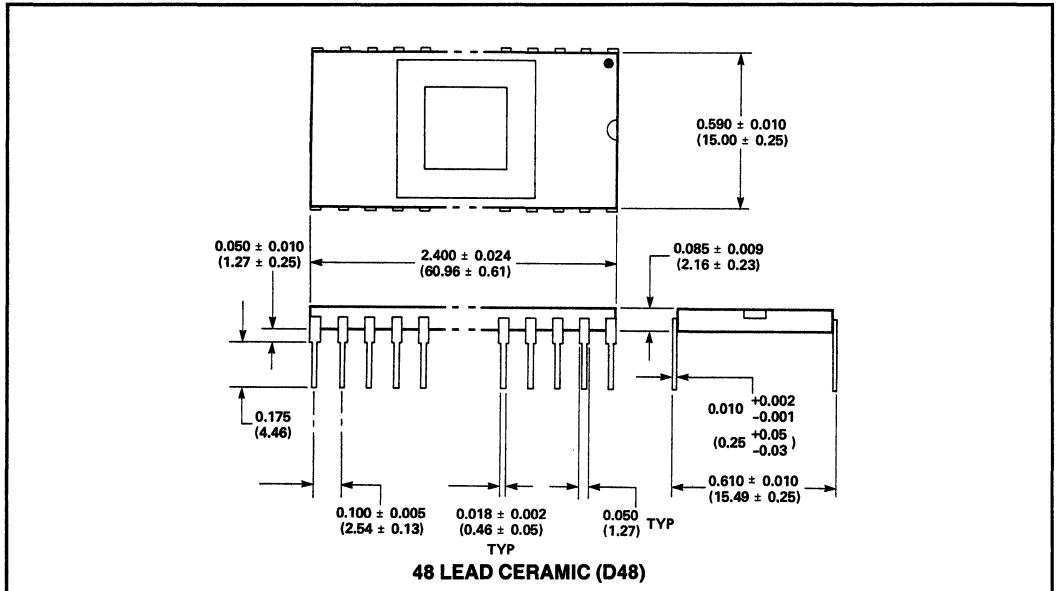
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



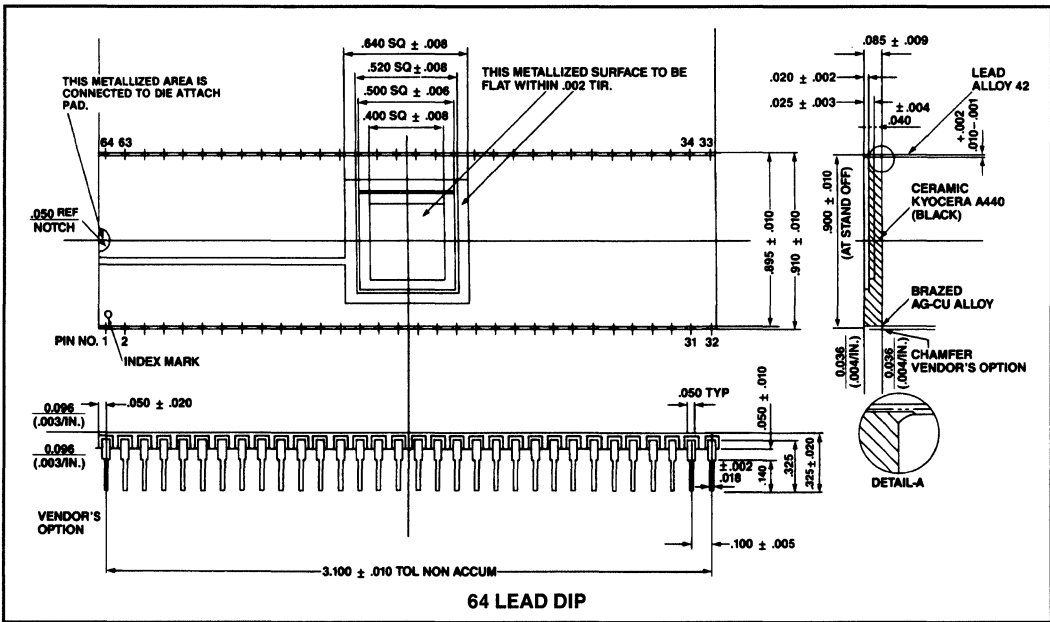
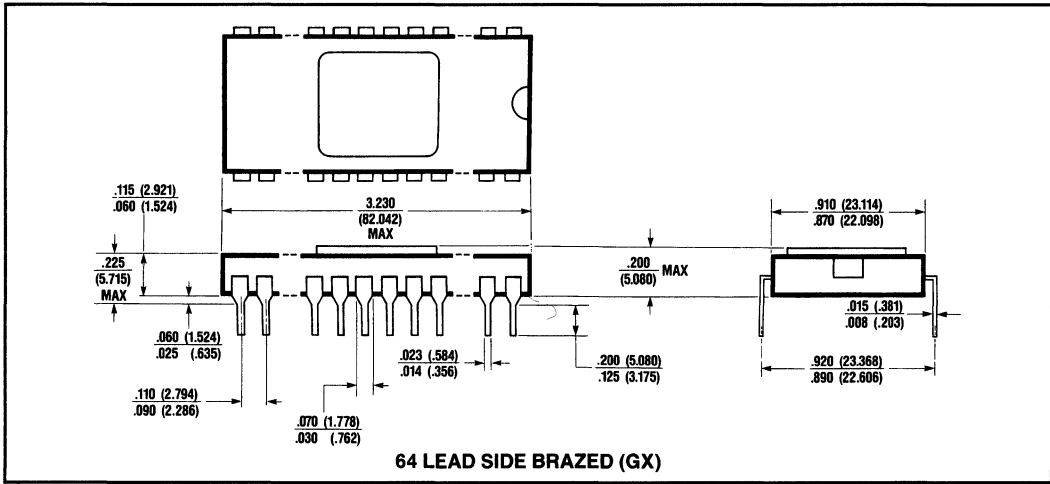
NOTE 1: PART MUST COMPLY TO SPECIFICATION.
 2: DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.
 3: PART IS SYMMETRICAL ABOUT THE CENTERLINES (C_L) SHOWN.

44 LEAD PLASTIC FLATPACK (M44)

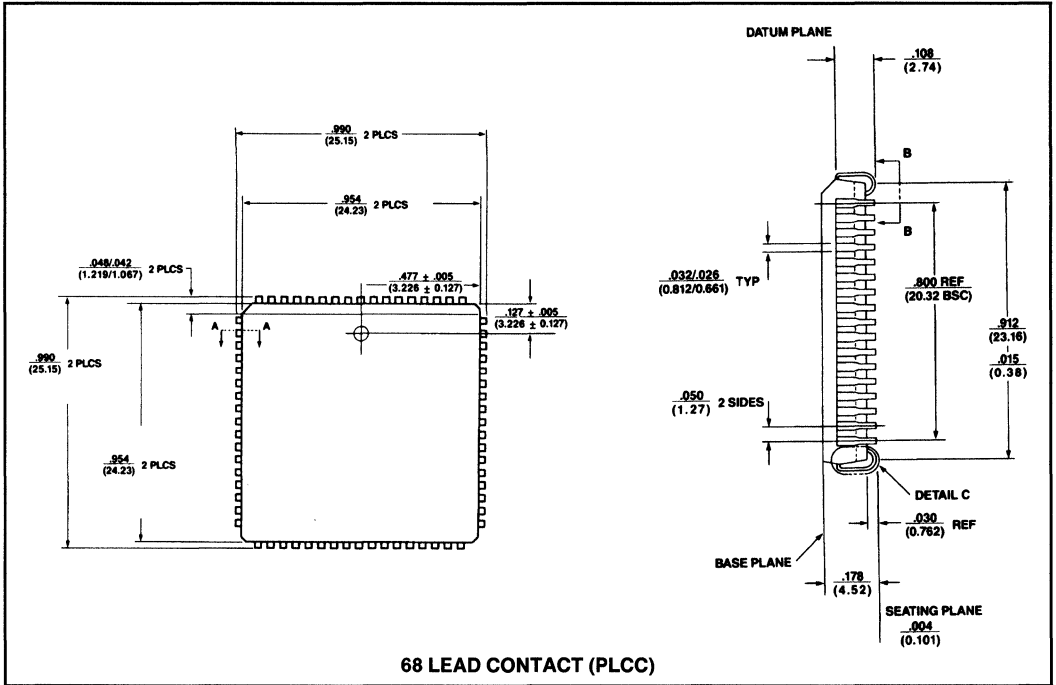
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



PACKAGE OUTLINES All dimensions given in inches and (millimeters).

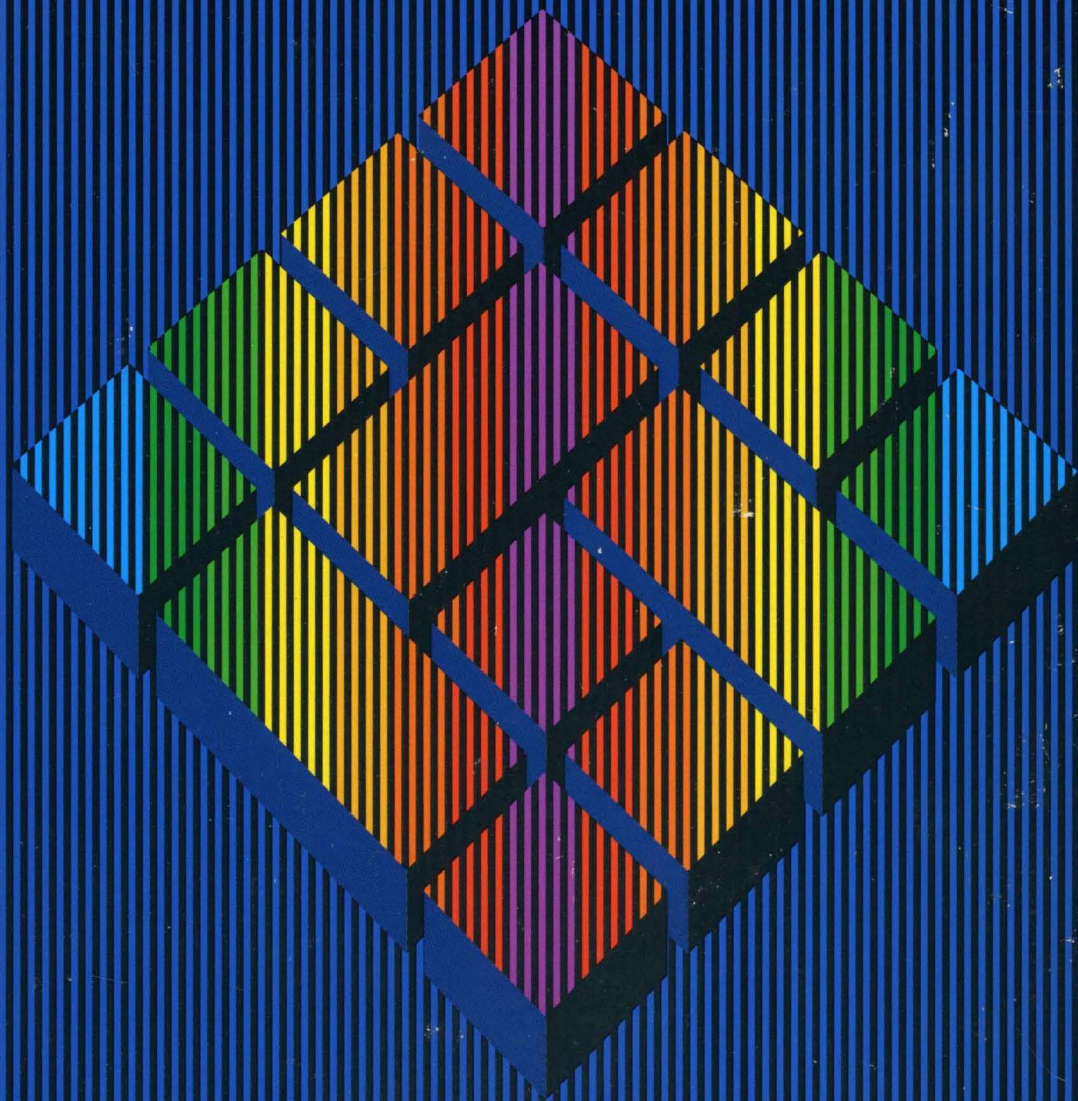


PACKAGE OUTLINES All dimensions given in inches and (millimeters).



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